5.0 Embedded Pentium® Processor With Voltage Reduction Technology Electrical Specifications

5.1 Absolute Maximum Ratings

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended operation beyond the maximum ratings may affect device reliability. Furthermore, although the embedded Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 34. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
3 V Supply voltage with respect to V_{SS}	–0.5 V to +4.6 V
3.1 V Supply voltage with respect to V_{SS}	–0.5 V to +4.1 V
3 V Only Buffer DC Input Voltage	–0.5 V to V_{CC3} +0.5; not to exceed 4.6 V[1]
5 V Safe Buffer DC Input Voltage	–0.5 V to 6.5 V[2, 3]

NOTES:
1. Applies to all SPGA embedded Pentium® processor with voltage reduction technology inputs except CLK.
2. Applies to CLK.
3. See Table 36.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

5.2 DC Specifications

Tables 35, 36 and 37 list the DC specifications that apply to the embedded Pentium processor with voltage reduction technology. The embedded Pentium processor with voltage reduction technology core operates at 3.1 V internally while the I/O interface operates at 3.3 V. The CLK input may be at 3.3 V or 5 V. Since the 3.3-V (5-V safe) input levels defined in Table 36 are the same as the 5-V TTL levels, the CLK input is compatible with existing 5V clock drivers.

Table 35. DC Specifications

T_{CASE} = 0 to 85° C; V_{CC2} = 3.1 V ± 165 mV; V_{CC3} = 3.3 V ± 165 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level, Note 1
V_{IH3}	Input High Voltage	2.0	V_{CC3}+0.3	V	TTL Level, Note 1
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, Note 1, Note 2
V_{OH3}	Output High Voltage	2.4		V	TTL Level, Note 1, Note 3
I_{CC2}	Power Supply Current from 3.1-V core supply		2775	mA	Note 4
I_{CC3}	Power Supply Current from 3.3-V I/O buffer supply		355	mA	Note 4

NOTES:
1. 3.3-V TTL levels apply to all signals except CLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and V_{CC2} = 3.1 V ± 165 mV and V_{CC3} = 3.3 V ± 165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.

Table 36. 3.3-V (5-V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level; applies to CLK only
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level; applies to CLK only

Table 37. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	Guaranteed by design.
C_O	Output Capacitance		20	pF	Guaranteed by design.
$C_{I/O}$	I/O Capacitance		25	pF	Guaranteed by design.
C_{CLK}	CLK Input Capacitance		15	pF	Guaranteed by design.
C_{TIN}	Test Input Capacitance		15	pF	Guaranteed by design.
C_{TOUT}	Test Output Capacitance		20	pF	Guaranteed by design.
C_{TCK}	Test Clock Capacitance		15	pF	Guaranteed by design.
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (for input without pull up or pull down resistors)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (for input without pull up or pull down resistors)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4 V (for input with pull down resistors)
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4 V (for input with pull up resistors)

5.2.1 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both on or both off within one second of each other.

5.3 AC Specifications

The AC specifications of the embedded Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All embedded Pentium processors with voltage reduction technology AC specifications are valid for V_{CC2} = 3.1 V $\pm$ 165 mV, V_{CC3} = 3.3 V $\pm$ 165 mV, and T_{CASE} = 0º C to 85º C.

5.3.1 Power and Ground

For clean on-chip power distribution, the embedded Pentium processor with voltage reduction technology has 25 V_{CC2} (3.1-V power), 28 V_{CC3} (3.3-V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC2}, V_{CC3} and V_{SS} pins of the processor. On the circuit board, all V_{CC2} pins must be connected to a 3.1-V V_{CC2} plane (or island) and all V_{CC3} pins must be connected to a 3.3-V V_{CC3} plane. All V_{SS} pins must be connected to a V_{SS} plane. Refer to Table 25 for a list of V_{CC2} and V_{CC3} pins.

5.3.2 Decoupling Recommendations

Transient power surges occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by minimizing the length of circuit board traces between the processor and the decoupling capacitors.

These capacitors should be evenly distributed around each component on the 3.3-V plane and the 3.1-V plane (or island). Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low power consumption level to a much higher level (or high to low). A typical example would be entering or exiting the Stop Grant state. Other examples include executing a HALT instruction (which causes the processor to enter the Auto HALT Powerdown state) or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Several bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µF range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point at which the regulated power supply output can react to the change in load. In order to reduce the net ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3-V plane and the 3.1-V plane or island) to ensure that these supply voltages stay within specified limits during changes in the power demands of the processor during operation.

For more detailed information, please contact Intel or refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems* application note (order number 242558).

Note: Capacitors degrade over time during use. As capacitors age, their capacity to store and hold a charge becomes compromised. Designing a board with below minimum acceptable bypass and bulk capacitors may have future system reliability consequences.

5.3.3 Connection Specifications

All NC pins must remain unconnected. Refer to Table 25 for a list of NC pins.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to ground.

5.3.4 AC Timings

The AC specifications given in Table 38 consist of output delays, input setup requirements and input hold requirements for the 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both 0 and 1 logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 38. AC Specifications (Sheet 1 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	ns	18	
t_{1b}	CLK Period Stability		±250	ps		1, 19
t_2	CLK High Time	4.0		ns	18	@2 V, Note 1
t_3	CLK Low Time	4.0		ns	18	@0.8 V, Note 1
t_4	CLK Fall Time	0.15	1.5	ns	18	2.0 V–0.8 V, Note 1
t_5	CLK Rise Time	0.15	1.5	ns	18	0.8 V–2.0 V, Note 1
t_{6a}	PWT, PCD, BE7#–BE0#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	ns	19	
t_{6b}	AP Valid Delay	1.0	8.5	ns	19	
t_{6c}	LOCK# Valid Delay	1.1	7.0	ns	19	
t_{6d}	ADS# Valid Delay	1.0	6.0	ns	19	
t_{6e}	A31–A3 Valid Delay	1.1	6.3	ns	19	
t_{6f}	M/IO# Valid Delay	1.0	5.9	ns	19	

NOTE: See Table 39 for table notes.

Table 38. AC Specifications (Sheet 2 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	20	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	19	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	19	4
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	19	4
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	19	4
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	19	4
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	19	
t_{10b}	HITM# Valid Delay	1.1	6.0	ns	19	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	19	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	19	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.3	7.5	ns	19	
t_{13}	D63–D0, DP3–DP0 Write Data Float Delay		10.0	ns	20	1
t_{14}	A31–A5 Setup Time	6.0		ns	21	20
t_{15}	A31–A5 Hold Time	1.0		ns	21	
t_{16a}	INV, AP Setup Time	5.0		ns	21	
t_{16b}	EADS# Setup Time	5.0		ns	21	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	21	
t_{18a}	KEN# Setup Time	5.0		ns	21	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	21	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	21	
t_{20}	BRDY# Setup Time	5.0		ns	21	
t_{21}	BRDY# Hold Time	1.0		ns	21	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	21	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	21	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	21	
t_{24b}	PEN# Setup Time	4.8		ns	21	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	21	
t_{25b}	HOLD Hold Time	1.5		ns	21	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	21	11, 15
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	21	12
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	21	11, 15, 16

NOTE: See Table 39 for table notes.

Table 38. AC Specifications (Sheet 3 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	21	12
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		14, 16
t_{31}	R/S# Setup Time	5.0		ns	21	11, 15, 16
t_{32}	R/S# Hold Time	1.0		ns	21	12
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		14, 16
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	2.8		ns	21	
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	21	
t_{36}	RESET Setup Time	5.0		ns	22	11, 15
t_{37}	RESET Hold Time	1.0		ns	22	12
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	22	16
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	22	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	22	11, 15, 16
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	22	12
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	22	To RESET falling edge, Note 15
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	22	To RESET falling edge, Note 21
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	22	To RESET falling edge, Note 21
t_{43a}	BF Setup Time	1.0		mS	22	To RESET falling edge, Note 18
t_{43b}	BF Hold Time	2.0		CLKs	22	To RESET falling edge, Note 18
t_{43c}	BE4# Setup Time	2.0		CLKs	22	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	22	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		ns	18	
t_{46}	TCK High Time	25.0		ns	18	@2 V, Note 1
t_{47}	TCK Low Time	25.0		ns	18	@0.8 V, Note 1
t_{48}	TCK Fall Time		5.0	ns	18	2.0 V–0.8 V, Notes 1, 8, 9
t_{49}	TCK Rise Time		5.0	ns	18	0.8 V–2.0 V, Notes 1, 8, 9

NOTE: See Table 39 for table notes.

Table 38. AC Specifications (Sheet 4 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{50}	TRST# Pulse Width	40.0		ns	24	Asynchronous, Note 1
t_{51}	TDI, TMS Setup Time	5.0		ns	23	7
t_{52}	TDI, TMS Hold Time	13.0		ns	23	7
t_{53}	TDO Valid Delay	2.8	20.0	ns	23	8
t_{54}	TDO Float Delay		25.0	ns	23	1, 8
t_{55}	All Non-Test Outputs Valid Delay	2.5	20.0	ns	23	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	23	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	23	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	23	3, 7, 10

NOTE: See Table 39 for table notes.

Table 39. Notes for Table 38

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100 percent tested. Guaranteed by design.
2. TTL input test waveforms are assumed to be 0 to 3-V transitions with 1 V/ns rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
5. 0.8 V/ns ≤ CLK input rise/fall time ≤ 8 V/ns.
6. 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55–58}$).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of two clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A31–A5 signals are sampled only on the CLK in which ADS# is active.
18. BF should be strapped to V_{CC3} or left floating.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. BUSCHK# is used as a reset configuration signal to select buffer size.
22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

Figure 18. Clock Waveform

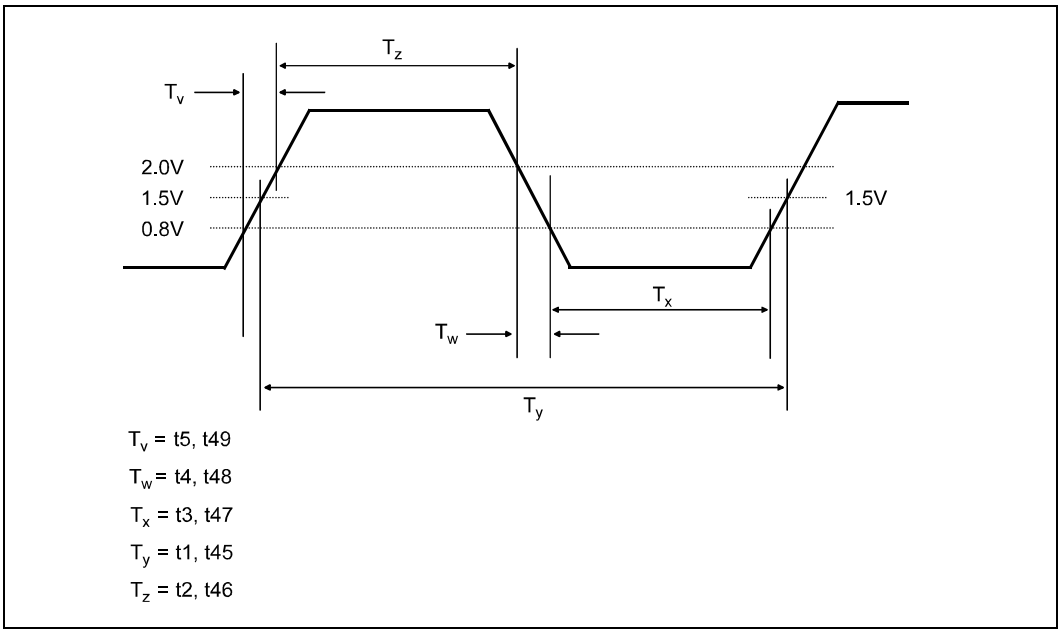


Figure 19. Valid Delay Timings

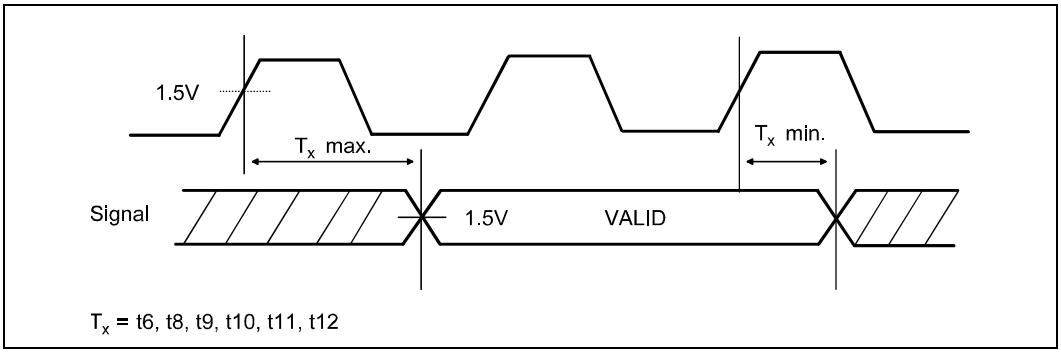


Figure 20. Float Delay Timings

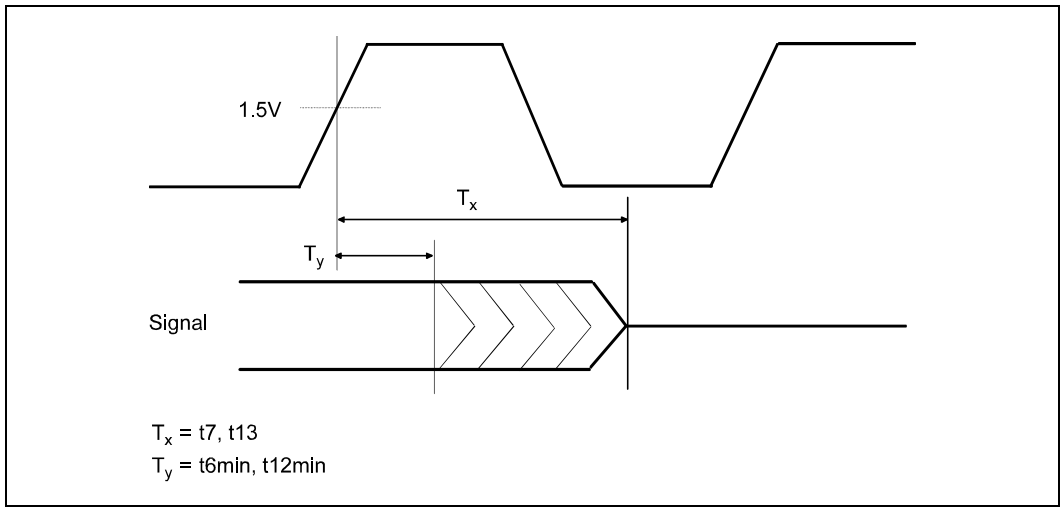


Figure 21. Setup and Hold Timings

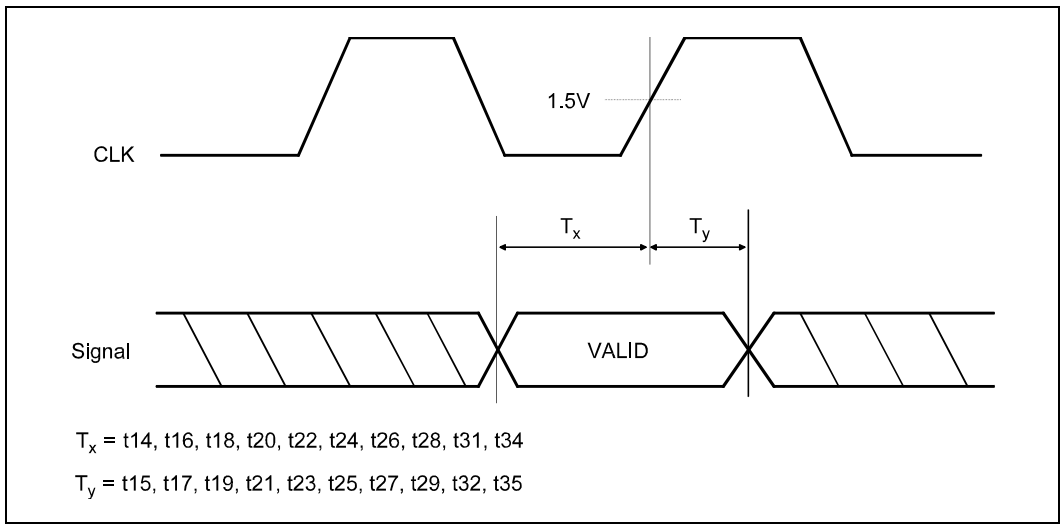


Figure 22. Reset and Configuration Timings

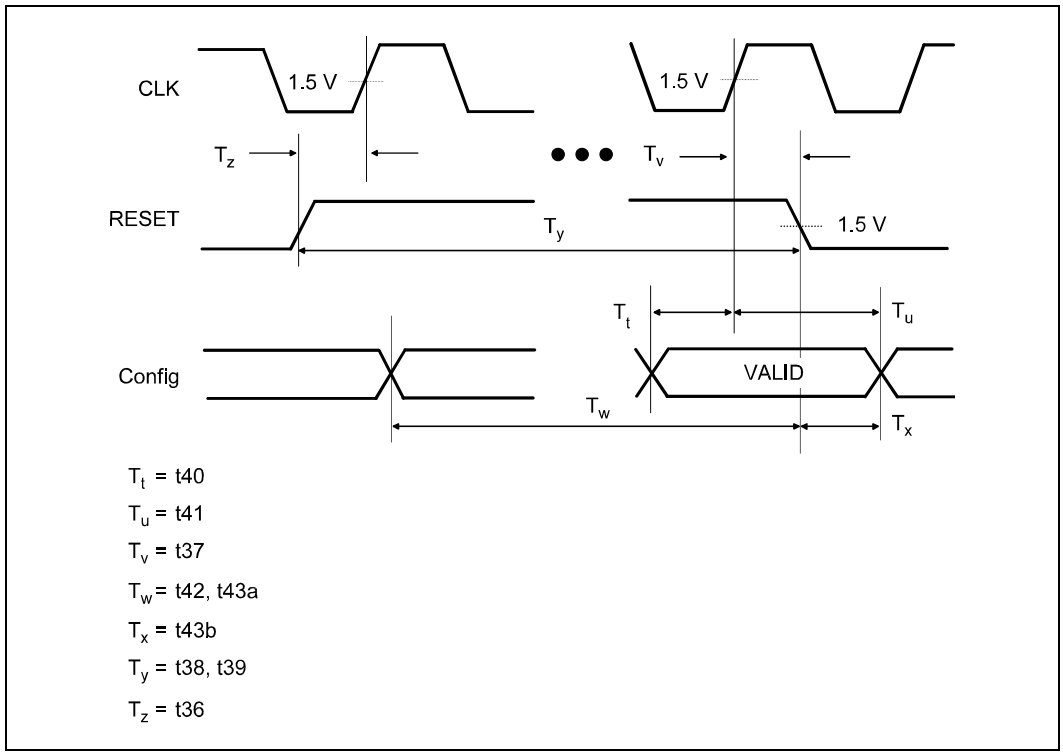


Figure 23. Test Timings

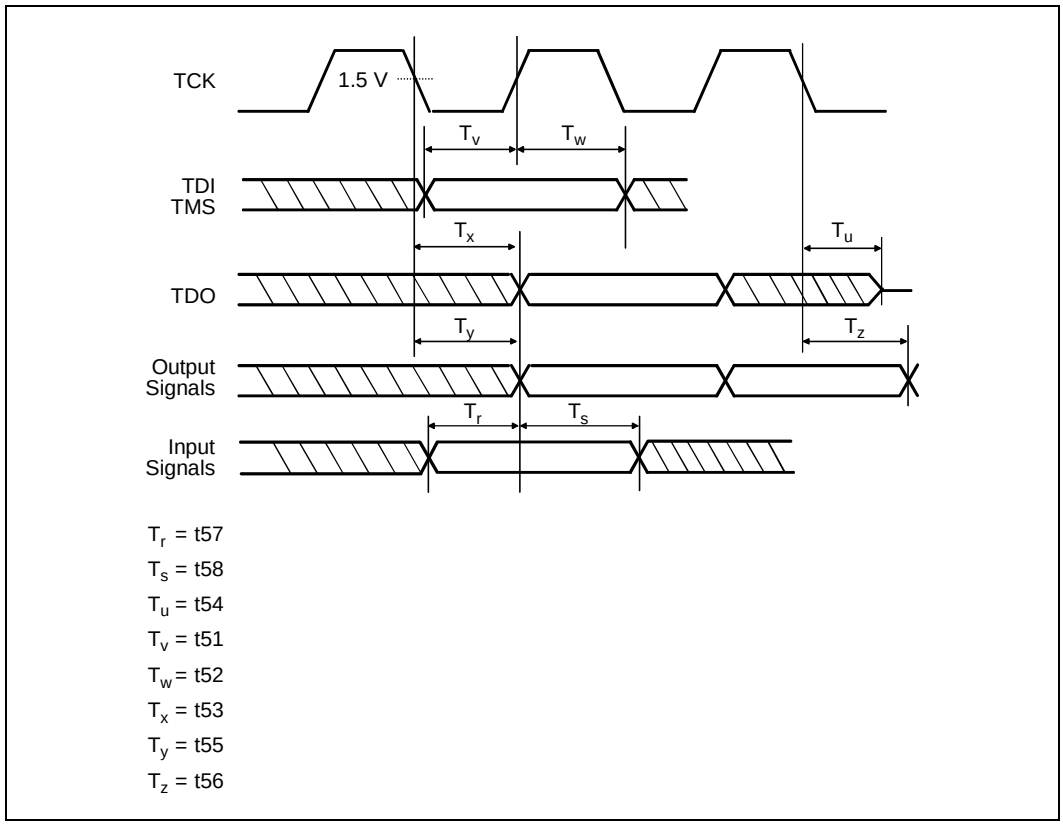
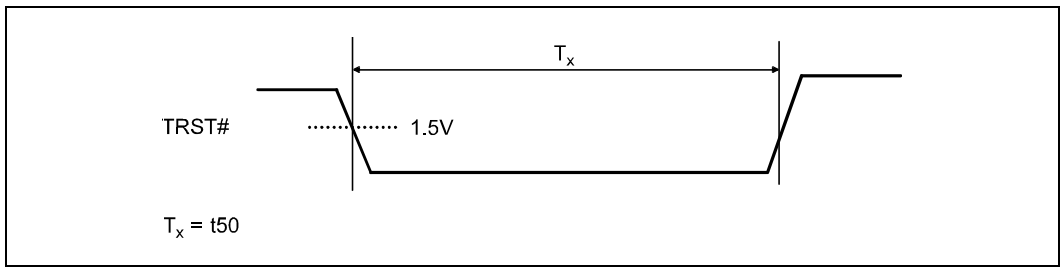


Figure 24. Test Reset Timings



5.4 I/O Buffer Models

This section describes the I/O buffer models of the embedded Pentium processor with voltage reduction technology.

The first-order I/O buffer model is a simplified representation of the complex input and output buffers used in the embedded Pentium processor with voltage reduction technology. Figure 25 and Figure 26 show the structure of the input buffer model and Figure 27 shows the output buffer model. Table 40 and Table 41 show the parameters used to specify these models.

Although simplified, these buffer models accurately model flight time and signal quality. For these parameters, there is very little added accuracy in the complete transistor model.

The following two models represent the input buffer models. The first model, Figure 25, represents all of the input buffers except for a special group of input buffers. The second model, Figure 26, represents these special buffers: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF# and CLK.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.

Figure 25. Input Buffer Model, Except Special Group

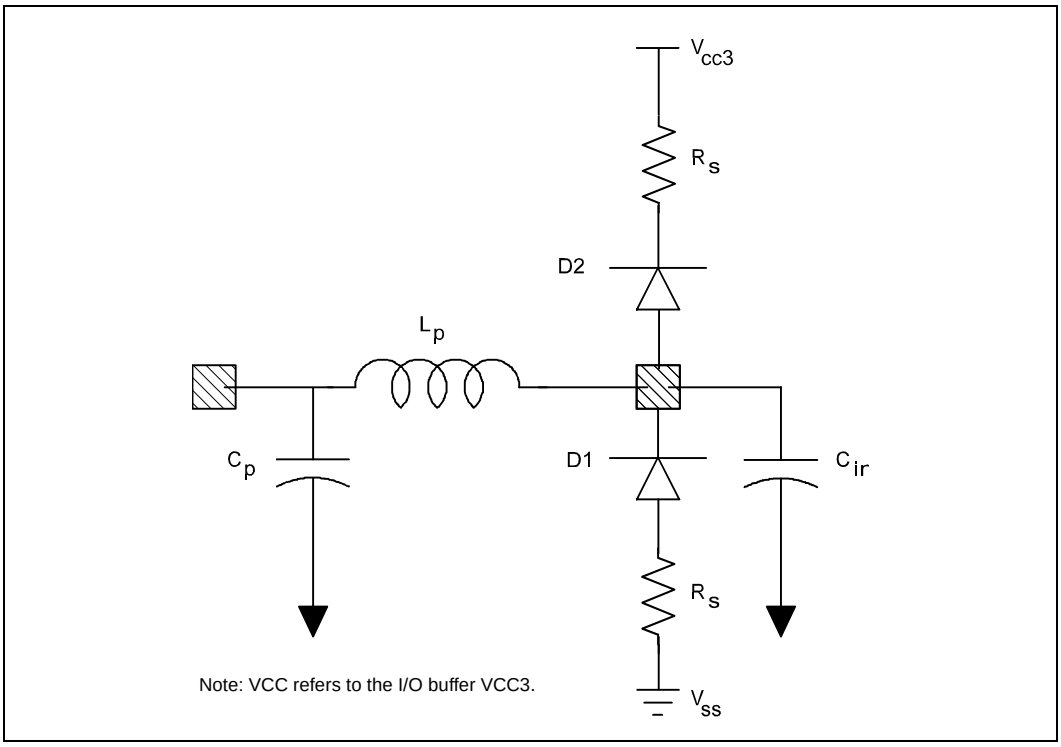


Figure 26. Input Buffer Model for Special Group

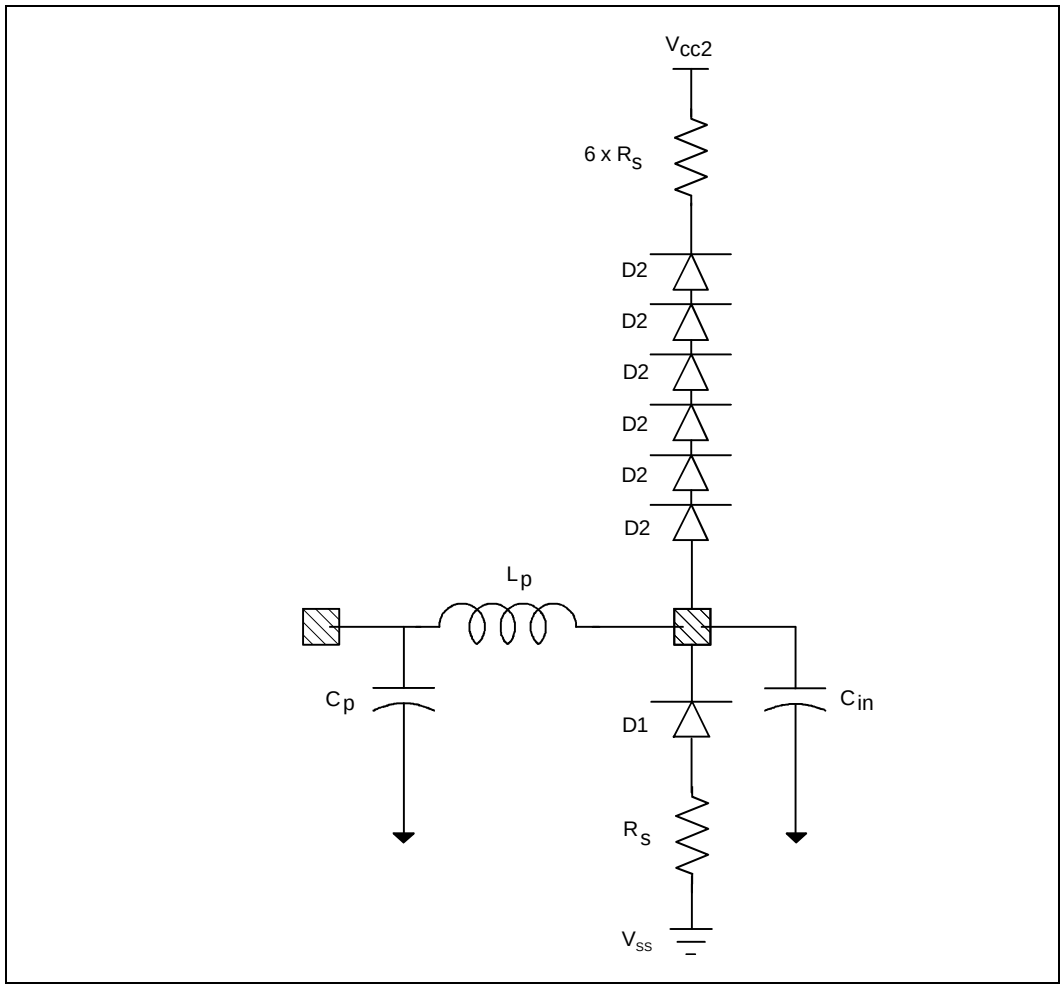


Table 40. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
C_{in}	Minimum and Maximum value of the capacitance of the input buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance
R_S	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 27 shows the structure of the output buffer model. This model is used for all of the output buffers of the embedded Pentium processor with voltage reduction technology.

Figure 27. First-Order Output Buffer Model

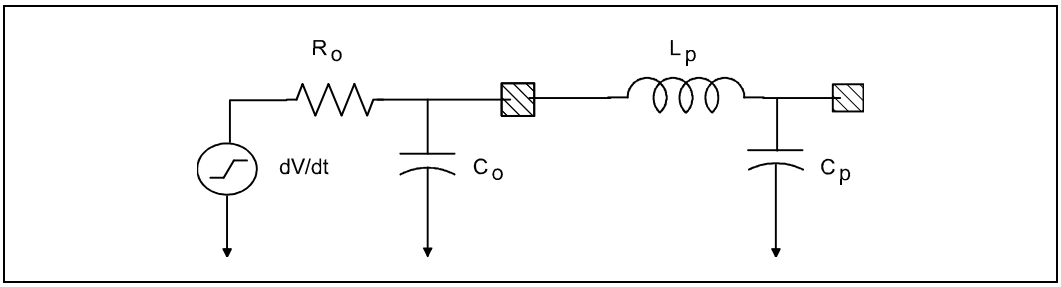


Table 41. Parameters Used in the Specification of the First-Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_o	Minimum and maximum value of the output impedance of the output buffer model
C_o	Minimum and Maximum value of the capacitance of the output buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance

5.4.1 Buffer Model Parameters

This section gives the parameters for each embedded Pentium processor with voltage reduction technology input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the embedded Pentium processor with voltage reduction technology have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 42 shows the drive level for BRDY# required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers get set to the same size during setup initialization.

The input, output and bidirectional buffer values of the embedded Pentium processor with voltage reduction technology are listed in Table 44. This table contains listings for all three types; do not confuse them during simulation. When a bidirectional pin is operating as an input, use the C_{in}, C_p and L_p values; when it is operating as a driver, use all of the data parameters.

Refer to Table 43 for the groupings of the buffers.

Table 42. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTE: For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

Table 43. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7#–BE5#, BP3–BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A31–A21, AP, BE4#–BE0#, CACHE#, D/C#, D63–D0, DP8–DP0, HLDA, LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A20–A3, ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

Table 44. Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/ns)		R_o (Ohms)		C_p (pF)		L_p (nH)		C_o/C_{in} (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					3.0	5.0	4.0	7.2	0.8	1.2
(input)	Falling					3.0	5.0	4.0	7.2	0.8	1.2
ER1	Rising					1.1	6.1	4.7	15.3	0.8	1.2
(input)	Falling					1.1	6.1	4.7	15.3	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.1	8.2	4.0	17.7	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.1	8.2	4.0	17.7	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.7	4.0	18.7	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.7	4.0	18.7	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.3	4.4	16.7	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	1.3	8.3	4.4	16.7	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	1.9	7.5	9.9	14.3	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.9	7.5	9.9	14.3	3.3	3.9

Table 45. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e–14 A	2.78e–16 A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983 V	0.967 V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

5.4.2 Signal Quality Specifications

Signals driven by the system into the embedded Pentium processor with voltage reduction technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: ringback and settling time.

5.4.2.1 Ringback

Excessive ringback can contribute to long-term degradation of the reliability of the embedded Pentium processor with voltage reduction technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC3} (or above V_{SS}) relative to the V_{CC3} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

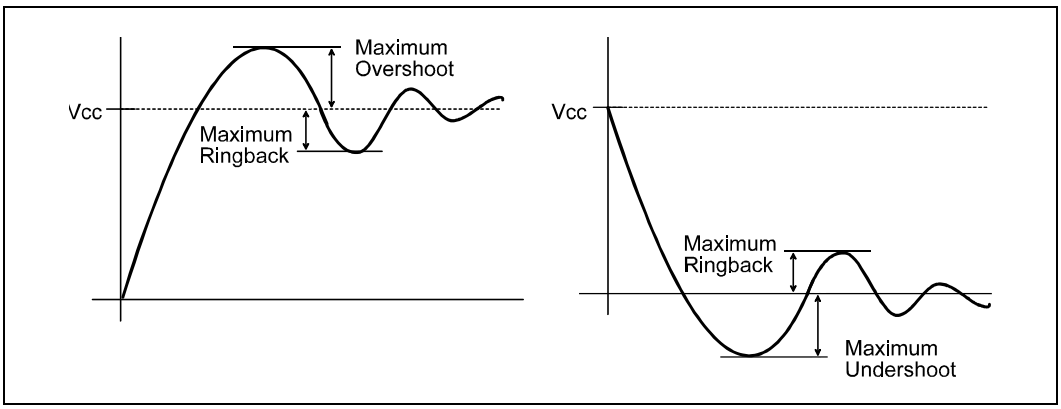
Maximum Ringback on Inputs = 0.8 V (with diodes)

If simulated without the input diodes, follow the maximum overshoot/undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively. If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC3} (below V_{SS}). The guideline assumes the absence of diodes on the input.

- The maximum overshoot/undershoot on the 3.3-V embedded Pentium processor with voltage reduction technology inputs (not CLK) = 1.4 V above V_{CC3} (without diodes)

Figure 28. Overshoot/Undershoot and Ringback Guidelines



5.4.2.2 Settling Time

The settling time is defined as the time required at the receiver for the signal to settle to within 10 percent of V_{CC3} or V_{SS}. Settling time is also the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects can dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, the settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur, simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

A typical design method would include a settling time that ensures that a signal is within 10 percent of V_{CC3} or V_{SS} for at least 2.5 ns prior to the end of the CLK period.

Figure 29. Settling Time