Embedded Pentium® Processor with Voltage Reduction Technology

Datasheet

Product Features

- Compatible with Large Software Base
  - — MS-DOS*, Windows*, OS/2*, UNIX*
- 32-Bit Processor with 64-Bit Data Bus
- Superscalar Architecture
  - — Two Pipelined Integer Units are Capable of Two Instructions/Clock
  - — Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - — 8-Kbyte Code, 8-Kbyte Write-Back Data
  - — MESI Cache Protocol
- Advanced Design Features
  - — Branch Prediction
  - — Virtual Mode Extensions
- Low-Voltage BiCMOS Silicon Technology
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Internal Error Detection Features
- SL Enhanced Power Management Features
  - — System Management Mode
  - — Clock Control
- Voltage Reduction Technology
  - — 3.1 V V_{CC} for Core Supply
  - — 3.3 V V_{CC} for I/O Buffer Supply
- Fractional Bus Operation
  - — 133-MHz Core/66-MHz Bus (iCOMP® Index 2.0 Rating of 111)†

†Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

The embedded Pentium® processor is fully compatible with the entire installed base of applications for DOS*, Windows*, OS/2*, and UNIX*, and all other software that runs on any earlier Intel 8086 family product. The embedded Pentium processor's superscalar architecture can execute two instructions per clock cycle. Branch prediction and separate caches also increase performance. Separate code and data caches reduce cache conflicts while remaining software transparent.

The embedded Pentium processor with voltage reduction technology has 3.3 million transistors. It is built on Intel's advanced low-voltage BiCMOS silicon technology, and has full SL Enhanced power management features, including System Management Mode (SMM) and clock control. The additional SL Enhanced features, 3.1 V core operation and 3.3 V I/O buffer operation, make the embedded Pentium processor with voltage reduction technology ideal for embedded designs.

Order Number: 273203-001
November 1998

Datasheet

Contents

Figures

Tables

Revision History

Date	Revision	Description
11/12/98	001	This is the first publication of this document

1.0 Introduction

The Intel® embedded Pentium® processor with voltage reduction technology is a reduced power version of the embedded Pentium processor. Voltage reduction technology allows the processor to interface with industry standard 3.3-volt components while its inner core, operating at 3.1 volts, consumes less power. The embedded Pentium processor with voltage reduction technology is available in a Staggered Pin Grid Array (SPGA) package. It has all the advanced features of the original Pentium processor except for the differences listed in "Differences from the Pentium Processor" on page 10.

The embedded Pentium processor with voltage reduction technology has several features that are ideal for embedded applications, including:

- 3.1-V core and 3.3-V I/O buffer V_{CC} inputs reduce power consumption significantly, while maintaining 3.3-V compatibility externally.
- The SL Enhanced feature set, which was initially implemented in the Intel486™ processor family.

The architecture and internal features of the embedded Pentium processor with voltage reduction technology are identical to the embedded Pentium processor specifications provided in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204), except that several features have been eliminated to streamline it for embedded applications.

This document should be used in conjunction with the following related embedded Pentium processor documents.

- *Embedded Pentium® Processor Family Developer's Manual* (order number: 273204)
- *Intel Architecture Software Developer's Manual*, Volumes 1–3 (order numbers 243190, 243191, and 243192)

2.0 Architecture Overview

The embedded Pentium processor with voltage reduction technology extends the Intel Pentium family of microprocessors. The embedded Pentium processor family consists of the embedded Pentium processor, the embedded Pentium processor with voltage reduction technology described in this document, the embedded Pentium processor with MMX™ technology, and the low-power embedded Pentium processor with MMX technology. "Pentium processor" is used in this document to refer to the entire Pentium processor family in general.

The embedded Pentium processor family architecture contains all the features of the Intel486 processor family, and provides significant enhancements including the following:

- Superscalar architecture
- Dynamic branch prediction
- Pipelined floating-point unit
- Improved instruction execution time
- Separate 8-Kbyte code and 8-Kbyte data caches
- Writeback MESI protocol in the data cache
- 64-Bit data bus
- Bus cycle pipelining

- Address parity
- Internal parity checking
- Execution tracing
- Performance monitoring
- IEEE 1149.1 boundary scan
- System Management Mode
- Virtual Mode extensions
- Voltage reduction technology
- SL Power management features

2.1 Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 processor family instruction set with extensions to accommodate some of the additional functionality of the Pentium processor. All application software written for the Intel386 and Intel486 family microprocessors runs on Pentium processors without modification. The on-chip memory management unit is completely compatible with the Intel386 family and Intel486 family of processors.

Pentium processors implement several enhancements to increase performance. The two instruction pipelines and the floating-point unit are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in Pentium processors. To support this, the processor has two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the BTB so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit (FPU) is up to ten times faster than the FPU used on the Intel486 processor for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache is 8 Kbytes with a 32-byte line size, and is two-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple-ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple-ported to support snooping and split-line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The cache can be enabled or disabled by software or hardware.

Pentium processors have a 64-bit data bus for fast data transfer. Burst read and burst writeback cycles are supported. In addition, bus cycle pipelining has been added to allow two bus cycles to occur simultaneously. The Memory Management Unit contains optional extensions to the architecture which allow 2-Mbyte and 4-Mbyte page sizes.

Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

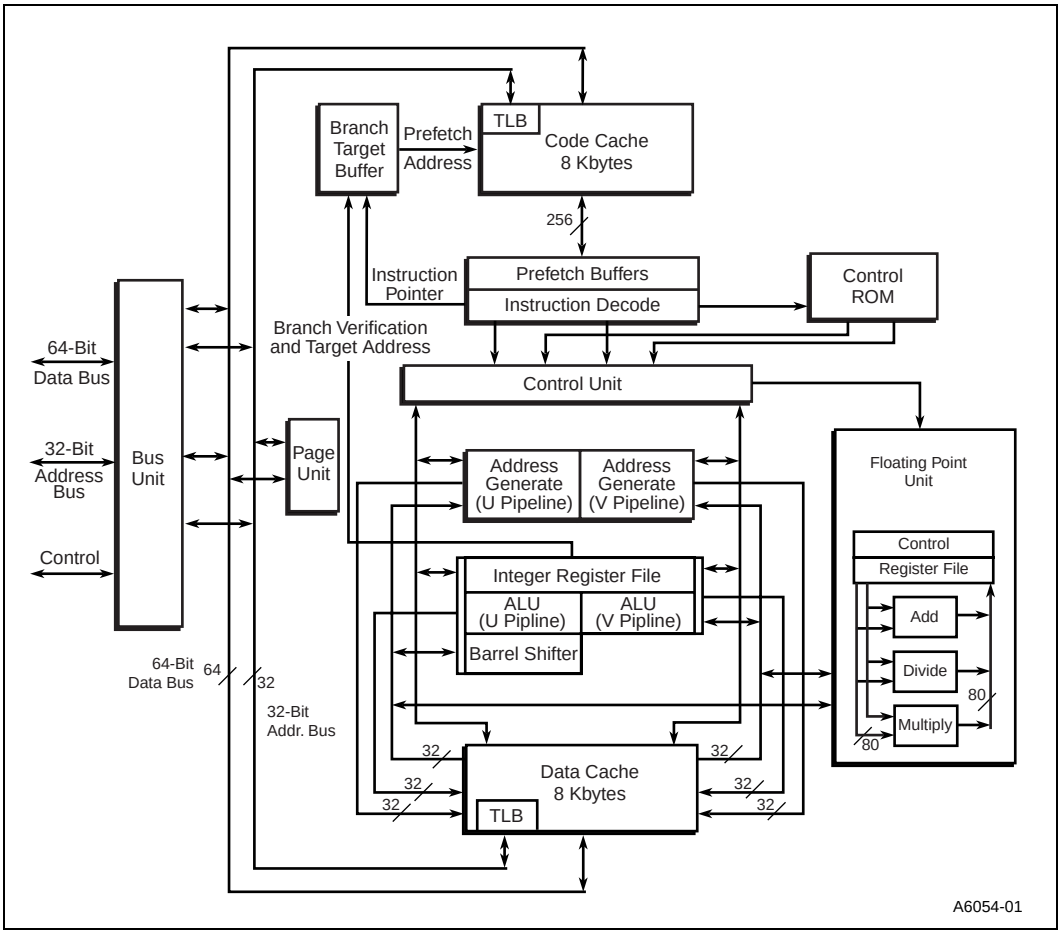
In addition, Pentium processors have implemented functional redundancy checking to provide maximum error detection of the processor and the interface to the processor. When functional redundancy checking is used, a second processor, the “checker” executes in lock-step with the “master” processor. The checker samples the master’s outputs, compares those values with the values it computes internally, and asserts an error signal if a mismatch occurs.

As more and more functions are integrated on-chip, the complexity of board level testing is increased. To address this, Pentium processors have increased test and debug capability. Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, Pentium processors provide four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 is a block diagram of the embedded Pentium processor with voltage reduction technology.

Figure 1. Pentium® Processor with Voltage Reduction Technology Block Diagram



The block diagram shows the two instruction pipelines, the “u” pipe and the “v” pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple-ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the processor can execute the instruction. The control ROM contains microcode to control the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

The Pentium processor supports clock control. When the clock to the processor is stopped, power dissipation is virtually eliminated. This makes the Pentium processor a good choice for energy-efficient designs.

The Pentium processor supports fractional bus operation. This allows the processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The Pentium processor contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

The processor’s architectural features are more fully described in the *Embedded Pentium® Processor Family Developer’s Manual* (order number 273204).

3.0 Packaging Information

3.1 Differences from the Pentium Processor

To better streamline the processor for embedded applications, the following features have been eliminated from the embedded Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 1 lists the corresponding pins that exist on the SPGA 3.3-V Pentium processor but have been removed from the embedded Pentium processor with voltage reduction technology.

Table 1. Signals Removed from the Pentium® Processor with Voltage Reduction Technology

Signal	Function
ADSC#	**Additional Address Status.** This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	**Additional Burst Ready.** This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	**CPU Type.** This signal is used for dual processing systems.
D/P#	**Dual/Primary processor identification.** This signal is only used for an upgrade processor.
FRCMC#	**Functional Redundancy Checking.** This signal is only used for error detection via processor redundancy, and requires two Pentium processors (master/checker).
PBGNT#	**Private Bus Grant.** This signal is only used for dual processing systems.
PBREQ#	**Private Bus Request.** This signal is used only for dual processing systems.
PHIT#	**Private Hit.** This signal is only used for dual processing systems.
PHITM#	**Private Modified Hit.** This signal is only used for dual processing systems.
PICCLK	**APIC Clock.** This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	**APIC's Programmable Interrupt Controller Data line 0.** PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	**APIC's Programmable Interrupt Controller Data line 1.** PICD1 shares a pin with APICEN (APIC Enable (on RESET)).

3.2 Pinout

The embedded Pentium processor with voltage reduction technology package has a pin array that is mechanically identical to the SPGA version of the 3.3-V Pentium processor, but some pins need to be connected differently. Table 1 lists the SPGA embedded Pentium processor with voltage reduction technology pins that are different from the SPGA 3.3-V Pentium processor.

The signals listed in Table 1 are now No Connect pins on the embedded Pentium processor with voltage reduction technology. Leave these pins unconnected. Table 4 includes the list of NC pins. Connection of these pins may result in component failure or incompatibility with processor steppings.

Note: The V_{CC2} pins are 3.1 V for the SPGA embedded Pentium processor with voltage reduction technology.

Figure 2 is the pin side SPGA pinout diagram. For a brief functional description of the pins, refer to Table 5. Additional Input and Output pin information is provided in Table 6, Table 7, and Table 8.

Figure 2. SPGA Pentium® Processor with Voltage Reduction Technology Pinout (Top Side View)

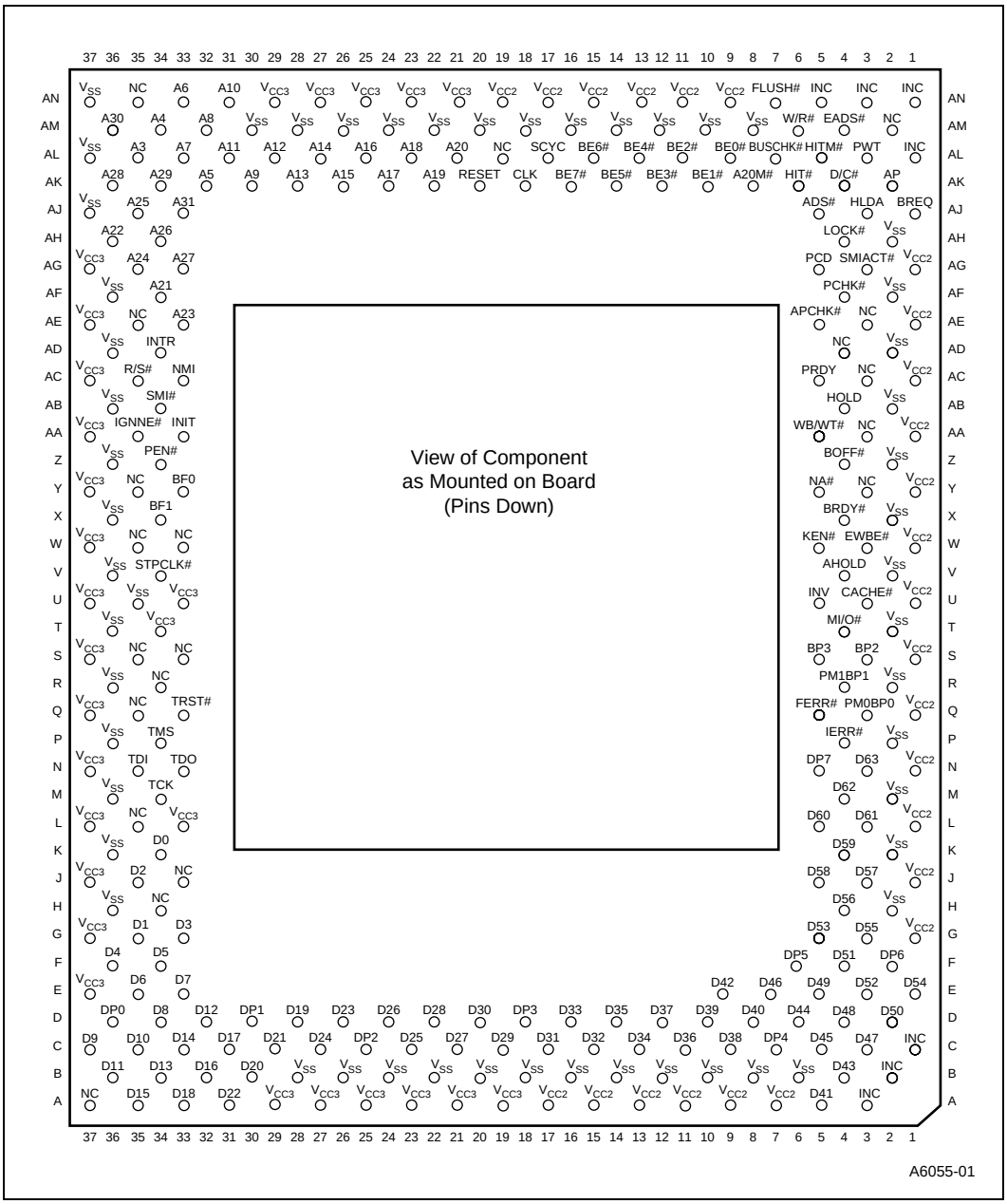
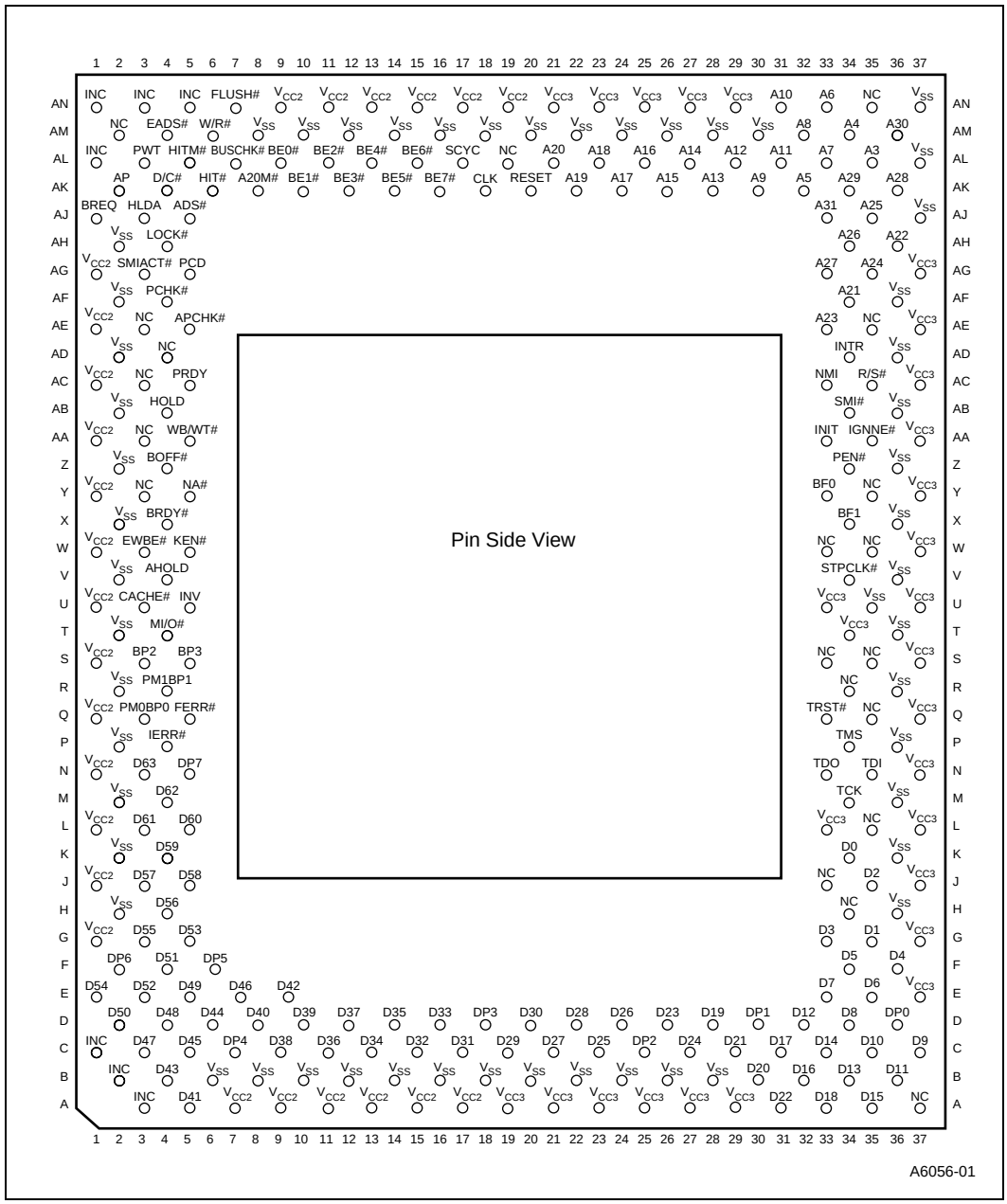


Figure 3. SPGA Pentium® Processor with Voltage Reduction Technology Pinout (Pin Side View)



3.2.1 Pin Cross Reference

Table 2. Pin Cross-Reference by Pin Name — Address and Data Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 3. Pin Cross-Reference by Pin Name — Control Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location
A20M#	AK08	NC	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	HIT#	AK06	PM0/BP0	Q03
NC	AM02	BUSCHK#	AL07	HITM#	AL05	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HLDA	AJ03	PRDY	AC05
AP	AK02	NC	Q35	HOLD	AB04	PWT	AL03
APCHK#	AE05	D/C#	AK04	IERR#	P04	R/S#	AC35
BE0#	AL09	NC	AE35	IGNNE#	AA35	RESET	AK20
BE1#	AK10	DP0	D36	INIT	AA33	SCYC	AL17
BE2#	AL11	DP1	D30	INTR/LINT0	AD34	SMI#	AB34
BE3#	AK12	DP2	C25	INV	U05	SMIACT#	AG03
BE4#	AL13	DP3	D18	KEN#	W05	TCK	M34
BE5#	AK14	DP4	C07	LOCK#	AH04	TDI	N35
BE6#	AL15	DP5	F06	M/IO#	T04	TDO	N33
BE7#	AK16	DP6	F02	NA#	Y05	TMS	P34
BOFF#	Z04	DP7	N05	NMI/LINT1	AC33	TRST#	Q33
BP2	S03	EADS#	AM04	PCD	AG05	W/R#	AM06
BP3	S05	EWBE#	W03	PCHK#	AF04	WB/WT#	AA05
BRDY#	X04	FERR#	Q05				
Clock Control							
CLK	AK18	BF0	Y33	BF1	Y35	STPCLK#	V34

Table 4. No Connect, Power and Ground Pins

V_{CC2}[1]				
A07	A17	Q01	AA01	AN19
A09	G01	S01	AC01	AN15
A11	J01	U01	AE01	AG01
A13	L01	W01	AN11	AN09
A15	N01	Y01	AN13	AN17
V_{CC3}				
A19	AA37	AN25	L33	U33
A21	AC37	AN27	L37	U37
A23	AE37	AN29	N37	W37
A25	AG37	E37	Q37	Y37
A27	AN21	G37	S37	
A29	AN23	J37	T34	
No Connect (NC)[2]				
A37	AE03	AN35	Q35	W33
AA03	AE35	H34	R34	W35
AC03	AL19	J33	S33	Y03
AD04	AM02	L35	S35	

NOTE:
1. These V_{CC2} pins are 3.3-V V_{CC} pins for the SPGA 3.3-V Pentium® processor. For the SPGA embedded Pentium processor with voltage reduction technology, these pins are 3.1-V V_{CC2} supplies for the SPGA core.
2. These NC pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

3.2.2 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.2.3 Pin Quick Reference

This section gives a brief functional description of each pin. For a detailed description, see the "Hardware Interface" chapter in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204). Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

Table 5. Pin Quick Reference

Symbol	Type	Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor emulates the address wraparound at 1 Mbyte that occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31–A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock in which the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that the correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#–BE5# BE4#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the processor for the current cycle. The byte enables are driven in the same clock as the address lines (A31–A3).
BF1–BF0	I	**Bus Frequency** determines the bus-to-core ratio. The bus frequency pins are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the embedded Pentium processor with voltage reduction technology, the BF1 pin should be strapped high, and the BF0 pin should be strapped low. This sets the bus-to-core ratio at 1/2. Other combinations are reserved.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
BP3–BP2 PM1/BP1– PM0/BP0	O	The **breakpoint** pins (BP3–BP0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.

Table 5. Pin Quick Reference

Symbol	Type	Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor does not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor's external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, and TRST# are specified with respect to the rising edge of CLK. It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the processor is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the processor samples the data bus when BRDY# is returned.
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the embedded Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63–D56; DP0 applies to D7–D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle is generated by the processor indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.

Table 5. Pin Quick Reference

Symbol	Type	Function
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after an inquire cycle that results in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA is driven inactive and the processor resumes driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock in which HLDA is deasserted.
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	The **ignore numeric error** input has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0 and the IGNNE# pin is asserted, the processor ignores any pending unmasked numeric exception and continues executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to ensure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock in which EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor does not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back-to-back locked cycles.

Table 5. Pin Quick Reference

Symbol	Type	Function
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to “1”, the processor will vector to the machine check exception before the beginning of the next instruction.
PM1/BP1–PM0/BP0	O	These pins function as part of the performance monitoring feature. The **breakpoint 1**–**0** pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine whether the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The **run/stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if three-state test mode will be entered or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles that are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.

Table 5. Pin Quick Reference

Symbol	Type	Function
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the embedded Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the processor recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2	I	These pins are the **3.1 V power inputs** to the embedded Pentium processor with voltage reduction technology.
VCC3	I	These pins are the **3.3 V power inputs** to the embedded Pentium processor with voltage reduction technology.
VSS	I	These pins are the **ground inputs** to the embedded Pentium processor with voltage reduction technology.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

3.2.4 Pin Reference Tables

Table 6. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE: All output and input/output pins are floated during three-state test mode (except TDO).

Table 7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

Table 8. Input/Output Pins

Name	Active Level	When Floated[1]	Qualified (when an input)	Internal Resistor
A31–A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#–BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown[2]
D63–D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7–DP0	n/a	Bus Hold, BOFF#	BRDY#	

NOTES:
1. All output and input/output pins are floated during three-state test mode (except TDO).
2. BE3#–BE0# have pulldowns during RESET only.

3.2.5 Pin Grouping According to Function

Table 9 organizes the pins with respect to their function.

Table 9. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

3.3 Mechanical Specifications

The embedded Pentium processor with voltage reduction technology is offered in an SPGA package without a heat spreader. The package is mechanically equivalent to the package used on the 3.3-V Pentium processor C2 stepping except that the SPGA embedded Pentium processor with voltage reduction technology will use a metal lid instead of a ceramic lid, and has the dimensions shown in Figure 4.

Figure 4. 296-Pin Staggered Pin Grid Array Package (SPGA)

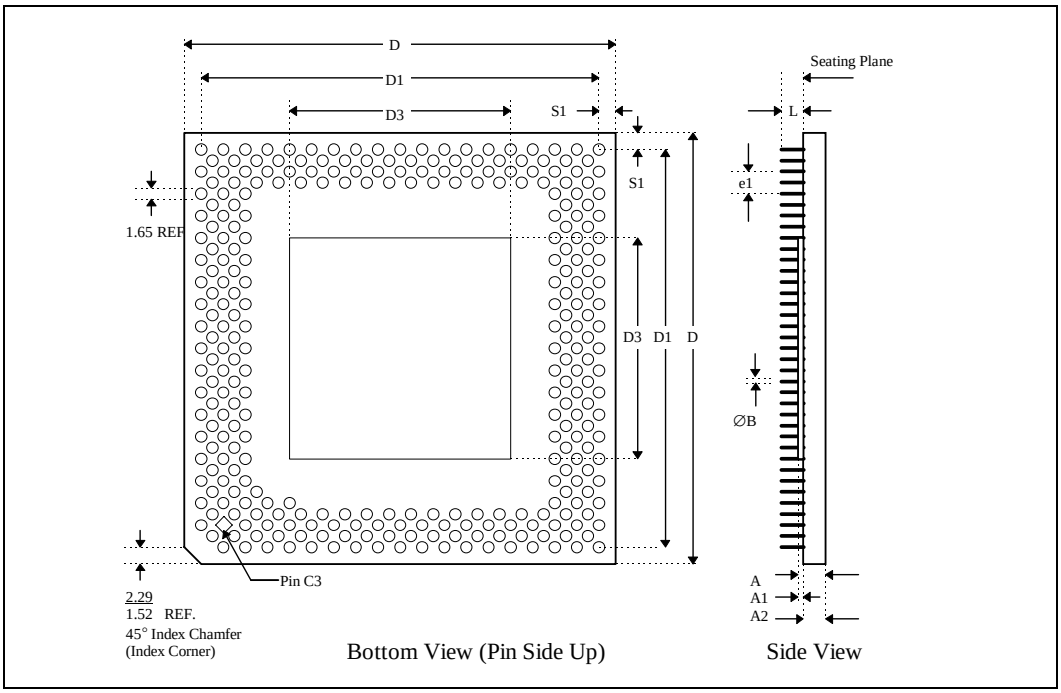


Table 10. 296-Pin Staggered Pin Grid Array Package Dimensions Key

	Millimeters			Inches		
Symbol	**Min**	**Max**	**Notes**	**Min**	**Max**	**Notes**
A	3.27	3.83	Metal Lid	0.129	0.151	Metal Lid
A1	0.66	0.86	Metal Lid	0.026	0.034	Metal Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

3.4 Thermal Specifications

The SPGA embedded Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE} (T_C), is within the specified range of 0° C to 85° C.

The power dissipation specification in Table 11 is provided for designing thermal solutions for operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is provided to assist in the design of a thermal solution for the device.

Table 11. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical[1]	Max[2]	Unit	Notes
Active Power Dissipation	3.0–4.0	7.9	Watts	
Stop Grant and Auto Halt Powerdown Power Dissipation		1.3	Watts	Note 3
Stop Clock Power Dissipation	0.02	0.05	Watts	Note 4

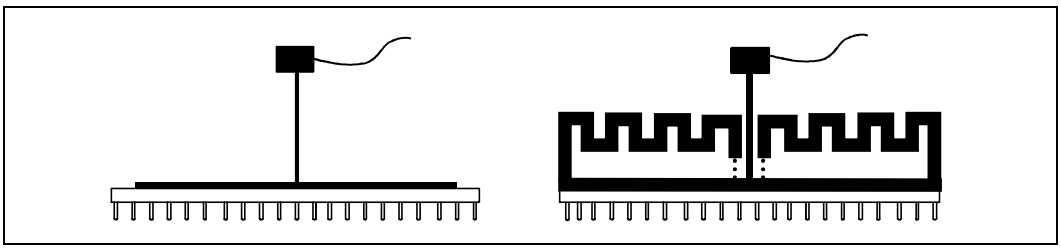
NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at V_{CC2} = 3.1 V and V_{CC3} = 3.3 V running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum Active Power Dissipation. It is determined using a worst-case instruction mix with V_{CC2} = 3.1 V and V_{CC3} = 3.3 V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

3.4.1 Measuring Thermal Values

To verify that the proper case temperature (T_C) is maintained for the embedded Pentium processor with voltage reduction technology, it should be measured at the center of the package top surface (encapsulant). To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done by using Omega Bond (part number: OB-100).
- Attach the thermocouple at a 90° angle as shown in Figure 5.

Figure 5. Technique for Measuring Case Temperature (T_C)



3.4.2 Thermal Equations

For the embedded Pentium processor with voltage reduction technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only requirement is that the case temperature (T_C) is met. To calculate T_A values, use the following equations:

$T_A = T_C – (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} – \theta_{JC}$

where,

T_A and T_C = ambient and case temperature (°C)
θ_{CA} = case-to-ambient thermal resistance (°C/W)
θ_{JA} = junction-to-ambient thermal resistance (°C/W)
θ_{JC} = junction-to-case thermal resistance (°C/W)
P = maximum power consumption in Watts (see Table 11)

Table 12 lists the θ_{CA} values for the Pentium processor with passive heatsinks.

Thermal data collection parameters:

- Heatsinks are omnidirectional pin aluminum alloy
- Features were based on standard extrusion practices for a given height
- Pin size ranged from 50 to 129 mils
- Pin spacing ranged from 93 to 175 mils
- Base thickness ranged from 79 to 200 mils
- Heatsink attach was 0.005" of thermal grease
- Using an attach thickness of 0.002” improves performance by approximately 0.3 °C/W

Table 12. Thermal Resistances for Embedded Pentium® Processors with Voltage Reduction Technology

Heatsink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (Linear ft/min)					
		0	100	200	400	600	800
0.25	1.25	9.4	8.3	6.9	4.7	3.9	3.3
0.35	1.25	9.1	7.8	6.3	4.3	3.6	3.1
0.45	1.25	8.7	7.3	5.6	3.9	3.2	2.8
0.55	1.25	8.4	6.8	5.0	3.5	2.9	2.6
0.65	1.25	8.0	6.3	4.6	3.3	2.7	2.4
0.80	1.25	7.3	5.6	4.2	2.9	2.5	2.3
1.00	1.25	6.6	4.9	3.9	2.9	2.4	2.1
1.20	1.25	6.2	4.6	3.6	2.7	2.3	2.1
1.40	1.25	5.7	4.2	3.3	2.5	2.2	2.0
Without Heatsink	1.7	14.5	13.8	12.6	10.5	8.6	7.5

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended operation beyond the maximum ratings may affect device reliability. Furthermore, although the embedded Pentium processor with voltage reduction technology contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 13. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
3 V Supply voltage with respect to V_{SS}	–0.5 V to +4.6 V
3.1 V Supply voltage with respect to V_{SS}	–0.5 V to +4.1 V
3 V Only Buffer DC Input Voltage	–0.5 V to V_{CC3} +0.5; not to exceed 4.6 V[1]
5 V Safe Buffer DC Input Voltage	–0.5 V to 6.5 V[2, 3]

NOTES:
1. Applies to all SPGA embedded Pentium® processor with voltage reduction technology inputs except CLK.
2. Applies to CLK.
3. See Table 15.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only.

4.2 DC Specifications

Tables 14, 15 and 16 list the DC specifications that apply to the embedded Pentium processor with voltage reduction technology. The embedded Pentium processor with voltage reduction technology core operates at 3.1 V internally while the I/O interface operates at 3.3 V. The CLK input may be at 3.3 V or 5 V. Since the 3.3-V (5-V safe) input levels defined in Table 15 are the same as the 5-V TTL levels, the CLK input is compatible with existing 5V clock drivers.

Table 14. DC Specifications

T_{CASE} = 0 to 85° C; V_{CC2} = 3.1 V ± 165 mV; V_{CC3} = 3.3 V ± 165 mV

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level, Note 1
V_{IH3}	Input High Voltage	2.0	V_{CC3}+0.3	V	TTL Level, Note 1
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, Note 1, Note 2
V_{OH3}	Output High Voltage	2.4		V	TTL Level, Note 1, Note 3
I_{CC2}	Power Supply Current from 3.1-V core supply		2775	mA	Note 4
I_{CC3}	Power Supply Current from 3.3-V I/O buffer supply		355	mA	Note 4

NOTES:
1. 3.3-V TTL levels apply to all signals except CLK.
2. Parameter measured at 4 mA.
3. Parameter measured at 3 mA.
4. This value should be used for power supply design. It was estimated for a worst-case instruction mix and V_{CC2} = 3.1 V ± 165 mV and V_{CC3} = 3.3 V ± 165 mV. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from stop clock to full active modes.

Table 15. 3.3-V (5-V Safe) DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL5}	Input Low Voltage	–0.3	0.8	V	TTL Level; applies to CLK only
V_{IH5}	Input High Voltage	2.0	5.55	V	TTL Level; applies to CLK only

Table 16. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	Guaranteed by design.
C_O	Output Capacitance		20	pF	Guaranteed by design.
$C_{I/O}$	I/O Capacitance		25	pF	Guaranteed by design.
C_{CLK}	CLK Input Capacitance		15	pF	Guaranteed by design.
C_{TIN}	Test Input Capacitance		15	pF	Guaranteed by design.
C_{TOUT}	Test Output Capacitance		20	pF	Guaranteed by design.
C_{TCK}	Test Clock Capacitance		15	pF	Guaranteed by design.
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (for input without pull up or pull down resistors)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{CC3}$ (for input without pull up or pull down resistors)
I_{IH}	Input Leakage Current		200	µA	V_{IN} = 2.4 V (for input with pull down resistors)
I_{IL}	Input Leakage Current		–400	µA	V_{IN} = 0.4 V (for input with pull up resistors)

4.2.1 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both on or both off within one second of each other.

4.3 AC Specifications

The AC specifications of the embedded Pentium processor with voltage reduction technology consist of setup times, hold times, and valid delays at 0 pF. All embedded Pentium processors with voltage reduction technology AC specifications are valid for V_{CC2} = 3.1 V $\pm$ 165 mV, V_{CC3} = 3.3 V $\pm$ 165 mV, and T_{CASE} = 0º C to 85º C.

4.3.1 Power and Ground

For clean on-chip power distribution, the embedded Pentium processor with voltage reduction technology has 25 V_{CC2} (3.1-V power), 28 V_{CC3} (3.3-V power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC2}, V_{CC3} and V_{SS} pins of the processor. On the circuit board, all V_{CC2} pins must be connected to a 3.1-V V_{CC2} plane (or island) and all V_{CC3} pins must be connected to a 3.3-V V_{CC3} plane. All V_{SS} pins must be connected to a V_{SS} plane. Refer to Table 4 for a list of V_{CC2} and V_{CC3} pins.

4.3.2 Decoupling Recommendations

Transient power surges occur as the processor is executing instruction sequences or driving large loads. To mitigate these high frequency transients, liberal high frequency decoupling capacitors should be placed near the processor.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by minimizing the length of circuit board traces between the processor and the decoupling capacitors.

These capacitors should be evenly distributed around each component on the 3.3-V plane and the 3.1-V plane (or island). Capacitor values should be chosen to ensure that they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low power consumption level to a much higher level (or high to low). A typical example would be entering or exiting the Stop Grant state. Other examples include executing a HALT instruction (which causes the processor to enter the Auto HALT Powerdown state) or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor. Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Several bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µF range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point at which the regulated power supply output can react to the change in load. In order to reduce the net ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor (on the 3.3-V plane and the 3.1-V plane or island) to ensure that these supply voltages stay within specified limits during changes in the power demands of the processor during operation.

For more detailed information, please contact Intel or refer to the *Pentium® Processor with Voltage Reduction Technology: Power Supply Design Considerations for Mobile Systems* application note (order number 242558).

Note: Capacitors degrade over time during use. As capacitors age, their capacity to store and hold a charge becomes compromised. Designing a board with below minimum acceptable bypass and bulk capacitors may have future system reliability consequences.

4.3.3 Connection Specifications

All NC pins must remain unconnected. Refer to Table 4 for a list of NC pins.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to ground.

4.3.4 AC Timings

The AC specifications given in Table 17 consist of output delays, input setup requirements and input hold requirements for the 66-MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 V for both 0 and 1 logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct operation.

Table 17. AC Specifications (Sheet 1 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz		
t_{1a}	CLK Period	15.0	30.0	ns	6	
t_{1b}	CLK Period Stability		±250	ps		1, 19
t_2	CLK High Time	4.0		ns	6	@2 V, Note 1
t_3	CLK Low Time	4.0		ns	6	@0.8 V, Note 1
t_4	CLK Fall Time	0.15	1.5	ns	6	2.0 V–0.8 V, Note 1
t_5	CLK Rise Time	0.15	1.5	ns	6	0.8 V–2.0 V, Note 1
t_{6a}	PWT, PCD, BE7#–BE0#, D/C#, W/R#, CACHE#, SCYC Valid Delay	1.0	7.0	ns	7	
t_{6b}	AP Valid Delay	1.0	8.5	ns	7	
t_{6c}	LOCK# Valid Delay	1.1	7.0	ns	7	
t_{6d}	ADS# Valid Delay	1.0	6.0	ns	7	
t_{6e}	A31–A3 Valid Delay	1.1	6.3	ns	7	
t_{6f}	M/IO# Valid Delay	1.0	5.9	ns	7	

NOTE: See Table 18 for table notes.

Table 17. AC Specifications (Sheet 2 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	8	1
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	7	4
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	7	4
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	7	4
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	7	4
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	7	4
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	7	
t_{10b}	HITM# Valid Delay	1.1	6.0	ns	7	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	7	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	7	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.3	7.5	ns	7	
t_{13}	D63–D0, DP3–DP0 Write Data Float Delay		10.0	ns	8	1
t_{14}	A31–A5 Setup Time	6.0		ns	9	20
t_{15}	A31–A5 Hold Time	1.0		ns	9	
t_{16a}	INV, AP Setup Time	5.0		ns	9	
t_{16b}	EADS# Setup Time	5.0		ns	9	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	9	
t_{18a}	KEN# Setup Time	5.0		ns	9	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	9	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	9	
t_{20}	BRDY# Setup Time	5.0		ns	9	
t_{21}	BRDY# Hold Time	1.0		ns	9	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	9	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	9	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	9	
t_{24b}	PEN# Setup Time	4.8		ns	9	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	9	
t_{25b}	HOLD Hold Time	1.5		ns	9	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	9	11, 15
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	9	12
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	9	11, 15, 16

NOTE: See Table 18 for table notes.

Table 17. AC Specifications (Sheet 3 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	9	12
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs		14, 16
t_{31}	R/S# Setup Time	5.0		ns	9	11, 15, 16
t_{32}	R/S# Hold Time	1.0		ns	9	12
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs		14, 16
t_{34}	D63–D0, DP7–DP0 Read Data Setup Time	2.8		ns	9	
t_{35}	D63–D0, DP7–DP0 Read Data Hold Time	1.5		ns	9	
t_{36}	RESET Setup Time	5.0		ns	10	11, 15
t_{37}	RESET Hold Time	1.0		ns	10	12
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	10	16
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	10	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	10	11, 15, 16
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	10	12
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	10	To RESET falling edge, Note 15
t_{42b}	Reset Configuration Signals (INIT, FLUSH#, BRDY#, BUSCHK#) Hold Time, Async.	2.0		CLKs	10	To RESET falling edge, Note 21
t_{42c}	Reset Configuration Signal (BRDY#, BUSCHK#) Setup Time, Async.	3.0		CLKs	10	To RESET falling edge, Note 21
t_{43a}	BF Setup Time	1.0		mS	10	To RESET falling edge, Note 18
t_{43b}	BF Hold Time	2.0		CLKs	10	To RESET falling edge, Note 18
t_{43c}	BE4# Setup Time	2.0		CLKs	10	To RESET falling edge
t_{43d}	BE4# Hold Time	2.0		CLKs	10	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		ns	6	
t_{46}	TCK High Time	25.0		ns	6	@2 V, Note 1
t_{47}	TCK Low Time	25.0		ns	6	@0.8 V, Note 1
t_{48}	TCK Fall Time		5.0	ns	6	2.0 V–0.8 V, Notes 1, 8, 9
t_{49}	TCK Rise Time		5.0	ns	6	0.8 V–2.0 V, Notes 1, 8, 9

NOTE: See Table 18 for table notes.

Table 17. AC Specifications (Sheet 4 of 4)

V_{CC2} = 3.1 V ±165 mV; V_{CC3} = 3.3 V ±165 mV; T_{CASE} = 0° C to 85° C; CL = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{50}	TRST# Pulse Width	40.0		ns	12	Asynchronous, Note 1
t_{51}	TDI, TMS Setup Time	5.0		ns	11	7
t_{52}	TDI, TMS Hold Time	13.0		ns	11	7
t_{53}	TDO Valid Delay	2.8	20.0	ns	11	8
t_{54}	TDO Float Delay		25.0	ns	11	1, 8
t_{55}	All Non-Test Outputs Valid Delay	2.5	20.0	ns	11	3, 8, 10
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	11	1, 3, 8, 10
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	11	3, 7, 10
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	11	3, 7, 10

NOTE: See Table 18 for table notes.

Table 18. Notes for Table 17

NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

1. Not 100 percent tested. Guaranteed by design.
2. TTL input test waveforms are assumed to be 0 to 3-V transitions with 1 V/ns rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
5. 0.8 V/ns ≤ CLK input rise/fall time ≤ 8 V/ns.
6. 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During probe mode operation, do not use the boundary scan timings ($t_{55–58}$).
11. Setup time is required to guarantee recognition on a specific clock.
12. Hold time is required to guarantee recognition on a specific clock.
13. All TTL timings are referenced from 1.5 V.
14. To guarantee proper asynchronous recognition, the signal must have been deasserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
15. This input may be driven asynchronously.
16. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be deasserted (inactive) for a minimum of two clocks before being returned active.
17. The D/C#, M/IO#, W/R#, CACHE#, and A31–A5 signals are sampled only on the CLK in which ADS# is active.
18. BF should be strapped to V_{CC3} or left floating.
19. These signals are measured on the rising edge of adjacent CLKs at 1.5 V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices.
20. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
21. BUSCHK# is used as a reset configuration signal to select buffer size.
22. Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

Figure 6. Clock Waveform

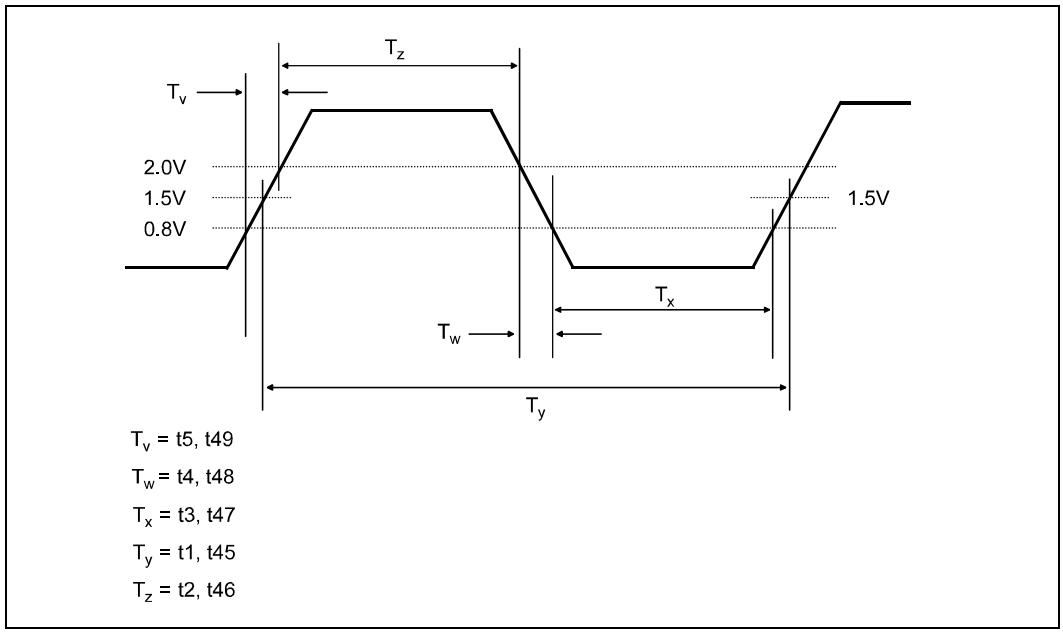


Figure 7. Valid Delay Timings

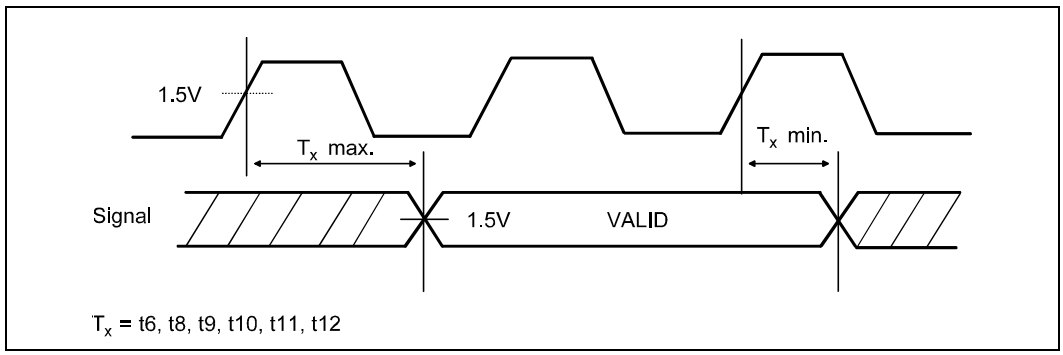


Figure 8. Float Delay Timings

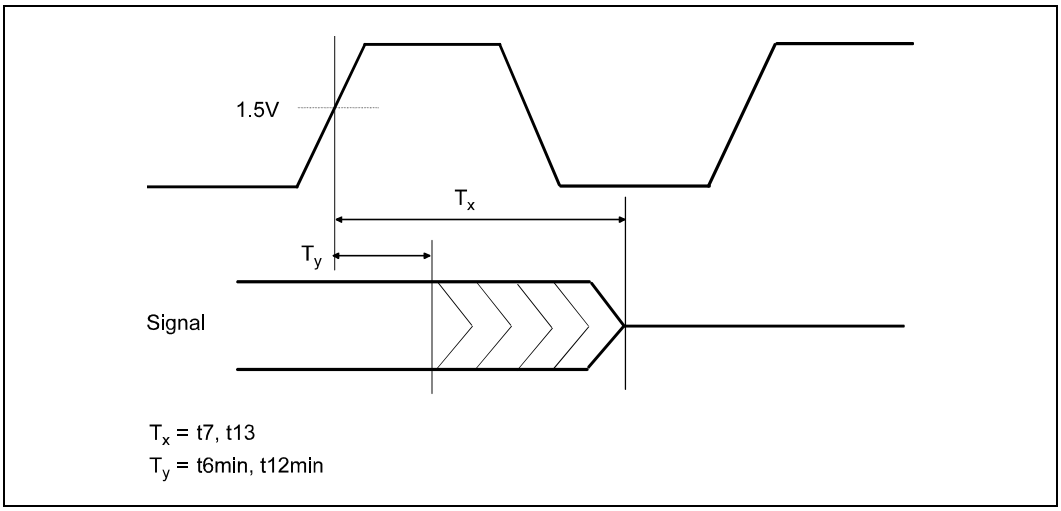


Figure 9. Setup and Hold Timings

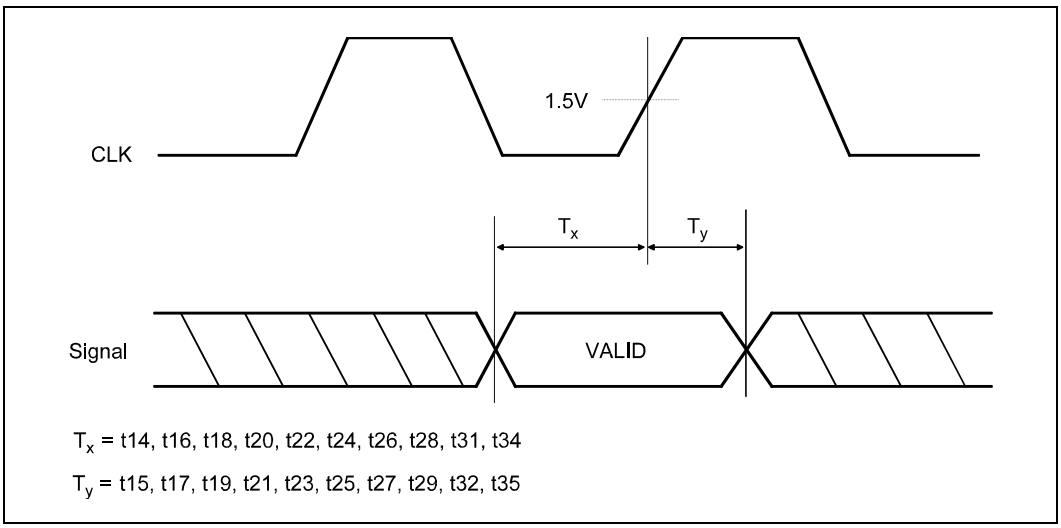
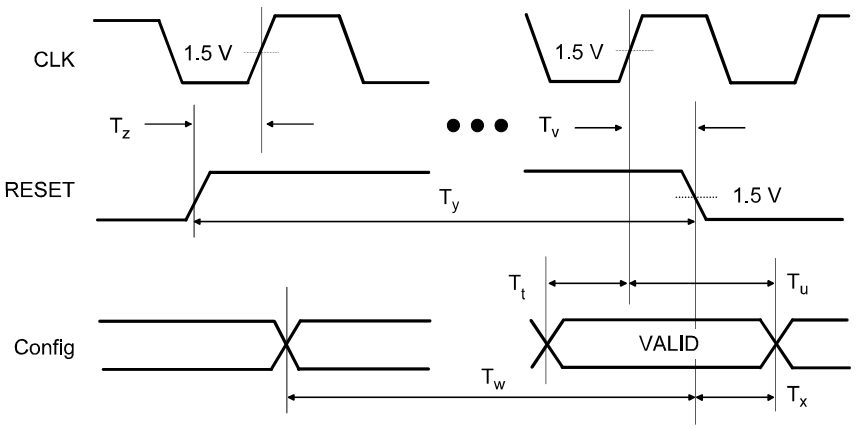


Figure 10. Reset and Configuration Timings



T_t = t40

T_u = t41

T_v = t37

T_w = t42, t43a

T_x = t43b

T_y = t38, t39

T_z = t36

Figure 11. Test Timings

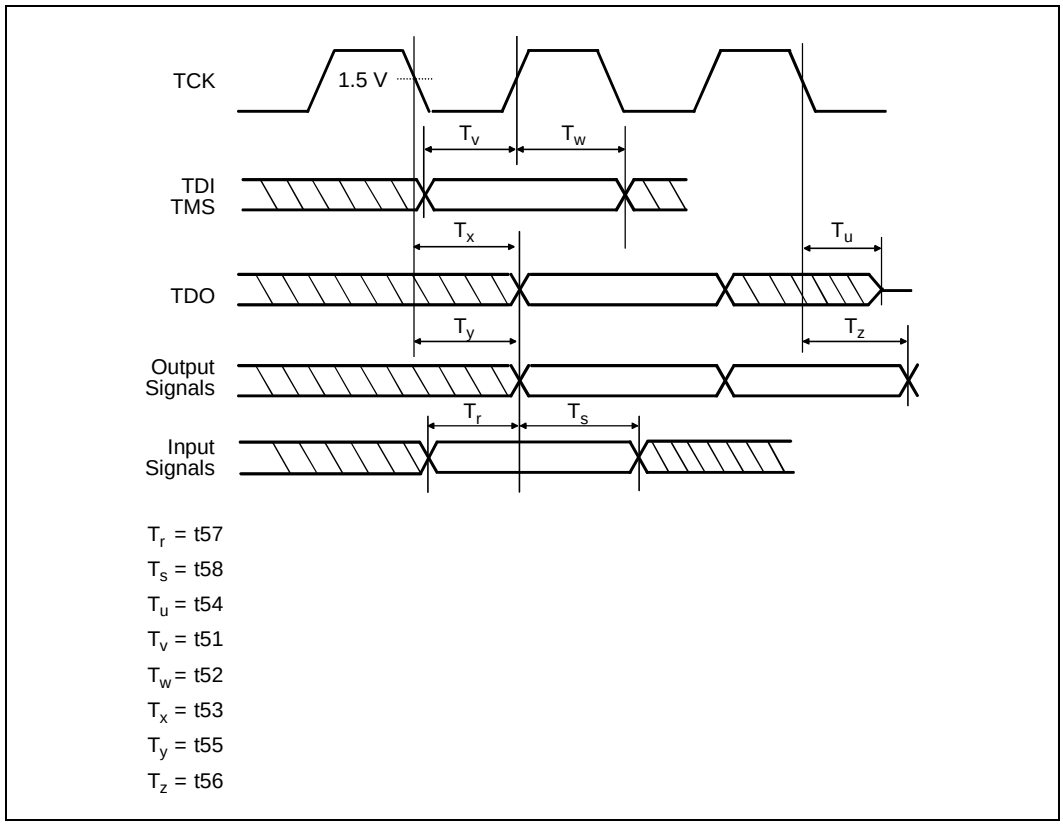
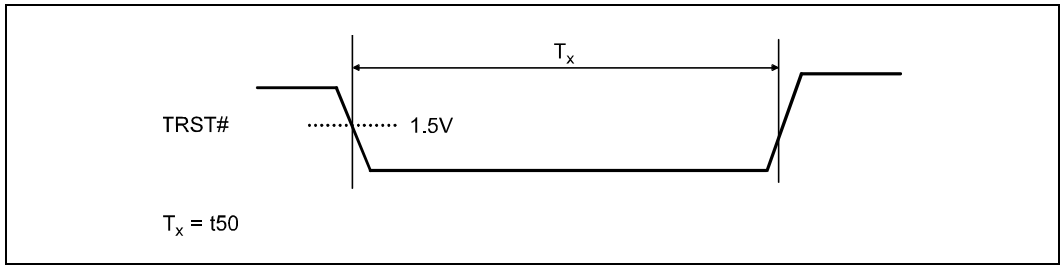


Figure 12. Test Reset Timings



4.4 I/O Buffer Models

This section describes the I/O buffer models of the embedded Pentium processor with voltage reduction technology.

The first-order I/O buffer model is a simplified representation of the complex input and output buffers used in the embedded Pentium processor with voltage reduction technology. Figure 13 and Figure 14 show the structure of the input buffer model and Figure 15 shows the output buffer model. Table 19 and Table 20 show the parameters used to specify these models.

Although simplified, these buffer models accurately model flight time and signal quality. For these parameters, there is very little added accuracy in the complete transistor model.

The following two models represent the input buffer models. The first model, Figure 13, represents all of the input buffers except for a special group of input buffers. The second model, Figure 14, represents these special buffers: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF# and CLK.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.

Figure 13. Input Buffer Model, Except Special Group

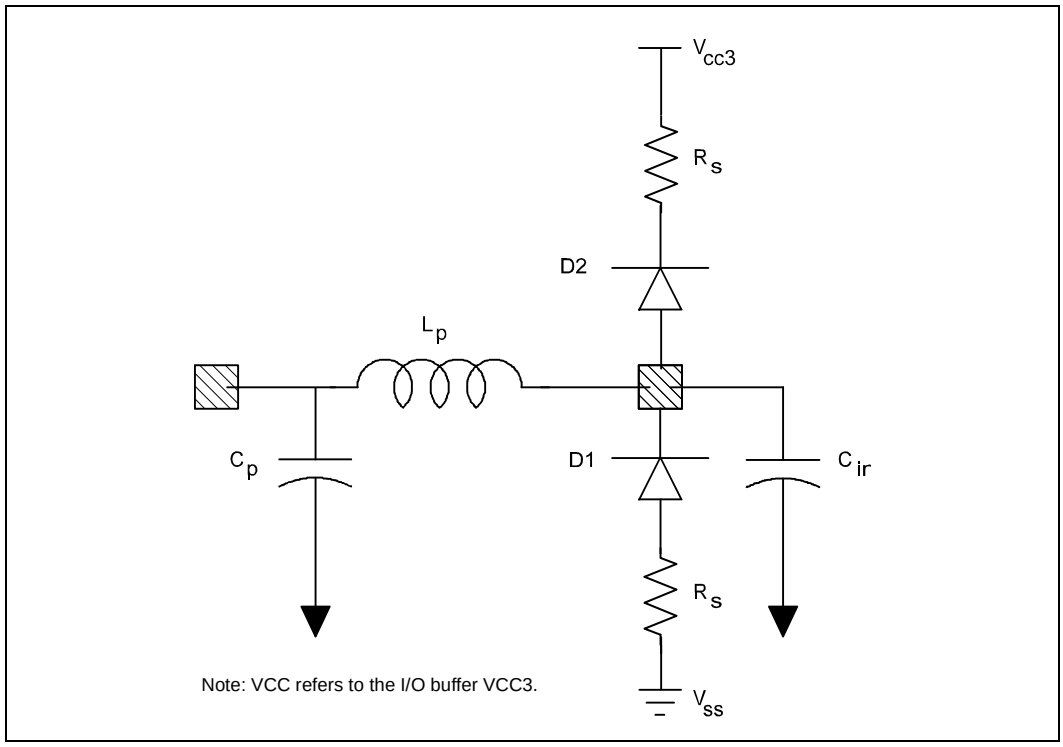


Figure 14. Input Buffer Model for Special Group

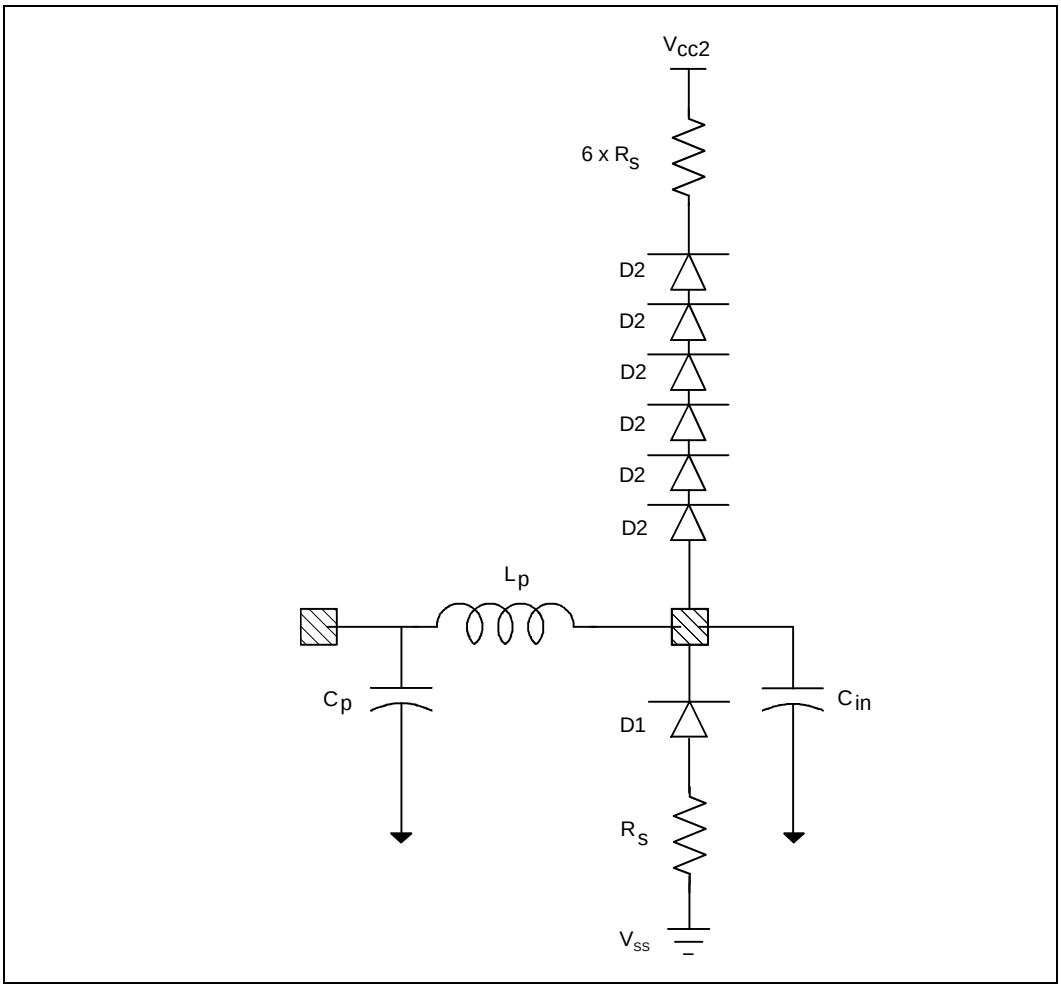


Table 19. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
C_{in}	Minimum and Maximum value of the capacitance of the input buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance
R_s	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 15 shows the structure of the output buffer model. This model is used for all of the output buffers of the embedded Pentium processor with voltage reduction technology.

Figure 15. First-Order Output Buffer Model

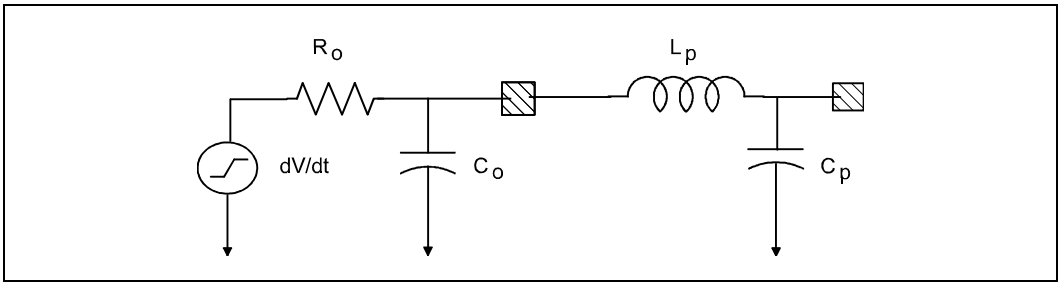


Table 20. Parameters Used in the Specification of the First-Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_o	Minimum and maximum value of the output impedance of the output buffer model
C_o	Minimum and Maximum value of the capacitance of the output buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance

4.4.1 Buffer Model Parameters

This section gives the parameters for each embedded Pentium processor with voltage reduction technology input, output and bidirectional signal, as well as the settings for the configurable buffers.

Some pins on the embedded Pentium processor with voltage reduction technology have selectable buffer sizes. These pins use the configurable output buffer EB2. Table 21 shows the drive level for BRDY# required at the falling edge of RESET to select the buffer strength. The buffer sizes selected should be the appropriate size required; otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices; all of the configurable buffers get set to the same size during setup initialization.

The input, output and bidirectional buffer values of the embedded Pentium processor with voltage reduction technology are listed in Table 23. This table contains listings for all three types; do not confuse them during simulation. When a bidirectional pin is operating as an input, use the C_{in}, C_p and L_p values; when it is operating as a driver, use all of the data parameters.

Refer to Table 22 for the groupings of the buffers.

Table 21. Buffer Selection Chart

Environment	BRDY#	Buffer Selection
Typical Stand Alone Component	1	EB2
Loaded Component	0	EB2A

NOTE: For correct buffer selection, the BUSCHK# signal must be held inactive (high) at the falling edge of RESET.

Table 22. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7#–BE5#, BP3–BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, U/O#	O	ED1	
A31–A21, AP, BE4#–BE0#, CACHE#, D/C#, D63–D0, DP8–DP0, HLDA, LOCK#, M/IO#, SCYC	I/O	EB1	EB1
A20–A3, ADS#, HITM#, W/R#	I/O	EB2/EB2A	EB2/EB2A
HIT#	I/O	EB3	EB3

Table 23. Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/ns)		R_o (Ohms)		C_p (pF)		L_p (nH)		C_o/C_{in} (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					3.0	5.0	4.0	7.2	0.8	1.2
(input)	Falling					3.0	5.0	4.0	7.2	0.8	1.2
ER1	Rising					1.1	6.1	4.7	15.3	0.8	1.2
(input)	Falling					1.1	6.1	4.7	15.3	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.1	8.2	4.0	17.7	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.1	8.2	4.0	17.7	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.7	4.0	18.7	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.7	4.0	18.7	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.3	4.4	16.7	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	1.3	8.3	4.4	16.7	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	1.9	7.5	9.9	14.3	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.9	7.5	9.9	14.3	3.3	3.9

Table 24. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e–14 A	2.78e–16 A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983 V	0.967 V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.4.2 Signal Quality Specifications

Signals driven by the system into the embedded Pentium processor with voltage reduction technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: ringback and settling time.

4.4.2.1 Ringback

Excessive ringback can contribute to long-term degradation of the reliability of the embedded Pentium processor with voltage reduction technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC3} (or above V_{SS}) relative to the V_{CC3} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

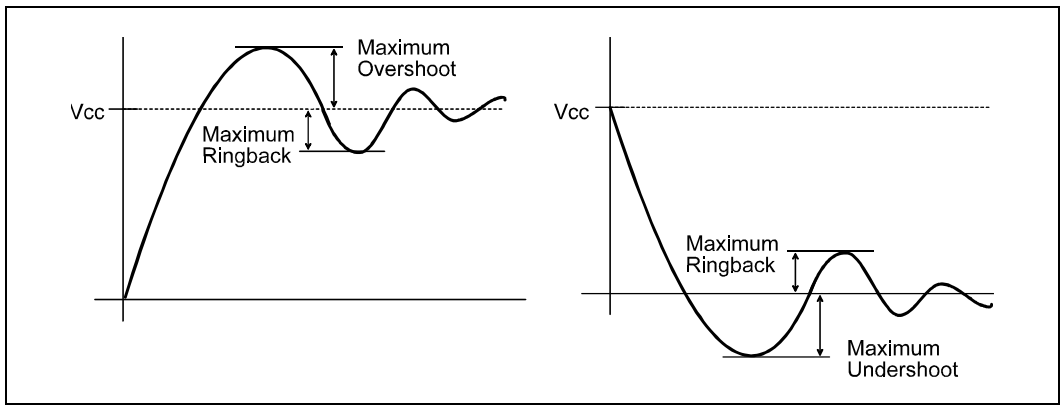
Maximum Ringback on Inputs = 0.8 V (with diodes)

If simulated without the input diodes, follow the maximum overshoot/undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively. If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC3} (below V_{SS}). The guideline assumes the absence of diodes on the input.

- The maximum overshoot/undershoot on the 3.3-V embedded Pentium processor with voltage reduction technology inputs (not CLK) = 1.4 V above V_{CC3} (without diodes)

Figure 16. Overshoot/Undershoot and Ringback Guidelines



4.4.2.2 Settling Time

The settling time is defined as the time required at the receiver for the signal to settle to within 10 percent of V_{CC3} or V_{SS}. Settling time is also the maximum time allowed for a signal to reach within 10 percent of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects can dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, the settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur, simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

A typical design method would include a settling time that ensures that a signal is within 10 percent of V_{CC3} or V_{SS} for at least 2.5 ns prior to the end of the CLK period.

Figure 17. Settling Time