Embedded Pentium® Processor with MMX™ Technology Flexible Motherboard Design Guidelines

Application Note

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Application Note

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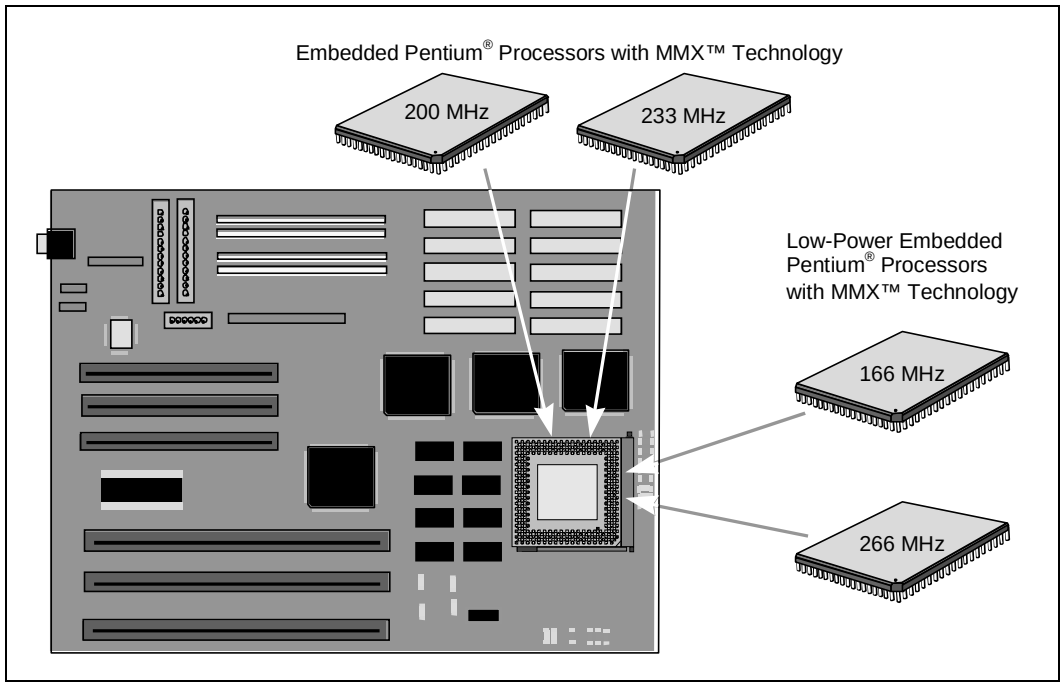
1.0 Introduction

This application note provides guidelines for designing a flexible motherboard that supports the Intel® Pentium® processor with MMX™ technology family.

Figure 1 illustrates a flexible motherboard design that supports embedded Pentium processors with MMX technology at 200/233 MHz and the new low-power embedded Pentium processors with MMX technology at 166/266 MHz manufactured with Intel's 0.25 micron fabrication process. The 0.25 micron process enables the processor to achieve faster speeds at lower voltages, reducing power consumption and heat dissipation while improving performance. The main difference between the two processors is their core and I/O voltages. The embedded Pentium processor with MMX technology has a core voltage (V_{CORE}) of 2.8 V and an I/O voltage ($V_{I/O}$) of 3.3 V. The low-power embedded Pentium processor with MMX technology has a V_{CORE} of 1.9 V and a $V_{I/O}$ of 2.5 V.

Figure 1. Embedded Pentium® Processor with MMX™ Technology Family Flexible Motherboard



Note: This application note presents design information specific to the PPGA package of the low-power embedded Pentium processor with MMX technology. This processor is also offered in the High-Thermal, Low-Temperature Plastic Ball Grid Array (HL-PBGA) package. This document may be used as a reference for designs using the HL-PBGA device. For more information on the low-power embedded Pentium processor with MMX technology in the HL-PBGA package, refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184). For details on the HL-PBGA package, refer to the *Intel Packaging Handbook* (order number 240800).

1.1 Features List for the Flexible Motherboard

A Pentium processor with MMX technology flexible motherboard should support the following features:

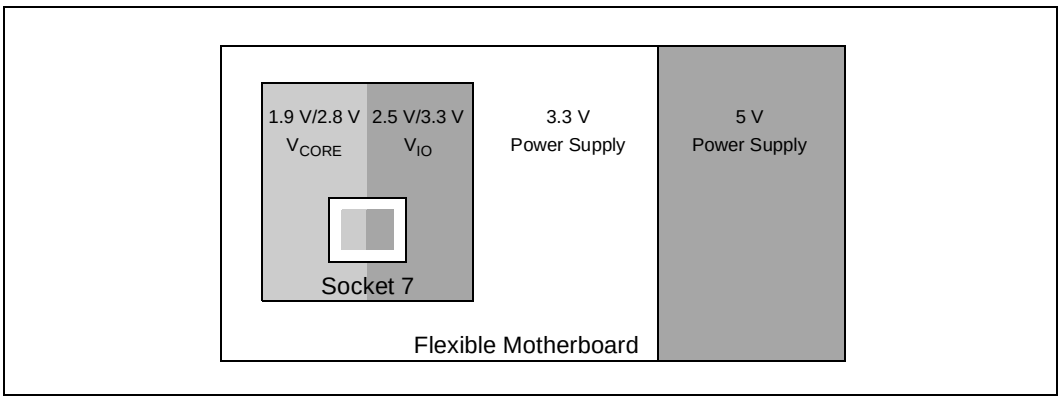
- **Split Power Islands**

  To accommodate split-plane processors, the flexible motherboard should have four separate power islands: V_{CORE} (V_{CC2}), $V_{I/O}$ (V_{CC3}), 3.3 V (3.3 V power supply) and 5 V (5 V power supply).

  The low-power embedded Pentium processor with MMX technology at 166/266 MHz uses the same split-power plane, V_{CORE} and $V_{I/O}$, as the embedded Pentium processor with MMX technology, except that the supply voltages are different. V_{CORE} and $V_{I/O}$ for the embedded Pentium processor with MMX technology are 2.8 V and 3.3 V, respectively. V_{CORE} and $V_{I/O}$ for the low-power embedded Pentium processor with MMX technology are 1.9 V and 2.5 V, respectively. Both processors require 3.3 V and 5 V power planes for external motherboard components such as DRAM (3.3 V) and the ISA bus (5 V).

  Figure 2 illustrates the four power planes for the Pentium processor with MMX technology family.

Figure 2. Split Power Planes on a Flexible Motherboard for the Pentium® Processor with MMX™ Technology Family



- **2.0 V/2.8 V Power Source for V_{CORE} Plane**

  The V_{CORE} plane supplies the core voltage (V_{CC2}) for the processor. The low-power embedded Pentium processors with MMX technology require 1.9 V (±142 mV) for core voltage. The embedded Pentium processors with MMX technology require 2.8 V (±100 mV).

  The flexible motherboard can implement this dual voltage power plane with a single linear or switching voltage regulator. See "Switching vs. Linear Voltage Regulators" on page 26 for design considerations for choosing a voltage supply. V_{CC2} pins for the low-power embedded Pentium processor with MMX technology are not 2.8 V-tolerant. Therefore, the flexible motherboard should have built-in precautions to ensure that the right voltage is supplied when a low-power embedded Pentium processor with MMX technology is installed in the socket.

  Refer to "VCC2DET# Auto-Detect Circuit" on page 33 for an example of a safeguard circuit.

- **2.5 V/3.3 V Power Source for $V_{I/O}$ Plane**

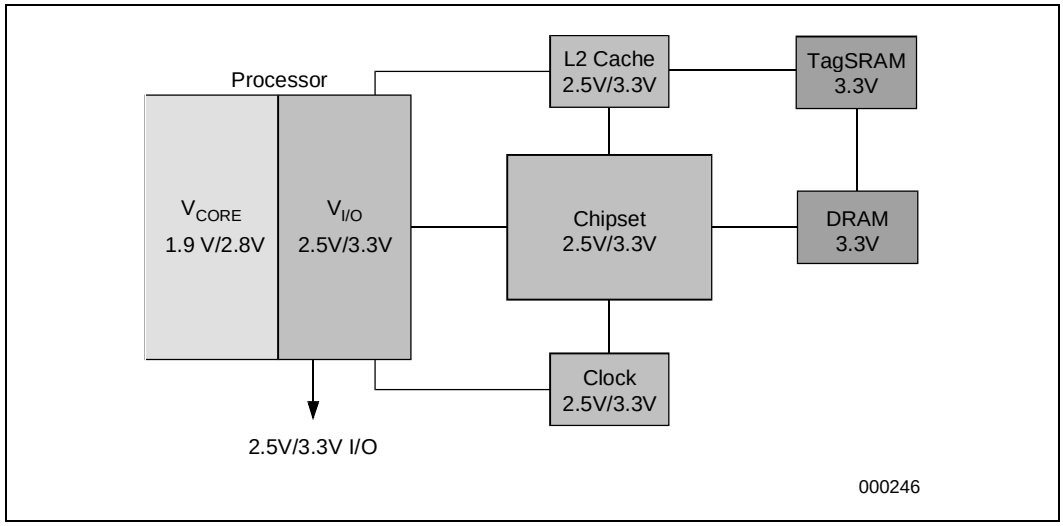
  The $V_{I/O}$ plane supplies the I/O voltage (V_{CC3}) for the processor, clock, host controller, and L2 cache (SRAM). The low-power embedded Pentium processor with MMX technology requires 2.5 V (2.375 V–2.625 V) for the I/O. The embedded Pentium processor with MMX technology requires 3.3 V (3.135 V–3.6 V). The clock, host controller, and L2 cache are special dual-voltage components that can run at either voltage.

A dual-voltage power plane on the flexible motherboard can be implemented with a single linear or switching voltage regulator. Figure 3 illustrates the I/O interface on the flexible motherboard.

V_{CC3} for the low-power embedded Pentium processor with MMX technology is not 3.3 V tolerant. Therefore, the flexible motherboard should have built-in precautions to ensure that the right voltage is supplied when a low-power embedded Pentium processor with MMX technology is installed in the socket.

Refer to "VCC2DET# Auto-Detect Circuit" on page 33 for an example of a safeguard circuit.

Figure 3. I/O Interface for the Flexible Motherboard



- **3.3 V Power Source**

  The flexible motherboard should provide a 3.3 V power plane for components such as the PCI bus, system memory (DRAM), and TagRAM (SRAM). The voltage for this plane can be from the 3.3 V source on the power supply unit or from a 3.3 V voltage regulator.

- **5 V Power Source**

  Components on the ISA bus, such as audio circuitry, keyboard/mouse controllers, and flash memory, require a 5 V plane.

- **Socket 7**

  The flexible motherboard should implement Socket 7. This processor socket accepts Socket 7 compatible processors in the Pentium processor with MMX technology family regardless of differences in their pin assignments or power plane implementation. Socket 7 is a 321-pin superset of the older 320-pin Socket 5 ZIF sockets. Socket 7 splits the 60 V_{CC} pins on Socket 5 into 28 V_{CC2} pins and 32 V_{CC3} pins. These pins are connected appropriately to the processor core voltage island and processor I/O voltage island.

- **Local Decoupling**

  Pentium processors with MMX technology may cause rapid fluctuation in current during transitions between "idle" states and "active" states. The flexible motherboard should provide adequate decoupling capacitors near the processor socket to prevent violation of the voltage supply range specifications, as documented in "Decoupling" on page 29.

- **Bus-to-Core Ratio**

  The flexible motherboard should provide jumpers for bus fraction pin strapping options that provide flexibility in configuring the ratio of external bus frequency to internal core frequency. The bus-to-core ratios can be 1/4, 2/7, 1/3, or 2/5. To support selecting between embedded Pentium processors with MMX technology and low-power embedded Pentium processors with MMX technology, jumpers should allow a high or low logic setting for three bus fraction pins (BF2, BF1 and BF0). When enabled, these pins should be pulled to logic high ($V_{I/O}$ voltage level).

- **Thermal and Mechanical Specifications**

  The flexible motherboard should be designed to meet the thermal and mechanical specifications of the Socket 7 Specification, Rev. 3.0.

- **BIOS Support**

  Each processor stepping is assigned a unique identification and feature signature. The CPUID instruction retrieves these signatures for identification. The flexible motherboard should provide a system BIOS capable of supporting all steppings for the Pentium processors with MMX technology. Using the CPUID instruction, the BIOS can determine whether the processor supports features such as the APIC. For more details, refer to "Processor ID with the CPUID Instruction" on page 16 and application note AP-485, *Intel Processor Identification with the CPUID Instruction* (order number 241618).

- **Multiple Voltage Clock Drivers**

  The flexible motherboard should include a clock driver that can drive clock inputs (CLK and PICCLK) on the processor at both 2.5 V and 3.3 V to ensure compatibility with all Pentium processors with MMX technology. The embedded Pentium processors with MMX technology require clock inputs of 3.3 V. The low-power embedded Pentium processors with MMX technology require clock inputs of 2.5 V.

- **Auto-Detect Configuration Circuit**

  Although it is possible to design the flexible motherboard to use jumpers and resistors to manually configure the board for each type of processor, it is recommended that an auto-detect configuration circuit be used instead. The circuit makes the flexible motherboard more user-friendly. The user does not need to reconfigure the board manually or remember jumper settings.

  The auto-detect circuit serves as a safeguard for the low-power embedded Pentium processor with MMX technology, which requires lower voltage levels than the embedded Pentium processor with MMX technology. This prevents incorrect voltage inputs to the processor, which could damage the processor and other components on the motherboard. Refer to "VCC2DET# Auto-Detect Circuit" on page 33 for more details.

1.2 Benefits of a Flexible Motherboard

A flexible motherboard design for the Pentium processor with MMX technology family offers several benefits:

- **Provides price/performance options**

  One flexible design, when populated by different members of the Pentium processor with MMX technology family, can provide a wide range of price/performance options. Other assembly-time options for motherboard components can provide additional flexibility. For example, external caches may use asynchronous SRAM for cost effectiveness or pipelined burst SRAM for higher performance. Synchronous DRAM may replace Extended Data Out (EDO) DRAM as main memory to maintain performance in cost-effective platforms with optional external cache memory.

- **Reduces the design and validation effort for multiple designs**

  A flexible motherboard does not have to be revised for every proliferation of the processor, thus reducing design and validation efforts. Instead, one board is designed to accept various processors that can be populated at build-time.

- **Reduces inventory and manufacturing costs**

  Only one motherboard design has to be manufactured and maintained in inventory, reducing overall inventory management and manufacturing costs. When product demand varies, the board can be populated with the processor that satisfies the current market demand.

- **Reduces debug and technical support costs**

  Only one motherboard has to be debugged. Field engineers and other support personnel need only to be trained on one motherboard design, thus reducing technical support effort.

2.0 Processor Design Considerations

This section describes considerations for designing a flexible motherboard for the family of Pentium processors with MMX technology. The differences between the embedded Pentium processor with MMX technology and the low-power embedded Pentium processor with MMX technology are discussed.

2.1 Overview of the Pentium® Processor with MMX™ Technology Family

Table 1 highlights the Pentium processor with MMX technology family's electrical and thermal specifications. Refer to "Related Resources" on page 49 to obtain specifications for each processor.

Table 1. Key Differences in the Pentium® Processors with MMX™ Technology Family (Sheet 1 of 2)

	Embedded Pentium® Processor with MMX™ Technology	Low-Power Embedded Pentium Processor with MMX Technology[1]
Core Frequency (MHz)	200, 233	166, 266
Bus Frequency (MHz)	66	66
Frequency Ratio[2]	1/3, 2/7	2/5, 1/4
Clock Level	3.3 V	2.5 V
Core Supply (V_{CC2})	2.8 V (±100 mV)	1.9 V (±142 mV)
I/O Supply (V_{CC3})	3.3 V (3.135 V–3.60 V)	2.5 V (2.375 – 2.625 V)
I_{CC2} [3,4]	6.50 A (233 MHz) 5.70 A (200 MHz)	4.0 A (266 MHz) 2.5 A (166 MHz)
I_{CC3} [3,5]	750 mA (233 MHz) 650 mA (200 MHz)	380 mA (266 MHz) 380 mA (166 MHz)
Max. Power[5]	17.0 W (233 MHz) 15.7 W (200 MHz)	7.6 W (266 MHz) 4.5 W (166 MHz)
V_{IL}	0.8 V	0.5 V
V_{IH}	2.0 V	V_{CC3} – 0.7 V
V_{OH}	N/A	V_{CC3} – 0.2 V (I_{OH} = 1 mA)

NOTES:
1. All data for the low-power embedded Pentium processor with MMX technology are best estimates at the time of this document's publication. Refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184) for the latest specifications.
2. Note that overshoot, undershoot and ringback are different between a embedded Pentium processor with MMX technology and a low-power embedded Pentium processor with MMX technology. Refer to "Overshoot, Undershoot and Ringback" on page 19.
3. The number shown represents worst case or maximum current/power.
4. I_{CC2} refers to V_{CC2} (core) supply current.
5. I_{CC3} refers to V_{CC3} (I/O) supply current.
6. Refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184) for complete AC timing specifications.

Table 1. Key Differences in the Pentium® Processors with MMX™ Technology Family (Sheet 2 of 2)

	Embedded Pentium® Processor with MMX™ Technology	Low-Power Embedded Pentium Processor with MMX Technology[1]
AC Timings [6]	N/A	Abus and Dbus min/max valid delays have changed
No. of V_{CC2} Pins	25	25
No. of V_{CC3} Pins	28	28
External Plane Type	Split	Split
Internal Plane Type	Split	Split
Package Type	296-pin PPGA	296-pin PPGA

NOTES:
1. All data for the low-power embedded Pentium processor with MMX technology are best estimates at the time of this document's publication. Refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184) for the latest specifications.
2. Note that overshoot, undershoot and ringback are different between a embedded Pentium processor with MMX technology and a low-power embedded Pentium processor with MMX technology. Refer to "Overshoot, Undershoot and Ringback" on page 19.
3. The number shown represents worst case or maximum current/power.
4. I_{CC2} refers to V_{CC2} (core) supply current.
5. I_{CC3} refers to V_{CC3} (I/O) supply current.
6. Refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184) for complete AC timing specifications.

The embedded Pentium processor with MMX technology is a Socket 7, split core I/O processor with a core voltage of 2.8 V and an I/O voltage of 3.3 V. It operates at 200 and 233 MHz core speeds with a 66 MHz external bus. It introduced several architectural enhancements to the classic Pentium processor family: an increase from 8 Kbytes to 16 Kbytes internal data and code cache size, better branch prediction, and support for MMX technology.

The low-power embedded Pentium processor with MMX technology is a lower power version of the Pentium processor with MMX technology, capable of running at speeds up to 266 MHz with V_{CORE} at 1.9 V and $V_{I/O}$ at 2.5 V. It is functionally identical to the Pentium processor with MMX technology with the following differences: voltage supplies, power consumption, no dual processing (DP) support, and no support for selectable buffer sizes. The low-power embedded Pentium processor with MMX technology is offered in a Socket 7 package, and is pin compatible with the embedded Pentium processor with MMX technology. See "Socket 7 Pin Diagram" on page 35 for pinouts.

The Intel430TX PCIset chipset directly supports the low-power embedded Pentium processor with MMX technology and the embedded Pentium processor with MMX technology. Level shifters can be used to interface the Intel430HX PCIset chipset to the low-power embedded Pentium processor with MMX technology. For more information, see *Interfacing the Low-Power Embedded Pentium Processor with MMX Technology to the 82439HX System Controller* (order number 273188).

2.2 External Features and Differences

This section discusses some of the differences between the external features of the embedded Pentium processor with MMX technology and those of the low-power embedded Pentium processor with MMX technology.

2.2.1 Bus Fraction (BF) Selection

The BF configuration pins are provided to select the allowable bus-to-core ratios: 1/4, 2/7, 1/3, and 2/5. Processors multiply the input CLK to achieve the higher internal core frequencies. The internal clock multiplier requires a constant frequency CLK input to within ±250 ps; therefore the CLK input cannot be changed dynamically.

The external bus frequency is set on power-up RESET through the CLK pin. All Pentium processors with MMX technology sample the BF2-BF0 pins on the falling edge of RESET to determine which bus-to-core ratio to use.

Warning: Do not float the BF pins at RESET for processors running at 166, 200, 233 or 266 MHz. When the BF pins are left floating, these processors will be configured for an 1/2 bus-to-core frequency ratio, which is unsupported on these processors.

Table 2 summarizes the operation of the BF pins for the Pentium processor with MMX technology. The BF2 pin was added to support the 1/4 ratio for the low-power embedded Pentium processor with MMX technology running at 266 MHz.

Table 2. Bus Frequency Selections for the Embedded Pentium® Processor with MMX™ Technology Family

BF2	BF1	BF0	Embedded Pentium® Processor with MMX Technology (200/233 MHz) Bus-to-Core Ratio	Low-Power Embedded Pentium Processor with MMX Technology (166/266 MHz) Bus-to-Core Ratio	Max Bus/Core Frequency (MHz)
0	0	0	Reserved	2/5	66/166
0	0	1	1/3	Reserved	66/200
0	1	0	Reserved†	Reserved†	66/133
0	1	1	2/7	Reserved	66/233
1	0	0	Reserved	1/4	66/266
1	X	X	Reserved	Reserved	N/A

† This is the default bus-to-core ratio for the embedded Pentium® processor with MMX™ technology and the low-power embedded Pentium processor with MMX technology. If the BF pins are left floating, the processor will be configured for a 1/2 bus-to-core frequency ratio, which is unsupported on these processors.

2.2.2 Pinout Considerations

The functional signals on the low-power embedded Pentium processor with MMX technology are compatible with the Pentium processor with MMX technology. However, some pin assignments have changed due to changes in the feature set. Table 3 provides a quick reference for pin changes. The major changes are described below in more detail.

- **V_{CC2}, V_{CC3}**
  On the embedded Pentium processor with MMX technology, the V_{CC3} of the internal bus logic is isolated from the V_{CC2} of the core logic. This allows the core to run at a lower voltage (2.8 V) in order to obtain faster core frequencies and reduce overall power consumption. The low-power embedded Pentium processor with MMX technology is designed the same way, except that V_{CC2} is 1.9 V and V_{CC3} is 2.5 V. The voltage for the core logic is supplied through the V_{CC2} pins and the voltage for the bus logic is supplied through the V_{CC3} pins. Therefore, the motherboard design splits the processor power plane into two separate core voltage islands: one that can supply 1.9 V or 2.8 V (V_{CC2}) and another that can supply 2.5 V or 3.3 V (V_{CC3}).
- **VCC2DET#**
  This signal is defined on the Pentium processor with MMX technology to indicate to the system which processor is installed in the processor socket. On the low-power embedded Pentium processor with MMX technology, the VCC2DET# pin is left floating (infinite impedance). For the embedded Pentium processor with MMX technology, the pin is internally connected to ground. A circuit designed to detect the VCC2DET# signal should have a weak pull-up resistor. This will cause the signal to be pulled high with a low-power embedded Pentium processor with MMX technology and to be driven low with an embedded Pentium processor with MMX technology. For a sample circuit, refer to "VCC2DET# Auto-Detect Circuit" on page 33.
  One additional note is that the VCC2DET# pin is also defined as floating for Pentium processors at 100/133/166 MHz. There should be minimal or no issues from this overlap, because low-power embedded Pentium processor with MMX technology and Pentium processors at 100/133/166 MHz are not normally supported on a single motherboard design.
- **BF2-BF0**
  The bus fraction selection pins determine the bus-to-core frequency ratio. The BF pins are sampled by the processor at RESET, and are not sampled by the processor again until another cold-boot (1 ms) assertion of RESET. The signal on the BF pins is not an indication of the bus speed, only the ratio of the processor core with respect to the bus. Table 2 summarizes the operation of the BF pins on Pentium processors with MMX technology.
- **CLK, PICCLK**
  The low-power embedded Pentium processor with MMX technology supports input and output levels of 2.5 V only. The clock (CLK) and APIC clock (PICCLK) are not 3.3 V tolerant. The clock inputs to the processor on the flexible motherboard are driven by a dual voltage 2.5 V/3.3 V clock driver: 2.5 V for the low-power embedded Pentium processor with MMX technology and 3.3 V for embedded Pentium processor with MMX technology.

Table 3 lists the pin differences between the embedded Pentium processor with MMX technology and the low-power embedded Pentium processor with MMX technology. Square brackets around a signal name indicate that the signal is defined only at RESET.

Table 3. Quick Pin Reference for the Low-Power Embedded Pentium® Processor with MMX™ Technology

Pin Name	I/O	Function
[BF0], [BF1], [BF2]	Input	The low-power embedded Pentium processor with MMX technology uses the BF0, BF1 and BF2 pins to determine the bus-to-core frequency ratio.[1] These pins are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF pins must not change values while RESET is active. When BF0, BF1 and BF2 are left floating, the low-power embedded Pentium processor with MMX technology defaults to a 1/2 bus-to-core ratio. The complete configuration table for BF pins is listed below. Bus Fraction functionality is further explained in "Overview of Voltage Supply and Split Power Planes" on page 21. BF2 / BF1 / BF0 / Fraction 0 / 0 / 0 / 2/5 0 / 0 / 1 / Reserved 0 / 1 / 0 / 1/2[2] 0 / 1 / 1 / Reserved 1 / 0 / 0 / 1/4 1 / X / X / Reserved
VCC2DET#	Output	The low-power embedded Pentium processor with MMX technology leaves this pin floating. The embedded Pentium processor with MMX technology drives the pin low.
CPUTYP, D/P#, FRCMC#, PBGNT#, PBREQ#, PHIT#, PHITM#, BRDYC#, ADSC#	N/A	These pins have been removed from the low-power embedded Pentium processor with MMX technology.

NOTES:
1. Refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184) for complete pinout specifications.
2. Default bus-to-core ratio if BF2-BF0 pins are left floating. This bus fraction is not supported by the low-power embedded Pentium processor with MMX technology.

2.2.3 Processor ID with the CPUID Instruction

The CPUID instruction allows the BIOS and software to determine the type and features of the microprocessor on which it is executing.

When executing CPUID, the low-power embedded Pentium processor with MMX technology behaves like the embedded Pentium processor with MMX technology:

- If the value in EAX is '0', then the 12-byte ASCII string "Genuine Intel" (little endian) is returned in EBX, EDX, and ECX. Also, a '1' is returned to EAX.
- If the value in EAX is '1', then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the low-power embedded Pentium processor with MMX technology are given in Figure 4, Figure 5, and Table 4.
- If the value in EAX is neither '0' or '1', the low-power embedded Pentium processor with MMX technology writes '0' to all registers.

Figure 4. EAX Bit Assignments for CPUID

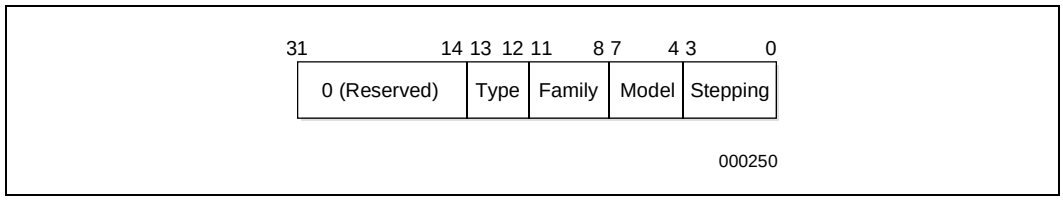
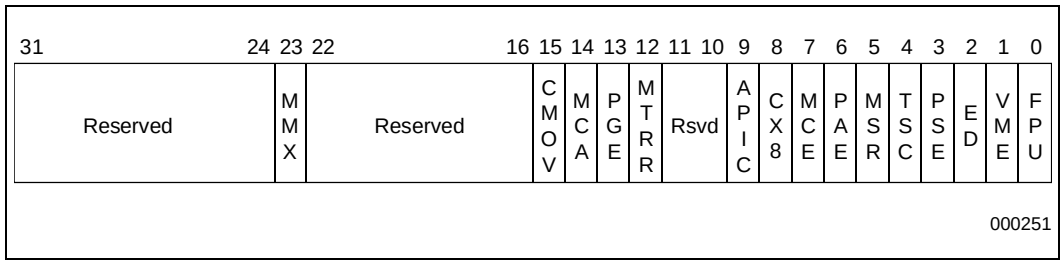


Figure 5. EDX Bit Assignments for CPUID



The following EAX and EDX values are defined for the CPUID instruction executed with EAX = '1'. The processor version EAX bit assignments are given in Figure 4.

Table 4. EDX Bit Assignment Definitions for CPUID

Bit	Value	Comments
0	1	FPU: Floating-Point Unit on-chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR: Pentium® Processor MSR
6	0	PAE: Physical Address Extension
7	1	MCE: Machine Check Exception
8	1	CX8: CMPXCHG8B Instruction
98	1	APIC: APIC on-chip†
10–11	R	Reserved–Do not write to these bits or rely on their values
12	0	MTRR: Memory Type Range Registers
13	0	PGE: Page Global Enable
14	0	MCA: Machine Check Architecture
15	1	CMOV: Conditional Move Instruction supported
16–22	R	Reserved–Do not write to these bits or rely on their values
23	1	Intel® Architecture MMX™ Technology supported
24–31	R	Reserved–Do not write to these bits or rely on their values

† Indicates that APIC is present and hardware-enabled (software disabling does not affect this bit).

The family field is the same for all Pentium processors (family = 5H). The model field is different: the embedded Pentium processor with MMX technology model number is 4H, and the low-power embedded Pentium processor with MMX technology model number is 8H. The stepping field has the same format as for the Pentium processor. For the low-power embedded Pentium processor with MMX technology, the stepping field returns 1H for A-step and 2H for B-step. The type field is defined as '00'.

The EDX bit assignments are shown in Figure 5 and Table 4.

After masking the reserve bits, all products based on the low-power embedded Pentium processor with MMX technology will get a value of 0x008003BF (when the APIC is enabled at boot) or 0x008001BF (when the APIC is disabled using the APICEN boot pin) in EDX upon completion of the CPUID instruction.

2.3 Electrical and Thermal Features and Differences

This section discusses some of the electrical and thermal features of the low-power embedded Pentium processor with MMX technology and highlights their differences from the embedded Pentium processor with MMX technology.

2.3.1 Thermal Analysis

The low-power embedded Pentium processor with MMX technology consumes 7.6 W at 266 MHz. The embedded Pentium processor with MMX technology consumes 17.0 W at 233 MHz. The chassis, heatsink, and fan for the embedded Pentium processor with MMX technology must be capable of dissipating 17 watts of power (power dissipation at 233 MHz) in order for T_{CASE} of the processor to remain within the specified temperature range (0° C to 70° C). Therefore, the maximum factor in thermal considerations lies with the embedded Pentium processor with MMX technology at 233 MHz. If the thermal solution is designed to handle the heat dissipation for a Pentium processor with MMX technology at 233 MHz, thermal requirements are satisfied for low-power embedded Pentium processor with MMX technology.

2.3.2 Split Power Supplies

The low-power embedded Pentium processor with MMX technology uses the same split power planes, V_{CORE} and $V_{I/O}$, as the embedded Pentium processor with MMX technology, except the supply voltages have changed. V_{CORE} and $V_{I/O}$ for the embedded Pentium processor with MMX technology are 2.8 V and 3.3 V, respectively, whereas V_{CORE} and $V_{I/O}$ for the low-power embedded Pentium processor with MMX technology are 1.9 V and 2.5 V, respectively. Therefore, V_{CORE} pins must be connected to a voltage supply that can supply 1.9 V and 2.8 V, and $V_{I/O}$ pins must be connected to a supply of 2.5 V and 3.3 V.

The $V_{I/O}$ plane supply should supply approximately 2.0 A. This plane not only powers the $V_{I/O}$ pins of the low-power embedded Pentium processor with MMX technology but also the host clock generator, chipset, L2 cache, and BF2-0 bus-to-core fraction pin pull-ups.

2.3.3 2.5 V Input and Output

The inputs and outputs of the low-power embedded Pentium processor with MMX technology are compatible with the 2.5 V JEDEC non-terminated digital interface standard. Both inputs and outputs are also 2.5 V TTL compatible, although the inputs cannot tolerate voltage swings above the 2.5 V V_{IN3} max. For the low-power embedded Pentium processor with MMX technology outputs, the Pentium processor with MMX technology system support components should use 2.5 V JEDEC compatible inputs. This is because the low-power embedded Pentium processor with MMX technology drives signals according to the 2.5 V JEDEC TTL specification.

For the low-power embedded Pentium processor with MMX technology inputs, the voltage must not exceed the 2.5 V V_{IN3} max specification. System support components can consist of 2.5 V devices or open-collector devices. In an open-collector configuration, the external resistor may be biased with the 2.5 V V_{CC3}.

2.3.4 V_{IL3} (MAX) and V_{IH3} (MIN)

V_{IL3} (MAX) for the low-power embedded Pentium processor with MMX technology is 0.5 V. This is a decrease from the embedded Pentium processor with MMX technology's specification of 0.8 V. V_{IH3} (MIN) for low-power embedded Pentium processor with MMX technology is V_{CC3} – 0.7 V. This is a change from the 2.0 V specification for the embedded Pentium processor with MMX technology.

2.3.5 Overshoot, Undershoot and Ringback

Signal quality specifications for the low-power embedded Pentium processor with MMX technology are different from the embedded Pentium processor with MMX technology. These specifications must be met to ensure that the components read data properly and that incoming signals do not affect the reliability of the component.

Refer to Table 5 and Table 6 for a summary of overshoot, undershoot, and ringback specifications for the low-power embedded Pentium processor with MMX technology. For more detailed signal quality specifications, refer to the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet (order number 273184).

Table 5. Overshoot Specification Summary

Specification Name	Value	Units
Threshold Level (CLK and PICCLK)	V_{CC3}, nominal +0.3	V
Threshold Level (all other inputs)	V_{CC3}, nominal +0.5	V
Maximum Overshoot Level (CLK and PICCLK)	V_{CC3}, nominal +0.6	V
Maximum Overshoot Level (all other inputs)	V_{CC3}, nominal +1.0	V
Maximum Threshold Duration	20% of clock period above threshold voltage	ns
Maximum Ringback	V_{CC3}, nominal –0.7	V

Table 6. Undershoot Specification Summary

Specification Name	Value	Units
Threshold Level	–0.3	V
Threshold Level (all other inputs)	–0.5	V
Minimum Undershoot Level (CLK and PICCLK)	–0.6	V
Minimum Undershoot Level (all other inputs)	–1.0	V
Maximum Threshold Duration	20% of clock period below threshold voltage	ns
Maximum Ringback	0.5	V

3.0 Flexible Motherboard Implementation

This chapter describes the implementation of a split plane flexible motherboard for the Pentium processors with MMX technology using Socket 7.

3.1 Overview of Voltage Supply and Split Power Planes

In order to support the Pentium processors with MMX technology with different voltage requirements, the flexible motherboard should include provisions for 1.9 V, 2.5 V, 2.8 V and 3.3 V supply voltages on three different power planes. Refer to Figure 2 on page 8 for a conceptual diagram of which power planes need which voltages.

The specific method for implementing the voltage supplies and partitioning the power planes depends on the actual design. Several options are feasible for designing a flexible motherboard for the Pentium processors with MMX technology. This section provides details for a design that provides flexibility and cost-savings options to the manufacturer.

For all designs, V_{CORE} must always be electrically isolated from all other power planes because all Pentium processors with MMX technology are split-plane processors, unlike the single-plane embedded Pentium processors. With the $V_{I/O}$ and 3.3 V power supply planes, however, it is possible to connect the two together when an embedded Pentium processor with MMX technology is used because both run at 3.3 V. This method, which is discussed further in "Voltage Supply and Split Power Planes Implementation and Cost-savings Build Options" on page 22, may provide cost-saving options to the manufacturer.

The most cost-effective way to implement the dual voltages on V_{CORE} and $V_{I/O}$ is to use 1.9 V/ 2.8 V and 2.5 V/3.3 V voltage regulators, respectively. Either a linear or switching voltage regulator can be used. Both options have advantages and disadvantages. The linear voltage regulator component is cheaper than the switching regulator. However, the linear voltage regulator generates more heat (dissipative nature), which may increase the cost of the thermal solution for the board. Also, linear regulators are not as reliable. Refer to "Switching vs. Linear Voltage Regulators" on page 26 for a more detailed comparison of switching and linear voltage regulators.

An auto-configure circuit based on the VCC2DET# signal can be implemented on the flexible motherboard to eliminate the need for jumper/resistor configuration and serve as a safeguard for the low-power embedded Pentium processor with MMX technology. Refer to "Pinout Considerations" on page 15 for a more detailed description of the VCC2DET# signal and how it can be used to safeguard the low-power embedded Pentium processor with MMX technology from higher voltage levels intended for the embedded Pentium processor with MMX technology.

In addition to supplying the correct voltage, the voltage supplies must supply enough current for all components on a particular power plane. The embedded Pentium processor with MMX technology at 233 MHz draws the most current (6.5 A) for its core. Therefore, the V_{CC2} supply voltage source must supply up to 6.5 A. As for the $V_{I/O}$ plane, the 2.5 V/3.3 V dual-voltage regulator must supply approximately 2.0 A[1] for the processor's I/O, L2 cache, and chipset.

Because the low-power embedded Pentium processor with MMX technology requires less power (4.0 A at 1.9 V for V_{CORE} and 380 mA at 2.5 V $V_{I/O}$) than the embedded Pentium processor with MMX technology, a design that meets the requirements for the embedded Pentium processor with MMX technology is adequate for both processor types.

1. The 2.0 A value is derived from the 0.75 A required by the V_{CC3} pins on the embedded Pentium® processor with MMX™ technology at 233 MHz, and an estimated 1.0 – 1.25 A for the L2 cache (512 Kbyte), chipset, host clock generator, and pull-ups for the BF[2:0] pins.

3.2 Voltage Supply and Split Power Planes Implementation and Cost-savings Build Options

This section discusses a sample flexible motherboard design for the Pentium processor with MMX technology family. The design allows the manufacturer to build motherboards that support all the members of the Pentium processor with MMX technology family or only one particular member. This flexibility can result in significant cost savings and increase the manufacturer's ability to adjust to market conditions without changing the motherboard design.

All three boards are based on one design, differing only in the components that are assembled on the board at build-time.

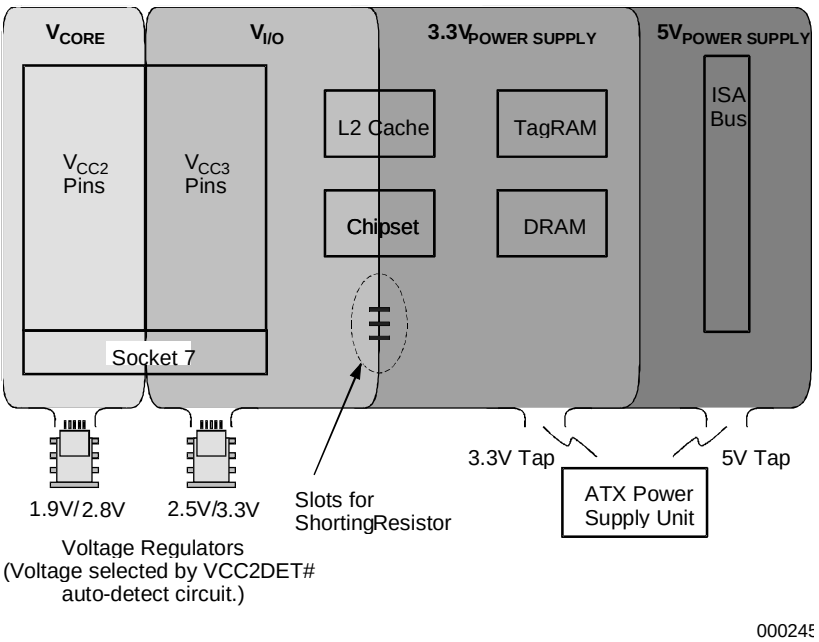
The conceptual design for the sample implementation is discussed first, followed by sections that detail the three boards and point out the flexibility and cost-savings features of each. Refer to "Switching vs. Linear Voltage Regulators" on page 26 for component options for voltage supplies.

3.2.1 Layout and Design of Sample Implementation

Figure 6 shows the basic layout for the sample implementation. The following list highlights the main features:

- V_{CORE} and $V_{I/O}$ are powered by a 1.9 V/2.8 V and 2.5 V/3.3 V voltage regulator, respectively.
- The L2 cache and chipset reside partially on the $V_{I/O}$ power plane and are powered by the 2.5 V/3.3 V voltage regulator.
- An auto-detect circuit driven by the VCC2DET# signal selects the correct voltage for the two dual-voltage regulators.
- The 3.3 V power supply plane is powered by the 3.3 V tap off the system power supply unit. DRAM, TagRAM, and other 3.3 V components reside on this power plane.
- The design is laid out to accept shorting resistors that can connect the $V_{I/O}$ and 3.3 V power supply power planes. This layout supports cost-savings build options. See "Board for the Embedded Pentium® Processor with MMX™ Technology Only" on page 25.

Figure 6. Basic Design of Sample Implementation



The embedded Pentium processor with MMX technology at 233 MHz draws the most current (6.5 A for I_{CC2} and 750 mA for I_{CC3}) in the Pentium processor with MMX technology family and therefore sets the maximum current that the two dual-voltage regulators must supply. (For I_{CC3}, the power from the L2 cache and chipset must also be factored in to determine the size of the voltage regulator. Estimated current draw required by the L2 cache and chipset is 1.0 A–1.25 A.)

The auto-configurable regulator circuit triggered by the VCC2DET# signal (see "Pinout Considerations" on page 15) makes it possible to support any processor in the Pentium processor with MMX technology family without the need for jumper/resistor configuration. It also serves as a safeguard for the low-power embedded Pentium processor with MMX technology, which is not 2.8 V or 3.3 V-tolerant for its V_{CORE} and $V_{I/O}$ pins, respectively.

When an embedded Pentium processor with MMX technology is plugged into a Socket 7, the VCC2DET# signal is low, causing the auto-detect circuit to toggle the 1.9 V/2.8 V voltage regulator to 2.8 V (V_{CORE}), and the 2.5 V/3.3 V voltage regulator to 3.3 V ($V_{I/O}$).

When a low-power embedded Pentium processor with MMX technology is plugged into a Socket 7, the floating VCC2DET# signal is pulled high by the weak pull-up resistor in the auto-configure circuit. This causes the 1.9 V/2.8 V voltage regulator to toggle to 1.9 V (V_{CORE}), and the 2.5 V/3.3 V voltage regulator to toggle to 2.5 V ($V_{I/O}$).

3.2.2 Board to Support All Members of the Pentium® Processor with MMX™ Technology Family

Configuring the sample design to support all members of the Pentium processor with MMX technology family is straightforward. This board follows the basic layout and design from "Layout and Design of Sample Implementation" on page 22, with the following requirement: The slots designed for the shorting resistors to connect the $V_{I/O}$ and 3.3 V power supply plane must remain empty. In other words, the resistors are not assembled onto the board. This maintains three separate power planes at all times, which is necessary to support the low-power embedded Pentium processor with MMX technology.

With the exception of this requirement, the flexible motherboard design follows the design outlined in "Layout and Design of Sample Implementation" on page 22:

- 1.9 V/2.8 V and 2.5 V/3.3 V voltage regulators power the V_{CORE} and $V_{I/O}$ power planes, respectively.
- 3.3 V power supply is powered from the 3.3 V tap off the system power supply unit.
- The auto-detect circuit driven by VCC2DET# selects the correct voltage level.

This is the most flexible of the options discussed in this document. This option offers two key advantages:

- This design gives the consumer an upgrade path from an embedded Pentium processor with MMX technology to a low-power embedded Pentium processor with MMX technology, without changing motherboards.
- From a manufacturer's perspective, this design offers the flexibility to adjust to changing market conditions with one motherboard. The decision of which processor to install in the system can be made at assembly time.

3.2.3 Board for the Low-Power Embedded Pentium® Processor with MMX™ Technology Only

Building a board to support only the low-power embedded Pentium processor with MMX technology is also straightforward. In fact, from a motherboard design perspective, it is identical to the all-members board discussed in "Board to Support All Members of the Pentium® Processor with MMX™ Technology Family" above.

- 1.9 V and 2.5 V voltage regulators power the V_{CORE} and $V_{I/O}$ power planes, respectively.
- 3.3 V power supply is powered from the 3.3 V tap off the system power supply unit.
- The auto-detect circuit driven by VCC2DET# selects the correct voltage level.
- Shorting resistor slots are left empty to maintain three separate power planes.

The primary reason for considering a board of this type is cost savings. The most compelling cost savings is in scaling back the thermal solution (e.g., heatsinks, fans) for the system. This is possible because the low-power embedded Pentium processor with MMX technology at 266 MHz consumes less power than the 233 MHz processor. Additional cost savings is possible using a 1.9 V voltage regulator that does not need to supply as much current, because I_{CC2} for the low-power processor at 266 MHz (4.0 A) is less than for the 233 MHz processor (6.5 A).

The 1.9 V and 2.5 V voltage regulator could be replaced with discrete 1.9 V and 2.5 V regulators, because this board supports only one processor. This provides some cost-savings, but the additional cost of changing the Bill of Materials (BOM) and modifying the assembly line to support this may outweigh the cost-savings.

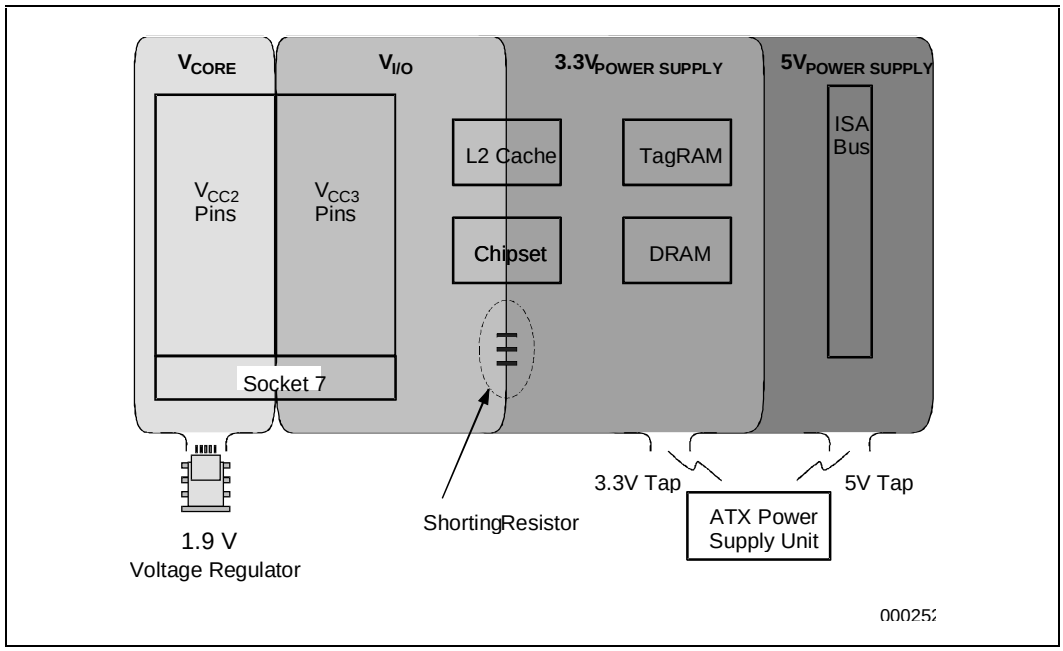
3.2.4 Board for the Embedded Pentium® Processor with MMX™ Technology Only

This board is based on the same design as the other options presented above. The main reason for considering this board is cost savings. This design takes advantage of the fact that with an embedded Pentium processor with MMX technology, both the $V_{I/O}$ and 3.3 V power supply planes are at 3.3 V. This opens the possibility of connecting the $V_{I/O}$ and 3.3 V power supply planes together, removing the need for one of the voltage regulators.

As shown in Figure 7, this design uses only one voltage regulator. Other features include:

- A 2.8 V voltage regulator to power the V_{CORE} power plane
- Shorting resistor slots that are stuffed with the resistors in order to connect the $V_{I/O}$ and 3.3 V power supply power plane
- $V_{I/O}$ and 3.3 V power supply power planes, which are powered from the 3.3 V tap off the system power supply unit[1]

Figure 7. Board for the Embedded Pentium® Processor with MMX™ Technology Only



1. Powering the V_{CC3} pins on the embedded Pentium® processor with MMX™ technology with the 3.3 V supply from the power supply unit is possible because the ATX power supply's 3.3 V supply specification meets the processor's requirements. The processor requires $V_{I/O}$ to be between 3.135 V and 3.6 V. The ATX power supply guarantees its 3.3 V supply at 3.3 V ±4% (3.168 V–3.432 V).

Stuffing the shorting resistors and removing the second voltage regulator normally used for the $V_{I/O}$ plane are the most significant differences between this board design and the other designs. The voltage tap from the power supply unit will be able to handle the voltage draw from the processor's I/O, L2 cache, and chipset, and from all other 3.3 V components (e.g., DRAM).

The main cost savings with this design comes in not needing the second voltage regulator. This saves a significant amount on the Bill of Materials (BOM). This can all be done at build-time with one motherboard design.

The voltage regulator could be replaced with a discrete 2.8 V regulator because this board supports only one processor. This provides some cost-savings, but the additional cost of changing the Bill of Materials (BOM) and modifying the assembly line to support this may outweigh the cost-savings.

3.3 Switching vs. Linear Voltage Regulators

Both switching and linear voltage regulators can be used as voltage supplies for the flexible motherboard. Both regulators have advantages and disadvantages. This section highlights the general working principles of the two types of regulators and the factors that will affect your decision.

3.3.1 General Principles Of Switching And Linear Voltage Regulators

In dissipative regulation of voltage or current (as in a linear voltage regulator), power is lost in the form of heat. The dissipative element, a power transistor, is given the task of "soaking up" the excess power, which can result in heat dissipation problems. It does not matter how sophisticated the control electronics are in such a power supply; the dissipative element functions as a rheostat, which is a relatively simple method of regulating power.

In the switching power supply, a switching device is substituted for the dissipative device. Control or regulation of power is achieved by varying the duty cycle or repetition rate of the switch rather than its resistance. The ideal switch does not absorb or dissipate power–it is either completely on or completely off, with no intermediate resistive state to dissipate power. As a result, the overall efficiency of a switching regulator is much higher than conventional dissipative-type power supplies. A comparison is provided in Table 7.

Table 7. Comparison Between Switching and Linear Voltage Regulators

Feature	Switching Regulator	Linear Regulator
Efficiency	65% to 85% is expected.	25% to 50% is expected.
Overall Regulation	1% is common specification. Tighter regulation is usually difficult to achieve	1% is common. Much tighter regulation is available at greater cost.
Ripple	20 to 50 mV peak-to-peak is average. Smaller ripple voltage is usually difficult to achieve.	5 mV peak-to-peak is average and lower values can be obtained at greater cost.
Temperature Rise	20°C to 40°C is easily achieved.	50° C to 100° C is average, depending upon heat dissipation techniques.
Cost	Cost decreases with higher switch rates. There is a general tendency for costs to decrease as semiconductors evolve. Cost crossover keeps decreasing.	Small linear regulators have a cost advantage. However, considering all the factors in the overall system, other cost factors become very significant in larger ratings.
Reliability	More parts, but recent designs capitalize on ICS. Enhanced reliability obtained from cooler operation.	Higher operating temperature often degrades reliability.
Power Density	2.5 to 4 or 5 W per cubic inch for 20- to 50-KHz switchers. Higher switching rates can yield 25 to 75 W per cubic inch.	0.3 to 1.0 W per cubic inch depending on power level, input voltage range, and heat dissipation hardware.
Isolation from Line Transients	Very good, often greater than 60 dB.	Generally inferior to switching types. Noisy line often affects load.
RFI and EMI	Can be troublesome. Requires attention to shielding, suppression and filtering.	Less likely to be an adverse factor.

3.3.2 Design Considerations for Voltage Supplies

This section discusses design considerations that should be taken into account when choosing between switching and linear voltage regulators.

3.3.2.1 Real Estate

Because linear regulators are relatively simple devices compared to switching regulators, they take up much less real estate. However, this gain is often offset by the larger heatsink required on a linear regulator. Also, in some designs, components cannot be placed under or around the immediate vicinity of the heatsink. Therefore, although the linear regulator itself is small, the amount of real estate required to implement it may be considerably greater.

3.3.2.2 Tolerance

Switching regulators inherently have more ripple than linear regulators because they switch on and off during operation. This is why more (large) capacitors are required in a switching regulator solution (see “Decoupling Capacitors” on page 28). However, the difference in ripple between the two type of regulators is in the tens of millivolts range. Unless the timing requirements of the processor or other component are marginal, the extra ripple introduced by the switching regulator should not be a major design consideration.

3.3.2.3 Thermal Considerations

With the dissipative nature of linear regulators, more heat will be generated, requiring a better thermal solution for the system (for example, a better thermal flow-through system or a bigger heatsink).

3.3.2.4 Decoupling Capacitors

Switching regulators need larger, more expensive decoupling capacitors as opposed to linear regulators, which only need smaller tantalum capacitors.

3.3.2.5 Cost of Component

Because switching regulators are more complex components, they generally cost more than simpler linear regulators.

3.4 Split Power Plane Layout

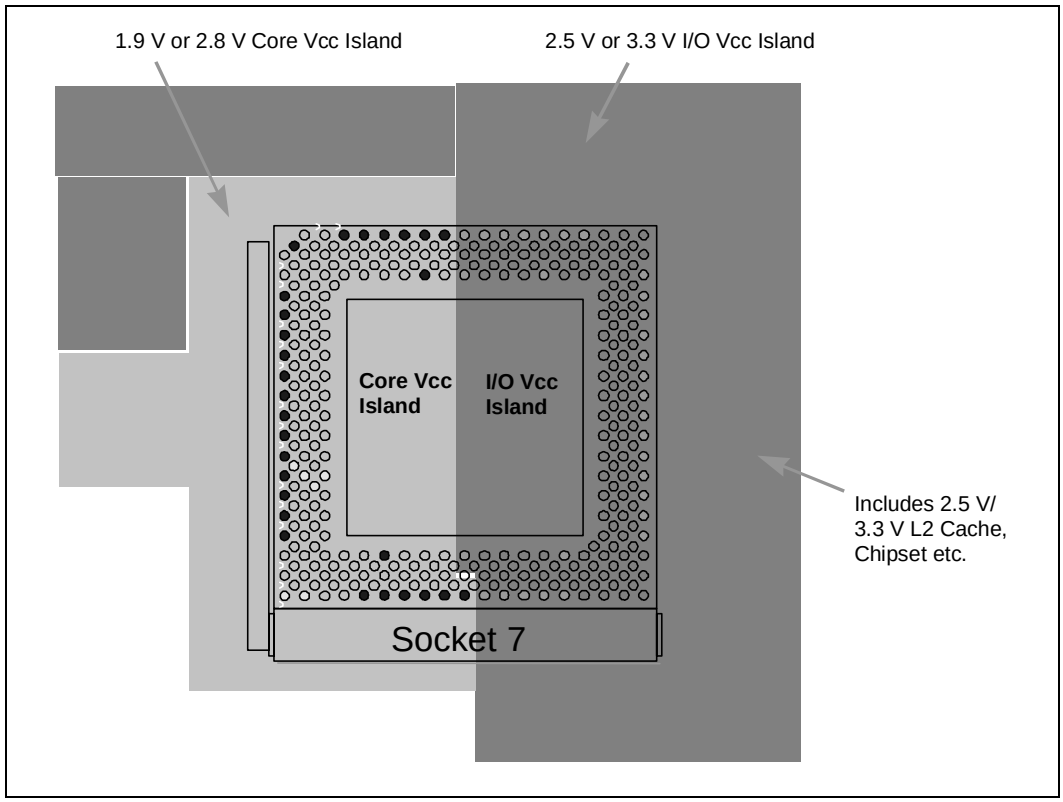
Implementing a power island on an existing power layer instead of assigning a separate power layer for core V_{CC} can be a more economical solution. The separate voltage island can be isolated from the other section of the power plane using an air gap. The size of the air gap is determined by analyzing the noise effects and board manufacturing capabilities (typically 10 to 20 mils).

Figure 8 shows a typical layout of the separate voltage islands in the processor area. It shows the core V_{CC} pins (V_{CC2}) clustered on one side of the processor to allow easy layout of the core voltage island. The remaining V_{CC} pins for the periphery (V_{CC3}) are located on the other side and are part of the I/O voltage island (refer to “Socket 7 Pin Diagram” on page 35).

The I/O V_{CC} island should also include other dual-voltage 2.5 V/3.3 V components that interface with the processor. A typical configuration would include 2.5 V/3.3 V cache SRAM, 2.5 V/3.3 V chipset I/O, and processor I/O on the same $V_{I/O}$ voltage island. This ensures that signals that provide an interface for the processor to the other dual-voltage 2.5 V/3.3 V components operate at the same voltage levels. This also avoids split plane crossovers for these signals. Removing split plane crossovers improves signal quality and reduces EMI/RFI effects.

Carefully routing the power source to the voltage islands should be done to avoid a significant voltage drop at the processor and an increase in thermal dissipation in the voltage islands. It is recommended that wide traces be used to prevent excessive voltage drop across the power plane. Vias and through-holes cutting through the power plane at critical widths should be avoided.

Figure 8. Processor Power Island Layout



3.5 Decoupling

Proper decoupling of the island power plane voltage and ground plane is essential due to the small size of the processor core voltage island, its isolation from the motherboard power plane, and support of varied voltage requirements. Appropriate decoupling capacitors are implemented on the voltage island near the processor to ensure that the processor voltage stays within specified limits during normal and transient conditions. There are two types of decoupling that need to be considered: bulk decoupling and high-frequency decoupling.

3.5.1 Bulk Decoupling

For the processors supported on the flexible motherboard, the power consumption can transition rapidly from a low level to a much higher level (or vice versa). This can happen during normal program execution or during specific events such as entering or exiting the Stop-Grant state. Another example is when executing a HALT instruction that causes the processor to enter the AutoHALT Power Down state or transition from HALT back to the Normal state. (The AutoHALT Power Down feature is always enabled, even when other power management features are not implemented.)

Because the voltage supply (regulator) cannot instantaneously respond to a sudden load change, bulk storage capacitors with low ESR (effective series resistance) are used to maintain the regulated supply voltage during the interval from when the current load changes to when the regulated power supply output reacts to the change. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

3.5.2 High Frequency Decoupling

To minimize noise, high frequency decoupling may be required to provide a short, low-impedance path to high frequency components such as high current spikes. Transient power surges can result when the processor drives its large address and data buses at high frequencies, particularly when driving large capacitive loads.

For high frequency decoupling, low inductance capacitors and interconnects are recommended for best high speed electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. Surface mount capacitors are preferable, because capacitors with long leads add inductance to the circuit. The capacitors should be RF grade, with low ESR and low inductance to reduce spikes.

3.5.3 Decoupling Recommendations

Table 8 shows the processor decoupling recommendations for the flexible motherboard for both the processor core and I/O voltage islands. This is based on simulation and testing of the voltage transients from the processor and the effects of motherboard decoupling.

Spice modeling (modeling worst case current transients including the processor package inductance, capacitance, routing, decoupling, and voltage regulator output inductance) should be used to estimate the amount of decoupling capacitance required for the processor voltage island.

It is highly recommended that the solution be simulated for a variety of variables in components, temperature, and lifetime degradation before committing to any change from the decoupling capacitor recommendation.

For bulk decoupling, tantalum capacitors are recommended over electrolytic capacitors. In general, electrolytic capacitors degrade at a much faster rate, are not as accurate, and are not as stable over temperature as tantalum capacitors.

For high speed decoupling in the processor core voltage island, low inductance 1-µF capacitors of X7R dielectric are recommended. These capacitors decouple the processor core for high frequency noise and control the voltage during very fast transients (less than 100 ns). Figure 9 shows that ceramic capacitors of X7R (or X7S) dielectric exhibit relatively stable capacitor characteristics over temperature compared to capacitors of Z5U- or Y5V-type dielectric. For example, at a typical operating temperature of 45°C, the Y5V dielectric can lose 45% of the initial rated capacitance.

Additional 0.1 µF capacitors between power planes (stitching capacitors) may be needed to improve EMI and signal return path. The need for these stitching capacitors is layout and design dependent. On the flexible motherboard for the a Pentium processor with MMX technology family, it is recommended to place one 0.1 µF capacitor near every three high speed signals (data and low address signals) that cross the V_{CORE}-$V_{I/O}$ power islands gap (within a distance of one inch). The placement of these stitching capacitors also depends on the specific design and layout of the motherboard.

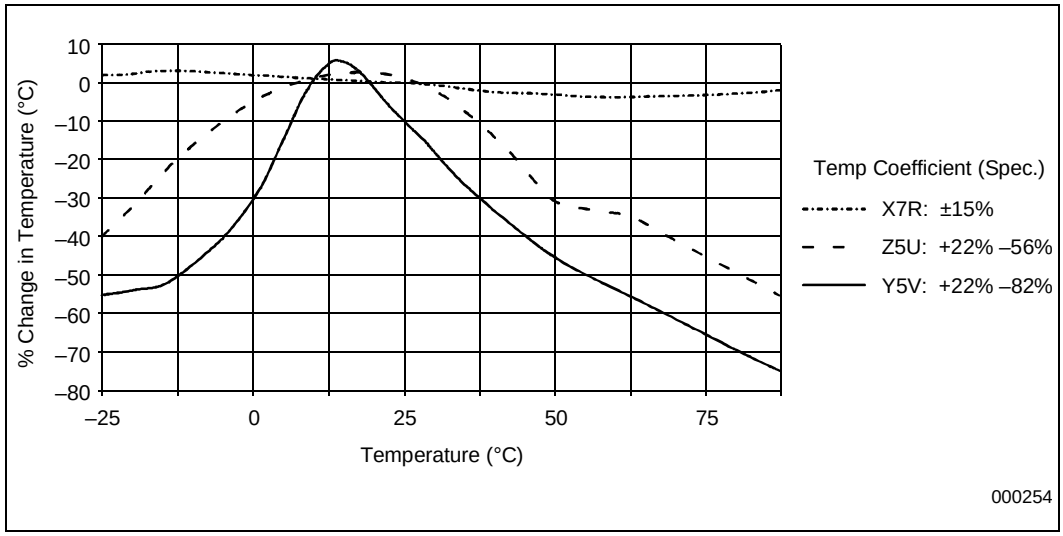
For information on measurement techniques for ensuring that motherboard designs are within V_{CC} noise and transients specification, refer to *AP-580: Voltage Guidelines for Pentium® Processors with MMX™ Technology Processors* application note (order number 243186).

Table 8. Decoupling Recommendations for Processor Core and I/O Voltage Islands

	Quantity	Value	ESR	ESL	Type
Processor core voltage island	4	100 µF	25 mOhms [1]	0.45 nH [2]	Tantalum
	25	1 µF	0.6 mOhms [3]	0.084 nH [4]	X7R dielectric, ceramic
Processor I/O voltage island [5]	12	0.1 µF	—	—	603 Type
Between V_{CC2} – V_{CC3} power planes	One for every three high-speed signals	0.1 µF	—	—	603 Type

NOTES:
1. ESR per capacitor should be less than 100 mOhms.
2. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.7 nH.
3. ESR per capacitor should be less than 15 mOhms.
4. ESL per capacitor (including 0.7 nH Via inductance per capacitor) should be less than 2.1 nH.
5. This does not include decoupling for components other than the processor in the 3.3 V I/O voltage island.

Figure 9. Typical Capacitance Change vs. Temperature



3.5.4 Placement of Decoupling Capacitors

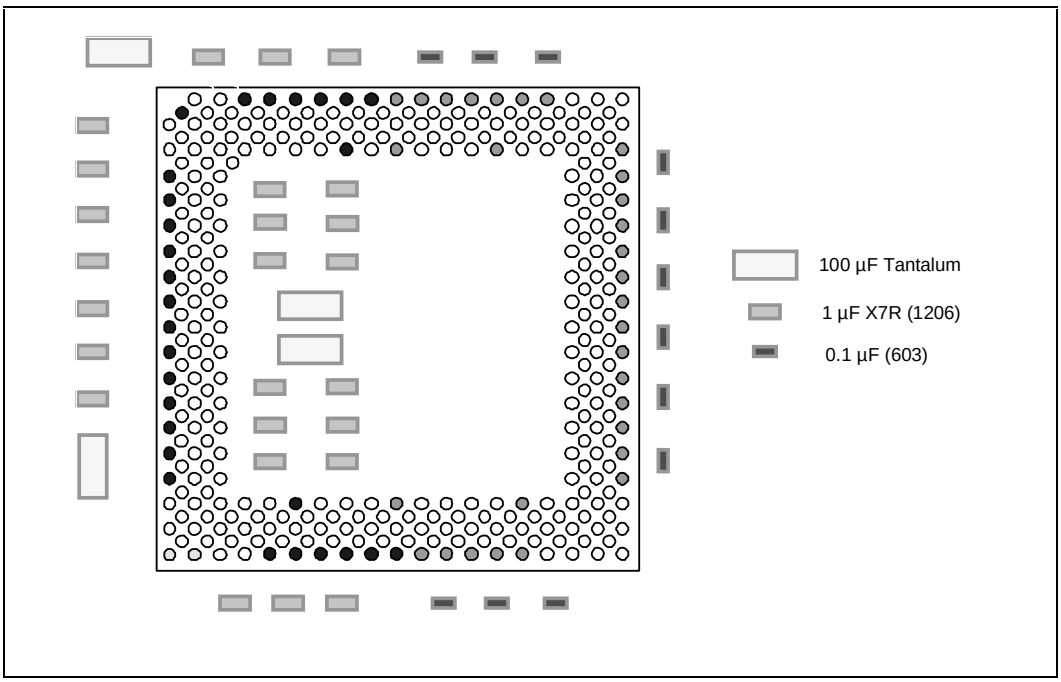
Figure 10 shows an example of how the recommended processor decoupling capacitors (Figure 8) should be placed inside the respective voltage islands on the flexible motherboard. The bulk capacitors should be placed near the processor inside the voltage island to ensure that the supply voltage stays within specified limits during changes in the supply current during operation. The 1-µF X7R capacitors should be evenly distributed inside the processor core voltage island inside and around the processor footprint. Figure 10 shows the twelve 0.1-µF capacitors evenly placed around the processor, close to the processor V_{CC3} pins inside the processor I/O voltage island.

In this example, all the capacitors are placed on one side of the board. If components are assembled on both sides of the board, these capacitors can be distributed between the top and bottom sides. When done this way, vias connecting the capacitor pads to the power and ground layers can be shared between the capacitors on the top and bottom sides. However, sharing vias (common vias) limits the total current flow, hindering fast transient response. Separate vias are preferable because they can lower the effective ESR. Use shared vias when there is no more space on the board.

The traces connecting the vias to the capacitor pads should be kept as short as possible. When it is difficult to reduce the length of the circuit board trace, the trace should be made wider to reduce the trace inductance.

Placement for the stitching capacitors between the V_{CORE}–$V_{I/O}$ power islands is not shown in Figure 10. This is because their placement depends on the exact layout and design of the motherboard (for example, whether the board has four or six layers, and how the socket is oriented in relation to other board components).

Figure 10. Example of Processor Decoupling Capacitor Placement



3.6 Signal Routing Guidelines

Because the power plane on the flexible motherboard is split into separate voltage islands, signal routing should be implemented in a way that minimizes crossovers between voltage islands for high-speed signals. Signal routing between the voltage islands and the system power plane should be limited to only those signals that must cross the gap between the island and the power plane. This avoids possible signal degradation from impedance discontinuity effects. Significant levels of EMI could be generated by electromagnetic radiation from high-speed traces (such as clocks, strobes, data lines and low address lines) when their return path is interrupted. On a multi-layer board, this return path is on the power or ground plane adjacent to the signal layer and directly under the signal trace. When this trace is routed over a break in the return path, the return current must find a longer path to maintain current continuity. The increased area generated by the signal trace and the length of this extended return path can lead to increased radiation levels from this signal trace.

The following guidelines should be followed when routing high-speed signals on the flexible motherboard:

- **Clocks and Strobes:** These signals should not be routed over breaks in the reference plane return path. The use of vias to connect between signal planes should be minimized, and the signal planes should be within 8 mils of the reference plane. Clock signals should be routed on the layer that is adjacent to the ground layer.
- **Data Bus and Low Address Lines:** These signals can be routed on any signal layer. However, it is desirable to minimize the number of traces crossing over splits in the return path plane. Among this group, signals that must cross the gap should be routed on the signal layer near the ground plane to minimize radiated emissions (using a via, a trace may be taken down to the layer that is referenced to the ground plane). On a four-layer board, the signal layer with the least potential for signal crossovers should be placed adjacent to the power plane. Capacitive decoupling across the split planes can also be used near signal crossovers (for those that cannot be avoided) to help reduce the magnitude of EMI radiation. Within an inch of the signal crossover violation, an 0.1-µF ceramic capacitor should be placed across the power plane gap, using one capacitor for every three trace violations (provided they are all within the one-inch limit).

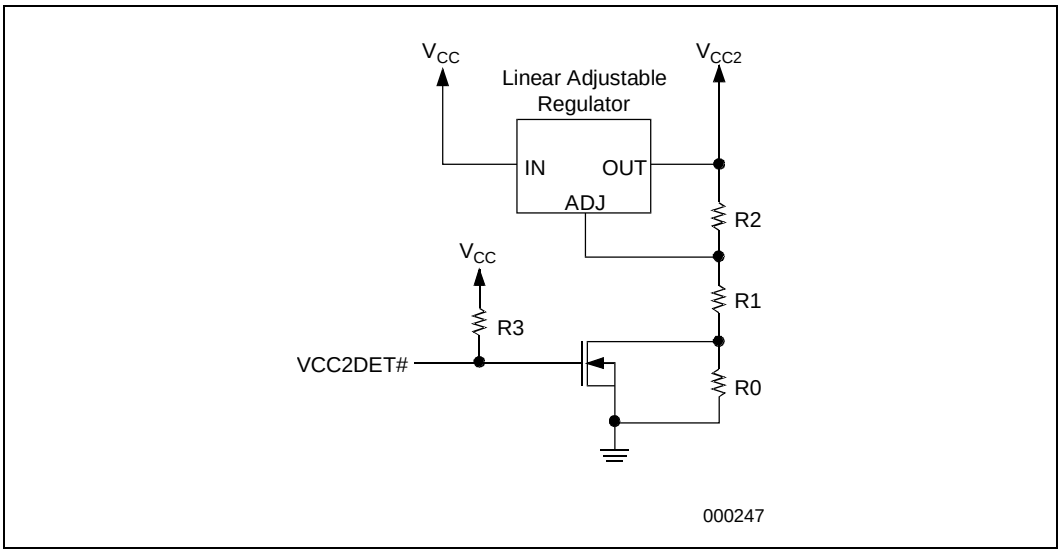
3.7 VCC2DET# Auto-Detect Circuit

Although jumpers and resistors could be used, an auto-detect circuit driven by the VCC2DET# signal is recommended for configuring the flexible motherboard for two main reasons:

- The auto-detect circuit makes the flexible motherboard more user-friendly. It eliminates the need for the user to manually configure the board for each processor or remember jumper settings. With an auto-detect circuit, the motherboard will automatically configure itself when the processor is inserted into the socket and powered on.
- The auto-detect circuit also serves as a safeguard against incorrect voltages to the low-power embedded Pentium processor with MMX technology. Because the low-power processor is not 2.8 V or 3.3 V tolerant, accidentally applying those voltages could damage it. An auto-detect circuit prevents this by automatically setting the voltage regulators to 1.9 V and 2.5 V, eliminating the possibility of human error.

Figure 11 is an example of implementing an auto-detect circuit.

Figure 11. VCC2DET# Auto-Detect Circuit



The auto-detect circuit can configure a number of settings. The 1.9 V/2.8 V and 2.5 V/3.3 V voltage regulators could be configured depending on the VCC2DET# signal. The auto-detect circuit can turn on or turn off a cooling fan depending on which processor is running. This circuit can configure any setting on the motherboard that is dependent on the processor.

The VCC2DET# pin is defined as floating for Pentium processors at 100/133/166 MHz, but there should be minimal or no issues from this overlap; the low-power embedded Pentium processor with MMX technology and the Pentium processors at 100/133/166 MHz are not normally supported on a single motherboard design.

3.8 BIOS/Software Considerations

Since the flexible motherboard can accommodate a variety of processors, the BIOS should be designed to support all processors that may be used. The BIOS code should use the CPUID instruction to identify the processor's CPUID signature (see "Processor ID with the CPUID Instruction" on page 16).

The fastest low-power embedded Pentium processor with MMX technology operates at 266 MHz (compared to the fastest embedded Pentium processor with MMX technology, which operates at 233 MHz). Therefore, BIOS code should not contain software timing loops and should be independent of the prefetch algorithm.

3.9 Dual Processor Design Considerations

The low-power embedded Pentium processor with MMX technology does not support dual processor (DP) mode. The flexible motherboard should not support dual processors.

4.0 Socket 7 Pin Diagram

Figure 12. Socket 7 Pinout—Top Side View

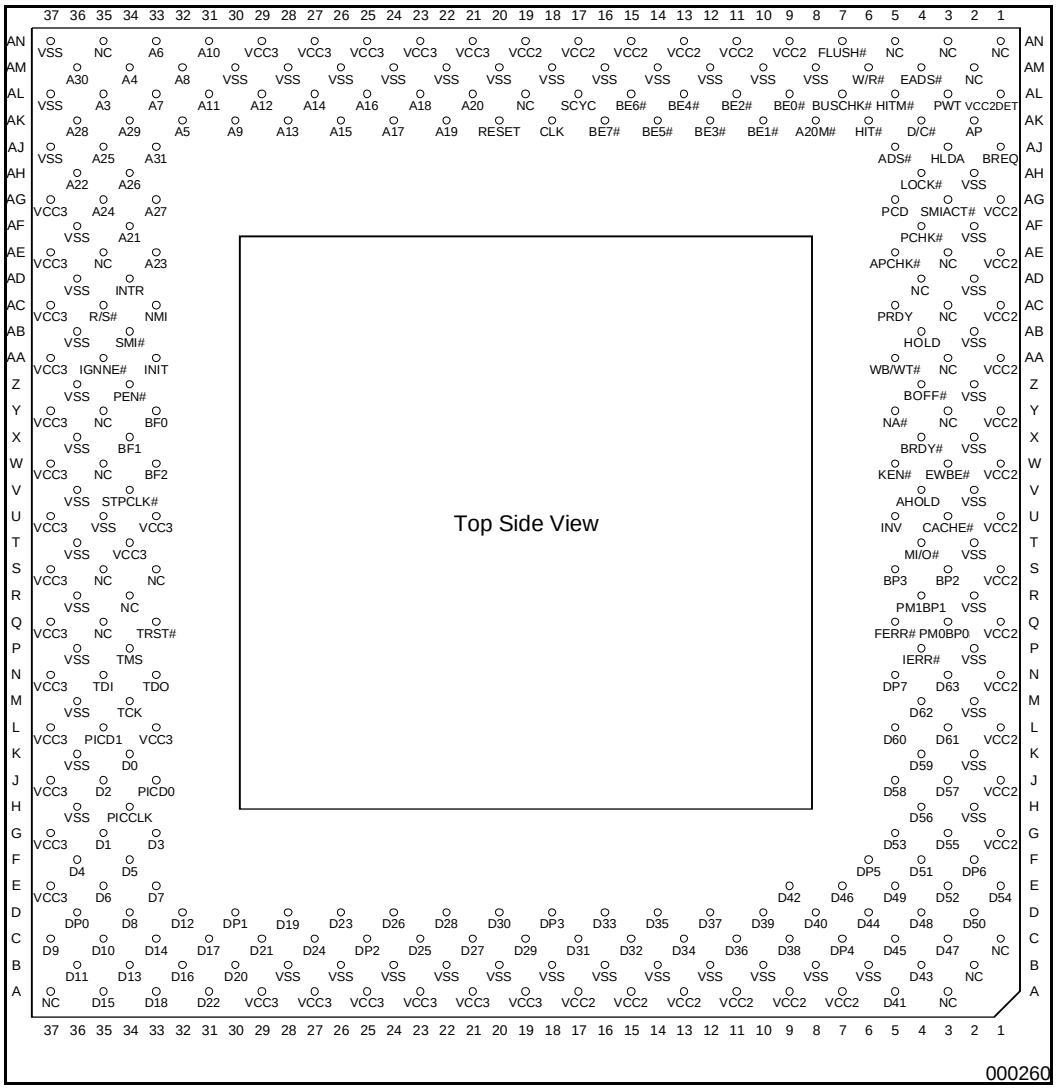
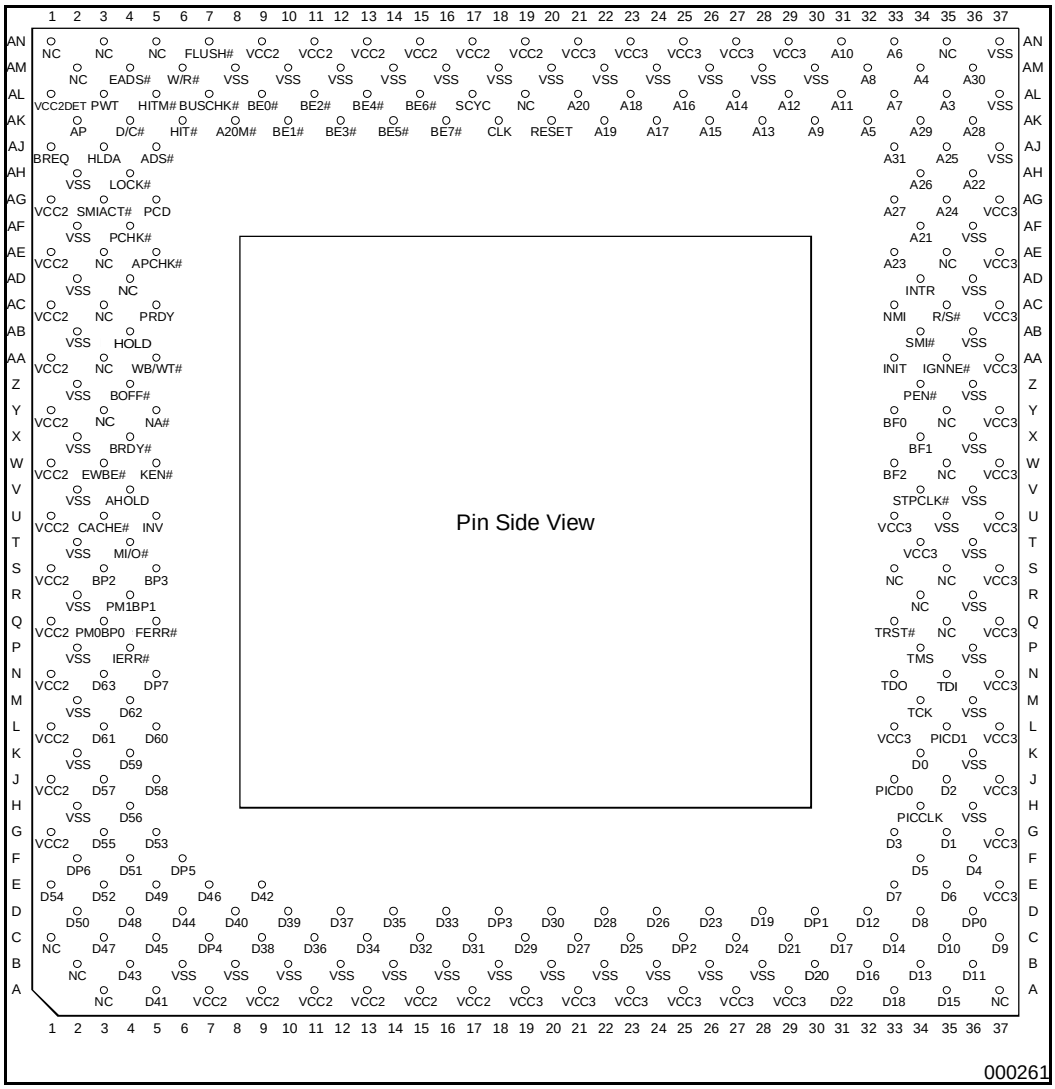


Figure 13. Socket 7 Pinout—Pin Side View



Socket 7 has the same pin definition as Socket 5 with the exception of the pins listed below.

Table 9. Socket 7 Pins that Differ from Socket 5

Symbol	Type	Name and Function
CLK, PICCLK	(I)	Unlike some Pentium® processors, the **Clock** and **Programmable Interrupt Controller Clock** inputs to Socket 7 are *not* 5 V tolerant. These inputs are driven by an appropriate 2.5 V or 3.3 V clock driver.
VCC2DET#	(O)	**V_{CC2} Detect** is defined for the Pentium processor with MMX™ technology family. The embedded Pentium processor with MMX technology, with a core voltage of 2.8 volts, always drives VCC2DET# low. The low-power embedded Pentium processor with MMX technology leaves this pin floating. This pin may be used to select the proper core voltage from a voltage regulator or system supply. The VCC2DET# system trace has a pull-up for proper use.
V_{CC2}	(I)	Socket 7 has 28 power supply pins defined for the core voltage on processors with separate power inputs.
V_{CC3}	(I)	Socket 7 has 32 power supply pins defined for the I/O voltage on processors with separate power inputs.

5.0 Heat Transfer Fundamentals

The objective of all thermal control programs in electronic packaging is the efficient removal of heat from the semiconductor junction to the ambient environment. Thermal management can be separated into three major phases:

1. Heat transfer processes within the semiconductor device.
2. Heat transfer from the device to a heat sink.
3. Heat transfer from the heat sink to the ambient environment.

The first phase is usually beyond the control of the packaging engineer because heat transfer characteristics are determined by the manufacturer of the device. To optimize heat transfer in the second and third phases, it is essential to understand the fundamental heat transfer processes and to have knowledge of material properties.

5.1 Thermal Theory

The rate at which heat flows through a material is proportional to the area normal to the heat flow and to the temperature gradient along the flow path. For one-dimensional, steady-state heat flow, the rate can be expressed by Fourier's Law:

$k = (q/A) \times (d/\Delta T)$

where:

k	=	thermal conductivity
q/A	=	heat flux (watts per unit area)
d	=	length of the heat flow path
ΔT	=	temperature gradient

Thermal conductivity, k, is an intrinsic property of a homogeneous material that describes the ability of that material to conduct heat. A higher value means that the material can conduct a greater heat flux for a given temperature gradient.

Inspection of Fourier's Law leads to another thermal property, thermal impedance – the temperature gradient caused by a unit rate of heat flow through a material of a given size. Thermal impedance is equal to:

$Ø = \Delta T/(q/A)$

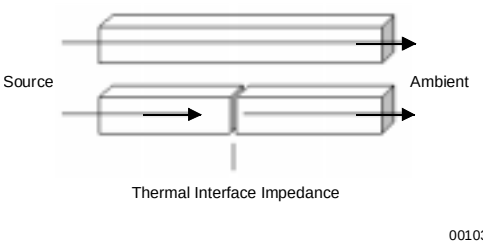
Thermal impedance is related to thermal conductivity by the rearrangement of Fourier's Law:

$k = d/Ø$

Unlike thermal conductivity, thermal impedance is proportional to the distance the heat must travel.

Fourier's Law describes heat flow within a solid. Suppose two solids are brought into contact and heat is conducted from one solid into the other. In addition to the normal temperature gradients within the solids, a significant temperature gradient is observed due to the interface between the two solids. See Figure 14. This is referred to as thermal interfacial impedance, or thermal contact resistance.

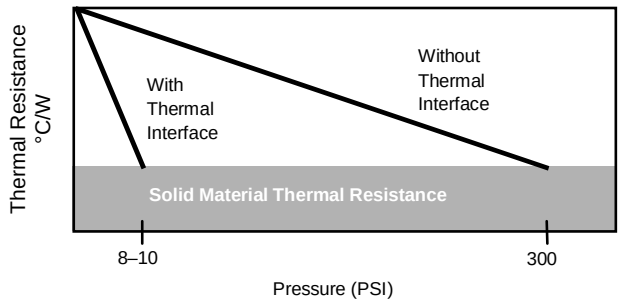
Figure 14. Thermal Flow to Ambient Environment



Contact resistance is caused by inherent irregularities of the contacting surfaces. Each surface, no matter how well polished, consists of peaks and valleys. The actual metal-to-metal contact area is a small fraction of the total contact area. Voids formed by valleys are filled with air and contribute little to the conduction of heat. The majority of the heat flow is constricted to the small areas of metal-to-metal contact. This accounts for the observed temperature gradient across the interface.

The thermal interfacial resistance of two solids can be minimized by increasing the normal pressure between the two adjoining surfaces of the solids. This action minimizes the air gaps and surface valleys. Theoretically, if enough pressure were applied, the adjoining metal surfaces of the two solids would eventually become a metal-to-metal contact. See Figure 15. As an example, 300 pounds per square inch (PSI) of pressure would have to be applied to two metal solids to form a metal-to-metal contact that provides an acceptable thermal interfacial resistance. However, from a manufacturing view, applying high pressure and creating devices that maintain this high pressure between two solids can be very expensive. Thus, other options of using thermal interface materials must be utilized.

Figure 15. Pressure Applied to Two Solids to Equal Thermal Resistance of a Single Solid



5.2 Thermal Interface Material Basics

Heat generated by a semiconductor device must be removed to the ambient environment to ensure the device's reliable operation. Unless space is available to provide sufficient forced convection cooling, this requires a series of physical interfaces to provide a thermally conductive path. Not only must these interfaces offer minimum resistance to heat flow, but they often must also provide electrical isolation. Such requirements can be met using conventional insulators coated with thermal grease, or with one-component thermal interface materials.

A thermally conductive insulating material should provide electrical isolation because the two metal surfaces are separated by the dielectric material. Thermal contact resistance has been minimized because the air gaps have been eliminated and replaced with a material whose thermal conductivity is much greater than that of air.

To perform successfully, thermal interface materials must have high dielectric strength, high thermal conductivity and sufficient pliancy to conform to both microscopic and macroscopic surface irregularities. They must also be sufficiently durable to survive a variety of assembly, use, and environmental conditions.

Composition – Thermal interface materials generally consist of a thermo-set elastomeric binder containing a dispersed, highly thermally conductive ceramic filler. This mixture is generally reinforced with glass fiber, metal foil, or dielectric film. The elastomer binder is typically a silicone molding resin cured at high temperatures and high pressure. Urethane elastomers have been introduced for use where silicone cannot be tolerated due to possible contamination. Ceramic fillers are added to the elastomer to increase its thermal conductivity. Typical fillers are boron nitride, aluminum oxide and magnesium oxide.

Thermal Conductivity – Thermal conductivity is a measure of the ability of a material to conduct heat only after heat has entered the material. This ability is determined by the material's composition (i.e., the type and ratio of thermal filler to elastomeric binder) and by the relative amount of reinforcing metal foil, glass fiber, or dielectric film. Thermal conductivity is usually expressed in units of Watt/m-K, where, W/m-K = (Cal/s-cm–°C x 420) = (BTU–in/hr–ft2–°F x 0.14).

Values reported in different literature must be used with caution unless the test method is clearly stated. Thermal conductivity is difficult to measure for thin, resilient interface materials. Many test methods cannot distinguish between contact resistance and sample resistance, leading to unrealistically low values. Other methods based on calculations from "TO-3 Thermal Impedance Data" may overestimate thermal conductivity.

In homogeneous materials, thermal conductivity is independent of physical dimensions. Un-reinforced materials can be considered homogeneous and their thermal conductivity is independent of thickness. All reinforced materials are non-homogeneous in that the reinforcing layer is a poor thermal conductor compared to the outer elastic layers, which are good thermal conductors. As sample thickness is increased, the reinforcing layer remains constant while the elastomeric layer expands. The ratio of good conductor to poor conductor increases, and the apparent, or total, thermal conductivity increases.

When making thermal calculations based on thermal conductivity, care must be exercised to take into account all contact resistances that may be present in the thermal path. Other complications resulting from non-uniform heat flow, such as hot spots and thin heat spreader plates, can cause an underestimated temperature differential between the junction and ambient, and lead to unsafe operating temperatures.

Thermal Impedance – Like thermal conductivity, thermal impedance is a measure of a material's ability to conduct heat. In addition, thermal impedance describes a material's ability to conform to irregular surfaces and minimize contact resistance.

Thermal interface materials can reduce contact resistance by conforming to two rough mating surfaces and eliminating air gaps. Most of these elastomeric materials are highly loaded with hard ceramic fillers. They require pressure to make them "flow" into the surface irregularities and reduce contact resistance.

The contact resistance is high at low pressures due to poor mating. As pressure is increased, the material begins to flow into the surface irregularities and the contact resistance decreases. At 300 to 500 psi, the contact resistance is essentially eliminated because thermal impedance is not influenced by further pressure increase. To illustrate, at 10 psi the thermal impedance due to contact resistance is three times as great as the resistance due to the material itself.

The pressure needed to achieve minimum thermal impedance is easily accommodated in most packages. In fact, secure attachment of components to heat sinks usually requires the same magnitude of force holding the component to the sink. However, recent developments, such as surface mount applications and heat sinking of microprocessors, require that good thermal contacts be made with minimum applied pressure. A new approach is required for applications in which an interface material must conform at very low pressure.

Suitable materials for such applications have been developed based on a precise balance of pliancy and thermal conductivity. By careful adjustment of filler level and binder elasticity, they are made with essentially no contact resistance below 10 psi.

Dielectric Strength – Measured according to ASTM D149, dielectric strength is defined as the AC voltage required to cause a breakdown of the insulating material being tested. The results are reported as the Dielectric Breakdown Voltage for a given thickness or as a Dielectric Strength in volts/mil.

Measurements using ASTM D149 yield values are obtained under controlled test conditions and may not accurately reflect actual field performance. Factors such as corona discharge, frequency, temperature and humidity can significantly affect the long-term insulating characteristics of a material. Allowances for creep and strike distance must often be made to meet electrical requirements. One effective technique is to use an interface insulator slightly larger than the base of the device case.

Volume Resistivity – Volume resistivity as determined by ASTM D257 is a measure of bulk electrical resistance. This property shows a strong inverse dependence on humidity and temperature. It is not unusual for volume resistivity to change by a factor of 105-106 when a material is exposed to more than 90% humidity. Increasing temperatures yield similar, though not such drastic, changes. These changes are completely reversible. When conditions are returned to normal, the volume resistivity also returns to the original value.

Elastomeric Properties – Thermal interface materials exhibit properties consistent with highly filled elastomers, such as compression deflection, stress relaxation, and compression set. Each property has a major impact on the long-term effectiveness of an interface material.

Compression Deflection – A solid elastomer, as opposed to a foam, is not compressible, but will yield when a load is applied. Under a compressive load, the material undergoes a deflection. The magnitude of the deformation is proportional to the load up to the elastic limit – the point at which the material ruptures and can no longer recover.

Stress Relaxation – When an elastomer is subject to a compressive load, it first undergoes deflection while the load is applied. This is followed by a slow relaxation process whereby the initial stress begins to decay. A natural rubber process, this stress decay is brought about by macromolecular rearrangement within the elastomer. The initial load causes the rubber to fill the gaps. There is then no further need for such high pressure. In time, the stress decays to a level at which it is insufficient to cause further rearrangement. This point, or percent stress loss, is dependent on several factors, including the nature of the elastomer and the level of loading.

Compression Set – When an elastomer is subject to a compressive load for an extended time, a part of the deflection becomes permanent and is not recoverable when the load is removed. This behavior is important only in designs in which the interface material must be unloaded and reloaded occasionally during its service life.

Chemical Resistance – Interface materials may come into short-term contact with solvents either in solder-flux and cleaning operations or through unintentional exposure to coolants, fluids, or lubricants. Contact with any number of solvents causes swelling of the exposed areas of elastomer interface materials. The severity of the swelling depends on the type of solvent, the duration of exposure, and the type of elastomer. Generally, solvents such as ketones, halogenated hydrocarbons and esters cause more swelling than alcohols or aromatics.

While the elastomer is swollen, its resistance to abrasion is reduced and care should be taken not to damage the material. The swelling phenomenon is reversible and the interface material returns to its normal state as the solvent evaporates. All physical, electrical, and thermal properties remain the same as before the exposure.

See “Vendors and Device Suppliers” on page 43 for thermal interface material manufacturers.

6.0 Vendors and Device Suppliers

6.1 Device Suppliers for Design Conversion

This section contains a list of suppliers for devices[1] to support the conversion of existing Pentium processors with MMX technology designs to designs that also support the low-power embedded Pentium processor with MMX technology. The list is not comprehensive and may not be all-inclusive or accurate for all vendor solutions. The list is intended to provide a reference of known suppliers and solutions. New components and suppliers may not be included. Omissions do not indicate or imply incompatibilities.

Table 10. Design Conversion Device Suppliers

	Embedded Pentium® Processors with MMX™ Technology	Low-Power Embedded Pentium Processor with MMX Technology	Supplier	Part Number
Switching Type Voltage Regulators	V_{CC3} = 3.3 V ±5% I_{CC3} = 750 mA V_{CC2} = 2.8 V ±100 mV I_{CC2} = 6.5 A	V_{CC3} = 2.5 V ±5% I_{CC3} = 380 mA V_{CC2} = 1.9 V ±142 mV I_{CC2} = 4.0 A	Linear Technology Maxim	
Clock Drivers		CKDM-66 specifications	Cypress ICS ICWI IMI	CY2277 9148F-02 W48S67-01H SC671D
SRAM/Cache (1 Mbit)	PB1.0 SRAM	PB1.5 SRAM	Cypress Hitachi IDT Mitsubishi (1 and 2 Mbit) Motorola Samsung Sony Toshiba	
TagRAMs			Cypress IDT Mitsubishi Toshiba	

1. Other brands and names are the property of their respective owners.

6.2 Vendor Contact List

Table 11. Voltage Regulators

Vendor	North America	Europe	Asia	Japan
Cherry	Tel: (401) 886-3305 Fax: (401) 885-5786			
Harris	Tel: (919) 405-3603 Fax: (919) 405-3651	Tel: (33) 1 346 54046 Fax: (33) 1 394-64054	Tel: (886) 2 716 9310 Fax: (886) 2 715 3029	Tel: (81) 3 3265 7571 Fax: (81) 3 3265 7575
Linear Tech	Tel: (408) 432-1900 Fax: (408) 434-0507	Tel: (49) 89 9642550 Fax: (49) 89 963147	Tel: (65) 753 2692 Fax: (65) 754 4112	
Linfinity	Tel: (714) 898-8121 Fax: (714) 893-2570			
Maxim	Tel: (408) 737-7600 Fax: (408) 737-7194	Tel: (44) 17 3430 3388 Fax: (44) 17 3430 5511	Tel: (886) 2558 6801 Fax: (886) 2555 6348	Tel: (81) 3 3232 6141 Fax: (81) 3 3232 6149
National	Tel: (408) 721-3753 Fax: (408) 721-8763	Tel: (49) 81 4135 1331 Fax: (49) 81 4135 1220	Tel: (852) 2737 1616 Fax: (852) 2736 9931	Tel: (81) 43 299 2373
Raytheon	Tel: (415) 9667734 Fax: (415) 966-7742	Tel: (44) 17 0566 5555 Fax: (44) 17 0566 3355	Tel: (81) 3 3406 5998 Fax: (81) 3 3406 5998	
Semtech	Tel: (805) 498-2111 Fax: (805) 498-3804	Tel: (44) 592-773520 Fax: (44) 592-774781	Tel: (886) 2 717 3389 Fax: (886) 2 713 0282	
Siliconix	Tel: (408)-970-5543 Fax: (408)-567-8910	Tel: (44) 344 485757 Fax: (44) 344 427371	Tel: (852) 2378 9715 Fax: (852) 2375 5733	Tel: (81) 3 5562 3321 Fax: (81) 3 5562 3316
Unitrode	Tel: (603) 429-8504 Fax: (603) 429-8963	Tel: (44) 181 318 1431 Fax: (44) 181 318 2549	Tel: 8522-722-1101 Fax: 8522-369-7596	
Unisem	Tel: (714) 453-1008 Fax: (714) 453-8748			

Table 12. Socket 7 Vendors

Vendor	North America	Europe	APAC	Japan
Amp	Tel: (910) 855-2247 Fax: (910) 855-2224	Tel: (44) 753-67-6892 Fax: (44) 753-67-6808	Tel: (81) 44-844-8086 Fax: (81) 44-812-3203	
Appros	Tel: (81) 45-941-4080			
Augat	Tel: (508) 699-9890 Fax: (508) 695-8111	Tel: (44) 952-670-281 Fax: (44) 952-670-342	Tel: (81) 44-853-5400 Fax: (81) 44-853-1113	
Foxconn	Tel: (408) 749-1228 Fax: (408) 749-1266		Tel: (886) 2-268-3466 Fax: (886) 2-268-3225	
Yamaichi	Tel: (408) 456-0797 Fax: (408) 456-0779	Tel: (49) 89-451021-43 Fax: (49) 89-451021-10	Tel: (886) 02-546-0507 Fax: (886) 02-546-0509	Tel: (81) 3-3778-6161 Fax: (81) 3-3778-6181
Berg/ McKenie	Tel: (510) 651-2700 Fax: (510) 651-1020			

Table 13. Decoupling Capacitor Vendors

Vendor	Part No.	Type	North America	APAC
AVX	1206YZ105KAT1A	1 µF, X7S	Tel: (803) 946-0616	Tel: (65) 258-2833 Fax: (65) 258-8221
	TPSD107K010R0100	100 µF, Tantalum	Fax: (803) 946-6678	Tel: (82) 2-785-6504 Fax: (82) 2-784-5411
Johanson Dielectrics	160R18W105K4	1 µF, X7R	Tel: (818) 364-9800 Fax: (818) 364-6100 NCTR (California only) Tel: (510) 624-8900 Fax: (510) 624-8905	Nanco Electronics Tel: (886) 2-758-4650 Fax: (886) 2-729-4209 Sales Dept (Hong Kong) Tel: (852) 765-3029 Fax: (852) 330-2560
KEMET Electronics	T495X107K010AS	100 µF, Tantalum	Richey-Cypress Elect. Tel: (408) 654-9100 Fax: (408) 566-0160	Tel: (800) 421-7258 Fax: (714) 713-0129
Murata Electronics	GRM40X7R105J016	1 µF, X7R	Sales Department Tel: (770) 436-1300 Fax: (770) 436-3030	Taiwan Tel: (886) 2-562-4218 Fax: (886) 2-536-6721 Hong Kong Tel: (852) 782-2618 Fax: (852) 782-1545 Korea Tel: (82) 2-730-7605 Fax: (82) 2-739-5483
TDK	CC1206HX7R105K	1 µF, X7R/X7S	Sales Department Tel: (847) 803-6100 Fax: (847) 803-6296	Korea Tel: (82) 2-554-6633 Fax: (82) 2-712-6631 Taiwan Tel: (886) 2-712-5090 Fax: (886) 2-712-3090 Hong Kong Tel: (852) 736-2238 Fax: (852) 736-2108

Table 14. Resistor Vendors

Vendor	Size	Type	Accuracy/Value	Contact
Thin Film Technology	1208	Thin	0.1%, 100–250 kΩ 0.5%, 10–250 kΩ	(507) 625-8445 Region Sales Mgrs
	0805	Thin	0.1%, 100–100 kΩ 0.5%, 10–1MΩ	West of Mississippi (except Texas and So. Calif.)
	0803	Thin	0.1%, 100–33 kΩ 0.5%, 10–330 kΩ	Southern US, east of Mississippi (inc. Texas)
	0402	Thin	0.5%, 10–100 kΩ	Northern U.S., east of Mississippi and Canada (310) 768-8923 Southern California
Dale Electronics	0603	Thin	0.5%, 10–100 kΩ	(402) 371-0080
		Thick	1%,2%, 10–1 MΩ	
	805	Thin	0.1%, 100–100 kΩ	
Koa Spear	805	Thin	0.1%, 100–100 kΩ	(814) 362-5536
		Thick	0.5-5%, 10–1 MΩ	
Beckman Industrial	0805	Thin	0.1%, 10K–100 kΩ	(214) 392-7616
		Thick	1-5%, 10–1 MW	
	0603	Thick	1-5%, 10–1 MW	

Table 15. 3.3 V Clock Driver Suppliers

Supplier	Phone	Fax
ICS	408-925-9493	408-925-9460
ICW	408-922-0202 ext 1131	408-922-0833
National Semiconductor	408-721-2990	408-732-6017
Cypress Semiconductor	206-821-9202 ext 325	206-820-8959
Texas Instruments	903-868-5694	903-868-5962
IDT	408-492-8366	408-492-8362
AMCC	619-535-6526	619-450-9885
Motorola	602-952-3046	602-952-3682
Triquint Semiconductor	503-644-3535	503-644-3198
IMI	408-263-6300	408-263-6571

Table 16. SRAM/TagRAM

U.S. Sales Office	Address	Phone	Fax
SRAM			
Cypress Semiconductor		(206) 821-9202 x325	(206) 820-8959
Hitachi America	2000 Sierra Point Parkway Brisbane, CA 94005	(800) 285-1601	(303) 297-0447
IDT		(408) 492-8366	(408) 492-8362
Mitsubishi Electric	1050 East Arques Avenue Sunnyvale, CA 94086	(408) 730-5900	(408) 732-9382
Motorola		(602) 952-3046	(602) 952-3682
Samsung	3566 North First Street San Jose, CA 95134	(408) 954-6957	(408) 954-7441
Sony	3300 Zanker Road, M/S SJ-3C4 San Jose, CA 95134	(408) 955-4397	(408) 955-5176
Toshiba America Electronic Components, Inc.	2460 N. First Street, Suite 180 San Jose, CA 95131	(408) 965-4200	(408) 432-8566
TagRAM			
Cypress Semiconductor		(206) 821-9202 x325	(206) 820-8959
IDT		(408) 492-8366	(408) 492-8362
Mitsubishi	1050 East Arques Avenue Sunnyvale, CA 94086	(408) 730-5900	(408) 732-9382
Toshiba America Electronic Components, Inc.	2460 N. First Street, Suite 180 San Jose, CA 95131	(408) 965-4200	(408) 432-8566

6.3 Thermal Interface, Heatsink, and Socket Suppliers

Table 17. Thermal Interface, Heatsink, an Socket Suppliers

Supplier	Address	Phone	Fax
Thermal Interface Material			
Chomerics, Div. of Parker Hannifin	77 Dragon Court Woburn, MA 01888	(617) 939-4163	(617) 938-6131
Heatsink/Fansink			
Aavid	One Kool Path P.O.Box 400 Laconia, NH 03247	(603) 528-3400	(603) 528-1478
Des Tech	No. 463, Kang Ning Street Hsi Chih Chen Taipei 22121, Taiwan	886-6-695-0462	886-2-695-0462
Evox Rifa	300 Tri-State International Suite 375 Lincolnshire, IL 60069	(847) 948-9511	(847) 948-9320
Global Win Technology	IF, No. 366, Tanan Road Shih Lin, Taipei, Taiwan	886-2-891-7388	886-2-881-7219
IERC	135 W. Magnolia Blvd. Burbank, CA 91502	(818) 842-7277	(818) 848-8872
Johnson Matthey	15128 East Euclid Ave. Spokane, WA 99216	(509) 922-8702	N/A
Megaland, Inc.	4962 El Camino Real Suite #109 Los Altos, CA 94022	(415) 967-2800	(415) 967-2878
Sanyo-Denki (Keymarc)	1-15 Kita Ohtsuka Toshima Tokyo 170, Japan	(310) 212-7724	813-3-917-4521
Thermalloy	2021 W. Valley View Lane Dallas, TX 75234	(214) 243-4321	(214) 241-4656
Chip Coolers, Inc.	333 Strawberry Field Road Warwick, RI 02886	(800) 227-0254	(401) 732-6119
EG&G Wakefield Engineering	60 Audubon Road Wakefield, MA 01880	(617) 245-5900	(617) 246-0874
Sockets			
AMP	19200 Stevens Creek Blvd. Cupertino, CA 95014	(408) 725-4984	(408) 725-4997
Andon	4 Court Drive Lincoln, RI 02865	(410) 333-0388	(410) 333-0287
Bergquist	5300 Edina Industrial Blvd. Edina, MN 55435	(612) 835-9096 x172	(612) 835-4156
Burndy	51 Richards Ave. P.O.Box 5200 Norwalk, CT 06856	(203) 852-8553	(203) 852-8556
Loranger	3000 Scott Blvd. Santa Clara, CA 95050	(408) 727-4234	(408) 727-5842
Mill Max	190 Pine Hollow Rd. Oyster Bay, NY 11771	(516) 922-6000 x209	(516) 922-0023

7.0 Related Resources

Table 18. Related Resources

Document Title	Order Number
Embedded Pentium® Processor Family Developer's Manual	273204
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Pentium® Processor with MMX™ Technology datasheet	243185
Pentium® Processor Specification Update	242480
Pentium® Processor with MMX™ Technology performance brief	243286
Intel 430TX PCIset: 82439TX System Controller (MTXC) datasheet	290559
AP-485: Intel Processor Identification with the CPUID Instruction	241618
AP-577: An Introduction to PPGA Packaging	243103
AP-579: Pentium® Processor Flexible Motherboard Design Guidelines	243187
AP-580: Voltage Guidelines for Pentium® Processors with MMX™ Technology	243186