Low-Power Embedded Pentium® Processor with MMX™ Technology

Datasheet

Product Features

- Support for MMX™ Technology
- Low-Power 0.25 Micron Process Technology
  - —1.9 V (166/266 MHz) Core Supply for PPGA
  - —1.8 V (166 MHz) or 2.0 V (266 MHz) Core Supply for HL-PBGA
  - —2.5 V I/O Interface (166/266 MHz)
- 32-Bit CPU with 64-Bit Data Bus
- Fractional Bus Operation
  - —166-MHz Core/66-MHz Bus
  - —266-MHz Core/66-MHz Bus
- Superscalar Architecture
  - —Enhanced Pipelines
  - —Two Pipelined Integer Units Capable of Two Instructions/Clock
  - —Pipelined MMX Technology
  - —Pipelined Floating-Point Unit
- Separate Code and Data Caches
  - —16-Kbyte Code, 16-Kbyte Write-Back Data
  - —MESI Cache Protocol
- Compatible with Large Software Base
  - —MS-DOS*, Windows*, OS/2*, UNIX*
- 4-Mbyte Pages for Increased TLB Hit Rate
- IEEE 1149.1 Boundary Scan
- Advanced Design Features
  - —Deeper Write Buffers
  - —Enhanced Branch Prediction Feature
  - —Virtual Mode Extensions
- Internal Error Detection Features
- On-Chip Local APIC Controller
- Power Management Features
  - —System Management Mode
  - —Clock Control
- 296-pin PPGA or 352-ball HL-PBGA

The Low-Power Embedded Pentium Processor with MMX Technology in the HL-PBGA package is also available in extended temperature ranges from -40°C to +115°C. For more information, see the *Extended Temperature Pentium® Processor with MMX™ Technology* datasheet, order number 273232.

Order Number: 273184-003
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Datasheet

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1.0 Introduction

The Low-Power Embedded Pentium® Processor with MMX™ Technology extends the Pentium processor family, providing additional performance and low power for embedded applications. The low-power embedded Pentium processor with MMX technology is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2*, and UNIX* and is one of the major microprocessors to support Intel MMX technology. Furthermore, the low-power embedded Pentium processor with MMX technology has superscalar architecture which can execute two instructions per clock cycle, and enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent.

The low-power embedded Pentium processor with MMX technology has 4.5 million transistors, is built on Intel's 0.25 micron manufacturing process technology and has full SL Enhanced power management features including System Management Mode (SMM) and clock control. The low-power embedded Pentium processor with MMX technology is available in a 296-pin Plastic Pin Grid Array (PPGA) or 352-ball High-Thermal Low-Profile–Plastic Ball Grid Array (HL-PBGA). The HL-PBGA package allows designers to use surface mount technology to create small form-factor designs. The additional SL Enhanced features, low-power dissipation and PPGA or HL-PBGA package make the low-power embedded Pentium processor with MMX technology ideal for embedded designs.

The Low-Power Embedded Pentium Processor with MMX Technology in the HL-PBGA package is available in extended temperature ranges from -40°C to +115°C. For details, see the *Extended Temperature Pentium® Processor with MMX™ Technology* datasheet, order number 273232.

1.1 Processor Features

The low-power embedded Pentium processors with MMX technology for high performance embedded applications (166 and 266 MHz) are fully compatible with the existing Pentium processors with MMX technology (200 and 233 MHz) with the following differences: voltage supplies, power consumption, and performance. Additionally, Pentium processors with MMX technology are socket compatible with the Pentium processor (100, 133, and 166 MHz), making it possible to design a flexible motherboard that supports both the Pentium processor and the embedded Pentium processors with MMX technology (166–266 MHz).

The low-power embedded Pentium processor with MMX technology has all the advanced architectural and internal features of the desktop version of the Pentium processor with MMX technology, except that several features have been eliminated. The differences are specified in "Differences from Desktop Processors" on page 14.

The low-power embedded Pentium processor with MMX technology has several features which allow for high-performance embedded designs. These features include the following:

- 1.9 V core (PPGA – 166/266 MHz)
- 1.8 V core (HL-PBGA – 166), 2.0 V core (HL-PBGA – 266)
- 2.5 V I/O buffer V_{CC3} inputs to reduce power consumption
- SL Enhanced feature set

This document should be used in conjunction with *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

2.0 Architecture Overview

The low-power embedded Pentium processor with MMX technology extends the family of Pentium processors with MMX technology. It is binary compatible with the 8086/88, 80286, Intel386™ DX, Intel386 SX,Intel486™ SX, IntelDX2™, IntelDX4™, and Pentium processors with voltage reduction technology (75–150 MHz).

The embedded Pentium processor family consists of the embedded Pentium processor (100, 133, and 166 MHz), the embedded Pentium processor with voltage reduction technology (133 MHz), the embedded Pentium processor with MMX technology (200, 233 MHz), and the low-power embedded Pentium processor with MMX technology (166, 266 MHz).

The low-power embedded Pentium processor with MMX technology contains all of the features of previous Intel architecture processors and provides significant enhancements and additions, including the following:

- Support for MMX™ Technology
- Superscalar Architecture
- Enhanced Branch Prediction Algorithm
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate 16-Kbyte Code Cache and 16-Kbyte Data Cache
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Enhanced Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- 0.25 Micron Process Technology
- SL Power Management Features
- Pool of Four Write Buffers Used by Both Pipes

2.1 Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 CPU family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 and Intel486 families of processors.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and the floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one that prefetches code in a linear fashion, and one that prefetches code according to the Branch Target Buffer (BTB) so that code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 processor. Faster algorithms provide up to 10x speed-up for common operations including add, multiply, and load.

Pentium processors include separate code and data caches integrated on-chip to meet performance goals. Each cache has a 32-byte line size and is 4-way set associative. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be writeback or writethrough on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are also triple ported to support snooping and split line accesses. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst writeback cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' MMU contains optional extensions to the architecture that allow 4-Kbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on-chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified four breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

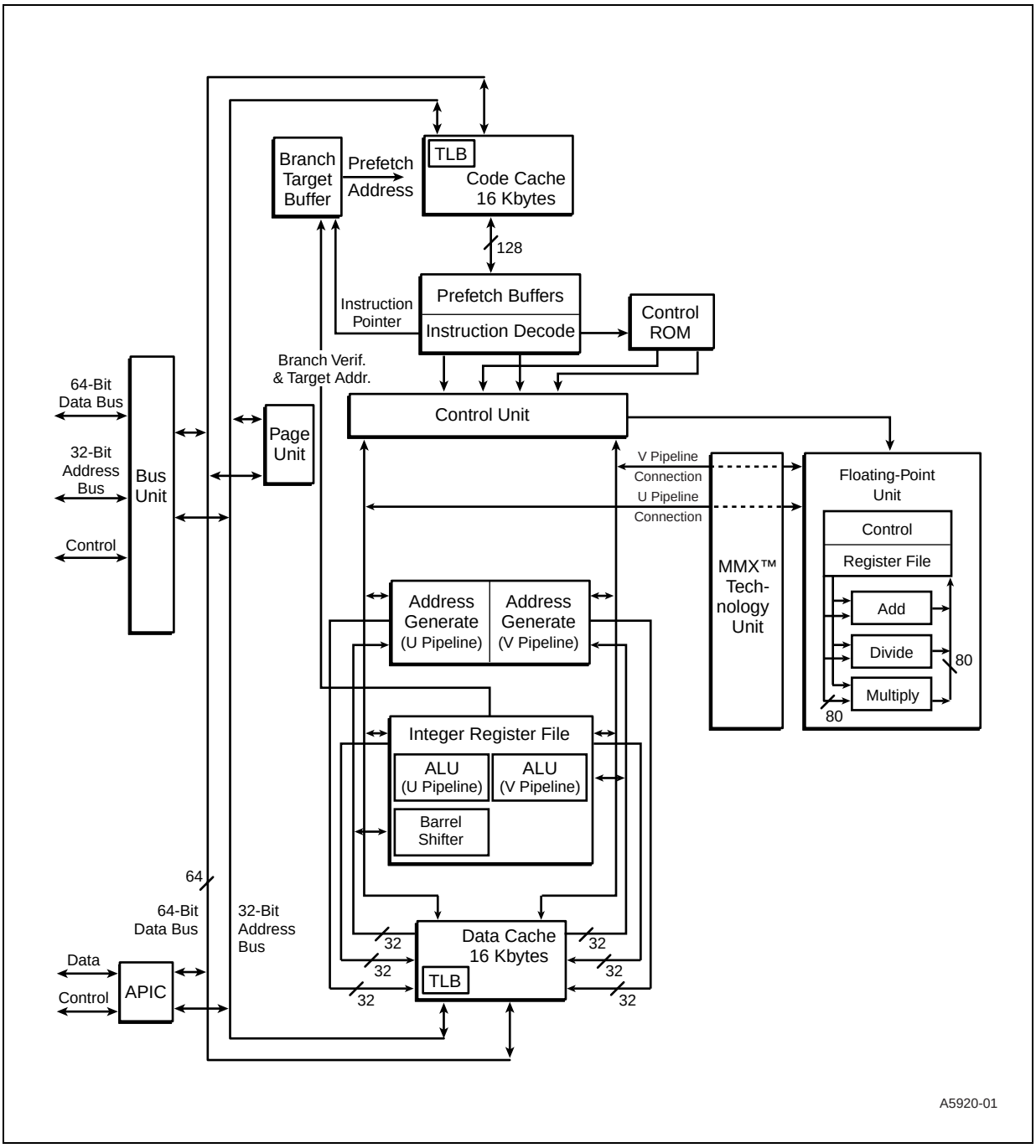
System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 shows a block diagram of the Pentium processor with MMX technology.

The block diagram shows the two instruction pipelines, the “u” pipe and “v” pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

Figure 1. Pentium® Processor with MMX™ Technology Block Diagram



The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processor contains a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

In addition to the SMM features described above, the Pentium processor supports clock control. When the clock to the processor is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor a good choice for low-power embedded designs.

The Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The low-power embedded Pentium processor with MMX technology contains an on-chip advanced programmable interrupt controller (APIC). This function is reserved for future multi-processing function.

The architectural features introduced in this section are more fully described in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

2.2 Pentium® Processor with MMX™ Technology

The Pentium processor with MMX technology for high-performance embedded designs is a significant addition to the Pentium processor family. Available at 166, 200, 233, and 266 MHz, it is the first microprocessor to support Intel MMX technology.

The Pentium processor with MMX technology is both software and pin compatible with previous members of the Pentium processor family. It contains 4.5 million transistors and is manufactured on lntel's enhanced 0.35 micron (200/233 MHz) or 0.25 micron (166/266 MHz) CMOS process, which allows voltage reduction technology for low power and high density.

In addition to the architecture described in the previous section for the Pentium processor family, the Pentium processor with MMX technology has several additional micro-architectural enhancements, which are described in the next section.

2.2.1 Full Support for Intel MMX™ Technology

MMX technology is based on the SIMD technique (Single Instruction, Multiple Data) which enables increased performance on a wide variety of multimedia and communications applications. Fifty-seven new instructions and four new 64-bit data types are supported in the Pentium processor with MMX technology. All existing operating system and application software are fully-compatible.

2.2.2 16-Kbyte Code and Data Caches

On-chip level-1 data and code cache sizes are 16 Kbytes each and are 4-way set associative on the Pentium processor with MMX technology. Large separate internal caches improve performance by reducing average memory access time and providing fast access to recently-used instructions and data. The instruction and data caches can be accessed simultaneously while the data cache supports two data references simultaneously. The data cache supports a write-back (or alternatively, write-through, on a line-by-line basis) policy for memory updates.

2.2.3 Improved Branch Prediction

Dynamic branch prediction uses the Branch Target Buffer (BTB) to boost performance by predicting the most likely set of instructions to be executed. The BTB has been improved on the Pentium processor with MMX technology to increase its accuracy. This processor has four prefetch buffers that can hold up to four successive code streams.

2.2.4 Enhanced Pipeline

An additional pipeline stage has been added and the pipeline has been enhanced to improve performance. The integration of the MMX technology pipeline with the integer pipeline is very similar to that of the floating-point pipeline. Under some circumstances, two MMX instructions or one integer and one MMX instruction can be paired and issued in one clock cycle to increase throughput. The enhanced pipeline is described in more detail in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

2.2.5 Deeper Write Buffers

A pool of four write buffers is now shared between the dual pipelines to improve memory write performance.

2.3 0.25 Micron Technology

The 0.25 micron technology is the state-of-the-art CMOS manufacturing process Intel unveiled on April 12, 1997, enabling the use of lower core supply to sub-2 V. As a result, the low-power embedded Pentium processor with MMX technology consumes significantly less power at even higher speeds.

3.0 Packaging Information

3.1 Differences from Desktop Processors

The following features have been eliminated in the low-power embedded Pentium processor with MMX technology: Upgrade, Dual Processing (DP), and Master/Checker functional redundancy.

Table 1 lists the corresponding pins that exist on the Pentium processor with MMX technology but have been removed on the low-power embedded Pentium processor with MMX technology.

Table 1. Signals Removed from the Low-Power Embedded Pentium® Processor with MMX™ Technology

Signal	Function
ADSC#	Additional Address Status. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	Additional Burst Ready. This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	CPU Type. This signal is used for dual processing systems.
D/P#	Dual/Primary processor identification. This signal is only used for an upgrade processor.
FRCMC#	Functional Redundancy Checking. This signal is only used for error detection via processor redundancy and requires two Pentium processors (master/checker).
PBGNT#	Private Bus Grant. This signal is only used for dual processing systems.
PBREQ#	Private Bus Request. This signal is used only for dual processing systems.
PHIT#	Private Hit. This signal is only used for dual processing systems.
PHITM#	Private Modified Hit. This signal is only used for dual processing systems.

3.2 PPGA Pinout and Pin Descriptions

The text orientation on the top side view drawings in this section represents the orientation of the ink mark on the actual packages. (Note that the text shown in this section is not the actual text that will be marked on the packages).

Figure 2. PPGA Package Top Side View

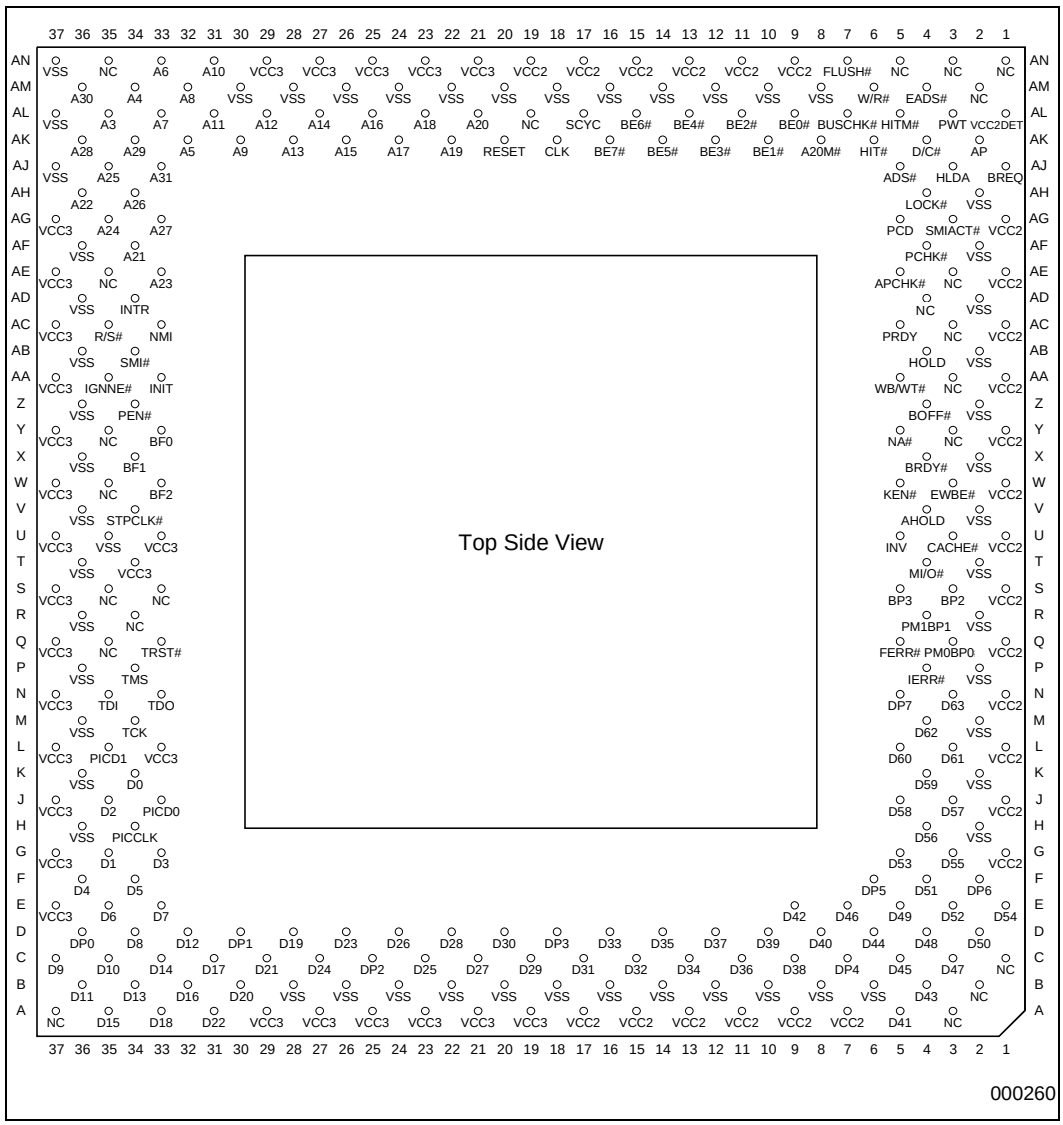


Figure 3. PPGA Package Pin Side View

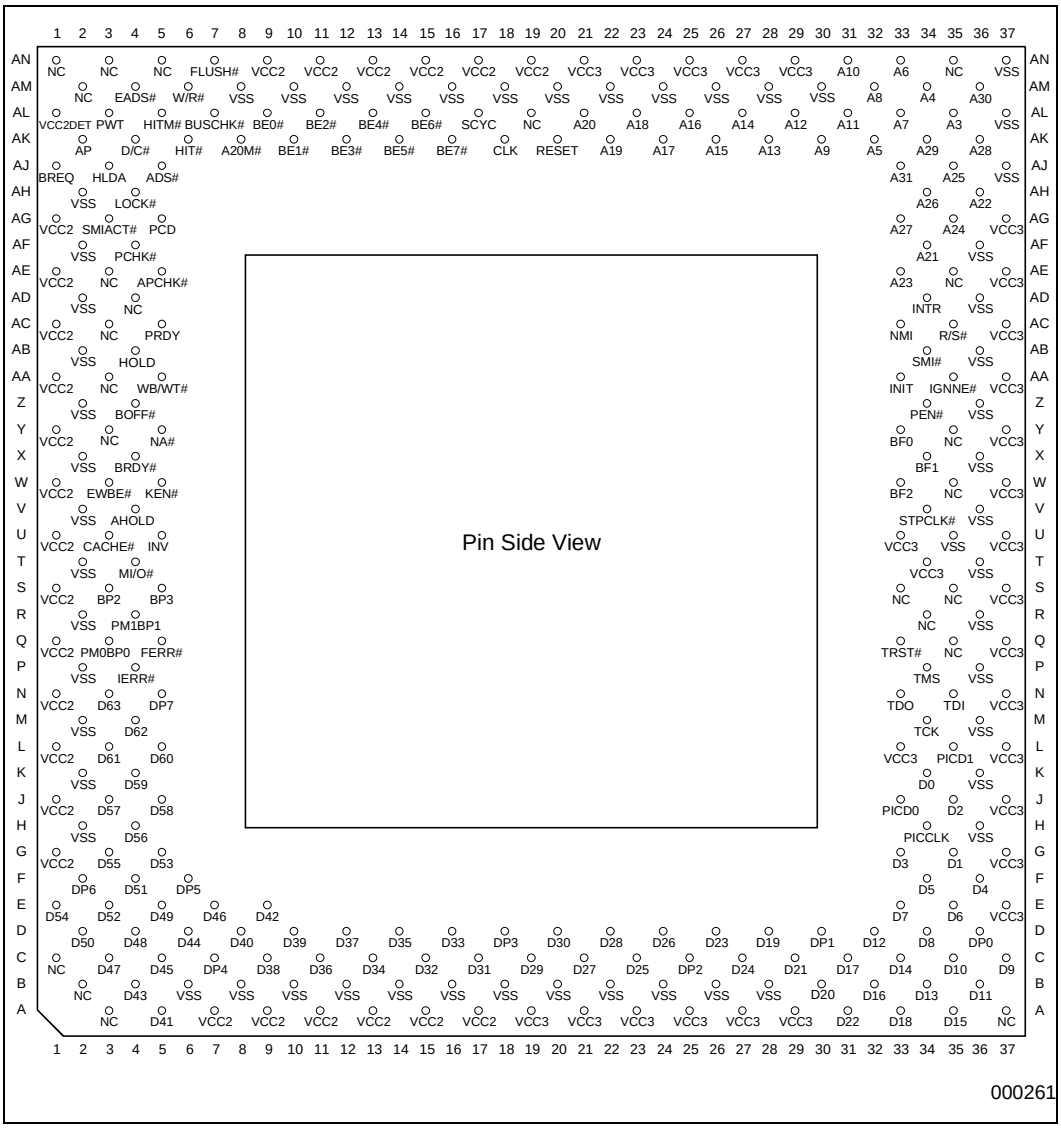


Table 2. Pin Cross Reference by Pin Name (PPGA Package) (Sheet 1 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address							
A3	AL35	A11	AL31	A19	AK22	A27	AG33
A4	AM34	A12	AL29	A20	AL21	A28	AK36
A5	AK32	A13	AK28	A21	AF34	A29	AK34
A6	AN33	A14	AL27	A22	AH36	A30	AM36
A7	AL33	A15	AK26	A23	AE33	A31	AJ33
A8	AM32	A16	AL25	A24	AG35		
A9	AK30	A17	AK24	A25	AJ35		
A10	AN31	A18	AL23	A26	AH34		
Data							
D0	K34	D16	B32	D32	C15	D48	D04
D1	G35	D17	C31	D33	D16	D49	E05
D2	J35	D18	A33	D34	C13	D50	D02
D3	G33	D19	D28	D35	D14	D51	F04
D4	F36	D20	B30	D36	C11	D52	E03
D5	F34	D21	C29	D37	D12	D53	G05
D6	E35	D22	A31	D38	C09	D54	E01
D7	E33	D23	D26	D39	D10	D55	G03
D8	D34	D24	C27	D40	D08	D56	H04
D9	C37	D25	C23	D41	A05	D57	J03
D10	C35	D26	D24	D42	E09	D58	J05
D11	B36	D27	C21	D43	B04	D59	K04
D12	D32	D28	D22	D44	D06	D60	L05
D13	B34	D29	C19	D45	C05	D61	L03
D14	C33	D30	D20	D46	E07	D62	M04
D15	A35	D31	C17	D47	C03	D63	N03
Control							
A20M#	AK08	BREQ	AJ01	HITM#	AL05	PM1/BP1	R04
ADS#	AJ05	BUSCHK#	AL07	HLDA	AJ03	PRDY	AC05
AHOLD	V04	CACHE#	U03	HOLD	AB04	PWT	AL03
AP	AK02	D/C#	AK04	IERR#	P04	R/S#	AC35
APCHK#	AE05	DP0	D36	IGNNE#	AA35	RESET	AK20
BE0#	AL09	DP1	D30	INIT	AA33	SCYC	AL17
BE1#	AK10	DP2	C25	INTR/ LINT0	AD34	SMI#	AB34
BE2#	AL11	DP3	D18	INV	U05	SMIACT#	AG03
BE3#	AK12	DP4	C07	KEN#	W05	TCK	M34
BE4#	AL13	DP5	F06	LOCK#	AH04	TDI	N35
BE5#	AK14	DP6	F02	M/IO#	T04	TDO	N33
BE6#	AL15	DP7	N05	NA#	Y05	TMS	P34
BE7#	AK16	EADS#	AM04	NMI/LINT1	AC33	TRST#	Q33
BOFF#	Z04	EWBE#	W03	PCD	AG05	VCC2DET#	AL01
BP2	S03	FERR#	Q05	PCHK#	AF04	W/R#	AM06

Table 2. Pin Cross Reference by Pin Name (PPGA Package) (Sheet 2 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
BP3	S05	FLUSH#	AN07	PEN#	Z34	WB/WT#	AA05
BRDY#	X04	HIT#	AK06	PM0/BP0	Q03		
APIC							
PICCLK	H34	PICD0	J33	PICD1 [APICEN]	L35		
Clock Control							
BF0	Y33	BF1	X34	BF2	W33	CLK	AK18
STPCLK#	V34						

Table 3. No Connect, Power Supply and Ground Pin Cross Reference (PPGA Package)

V_{CC2}							
A07	A15	J01	Q01	W01	AC01	AN09	AN15
A09	A17	L01	S01	Y01	AE01	AN11	AN17
A11	G01	N01	U01	AA01	AG01	AN13	AN19
A13							
V_{CC3}							
A19	A27	J37	Q37	U37	AA37	AG37	AN25
A21	A29	L37	S37	W37	AC37	AN29	AN23
A23	E37	L33	T34	Y37	AE37	AN27	AN21
A25	G37	N37	U33				
V_{SS}							
B06	B20	K02	R36	X36	AF02	AM12	AM26
B08	B22	K36	T02	Z02	AF36	AM14	AM28
B10	B24	M02	T36	Z36	AH02	AM16	AM30
B12	B26	M36	U35	AB02	AJ37	AM18	AN37
B14	B28	P02	V02	AB36	AL37	AM20	
B16	H02	P36	V36	AD02	AM08	AM22	
B18	H36	R02	X02	AD36	AM10	AM24	
No Connect (NC)							
A03		S33		AC03		AN01	
A37		S35		AD04		AN03	
B02		W35		AE03		AN05	
C01		Y03		AE35		AN35	
Q35		Y35		AL19			
R34		AA03		AM02			

NOTE: Shaded pins differ functionally from the Pentium® Processor with MMX™ Technology pinout.

3.3 HL-PBGA Pinout and Pin Descriptions

Figure 4. HL-PBGA Package Top Side View

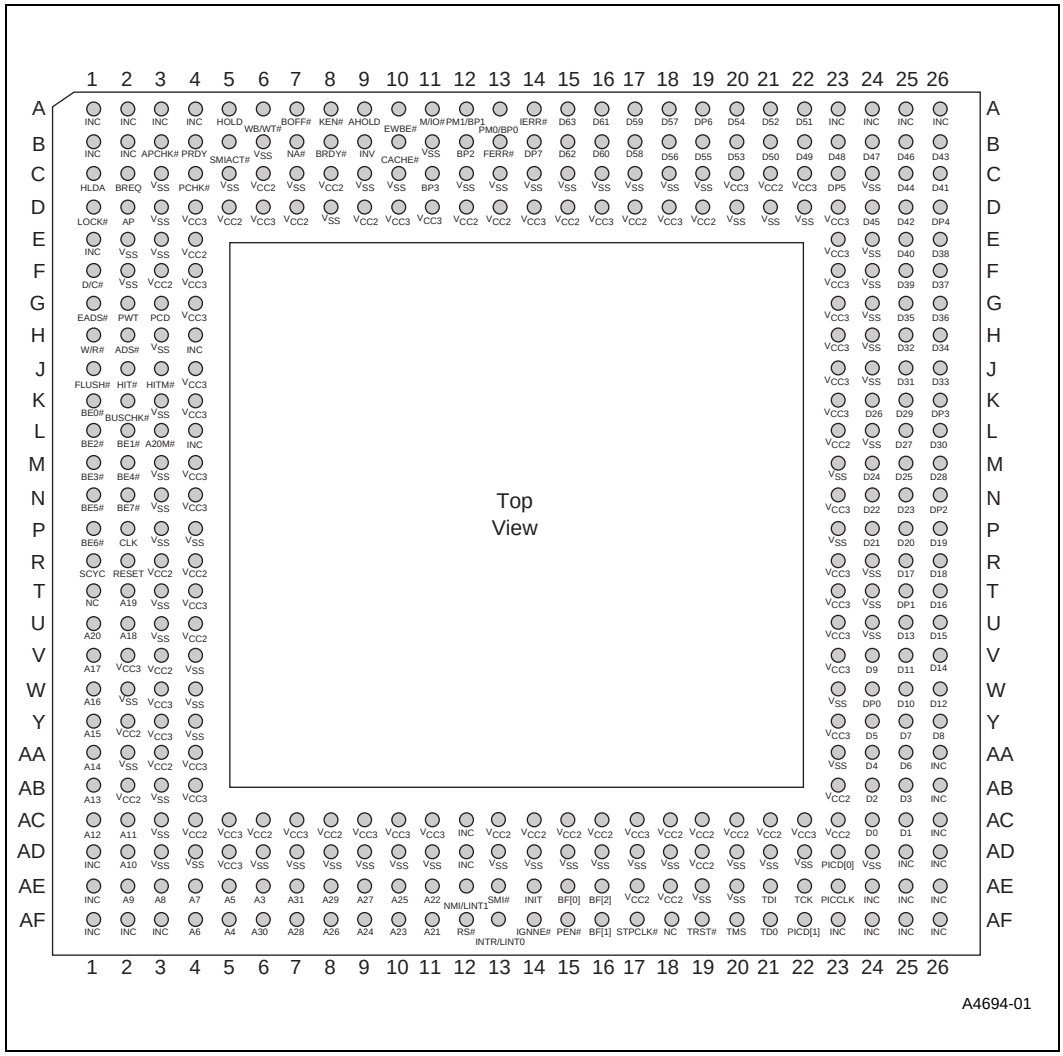


Figure 5. HL-PBGA Package Pin Side View

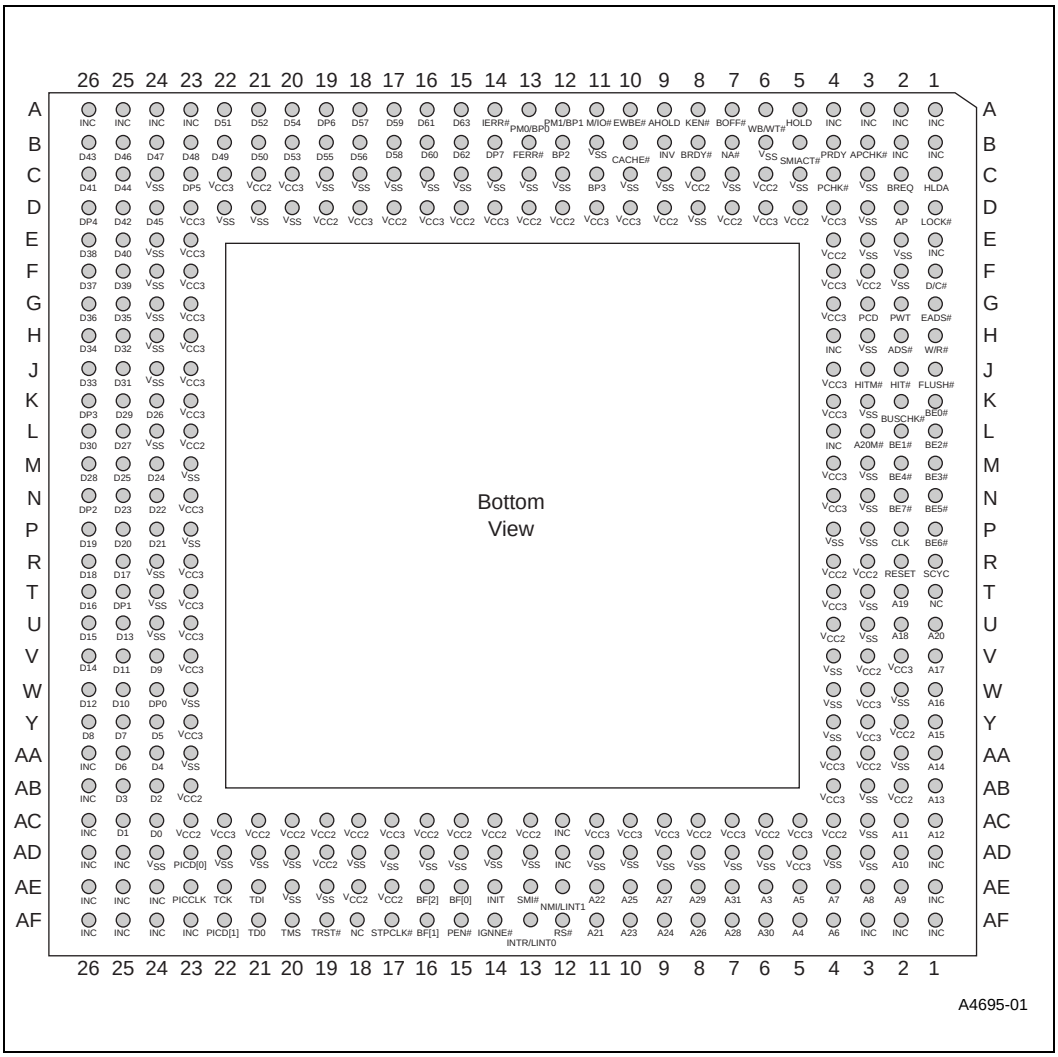


Table 4. Pin Cross Reference by Pin Name (HL-PBGA Package) (Sheet 1 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address							
A3	AE6	A11	AC2	A19	T2	A27	AE9
A4	AF5	A12	AC1	A20	U1	A28	AF7
A5	AE5	A13	AB1	A21	AF11	A29	AE8
A6	AF4	A14	AA1	A22	AE11	A30	AF6
A7	AE4	A15	Y1	A23	AF10	A31	AE7
A8	AE3	A16	W1	A24	AF9		
A9	AE2	A17	V1	A25	AE10		
A10	AD2	A18	U2	A26	AF8		
Data							
D0	AC24	D16	T26	D32	H25	D48	B23
D1	AC25	D17	R25	D33	J26	D49	B22
D2	AB24	D18	R26	D34	H26	D50	B21
D3	AB25	D19	P26	D35	G25	D51	A22
D4	AA24	D20	P25	D36	G26	D52	A21
D5	Y24	D21	P24	D37	F26	D53	B20
D6	AA25	D22	N24	D38	E26	D54	A20
D7	Y25	D23	N25	D39	F25	D55	B19
D8	Y26	D24	M24	D40	E25	D56	B18
D9	V24	D25	M25	D41	C26	D57	A18
D10	W25	D26	K24	D42	D25	D58	B17
D11	V25	D27	L25	D43	B26	D59	A17
D12	W26	D28	M26	D44	C25	D60	B16
D13	U25	D29	K25	D45	D24	D61	A16
D14	V26	D30	L26	D46	B25	D62	B15
D15	U26	D31	J25	D47	B24	D63	A15
Control							
A20M#	L3	BREQ	C2	HITM#	J3	PM1/BP1	A12
ADS#	H2	BUSCHK#	K2	HLDA	C1	PRDY	B4
AHOLD	A9	CACHE#	B10	HOLD	A5	PWT	G2
AP	D2	D/C#	F1	IERR#	A14	R/S#	AF12
APCHK#	B3	DP0	W24	IGNNE#	AF14	RESET	R2
BE0#	K1	DP1	T25	INIT	AE14	SCYC	R1
BE1#	L2	DP2	N26	INTR/ LINT0	AF13	SMI#	AE13
BE2#	L1	DP3	K26	INV	B9	SMIACT#	B5
BE3#	M1	DP4	D26	KEN#	A8	TCK	AE22
BE4#	M2	DP5	C23	LOCK#	D1	TDI	AE21
BE5#	N1	DP6	A19	M/IO#	A11	TDO	AF21
BE6#	P1	DP7	B14	NA#	B7	TMS	AF20
BE7#	N2	EADS#	G1	NMI/LINT1	AE12	TRST#	AF19
BOFF#	A7	EWBE#	A10	PCD	G3	W/R#	H1
BP2	B12	FERR#	B13	PCHK#	C4	WB/WT#	A6

Table 4. Pin Cross Reference by Pin Name (HL-PBGA Package) (Sheet 2 of 2)

Pin	Location	Pin	Location	Pin	Location	Pin	Location
BP3	C11	FLUSH#	J1	PEN#	AF15		
BRDY#	B8	HIT#	J2	PM0/BP0	A13		
APIC							
PICCLK	AE23	PICD0	AD23	PICD1 [APICEN]	AF22		
Clock Control							
BF0	AE15	BF1	AF16	BF2	AE16	CLK	P2
STPCLK#	AF17						

Table 5. No Connect, Power Supply and Ground Pin Cross Reference (HL-PBGA Package)

V_{CC2}							
C6	D9	D19	R4	AB2	AC13	AC19	AE17
C8	D12	E4	U4	AB23	AC14	AC20	AE18
C21	D13	F3	V3	AC4	AC15	AC21	
D5	D15	L23	Y2	AC6	AC16	AC23	
D7	D17	R3	AA3	AC8	AC18	AD19	
V_{CC3}							
C20	D14	F23	J23	N23	V2	AA4	AC10
C22	D16	G4	K4	R23	V23	AB4	AC11
D4	D18	G23	K23	T4	W3	AC5	AC17
D6	D23	H23	M4	T23	Y3	AC7	AC22
D10	E23	J4	N4	U23	Y23	AC9	AD5
D11	F4						
V_{SS}							
B6	C14	D20	H3	P4	W4	AD6	AD16
B11	C15	D21	H24	P23	W23	AD7	AD17
C3	C16	D22	J24	R24	Y4	AD8	AD18
C5	C17	E2	K3	T3	AA2	AD9	AD20
C7	C18	E3	L24	T24	AA23	AD10	AD21
C9	C19	E24	M3	U3	AB3	AD11	AD22
C10	C24	F2	M23	U24	AC3	AD13	AD24
C12	D3	F24	N3	V4	AD3	AD14	AE19
C13	D8	G24	P3	W2	AD4	AD15	AE20
No Connect (NC)							
AF18	T1						
Internal No Connect (INC)							
A1	A23	B1	L4	AC26	AD26	AE26	AF23
A2	A24	B2	AA26	AD1	AE1	AF1	AF24
A3	A25	E1	AB26	AD12	AE24	AF2	AF25
A4	A26	H4	AC12	AD25	AE25	AF3	AF26

3.4 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

3.5 Pin Quick Reference

This section gives a brief functional description of each pin. For a detailed description, see the Hardware Interface chapter in the *Embedded Pentium® Processor Family Developer's Manual.*

Note: All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The pins are classified as Input or Output based on their function in Master Mode. See the Error Detection chapter of the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for further information.

Table 6. Quick Pin Reference (Sheet 1 of 6)

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor with MMX™ technology emulates the address wraparound at 1 Mbyte, which occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31–A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31–A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#–BE5# BE4#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3).

Table 6. Quick Pin Reference (Sheet 2 of 6)

Symbol	Type	Name and Function
BF2–BF0	I	The **Bus Frequency** pins determine the bus-to-core frequency ratio. BF [2:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[2:0] must not change values while RESET is active. See Table 7 for Bus Frequency Selection. In order to override the internal defaults and guarantee that the BF[2:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pullup/pulldown resistor to V_{CC3} or ground. Driving these pins with active logic is not recommended unless stability during RESET can be guaranteed. During power up, RESET should be asserted prior to or ramped simultaneously with the core voltage supply to the processor.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.
BP3–BP2 PM/BP1–BP0	O	The **breakpoint** pins (BP3–0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception. To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST# and PICD0–1 are specified with respect to the rising edge of CLK. This pin is 2.5 V-tolerant-only on the low-power embedded Pentium processor with MMX technology. It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.

Table 6. Quick Pin Reference (Sheet 3 of 6)

Symbol	Type	Name and Function
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63–D56; DP0 applies to D7–D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using MS-DOS type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the processor will resume driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock that HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.

Table 6. Quick Pin Reference (Sheet 4 of 6)

Symbol	Type	Name and Function
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3; Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.

Table 6. Quick Pin Reference (Sheet 5 of 6)

Symbol	Type	Name and Function
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to “1”, the processor will vector to the machine check exception before the beginning of the next instruction.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor with MMX technology.
PICD0–PICD1 [APICEN]	I/O	**Programmable interrupt controller data lines 0–1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistor. These signals are multiplexed with APICEN.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1–0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the *Embedded Pentium® Processor Family Developer’s Manual* (Order Number 273204) for more details.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if three-state test mode will be entered or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.

Table 6. Quick Pin Reference (Sheet 6 of 6)

Symbol	Type	Name and Function
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2DET#	N/A	Differentiate between the Pentium Processor with MMX technology and the low-power embedded Pentium processor with MMX technology. This is an Internal No Connect (INC) pin on the low-power embedded Pentium processor with MMX technology. This pin is not defined on the HL-PBGA package.
V_{CC2}	I	These pins are the power inputs to the core: 1.9 V input for 166/266 MHz PPGA; 1.8 V for 166 MHz HL-PBGA; 2.0 V for 266 MHz HL-PBGA.
V_{CC3}	I	These pins are the 2.5 V power inputs to the I/O.
V_{SS}	I	These pins are the ground inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

3.6 Bus Fraction (BF) Selection

Each low-power embedded Pentium processor with MMX technology must be externally configured with the BF2–BF0 pins to operate in the specified bus fraction mode. Operation out of the specification is not supported. For example, a 266 MHz low-power embedded Pentium processor with MMX technology supports only the 1/4 bus fraction mode and not the 2/5 mode.

The BF configuration pins are provided to select the allowable bus/core ratios of 2/5 and 1/4. The low-power embedded Pentium processor with MMX technology multiplies the input CLK to achieve the higher internal core frequencies. The internal clock generator requires a constant frequency CLK input to within ±250 ps; therefore, the CLK input cannot be changed dynamically.

The external bus frequency is set during power-up Reset through the CLK pin. The low-power embedded Pentium processor with MMX technology samples the BF0, BF1 and BF2 pins on the falling edge of RESET to determine which bus/core ratio to use.

Table 7 summarizes the operation of the BF pins on the low-power embedded Pentium processor with MMX technology.

Note: BF pins must meet a 1 ms setup time to the falling edge of RESET and *must not change value while RESET is active*. Once a frequency is selected, it may not be changed with a warm reset. Changing this speed or ratio requires a "power on" RESET pulse initialization.

Table 7. Bus Frequency Selection

BF2	BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)
0	0	0	2/5	66/166
1	0	0	1/4	66/266

NOTE: All other BF2–BF0 settings are reserved on the low-power embedded Pentium processor with MMX technology.

3.7 The CPUID Instruction

The CPUID instruction allows software to determine the type and features of the processor on which it is executing. When executing CPUID, the low-power embedded Pentium processor with MMX technology behaves like the Pentium processor and the Pentium processor with MMX technology as follows:

- If the value in EAX is '0', then the 12-byte ASCII string "Genuine Intel" (little endian) is returned in EBX, EDX and ECX. Also, a '1' is returned to EAX.
- If the value in EAX is '1', then the processor version is returned in EAX and the processor capabilities are returned in EDX. The values of EAX and EDX for the low-power embedded Pentium processor with MMX technology are given below.
- If the value in EAX is neither '0' nor '1', the low-power embedded Pentium processor with MMX technology writes '0' to all registers.

The following EAX and EDX values are defined for the CPUID instruction executed with EAX = '1'. The processor version EAX bit assignments are given in Figure 6. The EDX bit assignments are shown in Figure 7.

Figure 6. EAX Bit Assignments for CPUID

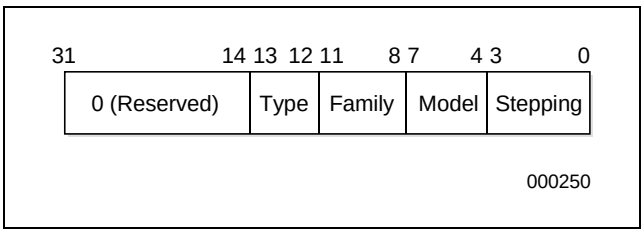
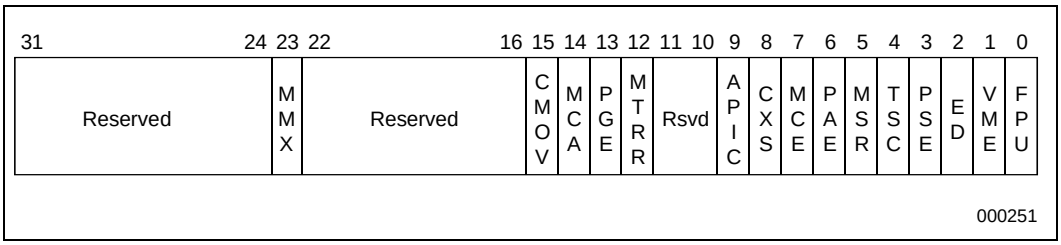


Figure 7. EDX Bit Assignments for CPUID



The type field for low-power embedded Pentium processor with MMX technology is the same as Pentium processor with MMX technology (type = 00H). The family field is the same as all other Pentium processors (family = 5H). However, the model field is different: the Pentium processor model number is 2H, the Pentium processor with MMX technology model number is 4H, and the low-power embedded Pentium processor with MMX technology model number is 8H. The stepping field indicates the revision number of a model. The stepping ID of A-step for the low-power embedded Pentium processor with MMX technology is 1H. Stepping ID will be documented in the low-power embedded Pentium processor with MMX technology stepping information.

After masking the reserve bits, all low-power embedded Pentium processor with MMX technology-based products will get a value of 0x008003BF (assuming the APIC is enabled at boot), or 0x008001BF (when the APIC is disabled, using the APICEN boot pin) in EDX upon completion of the CPUID instruction.

Table 8. EDX Bit Assignment Definitions for CPUID

Bit	Value	Comments
0	1	FPU: Floating-point Unit on-chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR Pentium® Processor MSR
6	0	PAE: Physical Address Extension
7	1	MCE: Machine Check Exception
8	1	CX8: CMPXCHG8B Instruction
9	1	APIC: APIC on-chip†
10–11	R	Reserved – Do not write to these bits or rely on their values
12	0	MTRR: Memory Type Range Registers
13	0	PGE: Page Global Enable
14	0	MCA: Machine Check Architecture
15–22	R	Reserved – Do not write to these bits or rely on their values
23	1	Intel Architecture with MMX™ technology supported
24–31	R	Reserved – Do not write to these bits or rely on their values

† Indicates that APIC is present and hardware enabled (software disabling does not affect this bit).

3.8 Boundary Scan Chain List

The boundary scan chain list for the low-power embedded Pentium processor with MMX technology is different than the Pentium processor with MMX technology due to the removal of some pins. The boundary scan register for the low-power embedded Pentium processor with MMX technology contains a cell for each pin. Following is the bit order of the low-power embedded Pentium processor with MMX technology boundary scan register (left to right, top to bottom):

TDI → disapsba†, PICD1, PICD0, Reserved, PICCLK, D0, D1, D2, D3, D4, D5, D6, D7, DP0, D8, D9, D10, D11, D12, D13, D14, D15, DP1, D16, D17, D18, D19, D20, D21, D22, D23, DP2, D24, D25, D26, D27, D28, D29, D30, D31, DP3, D32, D33, D34, D35, D36, D37, D38, D39, DP4, D40, D41, D42, D43, D44, D45, D46, diswr†, D47, DP5, D48, D49, D50, D51, D52, D53, D54, D55, DP6, D56, D57, D58, D59, D60, D61, D62, D63, DP7, IERR#, FERR#, PM0BP0, PM1BP1, BP2, BP3, MIO#, CACHE#, EWBE#, INV, AHOLD, KEN#, BRDYC#, BRDY#, BOFF#, NA#, WBWT#, HOLD, disbus†, disbusl†, dismisc†, dismisca†, SMIACT#, PRDY, PCHK#, APCHK#, BREQ, HLDA, AP, LOCK#, PCD, PWT, DC#, EADS#, ADS#, HITM#, HIT#, WR#, BUSCHK#, FLUSH#, A20M#, BE0#, BE1#, BE2#, BE3#, BE4#, BE5#, BE6#, BE7#, SCYC, CLK, RESET, disabus†, A20, A19, A18, A17, A16, A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A31, A30, A29, A28, A27, A26, A25, A24, A23, A22, A21, NMI, RS#, INTR, SMI#, IGNNE#, INIT, PEN#, Reserved, BF0, BF1, BF2, STPCLK#, Reserved, Reserved, Reserved, Reserved → TDO

“Reserved” includes the no connect “NC” signals on the low-power embedded Pentium processor with MMX technology.

The cells marked with a dagger (†) are control cells that are used to select the direction of bi-directional pins or three-state the output pins. If “1” is loaded into the control cell, the associated pin(s) are three-stated or selected as input. The following lists the control cells and their corresponding pins:

Disabus:	A31–A3, AP
Disbus:	BE7#–BE0#, CACHE#, SCYC, M/IO#, D/C#, W/R#, PWT, PCD
Disbusl:	ADS#, LOCK#, ADSC#
Dismisc:	APCHK#, PCHK#, PRDY, BP3, BP2, PM1/BP1, PM0/BP0, FERR#, SMIACT#, BREQ, HLDA, HIT#, HITM#
Dismisca:	IERR#
Diswr:	D63–D0, DP7–DP0
Disapsba:	PICD1–PICD0

3.9 Pin Reference Tables

Table 9. Output Pins

Name[1]	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#[2]	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	N/A	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	N/A	All states except Shift-DR and Shift-IR
VCC2DET#[3]	N/A	Differentiates between the Pentium® processor with MMX™ technology and the low-power embedded Pentium processor with MMX technology

NOTE:
1. All output and input/output pins are floated during three-state test mode (except TDO).
2. HITM# pin has an internal pull-up resistor.
3. This pin is not on the HL-PBGA pinout.

Table 10. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#	LOW	Asynchronous		
AHOLD	HIGH	Synchronous		
BF0	N/A	Synchronous/RESET	Pulldown	
BF1	N/A	Synchronous/RESET	Pullup	
BF2	N/A	Synchronous/RESET	Pulldown	
BOFF#	LOW	Synchronous		
BRDY#	LOW	Synchronous	Pullup	Bus State T2,T12,T2P
BUSCHK#	LOW	Synchronous	Pullup	BRDY#
CLK	N/A			
EADS#	LOW	Synchronous		
EWBE#	LOW	Synchronous		BRDY#
FLUSH#	LOW	Asynchronous		
HOLD	HIGH	Synchronous		
IGNNE#	LOW	Asynchronous		
INIT	HIGH	Asynchronous		
INTR	HIGH	Asynchronous		
INV	HIGH	Synchronous		EADS#
KEN#	LOW	Synchronous		First BRDY#/NA#
NA#	LOW	Synchronous		Bus State T2,TD,T2P
NMI	HIGH	Asynchronous		
PEN#	LOW	Synchronous		BRDY#
PICCLK	HIGH	Asynchronous	Pullup	
R/S#	N/A	Asynchronous	Pullup	
RESET	HIGH	Asynchronous		
SMI#	LOW	Asynchronous	Pullup	
STPCLK#	LOW	Asynchronous	Pullup	
TCK	N/A		Pullup	
TDI	N/A	Synchronous/TCK	Pullup	TCK
TMS	N/A	Synchronous/TCK	Pullup	TCK
TRST#	LOW	Asynchronous	Pullup	
WB/WT#	N/A	Synchronous		First BRDY#/NA#

Table 11. Input/Output Pins

Name	Active Level	When Floated(1)	Qualified (when an input)	Internal Resistor
A31–A3	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
AP	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
BE3#–BE0#	LOW	Bus Hold, BOFF#	RESET	Pulldown(2)
D63–D0	N/A	Bus Hold, BOFF#	BRDY#	
DP7–DP0	N/A	Bus Hold, BOFF#	BRDY#	
PICD0	N/A			Pullup
PICD1[APICEN]	N/A			Pulldown

NOTE:
1. All output and input/output pins are floated during three-state test mode (except TDO).
2. BE3#–BE0# have pulldowns during RESET only.

3.10 Pin Grouping According to Function

Table 12. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF[2:0]
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0–PICD1
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Clock Control	STPCLK#
Debugging	R/S#, PRDY

3.11 Mechanical Specifications

In mechanical terms, the low-power embedded Pentium processor with MMX technology 296-lead Plastic Staggered Pin Grid Array (PPGA) is completely identical to the Pentium processor with MMX technology PPGA package. The pins are arranged in a 37x37 matrix and the package dimensions are 1.95" x 1.95" (4.95 cm x 4.95 cm). Package summary information for the PPGA device is provided in Table 13. Figure 8 shows the package dimensions.

The HL-PBGA version of the low-power embedded Pentium processor with MMX technology is a new package type for the Pentium processor family. Package summary information for the HL-PBGA device is provided in Table 14. Figure 9 shows the package dimensions.

3.11.1 PPGA Package Mechanical Diagrams

Figure 8. PPGA Package Dimensions

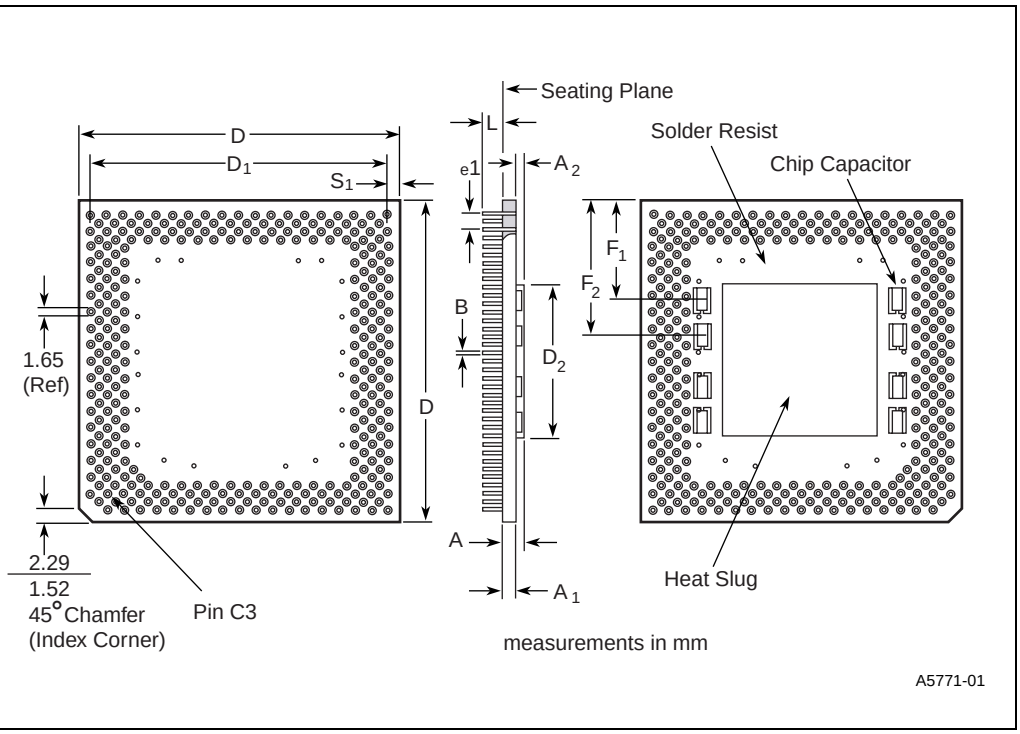


Table 13. PPGA Package Dimensions

Symbol	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	2.72	3.33	0.107	0.131
A1	1.83	2.23	0.072	0.088
A2	1.00 Nominal		0.039 Nominal	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D1	45.59	45.85	1.795	1.805
D2	23.44	23.95	0.923	0.943
el	2.29	2.79	0.090	0.110
L	3.05	3.30	0.120	0.130
N	296		296	
S1	1.52	2.54	0.060	0.100

3.11.2 HL-PBGA Package Mechanical Diagrams

Figure 9 shows the ceramic HL-PBGA package. The dimensions are listed in Table 14.

Figure 9. HL-PBGA Package Dimensions

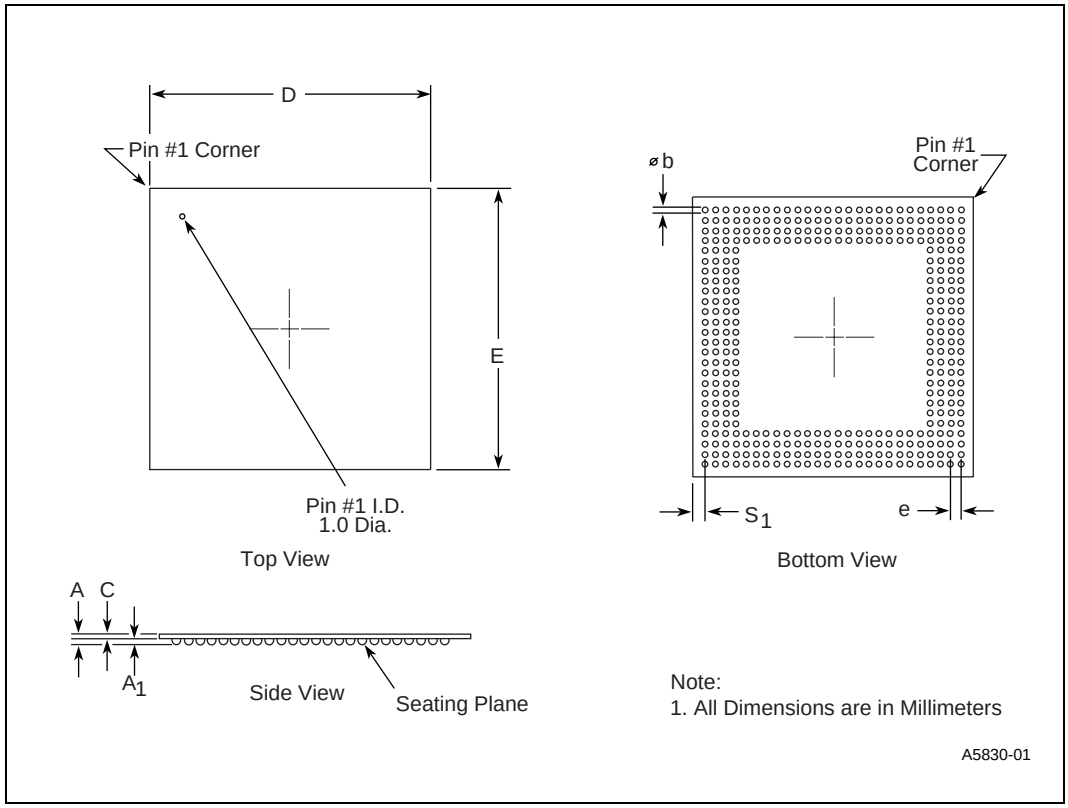


Table 14. HL-PBGA Package Dimensions

Symbol	Millimeters	
	Min	Max
A	1.41	1.67
A_1	0.56	0.70
b	0.60	0.90
c	0.85	0.97
D	34.90	35.10
E	34.90	35.10
e	1.27	
S_1	1.63 REF	

3.12 Thermal Specifications

The low-power embedded Pentium processor with MMX technology is specified for proper operation when case temperature, T_{CASE} (T_C), is within the specified range of 0° C to 85° C for the PPGA package, and 0° C to 95° C for the HL-PBGA package.

The Low-Power Embedded Pentium Processor with MMX Technology in the HL-PBGA package is also available in extended temperature ranges from -40°C to +115°C. For more information, see the *Extended Temperature Pentium® Processor with MMX™ Technology* datasheet, order number 273232.

3.12.1 Measuring Thermal Values

To verify that the proper T_C is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (smaller than 0.150" diameter) should be drilled through the heatsink to allow probing the center of the package. See Figure 10 for an illustration of how to measure T_C.

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega* (part number 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number OB-101).
- The thermocouple should be attached at a 90-degree angle as shown in Figure 10.
- The hole size should be smaller than 0.150" in diameter.
- Make sure there is no contact between thermocouple cement and heatsink base. The contact will affect the thermocouple reading.

3.12.2 Thermal Equations and Data

For the low-power embedded Pentium processor with MMX technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that T_C is met.

The equation used to calculate θ_{CA} is:

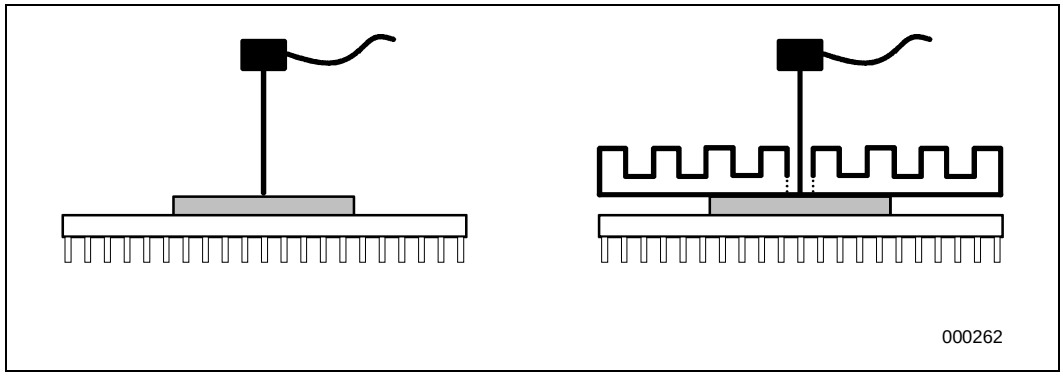
$$\theta_{CA} = \frac{T_C - T_A}{P}$$

Where:

T_A and T_C	=	Ambient and case temperature (°C)
θ_{CA}	=	Case-to-ambient thermal resistance (°C/Watt)
P	=	Maximum power consumption (Watt)

θ_{JC} is thermal resistance from die to package case. θ_{JC} values shown in Tables 15 and 16 are typical values. The actual θ_{JC} values depend on actual thermal conductivity and process of die attach. θ_{CA} is thermal resistance from package case to the ambient. θ_{CA} values shown in these tables are typical values. The actual θ_{CA} values depend on the heatsink design, interface between heatsink and package, airflow in the system, and thermal interactions between processor and surrounding components through PCB and the ambient.

Figure 10. Technique for Measuring T_C



3.12.3 Airflow Calculations for Maximum and Typical Power

Below is an example of determining the airflow required during maximum power consumption for the 166 MHz low-power embedded Pentium processor with MMX technology assuming an ambient air temperature of 50° C:

T_C (HL-PBGA) = 95° C

T_A = 50° C

$P_{HL\text{-}PBGA}$ = 4.1 W

θ_{CA} (HL-PBGA, without heat sink) = 10.98 °C/W

Figure 12 indicates that this example would require about 175 LFM without a heat sink, and about 25 LFM with a heat sink in the vertical orientation.

Below is an example of determining the airflow required during typical power consumption for the 166 MHz low-power embedded Pentium processor with MMX technology assuming an ambient air temperature of 50° C:

T_C (HL-PBGA) = 95° C

T_A = 50° C

$P_{HL\text{-}PBGA}$ = 2.9 W

θ_{CA} (HL-PBGA, without heat sink) = 15.52 °C/W

Figure 12 indicates that this example would require about 0 LFM without a heat sink. A heat sink may not be necessary for typical power and 50 °C ambient conditions.

3.12.4 PPGA Package Thermal Resistance Information

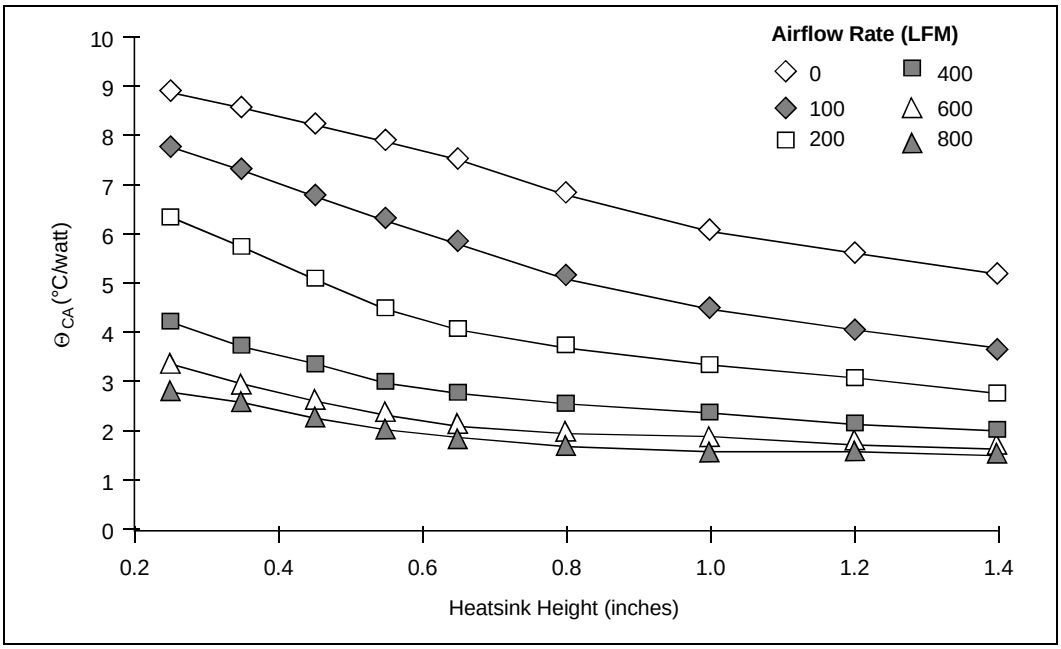
Table 15 lists the θ_{JC} and θ_{CA} values for the low-power embedded Pentium processor with MMX technology in the PPGA package with passive heatsinks.

Table 15. Thermal Resistances for PPGA Packages

Heatsink Height	θ_{JC}	θ_{CA} (°C/watt) vs. Laminar Airflow (linear ft/min)					
(inches)	(°C/watt)	0	100	200	400	600	800
0.25	0.5	8.9	7.8	6.4	4.3	3.4	2.8
0.35	0.5	8.6	7.3	5.8	3.8	3.1	2.6
0.45	0.5	8.2	6.8	5.1	3.4	2.7	2.3
0.55	0.5	7.9	6.3	4.5	3.0	2.4	2.1
0.65	0.5	7.5	5.8	4.1	2.8	2.2	1.9
0.80	0.5	6.8	5.1	3.7	2.6	2.0	1.8
1.00	0.5	6.1	4.5	3.4	2.4	1.9	1.6
1.20	0.5	5.7	4.1	3.1	2.2	1.8	1.6
1.40	0.5	5.2	3.7	2.8	2.0	1.7	1.5
None	1.3	12.9	12.2	11.2	7.7	6.3	5.4

NOTES:
1. Heatsinks are omni-directional pin aluminum alloy.
2. Features were based on standard extrusion practices for a given height: pin size ranged from 50 to 129 mils; pin spacing ranged from 93 to 175 mils; base thickness ranged from 79 to 200 mils.
3. Heatsink attach was 0.005" of thermal grease. Attach thickness of 0.002" will improve performance by approximately 0.3 watt.

Figure 11. Thermal Resistance vs. Heatsink Height, PPGA Packages



3.12.5 HL-PBGA Package Thermal Resistance Information

Table 16 lists the θ_{JC} values for the low-power embedded Pentium processor with MMX technology in the HL-PBGA package.

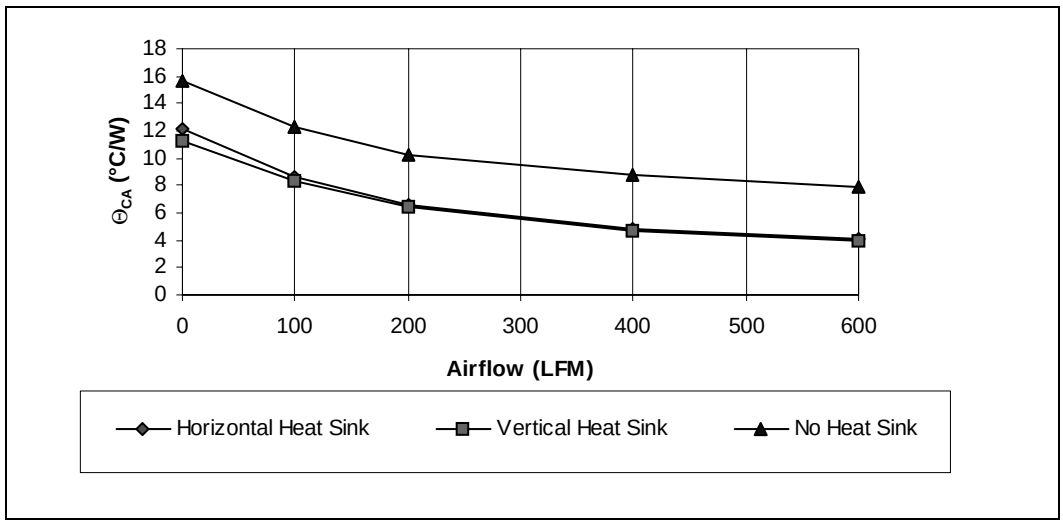
The thermal data collection conditions were:

- A bidirectional anodized aluminum alloy heat sink was used.
- Heat sink height was 7mm.
- In the horizontal orientation the component was mounted flush with the motherboard.
- In the vertical orientation the component was mounted on an add-in card perpendicular to the motherboard.

Table 16. Thermal Resistances for HL-PBGA Packages

Heatsink/ Orientation	θ_{JC} (°C/watt)	θ_{CA} (°C/watt) vs. Laminar Airflow (linear ft/min)				
		0	100	200	400	600
No Heat Sink	0.76	15.66	12.33	10.3	8.85	7.89
Horizontal	0.76	12.09	8.57	6.52	4.82	4.06
Vertical	0.76	11.33	8.34	6.38	4.69	3.95

Figure 12. Thermal Resistance vs. Airflow for HL-PBGA Package



4.0 Electrical Specifications

This section contains preliminary information on new products in production. The specifications are subject to change without notice.

4.1 Absolute Maximum Ratings

Warning: The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables. Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from Electrostatic Discharge (ESD), always take precautions to avoid high static voltages or electric fields.

Table 17. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
V_{CC3} supply voltage with respect to V_{SS}	–0.5 V to +3.2 V
V_{CC2} supply voltage with respect to V_{SS}	–0.5 V to +2.8 V
2.5 V only buffer DC input voltage	–0.5 V to V_{CC3}+0.5 V (not to exceed V_{CC3} max)

NOTE: The Low-Power Embedded Pentium Processor with MMX Technology in the HL-PBGA package is also available in extended temperature ranges from -40°C to +115°C. For more information, see the *Extended Temperature Pentium® Processor with MMX™ Technology* datasheet, order number 273232.

4.2 DC Specifications

Tables 19, 20, 21 and 22 list the DC specifications which apply to the low-power embedded Pentium processor with MMX technology.

4.2.1 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both ON or both OFF within one second of each other.

The I/O voltage V_{CC3} is 2.5 V. The core voltage V_{CC2} is 1.9 V for PPGA. The core voltage V_{CC2} for the HL-PBGA package type is 1.8 V (166 MHz) or 2.0 V (266 MHz).

Table 18. V_{CC} and T_{CASE} Specifications

Package	T_{CASE}	Supply	Min Voltage	Max Voltage	Voltage Tolerance	Frequency
PPGA	0°C to 85°C	V_{CC2}	1.750 V	2.04 V	1.9 V ± 7.5%	166/266 MHz
		V_{CC3}	2.375 V	2.625 V	2.5 V ± 5%	166/266 MHz
HL-PBGA	0°C to 95°C	V_{CC2}	1.665 V	1.935 V	1.8 V ± 7.5%	166 MHz
		V_{CC2}	1.85 V	2.15 V	2.0 V ± 7.5%	266 MHz
		V_{CC3}	2.375 V	2.625 V	2.5 V ± 5%	166/266 MHz

Table 19. DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.5	V	
V_{IH3}	Input High Voltage	V_{CC3} – 0.7	V_{CC3} + 0.3	V	TTL Level
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, (1)
V_{OH3}	Output High Voltage	V_{CC3} – 0.4 V_{CC3} – 0.2		V V	TTL Level, (2) TTL Level, (3)

NOTES:
1. Parameter measured at -4 mA.
2. Parameter measured at 3 mA.
3. Parameter measured at 1 mA; not 100% tested, guaranteed by design.

The values in Table 20 should be used for power supply design. The values were determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 20. I_{CC} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		2.35 (HL-PBGA) 2.5 (PPGA) 4.00	A A A	166 MHz 166 MHz 266 MHz
I_{CC3}	Power Supply Current		0.38 0.38	A A	166 MHz 266 MHz

Table 21. Power Dissipation Requirements for Thermal Design

Parameter	Typical(1)	Max(2)	Unit	Frequency
Thermal Design Power		4.1 (HL-PBGA) 4.5 (PPGA) 7.6	Watts Watts Watts	166 MHz 166 MHz 266 MHz
Active Power(3)	2.9 4.5		Watts Watts	166 MHz 266 MHz
Stop Grant/Auto Halt Powerdown Power Dissipation(4)		0.70 0.70	Watts Watts	166 MHz 266 MHz
Stop Clock Power(5)		0.06 0.06	Watts Watts	166 MHz 266 MHz

NOTES:
1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at the specified voltage running typical applications. This value is dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum thermal design power unless the system uses thermal feedback to limit processor's maximum power. The maximum thermal design power is determined using a worst-case instruction mix and also takes into account the thermal time constant of the package.
3. Active power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
4. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. When in this mode, the processor has a new feature which allows it to power down additional circuitry to enable lower power dissipation. This is the power without snooping at the specified voltage and with TR12 bit 21 set. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled). Stop grant/Auto Halt Powerdown power dissipation without TR12 bit 21 set may be higher. The Max rating may be changed in future specification updates.
5. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input. This is specified at a T_{CASE} of 50 °C.

Table 22. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}< V_{IN}<V_{CC3}$, (1)
I_{LO}	Output Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}< V_{IN}<V_{CC3}$, (1)
I_{IH}	Input High Leakage Current		200	µA	$V_{IN} = V_{CC3} - 0.4$ V, (3)
I_{IL}	Input Low Leakage Current		–400	µA	V_{IN} = 0.4 V (2, 5)

NOTES:
1. This parameter is for inputs/outputs without an internal pull up or pull down.
2. This parameter is for inputs with an internal pull up.
3. This parameter is for inputs with an internal pull down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

4.3 AC Specifications

The AC specifications of the low-power embedded Pentium processor with MMX technology consist of setup times, hold times, and valid delays at 0 pF.

4.3.1 Power and Ground

For clean on-chip power distribution, the PPGA has 25 V_{CC2} (core power), 28 V_{CC3} (I/O power) and 53 V_{SS} (ground) inputs. For the HL-PBGA package, there are 42 V_{CC3}, 37 V_{CC2} and 72 V_{SS} inputs.

Power and ground connections must be made to all external V_{CC2}, V_{CC3} and V_{SS} pins. On the circuit board, all V_{CC2} pins must be connected to a proper voltage V_{CC2} plane or island (core voltage determined by package type/frequency). All V_{CC3} pins must be connected to a 2.5 V V_{CC3}, plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 2 on page 17 for the list of V_{CC2}, V_{CC3} and V_{SS} pins.

4.3.2 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the processor. The processor's large address and data buses can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level power consumption to a high level one (or high to low power transition). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor.

Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor on both V_{CC2} plane and V_{CC3} plane to ensure that the supply voltages stay within specified limits during changes in the supply current during operation.

4.3.3 Connection Specifications

All NC/INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to ground.

4.3.4 AC Timings

The AC specifications given in Table 23 consist of output delays, input setup requirements and input hold requirements for the standard 66 MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to V_{CC3}/V_{CC2} for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, asynchronous inputs must be stable for correct operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Do not select a bus fraction and clock speed which will cause the processor to exceed its internal maximum frequency.

The following specifications apply to all standard TTL signals used with the Pentium processor family:

- TTL input test waveforms are assumed to be 0 to 2.5 V transitions with 1.0 V/ns rise and fall times.
- 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.
- All TTL timings are referenced from V_{CC3}/V_{CC2}.

Table 23. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 1 of 3)
(See Table 18 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 25)
	CLK Frequency	33.33	66.6	MHz		(1)
t_{1a}	CLK Period	15.0	30.0	ns	13	
t_{1b}	CLK Period Stability		±250	ps		(2, 3)
t_2	CLK High Time	4.0		ns	13	@V_{CC3} – 0.7 V, (2)
t_3	CLK Low Time	4.0		ns	13	@0.5 V, (2)
t_4	CLK Fall Time	0.15	1.5	ns	13	V_{CC3} – 0.7 V to 0.5 V, (2, 4)
t_5	CLK Rise Time	0.15	1.5	ns	13	0.5 V to V_{CC3} –0.7 V, (2, 4)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	14	
t_{6b}	AP Valid Delay	1.0	8.5	ns	14	
t_{6c}	LOCK#, Valid Delay	0.9	7.0	ns	14	
t_{6d}	ADS# Valid Delay	1.0	6.2	ns	14	
t_{6e}	A31–A3 Valid Delay	0.8	6.4	ns	14	
t_{6f}	M/IO# Valid Delay	0.8	6.2	ns	14	
t_{6g}	BE7#–BE0#, D/C#, W/R#, SCYC Valid Delay	0.8	7.0	ns	14	
t_7	ADS#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	15	(2)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	14	(5)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	14	(5)
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	14	(5)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	14	(5)
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	14	(5)
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	14	
t_{10b}	HITM# Valid Delay	0.9	6.0	ns	14	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	14	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	14	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.0	7.7	ns	14	
t_{13}	D63–D0, DP3–0 Write Data Float Delay		10.0	ns	15	(2)
t_{14}	A31–A5 Setup Time	6.0		ns	16	(6)
t_{15}	A31–A5 Hold Time	1.0		ns	16	
t_{16a}	INV, AP Setup Time	5.0		ns	16	
t_{16b}	EADS# Setup Time	5.0		ns	16	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	16	

Table 23. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 2 of 3)
(See Table 18 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 25)
t_{18a}	KEN# Setup Time	5.0		ns	16	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	16	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	16	
t_{20}	BRDY# Setup Time	4.75		ns	16	
t_{21}	BRDY# Hold Time	1.0		ns	16	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	16	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	16	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	16	
t_{24b}	PEN# Setup Time	4.8		ns	16	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	16	
t_{25b}	HOLD Hold Time	1.5		ns	16	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	16	(7, 8)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	16	(9)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	16	(8, 10, 17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	16	(9)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	16	(10, 11)
t_{31}	R/S# Setup Time	5.0		ns	16	(7, 8, 10)
t_{32}	R/S# Hold Time	1.0		ns	16	(9)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	16	(10, 11)
t_{34}	D63–D0, DP7–0 Read Data Setup Time	2.8		ns	16	
t_{35}	D63–D0, DP7–0 Read Data Hold Time	1.5		ns	16	
t_{36}	RESET Setup Time	5.0		ns	16	(7, 8)
t_{37}	RESET Hold Time	1.0		ns	17	(9)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	17	(10)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	17	Power up

Table 23. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 3 of 3)
(See Table 18 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 25)
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	17	(7, 8, 10)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	17	(9)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	17	To RESET falling edge, (8)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	17	To RESET falling edge
t_{43a}	BF2–BF0 Setup Time	1.0		mS	17	To RESET falling edge, (10)
t_{43b}	BF2–BF0 Hold Time	2.0		CLKs	17	To RESET falling edge, (12)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	17	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	17	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		ns	13	
t_{46}	TCK High Time	25.0		ns	13	@V_{CC3} –0.7 V, (2)
t_{47}	TCK Low Time	25.0		ns	13	@0.5 V, (2)
t_{48}	TCK Fall Time		5.0	ns	13	V_{CC3} –0.7 V to 0.5 V (2, 13, 14)
t_{49}	TCK Rise Time		5.0	ns	13	0.5 V to V_{CC3} –0.7 V, (2, 13, 14)
t_{50}	TRST# Pulse Width	40.0		ns	19	Asynchronous, (2)
t_{51}	TDI, TMS Setup Time	5.0		ns	19	(15)
t_{52}	TDI, TMS Hold Time	13.0		ns	19	(15)
t_{53}	TDO Valid Delay	3.0	20.0	ns	19	(13)
t_{54}	TDO Float Delay		25.0	ns	19	(2, 13)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	19	(13, 16, 17)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	19	(2, 13, 16, 17)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	19	(15, 16, 17)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	19	(15, 16, 17)

Table 24. APIC AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60a}	PICCLK Frequency	2	16.66	MHz		
t_{60b}	PICCLK Period	60	500	ns	13	
t_{60c}	PICCLK High Time	15		ns	13	
t_{60d}	PICCLK Low Time	15		ns	13	
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	13	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	13	
t_{60g}	PICD0–1 Setup Time	3		ns	16	To PICCLK
t_{60h}	PICD0–1 Hold Time	2.5		ns	16	To PICCLK
t_{60i}	PICD0–1 Valid Delay (L to H)	4	38	ns	14	From PICCLK, (18)
t_{60j}	PICD0–1 High Time (H to L)	4	22	ns	14	From PICCLK, (18)
t_{61}	PICCLK Setup Time	5.0			16	To CLK
t_{62}	PICCLK Hold Time	2.0			16	To CLK
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				(19)

Table 25. Notes to Tables 23 and 24

1. CLK input frequency must be either 33.33 MHz (+1 MHz) or 66.6 MHz (–1 MHz). Operation in the range between 33.33 MHz and 66.6 MHz is not supported.
2. Not 100 percent tested. Guaranteed by design.
3. These signals are measured on the rising edge of adjacent CLKs at V_{CC3}/V_{CC2}. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within +250 ps, and therefore the CLK input cannot be changed dynamically.
4. 0.87 V/ns ≤ CLK input rise/fall time ≤ 8.7 V/ns.
5. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
6. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
7. Setup time is required to guarantee recognition on a specific clock.
8. This input may be driven asynchronously.
9. Hold time is required to guarantee recognition on a specific clock.
10. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
11. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
12. BF2–BF0 should be strapped to V_{CC3} or V_{SS}.
13. Referenced to TCK falling edge.
14. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
15. Referenced to TCK rising edge.
16. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
17. During probe mode operation, do not use the boundary scan timings (t_{55}–t_{58}).
18. This assumes an external pull-up resistor to V_{CC} and a lumped capacitive load. The pull-up resistor must be between 300 Ω and 1 KΩ, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 6 ns and 36 ns.
19. The CLK to PICCLK ratio has to be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4.

Figure 13. Clock Waveform

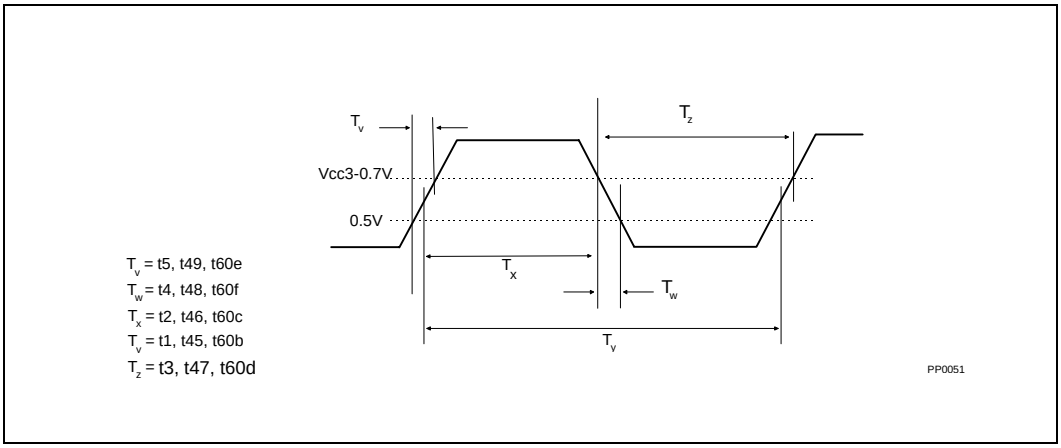


Figure 14. Valid Delay Timings

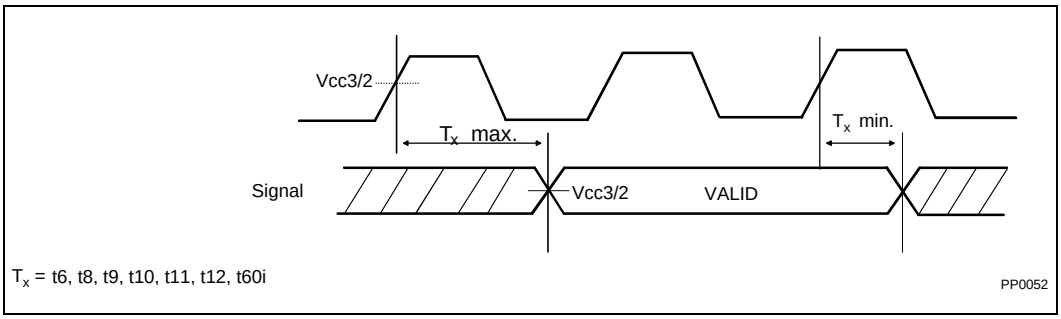


Figure 15. Float Delay Timings

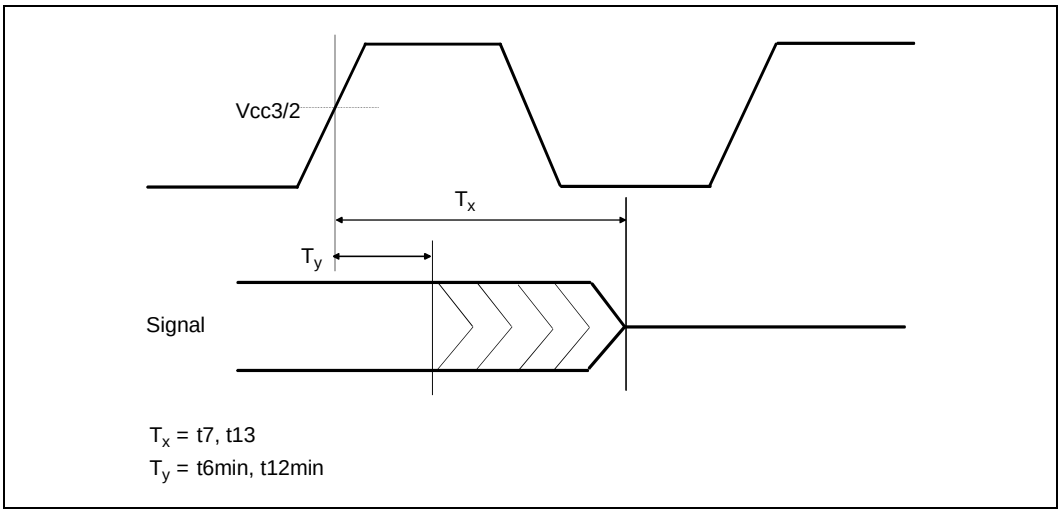
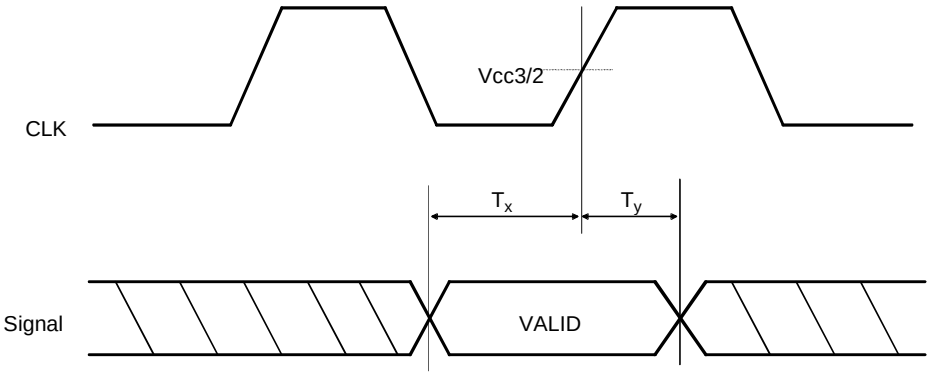


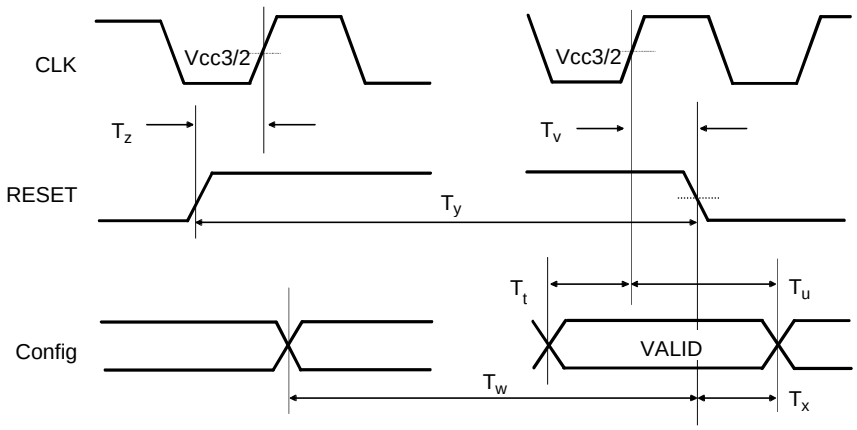
Figure 16. Setup and Hold Timings



T_x = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK), t61

T_y = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t62

Figure 17. Reset and Configuration Timings



T_t = t40

T_u = t41

T_v = t37

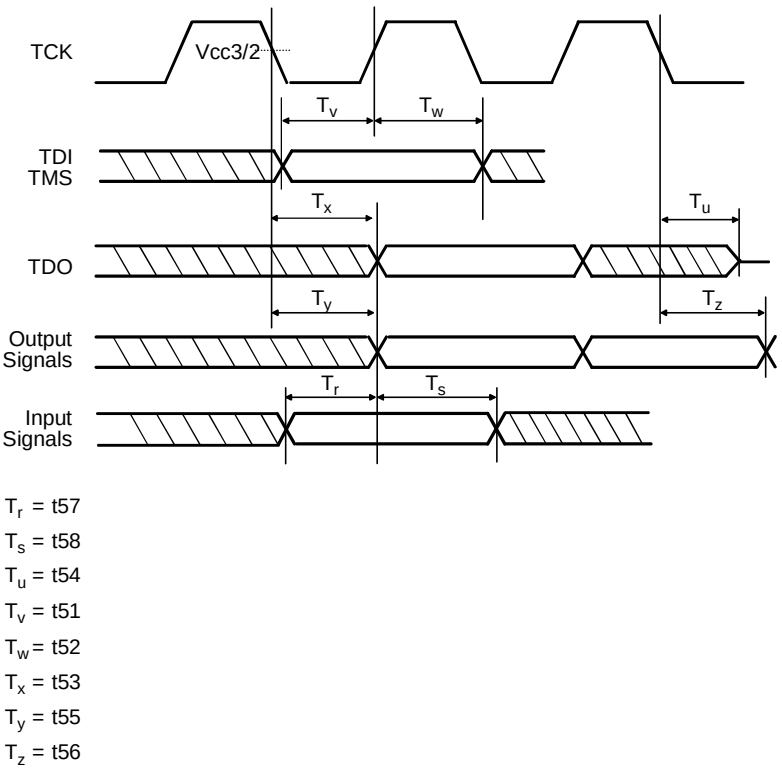
T_w = t42, t43c, t43e, t87

T_x = t43b, t43d, t43f, t88

T_y = t38, t39

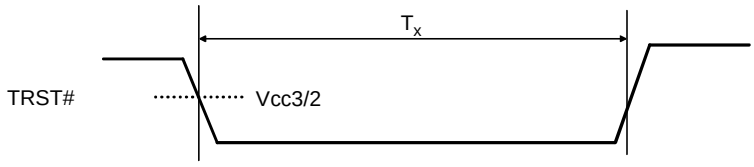
T_z = t36

Figure 18. Test Timings



T_r = t57
T_s = t58
T_u = t54
T_v = t51
T_w = t52
T_x = t53
T_y = t55
T_z = t56

Figure 19. Test Reset Timings



T_x = t50

4.4 I/O Buffer Models

This section describes the I/O buffer models of the low-power embedded Pentium processor with MMX technology.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used. Figure 20 shows the structure of the input buffer model and Figure 21 shows the output buffer model. Table 26 and 27 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (R_S) are a part of the diode model. Remove these when removing the diodes from the input model.

Figure 20. First Order Input Buffer Model

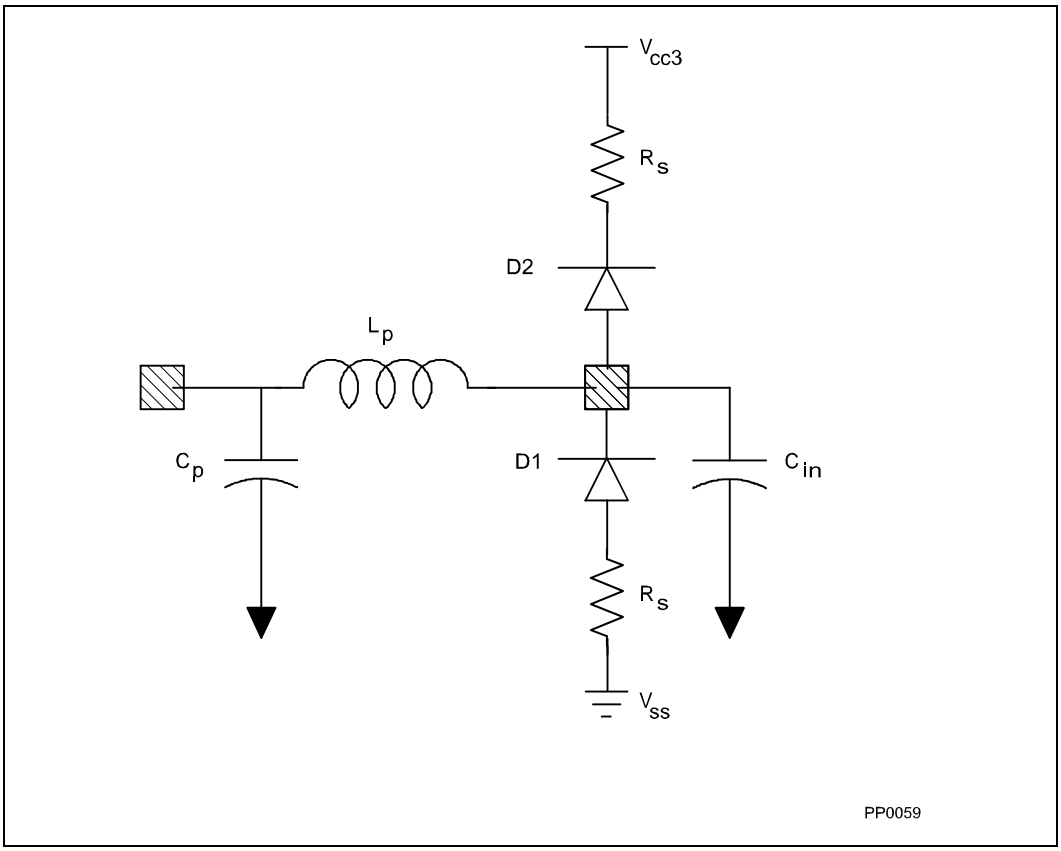


Table 26. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
C_{in}	Minimum and Maximum value of the capacitance of the input buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance
R_S	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 21. First Order Output Buffer Model

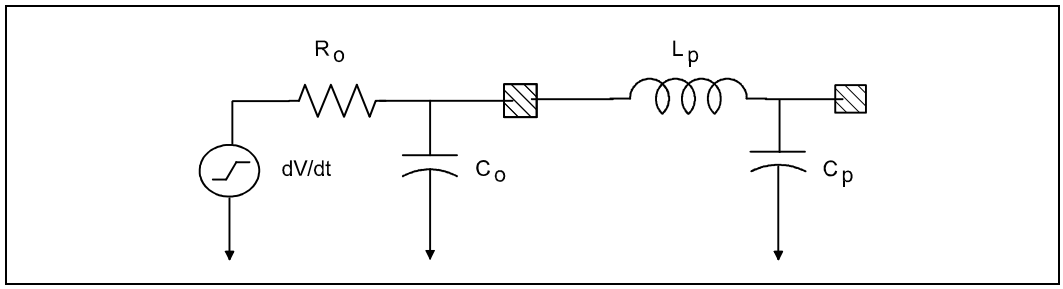


Table 27. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_O	Minimum and maximum value of the output impedance of the output buffer model
C_O	Minimum and Maximum value of the capacitance of the output buffer model
L_P	Minimum and Maximum value of the package inductance
C_P	Minimum and Maximum value of the package capacitance

4.4.1 Buffer Model Parameters

This section gives the parameters for each input, output and bidirectional buffers.

The input, output and bidirectional buffer values of the processor are listed in Table 29. These tables contain listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the C_{IN}, C_P and L_P values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 28 for the groupings of the buffers.

The input, output and bidirectional buffer's values are listed below. These tables contain listings for all three types. When a bidirectional pin is operating as an input, just use the C_{IN}, C_P and L_P values, if it is operating as a driver use all the data parameters.

Table 28. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7–BE5#, BP3–BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO	O	ED1	
A31–A3, AP, BE4#–BE0#, CACHE#, D/C#, D63–D0, DP8–DP0, HLDA, LOCK#, M/IO#, SCYC, ADS#, HITM#, HIT#, W/R#, PICD0, PICD1	I/O	EB1	EB1

Table 29. Input, Output and Bidirectional Buffer Model Parameters for PPGA Package

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					1.1	5.3	7.7	15.3	0.8	1.2
(input)	Falling					1.1	5.3	7.7	15.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.1	5.8	8.1	16.3	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.1	5.8	8.1	16.3	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.3	7.0	8.2	18.4	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.3	7.0	8.2	18.4	2.0	2.6

Table 30. Preliminary Input, Output and Bidirectional Buffer Model Parameters for HL-PBGA Package

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					0.2	0.4	6.4	11.3	0.8	1.2
(input)	Falling					0.2	0.4	6.4	11.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.5	5.4	11.7	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.5	5.4	11.7	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.4	5.2	10.3	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.4	5.2	10.3	2.0	2.6

NOTE: The data in this table is based on preliminary design information. Input, output and bidirectional buffer values are being characterized at this time.

Table 31. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
I_S	Saturation Current	1.4e–14A	2.78e–16A
N	Emission Coefficient	1.19	1.00
R_S	Series Resistance	6.5 Ω	6.5 Ω
T_T	Transit Time	3 ns	6 ns
V_J	PN Potential	0.983 V	0.967 V
C_{J0}	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

4.5 Signal Quality Specifications

Signals driven by the system into the low-power embedded Pentium processor with MMX technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component.

4.5.1 Overshoot

The maximum overshoot and overshoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- Maximum overshoot specification: The maximum overshoot of the CLK/PICCLK signals should not exceed V_{CC2}, nominal +0.6 V. The maximum overshoot of all other input signals should not exceed V_{CC3}, nominal +1.0 V.
- Overshoot threshold duration specification: The overshoot threshold duration is defined as the sum of all time during which the input signal is above V_{CC3}, nominal +0.3 V, within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

Refer to Table 32 for a summary of the overshoot specifications for the low-power embedded Pentium processor with MMX technology.

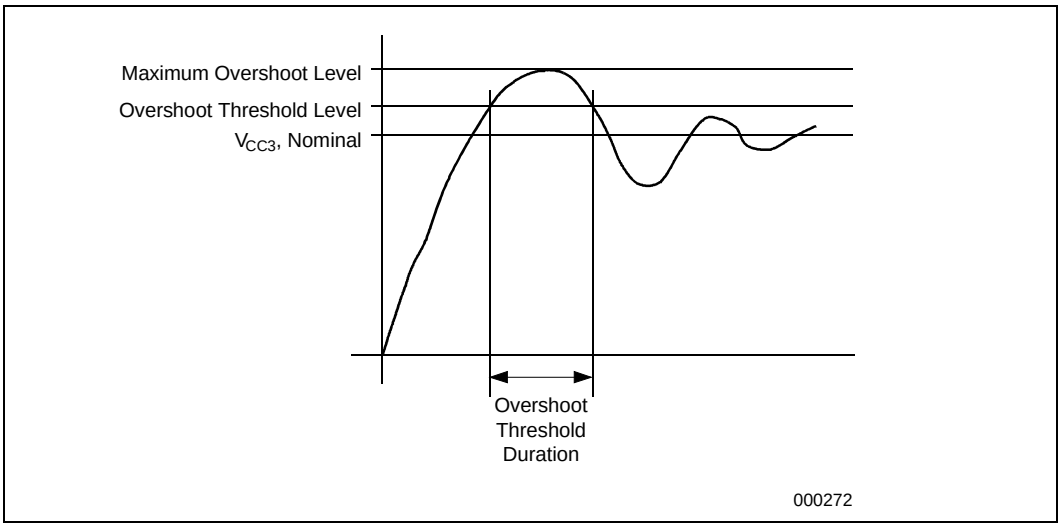
Table 32. Overshoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	V_{CC3}, nominal +0.3	V	(1, 2)
Maximum Overshoot Level (CLK and PICCLK)	V_{CC3}, nominal +0.6	V	(1, 2)
Maximum Overshoot Level (all other inputs)	V_{CC3}, nominal +1.0	V	(1, 2)
Maximum Threshold Duration	20% of clock period above threshold voltage	ns	(2)
Maximum Ringback	V_{CC3}, nominal –0.7	V	(1, 2)

NOTES:

1. V_{CC3}, nominal refers to the voltage measured at the V_{CC3} pins.
2. See Figure 22 and Figure 24.

Figure 22. Maximum Overshoot Level, Overshoot Threshold Level and Overshoot Threshold Duration



4.5.2 Undershoot

The maximum undershoot and undershoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- Maximum undershoot specification: The maximum undershoot of the CLK/PICCLK signals must not drop below –0.6 V. The maximum undershoot of all other input signals must not drop below –1.0 V.
- Undershoot threshold duration specification: The undershoot threshold duration is defined as the sum of all time during which the input signal is below –0.3 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

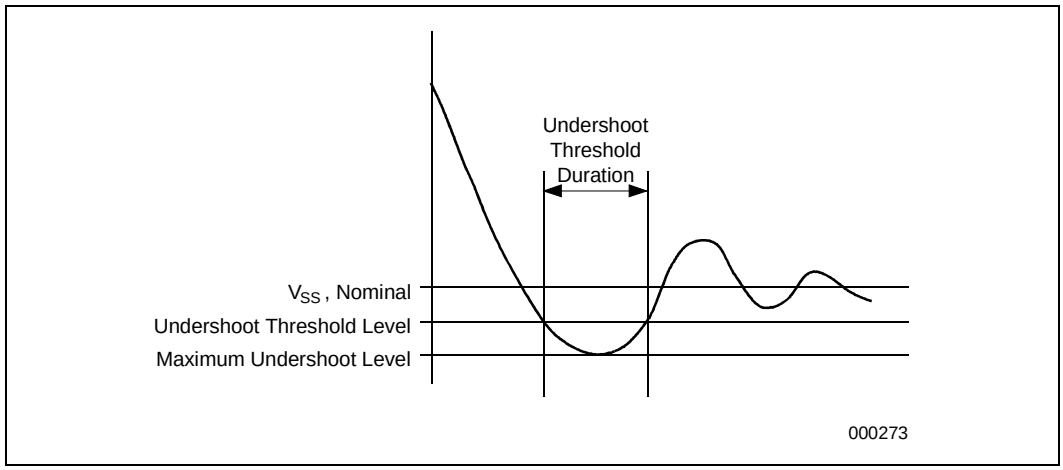
Refer to Table 33 for a summary of the undershoot specifications for the low-power embedded Pentium processor with MMX technology.

Table 33. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	–0.3	V	(1)
Minimum Undershoot Level (CLK and PICCLK)	–0.6	V	(1)
Minimum Undershoot Level (all other inputs)	–1.0	V	(1)
Maximum Threshold Duration	20% of clock period below threshold voltage	ns	(1)
Maximum Ringback	0.5	V	(1)

NOTE:
1. See Figure 23 and Figure 25.

Figure 23. Maximum Undershoot Level, Undershoot Threshold Level and Undershoot Threshold Duration



4.5.3 Ringback

Excessive ringback can contribute to long-term reliability degradation of the low-power embedded Pentium processor with MMX technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC3} (or above V_{SS}) relative to the V_{CC3} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specifications. By meeting the overshoot/undershoot specifications, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification. The maximum ringback specification for inputs to the low-power embedded Pentium processor with MMX technology is described as follows:

- Maximum ringback specification: The maximum ringback of inputs associated with their high states (overshoot) must not drop below V_{CC3} −1.0 V as shown in Figure 24. Similarly, the maximum ringback of inputs associated with their low states (undershoot) must not exceed 0.5 V as shown in Figure 25.
- Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC} (below V_{SS}). The guideline assumes the absence of diodes on the input.

Figure 24. Maximum Ringback Associated with the Signal High State

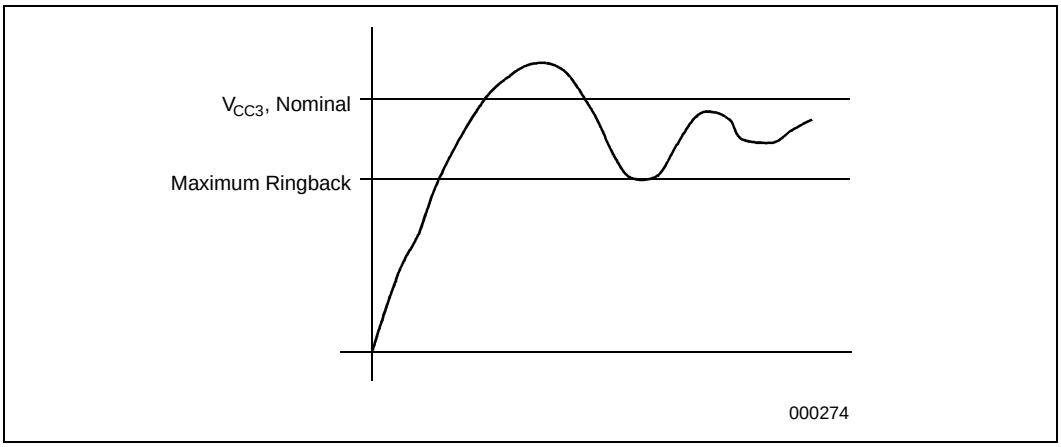
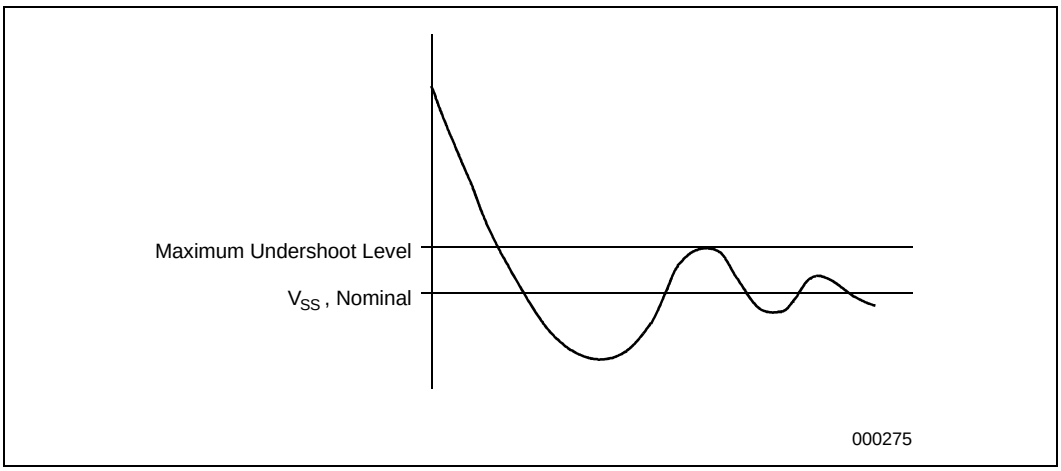


Figure 25. Maximum Ringback Associated with the Signal Low State



4.5.4 Settling Time

The settling time is defined as the time a signal requires the receiver to settle within 10 percent of V_{CC3} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

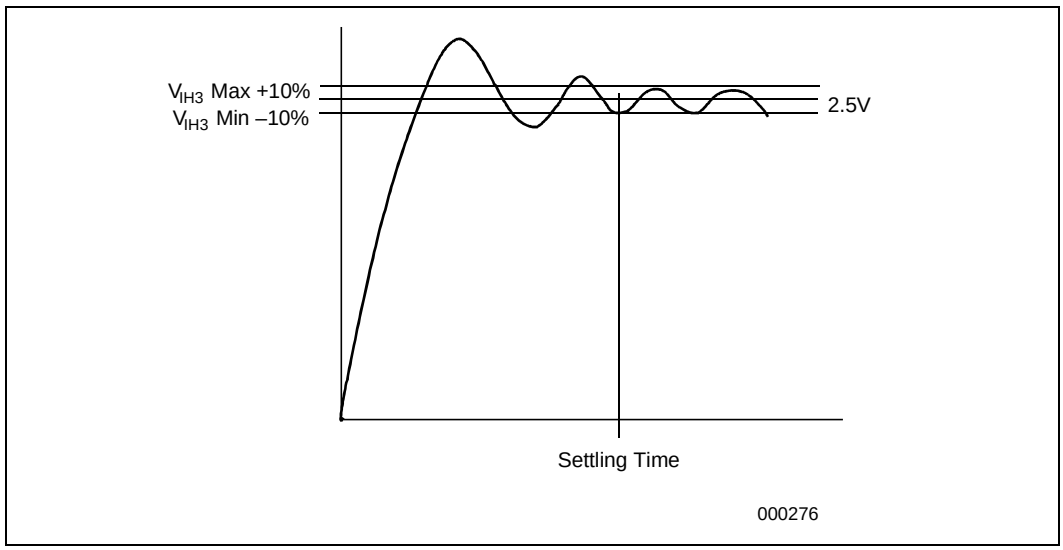
Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. Second order, and other, effects on a physical board serve to dampen the signal at the receiver. Because of these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

To make sure that there is no impact on the flight times of the signals if the waveform has not settled, settling time is simulated at the slow corner. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendations will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts. Use the following procedure to verify board simulation and tuning with concerns for settling time:

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur (signal requires more than 12.5 ns to settle to ±10% of its final value), simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If, however, flight times are not consistent over the five consecutive cycles, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled. Maximum Settling Time to within 10 percent of V_{IH} or V_{IL} is 12.5 ns at 66 MHz.

Figure 26. Settling Time



4.5.5 Measurement Methodology

The waveform of the input signals should be measured at the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 ms/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. A 1-MΩ probe with loading of less than 1 pF is recommended. The measurement should be taken at the input pins and their nearest V_{SS} pins.

4.6 Measuring Maximum Overshoot, Undershoot and Ringback

The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 ns/div (for CLK) or 20 ns/div (for other inputs) for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum overshoot and associated ringback with the largest possible granularity. Similarly, readjust the vertical position to measure the maximum undershoot and associated ringback. There is no allowance for crossing the maximum overshoot, maximum undershoot or maximum ringback specifications.

4.7 Measuring Overshoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The overshoot threshold duration is defined as the sum of all time during which the input signal is above V_{CC3} nominal + 0.3 V within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

4.8 Measuring Undershoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below –0.3 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.