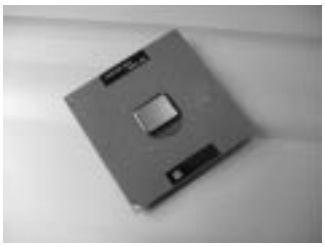
Pentium® III Processor for the PGA370 Socket at 500E MHz and 550E MHz

Datasheet

Product Features

- Available at 500 MHz and 550 MHz. 'E' denotes support for Advanced Transfer Cache and Advanced System Buffering
- System bus frequency at 100 MHz
- Available in versions that incorporate 256 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache with Error Correcting Code (ECC))
- Dual Independent Bus (DIB) architecture: Separate dedicated external System Bus and dedicated internal high-speed cache bus
- Internet Streaming SIMD Extensions for enhanced video, sound and 3D performance
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Dynamic execution micro architecture
- Intel Processor Serial Number
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- Flip Chip Pin Grid Array (FC-PGA) packaging technology; FC-PGA processors deliver high performance with improved handling protection and socketability
- Integrated high performance 16 KB instruction and 16 KB data, nonblocking, level one cache
- Double Quad Word Wide(256bit) cache data bus provides extremely high throughput on read/store operations.
- 8-way cache associativity provides improved cache hit rate on reads/store operations.
- Error-correcting code for System Bus data

The Intel® Pentium® III processor is designed for high-performance desktops and for workstations and servers. It is binary compatible with previous Intel Architecture processors. The Pentium III processor provides great performance for applications running on advanced operating systems such as Windows* 98, Windows NT and UNIX*. This is achieved by integrating the best attributes of Intel processors—the dynamic execution, Dual Independent Bus architecture plus Intel MMX™ technology and Internet Streaming SIMD Extentions—bringing a new level of performance for systems buyers. The Pentium III extends the power of the Pentium II processor with performance headroom for business media, communication and internet capabilities. Systems based on Pentium III processors also include the latest features to simplify system management and lower the cost of ownership for large and small business environments. The Pentium III processor offers great performance for today's and tomorrow's applications.



FC-PGA Package

October 1999

Order Number: 245264-001

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1.0 Introduction

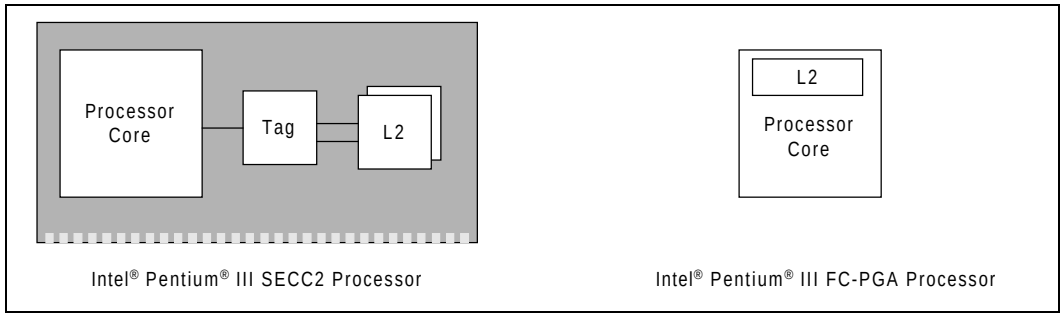
The Intel® Pentium® III processor for the PGA370 socket is the next member of the P6 family, in the Intel IA-32 processor line and hereafter will be referred to as the “Pentium III processor”, or simply “the processor”. The processor uses the same core and offers the same performance as the Intel® Pentium® III processor for the SC242 connector, but utilizes a new package technology called flip-chip pin grid array, or FC-PGA. This package utilizes the same 370-pin zero insertion force socket (PGA370) used by the Intel® Celeron™ processor. Thermal solutions are attached directly to the back of the processor core package without the use of a thermal plate or heat spreader.

The Pentium III processor, like its predecessors in the P6 family of processors, implements a Dynamic Execution microarchitecture—a unique combination of multiple branch prediction, data flow analysis, and speculative execution. This enables these processors to deliver higher performance than the Intel Pentium processor, while maintaining binary compatibility with all previous Intel Architecture processors. The processor also executes Intel® MMX™ technology instructions for enhanced media and communication performance just as it’s predecessor, the Intel Pentium III processor. The Pentium III processor executes Internet Streaming SIMD Extensions for enhanced floating point and 3-D application performance. In addition, the Pentium III processor extends the concept of processor identification with the addition of a processor serial number. Refer to the *Intel® Processor Serial Number* application note (Order Number 245125) for more detailed information. The Pentium III processor utilizes multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The processor includes an integrated on-die, 256KB, 8-way set associative level-two (L2) cache. The L2 cache implements the new Advanced Transfer Cache (ATC) Architecture with a 256-bit wide bus. The processor also includes a 16KB level one (L1) instruction cache and 16KB L1 data cache. These cache arrays run at the full speed of the processor core. As with the Intel Pentium III processor for the SC242 connector, the Pentium III processor for the PGA370 socket has a dedicated L2 cache bus, thus maintaining the dual independent bus architecture to deliver high bus bandwidth and performance (see Figure 1). Memory is cacheable for 64 GB of addressable memory space, allowing significant headroom for desktop systems. Refer to the *Pentium® III Processor Specification Update* document to determine the cacheability and cache configuration options for a specific processor. The Specification Update document can be requested at your nearest Intel sales office.

The processor utilizes the same processing system bus technology as the Pentium II processor. This allows for a higher level of performance for uni-processor systems. The system bus uses a variant of GTL+ signaling technology called Assisted Gunning Transceiver Logic (AGTL+) signaling technology.

Figure 1. Second Level (L2) Cache Implementation



1.1 Terminology

In this document, a '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "system bus" refers to the interface between the processor, system core logic (a.k.a. theAGPset components), and other bus agents. The term "cache bus" refers to the interface between the processor and the on-die L2 cache components. The cache bus does NOT connect to the system bus, and is not visible to other agents on the system bus.

1.1.1 Package and Processor Terminology

The following terms are used often in this document and are explained here for clarification:

- **Pentium® III processor** - The entire product including all internal components.
- **PGA370 socket** - 370-pin Zero Insertion Force (ZIF) socket which a FC-PGA or PPGA packaged processor plugs into.
- **FC-PGA** - Flip Chip Pin Grid Array. The package technology used on Pentium III processors for the PGA370 socket.
- **Advanced Transfer Cache (ATC)** - New L2 cache architecture unique to the 0.18 micron Pentium III processors. ATC consists of microarchitectural improvements that provide a higher data bandwidth interface into the processor core that is completely scaleable with the processor core frequency.
- **Keep-out zone** - The area on or near a FC-PGA packaged processor that system designs can not utilize.
- **Keep-in zone** - The area of a FC-PGA packaged processor that thermal solutions may utilize.
- **OLGA** - Organic Land Grid Array. The package technology for the core used in S.E.C.C. 2 processors that permits attachment of the heatsink directly to the die.
- **PPGA - Plastic Pin Grid Array.** The package technology used for Intel® Celeron™ processors which utilize the PGA370 socket.
- **Processor** - For this document, the term processor is the generic form of the Pentium III processor for the PGA370 socket in the FC-PGA package.
- **Processor core** - The processor's execution engine.
- **S.E.C.C.** - The processor package technology called "Single Edge Contact Cartridge". Used with Intel® Pentium® II processors.
- **S.E.C.C. 2** - The follow-on to S.E.C.C. processor package technology. This differs from its predecessor in that it has no extended thermal plate, thus reducing thermal resistance. Used with Intel® Pentium® III processors and latest versions of the Intel® Pentium® II processor.
- **SC242** - The 242-contact slot connector (previously referred to as slot 1 connector) that the S.E.C.C. and S.E.C.C. 2 plug into, just as the Intel® Pentium® Pro processor uses socket 8.

The cache and L2 cache are industry designated names.

1.1.2 Processor Naming Convention

A letter(s) is added to certain processors (e.g., 550E MHz) when the core freqnency alone may not uniquely identify the processor. Below is a summary what each letter means as well as a table listing all the available Pentium III processors for the PGA370 socket.

"E" — Processor with "Advanced Transfer Cache" (CPUID 068xh and greater)

Table 1. Processor Identification

Processor	Core Frequency (MHz)	System Bus Frequency (MHz)	L2 Cache Size (KB)	L2 Cache Type	CPUID[1]
500E	500	100	256	ATC	068xh
550E	550	100	256	ATC	068xh

NOTES:
1. Refer to the *Pentium® III Processor Specification Update* for the exact CPUID for each processor.
2. ATC = Advanced Transfer Cache. ATC is an L2 Cache integrated on the same die as the processor core. With ATC, the interface between the processor core and L2 Cache is 256-bits wide, runs at the same frequency as the processor core and has enhanced buffering.

1.2 Related Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents [1,2].

Document	Intel Order Number
AP-485, *Intel® Processor Identification and the CPUID Instruction*	241618
AP-585, *Pentium® II Processor GTL+ Guidelines*	243330
AP-589, *Design for EMI*	243334
AP-905, *Pentium® III Processor Thermal Design Guidelines*	245087
AP-907, *Pentium® III Processor Power Distribution Guidelines*	245085
AP-909, Intel® Processor Serial Number	245125
Intel® Architecture Software Developer's Manual	243193
Volume I: Basic Architecture	243190
Volume II: Instruction Set Reference	243191
Volume III: System Programming Guide	243192
P6 Family of Processors Hardware Developer's Manual	244001
IA-32 Processors and Related Products 1999 Databook	243565
Intel® Pentium® II Processor Developer's Manual	243502
Intel® Pentium® III Processor Datasheet	244452
Intel® Pentium® III Processor Specification Update	244453
Intel® Celeron™ Processor Datasheet	243658
Intel® Celeron™ Processor Specificiation Update	243748
370-Pin Socket (PGA370) Design Guidelines	244410
PGA370 Heat Sink Cooling in MicroATX Chassis	245025

Document	Intel Order Number
Intel® 810E Chipset Platform Design Guide [3]	
Intel® 820 Chipset Platform Design Guide [3]	
Intel® 840 Chipset Platform Design Guide [3]	
CK98 Clock Synthesizer/Driver Specification [3]	
Intel® *810E Chipset Clock Synthesizer/Driver Specification* [3]	
VRM 8.4 DC-DC Converter Design Guidelines [3]	
Intel® Pentium® III Processor for the PGA370 Socket I/O Buffer Models, XTK/XNS* Format [3]	
Intel® Pentium® Pro Processor BIOS Writer's Guide [3]	
Extensions to the Intel® Pentium® Pro Processor BIOS Writer's Guide [3]	
Intel® Pentium® III Thermal/Mechanical Solution Functional Guidelines	245241

NOTES:
1. Unless otherwise noted, this reference material can be found on the Intel Developer's Website located at http://developer.intel.com.
2. For a complete listing of Intel® Pentium® III processor reference material, please refer to the Intel Developer's Website at http://developer.intel.com/design/PentiumIII/.
3. This material is available through an Intel field sales representative.

2.0 Electrical Specifications

2.1 Processor System Bus and V_{REF}

The Pentium III processor signals use a variation of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

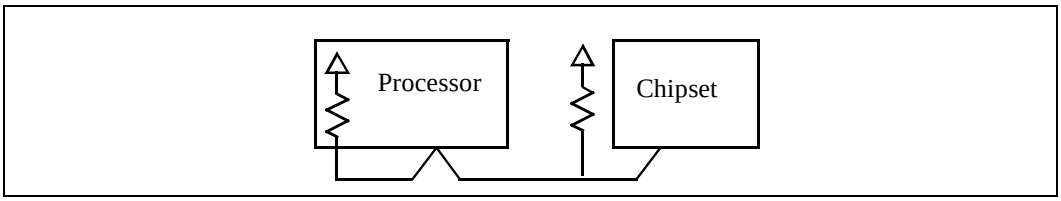
The Intel® Pentium® Pro processor system bus specification is similar to the GTL specification, but was enhanced to provide larger noise margins and reduced ringing. The improvements are accomplished by increasing the termination voltage level and controlling the edge rates. This specification is different from the GTL specification, and is referred to as GTL+. For more information on GTL+ specifications, see the GTL+ buffer specification in the *Intel® Pentium® II Processor Developer's Manual*.

Current P6 family processors vary from the Intel Pentium Pro processor in their output buffer implementation. The buffers that drive the system bus signals on the Intel Celeron, Pentium II, and Pentium III processors are actively driven to $V_{CC_{CORE}}$ for one clock cycle after the low to high transition to improve rise times. These signals should still be considered open-drain and require termination to a supply that provides the high signal level. Because this specification is different from the GTL+ specification, it is referred to as AGTL+, or Assisted GTL+ in this and other documentation. AGTL+ logic and GTL+ logic are compatible with each other and may both be used on the same system bus. For more information on AGTL+ routing, see the appropriate platform design guide.

AGTL+ inputs use differential receivers which require a reference signal (V_{REF}). V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1, and is supplied by the motherboard to the PGA370 socket for the processor core. Local V_{REF} copies should also be generated on the motherboard for all other devices on the AGTL+ system bus. Termination (usually a resistor at each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the transmission line. The processor contains on-die termination resistors that provide termination for one end of the AGTL+ bus, except for RESET#. These specifications assume another resistor at the end of each signal trace to ensure adequate signal quality for the AGTL+ signals and provide backwards compatibility for the Intel Celeron processor; see Table 9 for the bus termination voltage specifications for AGTL+. Refer to the *Intel® Pentium® II Processor Developer's Manual* for the AGTL+ bus specification. Solutions exist for single-ended termination as well, though this implementation changes system design and eliminate backwards compatibility for Intel Celeron processors in the PPGA package. Single-ended termination designs must still provide an AGTL+ termination resistor on the motherboard for the RESET# signal. Figure 2 is a schematic representation of the AGTL+ bus topology for the Pentium III processors in the PGA370 socket.

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus including trace lengths is highly recommended when designing a system with a heavily loaded AGTL+ bus, especially for systems using a single set of termination resistors (i.e., those on the processor die). Such designs will not match the solution space allowed for by installation of termination resistors on the baseboard.

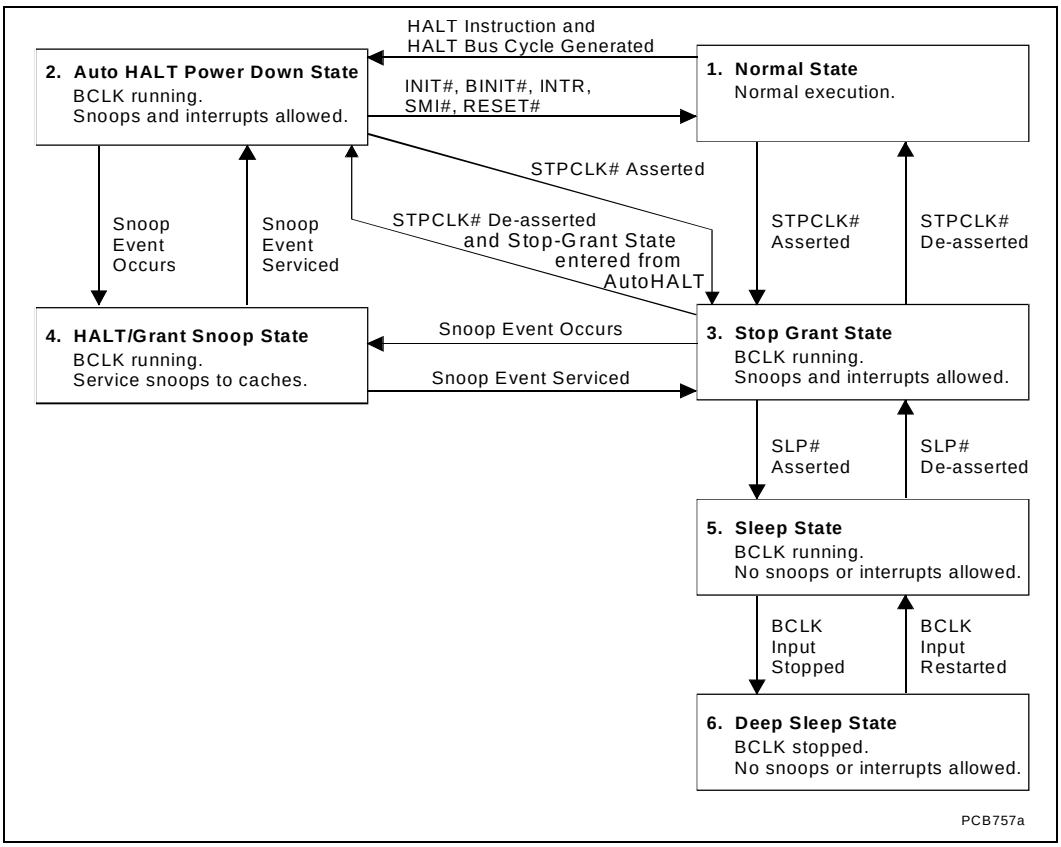
Figure 2. AGTL+ Bus Topology In Uniprocessor Configuration



2.2 Clock Control and Low Power States

processors allow the use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 3 for a visual representation of the processor low power states.

Figure 3. Stop Clock State Machine



For the processor to fully realize the low current consumption of the Stop-Grant, Sleep, and Deep Sleep states, a Model Specific Register (MSR) bit must be set. For the MSR at 02AH (Hex), bit 26 must be set to a '1' (this is the power on default setting) for the processor to stop all internal clocks during these modes. For more information, see the *Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide*.

2.2.1 Normal State—State 1

This is the normal operating state for the processor.

2.2.2 AutoHALT Powerdown State—State 2

AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

FLUSH# will be serviced during the AutoHALT state, and the processor will return to the AutoHALT state.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

2.2.3 Stop-Grant State—State 3

The Stop-Grant state on the processor is entered when the STPCLK# signal is asserted.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# and FLUSH# will not be serviced during the Stop-Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 2.2.4). A transition to the Sleep state (see Section 2.2.5) will occur with the assertion of the SLP# signal.

While in Stop-Grant State, SMI#, INIT#, and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized and serviced upon return to the Normal state.

2.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

2.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from the Stop-Grant state. Once in the Stop-Grant state, the SLP# pin can be asserted, causing the processor to enter the Sleep state. The SLP# pin is not recognized in the Normal or AutoHALT states.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK input (see Section 2.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin can be deasserted if another asynchronous system bus event occurs. The SLP# pin has a minimum assertion of one BCLK period.

2.2.6 Deep Sleep State—State 6

The Deep Sleep state is the lowest power state the processor can enter while maintaining context. The Deep Sleep state is entered by stopping the BCLK input (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK is stopped. It is recommended that the BLCK input be held low during the Deep Sleep State. Stopping of the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep state. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

2.2.7 Clock Control

BCLK provides the clock signal for the processor and on die L2 cache. During AutoHALT Power Down and Stop-Grant states, the processor will process a system bus snoop. The processor will not stop the clock to the L2 cache during AutoHALT Power Down or Stop-Grant states. Entrance into the Halt/Grant Snoop state will allow the L2 cache to be snooped, similar to the Normal state.

When the processor is in Sleep and Deep Sleep states, it will not respond to interrupts or snoop transactions. During the Sleep state, the internal clock to the L2 cache is not stopped. During the Deep Sleep state, the internal clock to the L2 cache is stopped. The internal clock to the L2 cache will be restarted only after the internal clocking mechanism for the processor is stable (i.e., the processor has re-entered Sleep state).

PICCLK should not be removed during the AutoHALT Power Down or Stop-Grant states. PICCLK can be removed during the Sleep or Deep Sleep states. When transitioning from the Deep Sleep state to the Sleep state, PICCLK must be restarted with BCLK.

2.3 Power and Ground Pins

The operating voltage of the Pentium III processor for the PGA370 socket is the same for the core and the L2 cache; VCC_{CORE}. There are four pins defined on the package for voltage identification (VID). These pins specify the voltage required by the processor core. These have been added to cleanly support voltage specification variations on current and future processors.

For clean on-chip power and voltage reference distribution, the Pentium III processors in the FC-PGA package have 75 VCC_{CORE}, 8 V_{REF}, 15 V_{TT}, and 77 V_{SS} (ground) inputs. VCC_{CORE} inputs supply the processor core, including the on-die L2 cache. V_{TT} inputs (1.5V) are used to provide an AGTL+ termination voltage to the processor, and the V_{REF} inputs are used as the AGTL+ reference voltage for the processor. Note that not all V_{TT} inputs must be connected to the V_{TT} supply. Refer to Section 5.3 for more details.

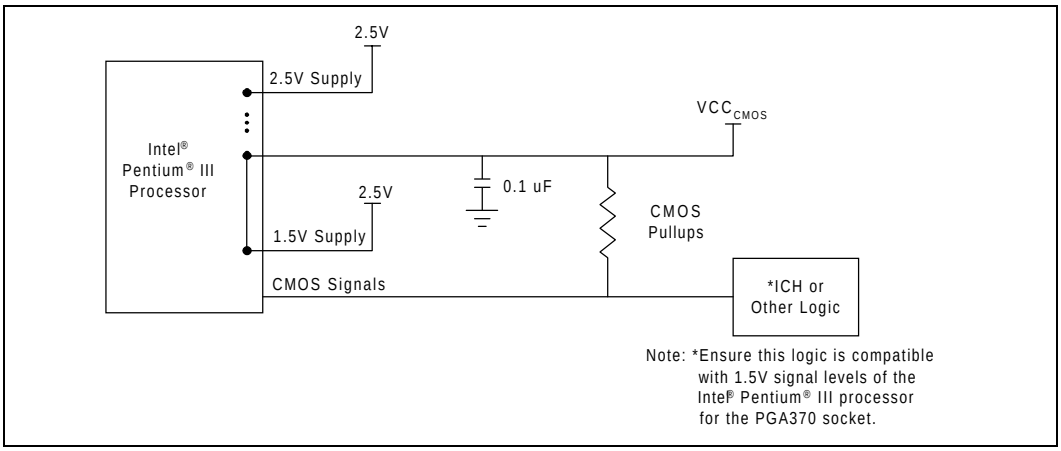
On the motherboard, all VCC_{CORE} pins must be connected to a voltage island (an island is a portion of a power plane that has been divided, or an entire plane). In addition, the motherboard must implement the V_{TT} pins as a voltage island or large trace. Similarly, all V_{SS} pins must be connected to a system ground plane.

Three additional power related pins exist on a processors utilizing the PGA370 socket. They are $VCC_{1.5}$, $VCC_{2.5}$ and VCC_{CMOS}.

The VCC_{CMOS} pin provides the CMOS voltage for the pull-up resistors required on the system platform. A 2.5V source must be provided to the $VCC_{2.5}$ pin and a 1.5V source must be provided to the $VCC_{1.5}$ pin. The source for $VCC_{1.5}$ must be the same as the one supplying V_{TT}. The processor routes the compatible CMOS voltage source (1.5V or 2.5V) through the package and out to the VCC_{CMOS} output pin. Processors based on 0.25 micron technology, such as the Intel Celeron processor, utilize 2.5V CMOS buffers. Processors based on 0.18 micron technology, such as the Pentium III processor for the PGA370 socket, utilize 1.5V CMOS buffers. The signal $VCORE_{DET}$ can be used by hardware on the motherboard to detect which CMOS voltage the processor requires. A $VCORE_{DET}$ connected to Vss within the processor indicates a 1.5V requirement on VCC_{CMOS}. Refer to Figure 4.

Each power signal must meet the specifications stated in Table 6 on page 22.

Figure 4. Processor VCC_{CMOS} Package Routing



2.3.1 Phase Lock Loop (PLL) Power

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL. Please refer to the Phase Lock Loop Power section in the *appropriate platform design guide* for the recommended filter specifications.

2.4 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. The fluctuations can cause voltages on power planes to sag below their nominal values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 6. Failure to do so can result in timing violations (in the event of a voltage sag) or a reduced lifetime of the component (in the event of a voltage overshoot). **Unlike SC242 based designs, motherboards utilizing the PGA370 socket must provide high frequency decoupling capacitors on all power planes for the processor.**

2.4.1 Processor VCC_{CORE} Decoupling

The regulator for the VCC_{CORE} input must be capable of delivering the $dICC_{CORE}/dt$ (defined in Table 6) while maintaining the required tolerances (also defined in Table 6). Failure to meet these specifications can result in timing violations (during VCC_{CORE} sag) or a reduced lifetime of the component (during VCC_{CORE} overshoot).

2.4.2 Processor System Bus AGTL+ Decoupling

The processor requires both high frequency and bulk decoupling on the system motherboard for proper AGTL+ bus operation. See the AGTL+ buffer specification in the *Intel® Pentium® II Processor Developer's Manual* for more information. Also, refer to the appropriate platform design guide for recommended capacitor component placement.

2.5 Processor System Bus Clock and Processor Clocking

The BCLK input directly controls the operating speed of the system bus interface. All AGTL+ system bus timing parameters are specified with respect to the rising edge of the BCLK input. See the *P6 Family of Processors Hardware Developer's Manual* for further details.

2.6 Voltage Identification

There are four voltage identification pins on the PGA370 socket. These pins can be used to support automatic selection of $V_{CC_{CORE}}$ voltages. These pins are not signals, but are either an open circuit or a short circuit to ground (V_{SS}) on the processor. The combination of opens and shorts defines the voltage required by the processor core. The VID pins are needed to cleanly support voltage specification variations on current and future processors. VID[3:0] are defined in Table 2. A '1' in this table refers to an open pin and a '0' refers to a short to ground. The voltage regulator or VRM must supply the voltage that is requested or disable itself.

To ensure a system is ready for current and future processors, the range of values in **bold** in Table 2 should be supported. A smaller range will risk the ability of the system to migrate to a higher performance processor and/or maintain compatibility with current processors.

Table 2. Voltage Identification Definition [1, 2]

VID3	VID2	VID1	VID0	$V_{CC_{CORE}}$
1	1	1	1	**1.30**
1	1	1	0	**1.35**
1	1	0	1	**1.40**
1	1	0	0	**1.45**
1	0	1	1	**1.50**
1	0	1	0	**1.55**
1	0	0	1	**1.60**[3]
1	0	0	0	**1.65**[3]
1	0	1	1	**1.70**[3]
0	1	1	0	**1.75**[3]
0	1	0	1	**1.80**[3]
0	1	0	0	**1.85**[3]
0	0	1	1	**1.90**[3]
0	0	1	0	**1.95**[3]
0	0	0	1	**2.00**[3]
0	0	0	0	**2.05**[3]
1	1	1	1	**No Core**

NOTES:
1. 0 = Processor pin connected to V_{SS}.
2. 1 = Open on processor; may be pulled up to TTL V_{IH} on baseboard.
3. To ensure a system is ready for the Intel® Pentium® III and Intel® Celeron™ processors, the values in **BOLD** in Table 2 should be supported.

Note that the '1111' (all opens) ID can be used to detect the absence of a processor core in a given socket as long as the power supply used does not affect these lines. Detection logic and pull-ups should not affect VID inputs at the power source (see Section 7.0).

The VID pins should be pulled up to a TTL-compatible level with external resistors to the power source of the regulator only if required by the regulator or external logic monitoring the VID[3:0] signals. The power source chosen must be guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the processor supply going above the specified VCC_{CORE} in the event of a failure in the supply for the VID lines. In the case of a DC-to-DC converter, this can be accomplished by using the input voltage to the converter for the VID line pull-ups. A resistor of greater than or equal to 10 kΩ may be used to connect the VID signals to the converter input. Note that no changes have been made to the physical connector or pin definitions between the Intel-enabled VRM 8.2 and VRM 8.4 specifications. Intel requires that designs utilize VRM 8.4 specifications to meet the Pentium III processor requirements.

2.7 Processor System Bus Unused Pins

All RESERVED pins must remain unconnected unless specifically noted. Connection of these pins to VCC_{CORE}, V_{REF}, V_{SS}, V_{TT}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 5.3 for a pin listing of the processor and the location of each RESERVED pin.

PICCLK must be driven with a valid clock input and the PICD[1:0] signals must be pulled-up to VCC_{CMOS} even when the APIC will not be used. A separate pull-up resistor must be provided for each PICD signal.

For reliable operation, always connect unused inputs or bidirectional signals to their deasserted signal level. The pull-up or pull-down resistor values are system dependent and should be chosen such that the logic high (V_{IH}) and logic low (V_{IL}) requirements are met. See Table 8 for DC specifications of non-AGTL+ signals.

Unused AGTL+ inputs must be properly terminated to V_{TT} on PGA370 socket motherboards which support the Intel Celeron and the Pentium III processors. For designs that intend to only support the Pentium III processor, unused AGTL+ inputs will be terminated by the processor's on-die termination resistors and thus do not need to be terminated on the motherboard. However, RESET# must always be terminated on the motherboard as the Pentium III processor for the PGA370 socket does not provide on-die termination of this AGTL+ input.

For unused CMOS inputs, active low signals should be connected through a pull-up resistor to VCC_{CMOS} and meet V_{IH} requirements. Unused active high CMOS inputs should be connected through a pull-down resistor to ground (V_{ss}) and meet V_{IL} requirements. Unused CMOS outputs can be left unconnected. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

2.8 Processor System Bus Signal Groups

To simplify the following discussion, the processor system bus signals have been combined into groups by buffer type. All P6 family processor system bus outputs are open drain and require a high-level source provided termination resistors. However, the Pentium III processor for the PGA370 socket includes on-die termination. **Motherboard designs which also support Intel Celeron processors in the PPGA package will need to provide AGTL+ termination on the system motherboard as well.**

AGTL+ input signals have differential input buffers which use V_{REF} as a reference signal. AGTL+ output signals require termination to 1.5 V. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

The PWRGOOD, BCLK, and PICCLK inputs can each be driven from ground to 2.5 V. Other CMOS inputs (A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SMI, SLP#, and STPCLK#) are only 1.5 V tolerant and must be pulled up to VCC_{CMOS}. The CMOS, APIC, and TAP outputs are open drain and must be pulled high to VCC_{CMOS}. This ensures correct operation for current Intel Pentium III and Intel Celeron™ processors.

The groups and the signals contained within each group are shown in Table 3. Refer to Section 7.0 for a description of these signals.

Table 3. System Bus Signal Groups [1]

Group Name	Signals
AGTL+ Input	BPRI#, DEFER#, RESET#[6], RS[2:0]#, RSP#, TRDY#
AGTL+ Output	PRDY#
AGTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#[2], D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
CMOS Input[3]	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, SLP#, SMI#, STPCLK#
CMOS Input[4]	PWRGOOD
CMOS Output[3]	FERR#, IERR#, THERMTRIP#
System Bus Clock[4]	BCLK
APIC Clock[4]	PICCLK
APIC I/O[3]	PICD[1:0]
TAP Input[3]	TCK, TDI, TMS, TRST#
TAP Output[3]	TDO
Power/Other[5]	BSEL[1:0], CLKREF, CPUPRES#, EDGCTRL, PLL[2:1], RESET2#, SLEWCTRL, THERMDN, THERMDP, RTTCTRL[7], $VCORE_{DET}$, VID[3:0], $VCC_{1.5}$, $VCC_{2.5}$, VCC_{CMOS}, VCC_{CORE}, V_{REF}, V_{SS}, V_{TT}, Reserved

NOTES:
1. See Section 7.0 for information on the these signals.
2. The BR0# pin is the only BREQ# signal that is bidirectional. See Section 7.0 for more information. The internal BREQ# signals are mapped onto the BR[1:0]# pins after the agent ID is determined.
3. These signals are specified for VCC_{CMOS} (1.5 V for the Pentium III processor) operation).
4. These signals are 2.5 V tolerant.
5. VCC_{CORE} is the power supply for the processor core and is described in Section 2.6.
   VID[3:0] is described in Section 2.6.
   V_{TT} is used to terminate the system bus and generate V_{REF} on the motherboard.
   V_{SS} is system ground.
   $VCC_{1.5}$, $VCC_{2.5}$, VCC_{CMOS} are described in Section 2.3.
   BSEL[1:0] is described in Section 2.8.2 and Section 7.0.
   All other signals are described in Section 7.0.
6. RESET# must always be terminated to V_{TT} on the motherboard, on-die termination is not provided for this signal.
7. This signal is used to control the value of the processor on-die termination resistance. Refer to the platform design guide for the recommended pulldown resistor value.

2.8.1 Asynchronous vs. Synchronous for System Bus Signals

All AGTL+ signals are synchronous to BCLK. All of the CMOS, Clock, APIC, and TAP signals can be applied asynchronously to BCLK.

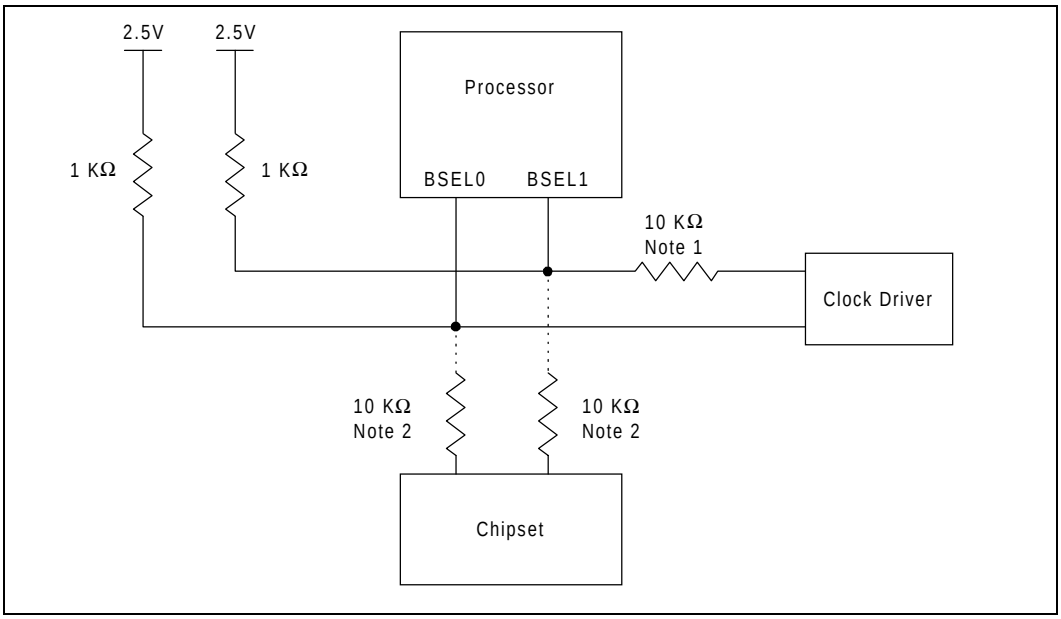
All APIC signals are synchronous to PICCLK. All TAP signals are synchronous to TCK.

2.8.2 System Bus Frequency Select Signals (BSEL[1:0])

These signals are used to select the system bus frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All system bus agents must operate at the same frequency. **Currently available Pentium lll processors for the PGA370 socket operate at 100 MHz system bus frequency only.** Individual processors will only operate at their specified front side bus (FSB) frequency.

The BSEL0 signal will float from the processor and should be pulled up to a logic high by a resistor located on the motherboard. The BSEL0 signal can be incorporated into RESET# logic on the motherboard if 66 MHz operation is unsupported, as demonstrated in Figure 5. Refer to the appropriate clock synthesizer design guidelines and platform design guide for more details on the bus frequency select signals.

Figure 5. BSEL[1:0] Example for a 100 MHz System Design



NOTES:
1. Some clock drivers may require a series resistor on their BSEL1 input.
2. Some chipsets may connect to the BSEL[1:0] signals and require a series resistor. See the appropriate platform design guide for implementation details.

Table 4. Frequency Select Truth Table for BSEL[1:0]

BSEL1	BSEL0	Frequency
0	0	66 MHz (unsupported)
0	1	100 MHz
1	0	Reserved
1	1	Reserved

2.9 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor be the first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect the rest of the chain unless one of the other components is capable of accepting a 1.5V input. Similar considerations must be made for TCK, TMS, and TRST# signals.

2.10 Maximum Ratings

Table 5 contains processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables in Section 2.11 through Section 2.13. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	–40	85	°C	
$V_{CC_{CORE}}$ and V_{TT}	Processor core voltage and termination supply voltage with respect to V_{SS}	–0.5	2.1	V	
$V_{in_{AGTL}}$	AGTL+ buffer input voltage	V_{TT} - 2.18	2.18	V	1, 2
$V_{in_{CMOS}1.5}$	CMOS buffer DC input voltage with respect to V_{SS}	V_{TT} - 2.18	2.18	V	1, 2, 3
$V_{in_{CMOS}2.5}$	CMOS buffer DC input voltage with respect to V_{SS}	-0.58	3.18	V	4
I_{VID}	Max VID pin current		5	mA	
$I_{CPUPRES\#}$	Max CPUPRES# pin current		5	mA	

NOTES:
1. Input voltage can never exceed V_{SS} + 2.18 volts.
2. Input voltage can never go below V_{TT} - 2.18 volts.
3. Parameter applies to CMOS (except BCLK, PICCLK, and PWRGOOD), APIC, and TAP bus signal groups only.
4. Parameter applies to CMOS signals BCLK, PICCLK, and PWRGOOD only.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the PGA370 socket pins (bottom side of the motherboard). See Section 7.0 for the processor signal descriptions and Section 5.3 for the signal listings.

Most of the signals on the processor system bus are in the AGTL+ signal group. These signals are specified to be terminated to 1.5V. The DC specifications for these signals are listed in Table 7 on page 24.

To allow connection with other devices, the clock, CMOS, APIC, and TAP signals are designed to interface at non-AGTL+ levels. The DC specifications for these pins are listed in Table 8 on page 24.

Table 6 through Table 9 list the DC specifications for the Pentium III processor for the PGA370 socket. Specifications are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 6. Voltage and Current Specifications [1, 2] (Sheet 1 of 2)

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
$V_{CC_{CORE}}$	V_{CC} for processor core	500E MHz 550E MHz		1.60 1.60		V V	3, 4 3, 4
V_{TT}, $V_{CC_{1.5}}$	Static AGTL+ bus termination voltage		1.455	1.50	1.545	V	1.5 ±3% [5, 16]
V_{TT}, $V_{CC_{1.5}}$	Transient AGTL+ bus termination voltage		1.365	1.50	1.635	V	1.5 ±9% [5]
V_{REF}	AGTL+ input reference voltage		-2%	2/3 V_{TT}	+2%	V	±2%, 7
V_{CLKREF}	CLKREF input reference voltage		1.169	1.25	1.331	V	±6.5%, 15
Baseboard $V_{CC_{CORE}}$ Tolerance, Static	Processor core voltage static tolerance level at the PGA370 socket pins		–0.080		0.040	V	6
Baseboard $V_{CC_{CORE}}$ Tolerance, Transient	Processor core voltage transient tolerance level at the PGA370 socket pins		–0.130		0.080	V	6
$I_{CC_{CORE}}$	I_{CC} for processor core	500E MHz 550E MHz			11.0 11.0	A A	3, 8, 9 3, 8, 9
$I_{CC_{CMOS}}$	I_{CC} for $V_{CC_{CMOS}}$				250	mA	
I_{CLKREF}	CLKREF voltage supply current				60	µA	
$I_{V_{TT}}$	Termination voltage supply current				2.7	A	10
I_{SGnt}	I_{CC} Stop-Grant for processor core				2.5	A	8, 11
I_{SLP}	I_{CC} Sleep for processor core				2.5	A	8
I_{DSLP}	I_{CC} Deep Sleep for processor core				2.2	A	

Table 6. Voltage and Current Specifications [1, 2] (Sheet 2 of 2)

Symbol	Parameter	Core Freq	Min	Typ	Max	Unit	Notes
$dICC_{CORE}/dt$	Power supply current slew rate				240	A/µs	12, 13, 14
dI_{VTT}/dt	Termination current slew rate				8	A/µs	12, 13, See Table 9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All specifications in this table apply only to the Pentium III processor for the PGA370 socket. For motherboard compatibility with the Intel Celeron processor, see the *Intel® Celeron™ Processor Datasheet*.
3. Vcc_{CORE} and Icc_{CORE} supply the processor core and the on-die L2 cache.
4. Use the “typical voltage” specification with the “tolerance specifications” to provide correct voltage regulation to the processor.
5. V_{TT} and $Vcc_{1.5}$ must be held to 1.5V ±9% while the AGTL+ bus is active. It is required that V_{TT} and $Vcc_{1.5}$ be held to 1.5V ±3% while the processor system bus is static (idle condition). ±3% is the required design target; ±9% will come from the transient noise added. This is measured at the PGA370 socket pins on the bottom side of the baseboard.
6. These are the tolerance requirements, across a 20 MHz frequency bandwidth, measured at the processor socket pin on the soldered-side of the motherboard. VCC_{CORE} must return to within the static voltage specification within 100 ms after a transient event; see the VRM 8.4 DC-DC Converter Design Guidelines for further details.
7. V_{REF} should be generated from V_{TT} by a voltage divider of 1% resistors or 1% matched resistors. Refer to the Intel® *Pentium® II Processor Developer’s Manual* for more details on V_{REF}.
8. Max I_{CC} measurements are measured at V_{CC} typical voltage, maximum temperature, under a maximum signal loading conditions. The Max Icc currents specified do not occur simultaneously under the stress measurement condition.
9. Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} (Vcc_{CORE_TYP}). In this case, the maximum current level for the regulator, Icc_{CORE_REG}, can be reduced from the specified maximum current Icc_{CORE_MAX} and is calculated by the equation:

$$Icc_{CORE\_REG} = Icc_{CORE\_MAX} \times (Vcc_{CORE\_TYP} - Vcc_{CORE\_STATIC\_TOLERANCE}) / Vcc_{CORE\_TYP}$$

10. The current specified is the current required for a single processor. A similar amount of current is drawn through the termination resistors on the opposite end of the AGTL+ bus, unless single-ended termination is used (see Section 2.1).
11. The current specified is also for AutoHALT state.
12. Maximum values are specified by design/characterization at nominal Vcc_{CORE}.
13. Based on simulation and averaged over the duration of any change in current. Use to compute the maximum inductance tolerable and reaction time of the voltage regulator. This parameter is not tested.
14. dI_{CC}/dt specifications are measured and specified at the PGA370 socket pins.
15. CLKREF must be held to 1.25V ±6.5%. This tolerance accounts for a ±5% power supply and ±1% resistor divider tolerance. It is recommended that the motherboard generate the CLKREF reference from either the 2.5V or 3.3V supply. V_{TT} should not be used due to risk of AGTL+ switching noise coupling to this analog reference.
16. Static voltage regulation includes: DC output initial voltage set point adjust, Output ripple and noise, Output load ranges specified in the tables above.

Table 7. AGTL+ Signal Groups DC Specifications [1,]

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	–0.150	V_{REF} - 0.200	V	6
V_{IH}	Input High Voltage	V_{REF} + 0.200	V_{TT}	V	2, 3, 6
Ron	Buffer On Resistance		16.67	Ω	5
I_L	Leakage Current for inputs, outputs, and I/O		±100	µA	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. All inputs, outputs, and I/O pins must comply with the signal quality specifications in Section 3.0.
3. Minimum and maximum V_{TT} are given in Table 9 on page 25.
4. ($0 \le V_{IN} \le 1.5$ V +3%).
5. Refer to the processor I/O Buffer Models for I/V characteristics.
6. Steady state input voltage must not be above V_{SS} + 1.65V or below V_{TT} - 1.65V.

Table 8. Non-AGTL+ Signal Group DC Specifications [1]

Symbol	Parameter	Min	Max	Unit	Notes
$V_{IL_{1.5}}$	Input Low Voltage	–0.150	V_{REF} - 0.200	V	9
$V_{IL_{2.5}}$	Input Low Voltage	-0.58	0.700	V	5, 8
$V_{IH_{1.5}}$	Input High Voltage	V_{REF} + 0.200	V_{TT}	V	6, 9
$V_{IH_{2.5}}$	Input High Voltage	2.000	3.18	V	5, 8
V_{OL}	Output Low Voltage		0.400	V	2
V_{OH}	Output High Voltage		V_{TT}	V	7, 9, All outputs are open-drain
I_{OL}	Output Low Current	9		mA	10
I_{LI}	Input Leakage Current		±100	µA	3, 6
I_{LO}	Output Leakage Current		±100	µA	4, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentum III processors at all frequencies.
2. Parameter measured at 9 mA (for use with TTL inputs).
3. ($0 \le V_{IN} \le 2.5$V +5%).
4. ($0 \le V_{OUT} \le 2.5$V +5%).
5. For BCLK specifications, refer to Table 17 on page 33.
6. ($0 \le V_{IN} \le 1.5$V +3%).
7. ($0 \le V_{OUT} \le 1.5$V +3%).
8. Applies to non-AGTL+ signals BCLK, PICCLK, and PWRGOOD.
9. Applies to non-AGTL+ signals **except** BCLK, PICCLK, and PWRGOOD.
10. These values are specified at the processor pins.

2.12 AGTL+ System Bus Specifications

It is recommended that the AGTL+ bus be routed in a daisy-chain fashion with termination resistors to V_{TT}. These termination resistors are placed electrically between the ends of the signal traces and the V_{TT} voltage supply and generally are chosen to approximate the system platform impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Refer to the appropriate platform design guide for more information

Table 9 below lists the nominal specification for the AGTL+ termination voltage (V_{TT}). The AGTL+ reference voltage (V_{REF}) is generated on the system motherboard and should be set to 2/3 V_{TT} for the processor and other AGTL+ logic. It is important that the baseboard impedance be specified and held to a ±15% tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on the AGTL+ buffer specification, see the *Intel® Pentium® II Processor Developer's Manual* and AP-585, *Intel® Pentium® II Processor AGTL+ Guidelines*.

Table 9. Processor AGTL+ Bus Specifications [1, 2]

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{TT}	Bus Termination Voltage		1.50		V	3
On-die R_{TT}	Termination Resistor	40		130	Ω	4
V_{REF}	Bus Reference Voltage	0.950	2/3 V_{TT}	1.05	V	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. Pentium III processors for the PGA370 socket contain AGTL+ termination resistors on the processor die, except for the RESET# input.
3. V_{TT} and $Vcc_{1.5}$ must be held to 1.5V ±9%. It is required that V_{TT} and $Vcc_{1.5}$ be held to 1.5V ±3% while the processor system bus is idle (static condition). This is measured at the PGA370 socket pins on the bottom side of the baseboard.
4. The value of the on-die R_{TT} is determined by the resistor value measured by the RTTCTRL signal pin. The on-die R_{TT} tolerance is ±15% based on the RTTCTRL resistor pulldown of ±1%. See Section 7.0 for more details on the RTTCTRL signal. Refer to the recommendation guidelines for the specific chipset/processor combination.
5. V_{REF} is generated on the motherboard and should be 2/3 V_{TT} ±2% nominally. Insure that there is adequate V_{REF} decoupling on the motherboard.

2.13 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the socket pins on the bottom of the motherboard. Unless otherwise specified, timings are tested at the processor pins during manufacturing. Timings at the processor pins are specified by design characterization. See Section 7.0 for the processor signal definitions.

Table 10 through Table 16 list the AC specifications associated with the processor system bus. These specifications are broken into the following categories: Table 10 contains the system bus clock specifications, Table 12 contains the AGTL+ specifications, Table 13 contains the CMOS signal group specifications, Table 14 contains timings for the reset conditions, Table 15 and covers APIC bus timing, and Table 16 covers TAP timing.

All processor system bus AC specifications for the AGTL+ signal group are relative to the rising edge of the BCLK input. All AGTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium III processor in the FC-PGA package in Viewlogic* XTK/XNS* model format (formerly known as QUAD format) as the *Pentium III Processor for the PGA370 Socket I/O Buffer Models, XTK/XNS Format* (Electronic Format). An electronic copy of the I/O Buffer Model for the AGTL+ and CMOS signals is available at Intel's Developer's Website (http://developer.intel.com). The model is for use in single processor designs and assumes the presence of motherboard R_{TT} values as described in Table 9 on page 25.

AGTL+ layout guidelines are also available in the appropriate platform design guide.

Care should be taken to read all notes associated with a particular timing parameter.

Table 10. System Bus AC Specifications (Clock)[1, 2, 3]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
System Bus Frequency		100.00		MHz		4
T1: BCLK Period	10.0			ns	6	4, 5, 10
T2: BCLK Period Stability			±250	ps		6, 7, 10
T3: BCLK High Time	2.5			ns	6, 12	9, 10
T4: BCLK Low Time	2.4			ns	6, 12	9, 10
T5: BCLK Rise Time	0.4		1.6	ns	6, 12	8, 11
T6: BCLK Fall Time	0.4		1.6	ns	6, 12	8, 11

1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00V at the processor pins.
3. N/A
4. The internal core clock frequency is derived from the processor system bus clock. The system bus clock to core clock ratio is determined during initialization. Individual processors will only operate at their specified system bus frequency. Table 11 shows the supported ratios for each processor.
5. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the appropriate clock synthesizer/driver specification for details.
6. Due to the difficulty of accurately measuring clock jitter in a system, it is recommended that a clock driver be used that is designed to meet the period stability specification into a test load of 10 to 20 pF. This should be measured on the **rising edges of adjacent BCLKs crossing 1.25V at the processor pin**. The jitter present must be accounted for as a component of BCLK timing skew between devices.
7. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The –20 dB attenuation point, as measured into a 10 to 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the appropriate clock synthesizer/driver specification for details
8. BCLK Rise time is measure between 0.5V–2.0V. BCLK fall time is measured between 2.0V–0.5V.
9. BCLK high time is measured as the period of time above 2.0V. BCLK low time is measured as the period of time below 0.5V
10. This specification applies to Pentium III processors operating at a system bus frequency of 100 MHz.
11. Not 100% tested. Specified by design characterization as a clock driver requirement.

Table 11. Valid System Bus to Core Frequency Ratios [1, 2, 3]

Processor	Core Frequency (MHz)	BCLK Frequency (MHz)	Frequency Multiplier	L2 Cache (MHz)
500E	500	100	5	500
550E	550	100	11/2	550

NOTE:
1. Contact your local Intel representative for the latest information on processor frequencies and/or frequency multipliers.
2. While other bus ratios are defined, operation at frequencies other than those listed are not supported by the Pentium III processor.
3. Individual processors will only operate at their specified system bus frequency.

Table 12. System Bus AC Specifications (AGTL+ Signal Group)[1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T7: AGTL+ Output Valid Delay	0.20	3.25	ns	7	4, 10
T8: AGTL+ Input Setup Time	1.20		ns	8	5, 6, 7, 10
T9: AGTL+ Input Hold Time	1.00		ns	8	8, 10
T10: RESET# Pulse Width	1.00		ms	9	6, 9, 10

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the AGTL+ signals are referenced to the BCLK rising edge at 1.25V at the processor pin. All AGTL+ signal timings (compatibility signals, etc.) are referenced at 1.00V at the processor pins.
4. Valid delay timings for these signals are specified into 50Ω to 1.5V, V_{REF} at 1.0 V ±2% and with 56Ω on-die R_{TT}.
5. A minimum of 3 clocks must be guaranteed between two active-to-inactive transitions of TRDY#.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously. For 2-way MP systems, RESET# should be synchronous.
7. Specification is for a minimum 0.40 V swing from V_{REF} - 200 mV to V_{REF} + 200 mV. This assumes an edge rate of 0.3V/ns.
8. Specification is for a maximum 1.0 V swing from V_{TT} - 1V to V_{TT}. This assumes an edge rate of 3V/ns.
9. This should be measured after $V_{CC_{CORE}}$, V_{TT}, $V_{CC_{CMOS}}$, and BCLK become stable.
10. This specification applies to the Pentium III processor running at 100 MHz system bus frequency

Table 13. System Bus AC Specifications (CMOS Signal Group) [1, 2, 3, 4]

T# Parameter	Min	Max	Unit	Figure	Notes
T14: CMOS Input Pulse Width, except PWRGOOD	2		BCLKs	6	Active and Inactive states
T15: PWRGOOD Inactive Pulse Width	10		BCLKs	6, 10	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies
2. These specifications are tested during manufacturing.
3. These signals may be driven asynchronously.
4. All CMOS outputs shall be asserted for at least 2 BCLKs.
5. When driven inactive or after $V_{CC_{CORE}}$, V_{TT}, $V_{CC_{CMOS}}$, and BCLK become stable.

Table 14. System Bus AC Specifications (Reset Conditions) [1]

T# Parameter	Min	Max	Unit	Figure	Notes
T16: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Setup Time	4		BCLKs	9	Before deassertion of RESET#
T17: Reset Configuration Signals (A[14:5]#, BR0#, INIT#) Hold Time	2	20	BCLKs	9	After clock that deasserts RESET#
T18: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Setup Time					2
T19: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Delay Time					2
T20: Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]) Hold Time					2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. This parameter does not apply to the Pentium III processor. The Pentium III processor does not sample these signals at RESET# to determine the multiplier ratio as some previous Intel processors have done. The multiplier ratio is set during manufacturing for each processor and cannot be changed. The multiplier ratios are defined in Table 11.

Table 15. System Bus AC Specifications (APIC Clock and APIC I/O)[1, 2, 3]

T# Parameter	Min	Max	Unit	Figure	Notes
T21: PICCLK Frequency	2.0	33.3	MHz		
T22: PICCLK Period	30.0	500.0	ns	6	
T23: PICCLK High Time	10.5		ns	6	@ > 1.7V
T24: PICCLK Low Time	10.5		ns	6	@ < 0.7V
T25: PICCLK Rise Time	0.25	3.0	ns	6	(0.7V - 1.7V)
T26: PICCLK Fall Time	0.25	3.0	ns	6	(1.7V - 0.7V)
T27: PICD[1:0] Setup Time	5.0		ns	8	4
T28: PICD[1:0] Hold Time	2.5		ns	8	4
T29a: PICD[1:0] Valid Delay (Rising Edge)	1.5	8.7	ns	6, 7	4, 5, 6
T29b: PICD[1:0] Valid Delay (Falling Edge)	1.5	12.0	ns	6, 7	4, 5, 6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to Pentium III processors at all frequencies.
2. These specifications are tested during manufacturing.
3. All AC timings for the APIC I/O signals are referenced to the PICCLK rising edge at 1.25 V at the processor pins. All APIC I/O signal timings are referenced at 0.75 V at the processor pins.
4. Referenced to PICCLK rising edge.
5. For open drain signals, valid delay is synonymous with float delay.
6. Valid delay timings for these signals are specified into 150Ω load pulled up to 1.5 V.

Table 16. System Bus AC Specifications (TAP Connection)[1, 2, 3]

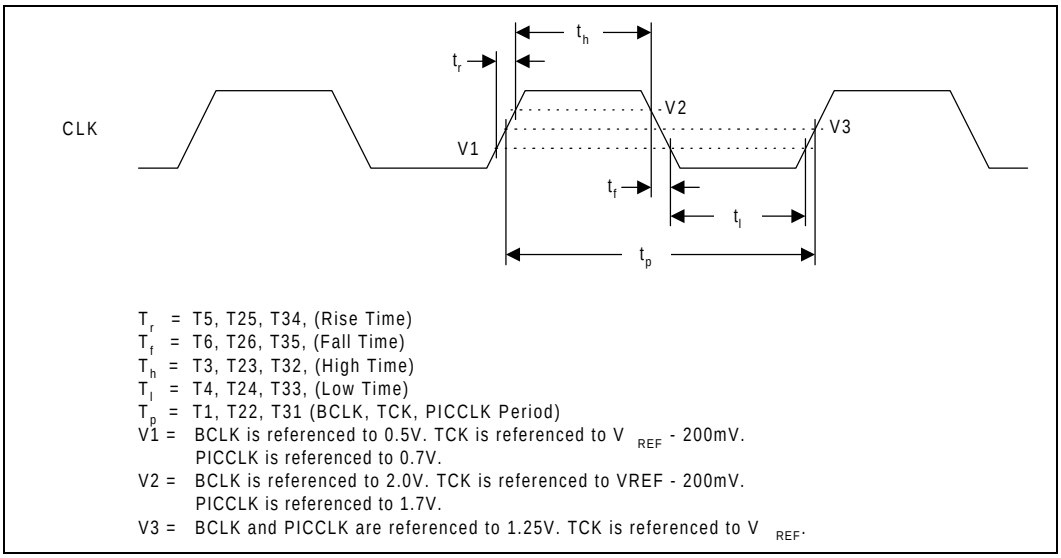
T# Parameter	Min	Max	Unit	Figure	Notes
T30: TCK Frequency		16.667	MHz		
T31: TCK Period	60.0		ns	6	
T32: TCK High Time	25.0		ns	6	V_{REF} + 0.200V, [10]
T33: TCK Low Time	25.0		ns	6	V_{REF} - 0.200V, [10]
T34: TCK Rise Time		5.0	ns	6	(V_{REF} - 0.200V) - (V_{REF} + 0.200V), [4, 10]
T35: TCK Fall Time		5.0	ns	6	(V_{REF} + 0.200V) - (V_{REF} - 0.200V), [4, 10]
T36: TRST# Pulse Width	40.0		ns	12	Asynchronous, [10]
T37: TDI, TMS Setup Time	5.0		ns	11	5
T38: TDI, TMS Hold Time	14.0		ns	11	5
T39: TDO Valid Delay	1.0	10.0	ns	11	6, 7
T40: TDO Float Delay		25.0	ns	11	6, 7, 10
T41: All Non-Test Outputs Valid Delay	2.0	25.0	ns	11	6, 8, 9
T42: All Non-Test Inputs Setup Time		25.0	ns	11	6, 8, 9, 10
T43: All Non-Test Inputs Setup Time	5.0		ns	11	5, 8, 9
T44: All Non-Test Inputs Hold Time	13.0		ns	11	5, 8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processors frequencies.
2. All AC timings for the TAP signals are referenced to the TCK rising edge at 0.75 V at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.75 V at the processor pins.
3. These specifications are tested during manufacturing, unless otherwise noted.
4. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16.667 MHz.
5. Referenced to TCK rising edge.
6. Referenced to TCK falling edge.
7. Valid delay timing for this signal is specified to 1.5 V.
8. Non-Test Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to TAP operations.
9. During Debug Port operation, use the normal specified timings rather than the TAP signal timings.
10. Not 100% tested. Specified by design characterization.

Note: For Figure 6 through Figure 12, the following apply:

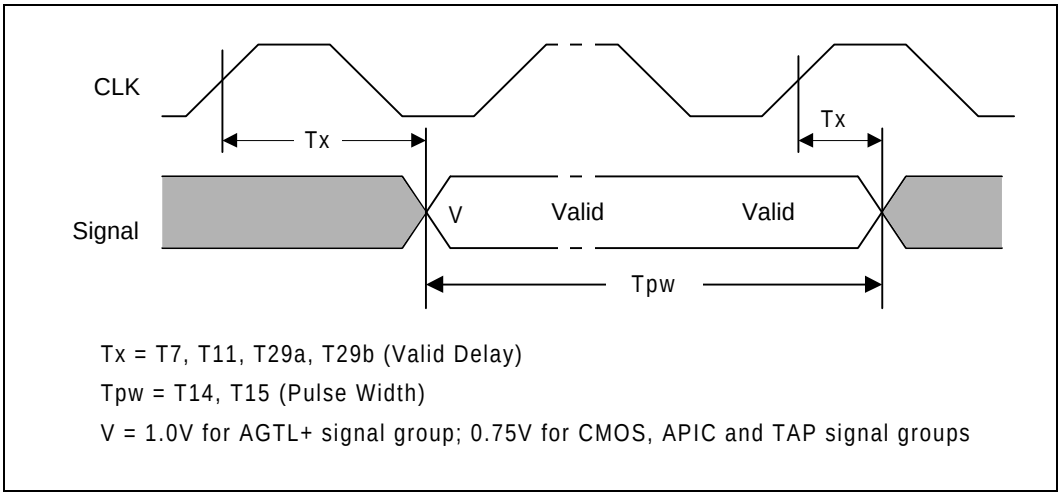
1. Figure 6 through Figure 12 are to be used in conjunction with Table 10 through Table 16.
2. All AC timings for the AGTL+ signals at the processor pins are referenced to the BCLK rising edge at 1.25 V. All AGTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor pins.
3. All AC timings for the APIC I/O signals at the processor pins are referenced to the PICCLK rising edge at 1.25 V. All APIC I/O signal timings are referenced at 0.75 V at the processor pins.
4. All AC timings for the TAP signals at the processor pins are referenced to the TCK rising edge at 0.75 V. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.75 V at the processor pins.

Figure 6. BCLK, PICCLK, and TCK Generic Clock Waveform



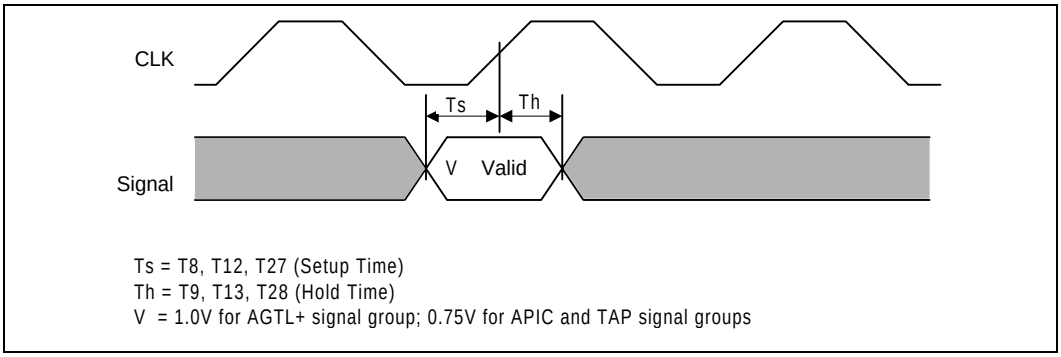
T_r = T5, T25, T34, (Rise Time)
T_f = T6, T26, T35, (Fall Time)
T_h = T3, T23, T32, (High Time)
T_l = T4, T24, T33, (Low Time)
T_p = T1, T22, T31 (BCLK, TCK, PICCLK Period)
V1 = BCLK is referenced to 0.5V. TCK is referenced to V_{REF} - 200mV. PICCLK is referenced to 0.7V.
V2 = BCLK is referenced to 2.0V. TCK is referenced to VREF - 200mV. PICCLK is referenced to 1.7V.
V3 = BCLK and PICCLK are referenced to 1.25V. TCK is referenced to V_{REF}.

Figure 7. System Bus Valid Delay Timings



Tx = T7, T11, T29a, T29b (Valid Delay)
Tpw = T14, T15 (Pulse Width)
V = 1.0V for AGTL+ signal group; 0.75V for CMOS, APIC and TAP signal groups

Figure 8. System Bus Setup and Hold Timings



Ts = T8, T12, T27 (Setup Time)
Th = T9, T13, T28 (Hold Time)
V = 1.0V for AGTL+ signal group; 0.75V for APIC and TAP signal groups

Figure 9. System Bus Reset and Configuration Timings

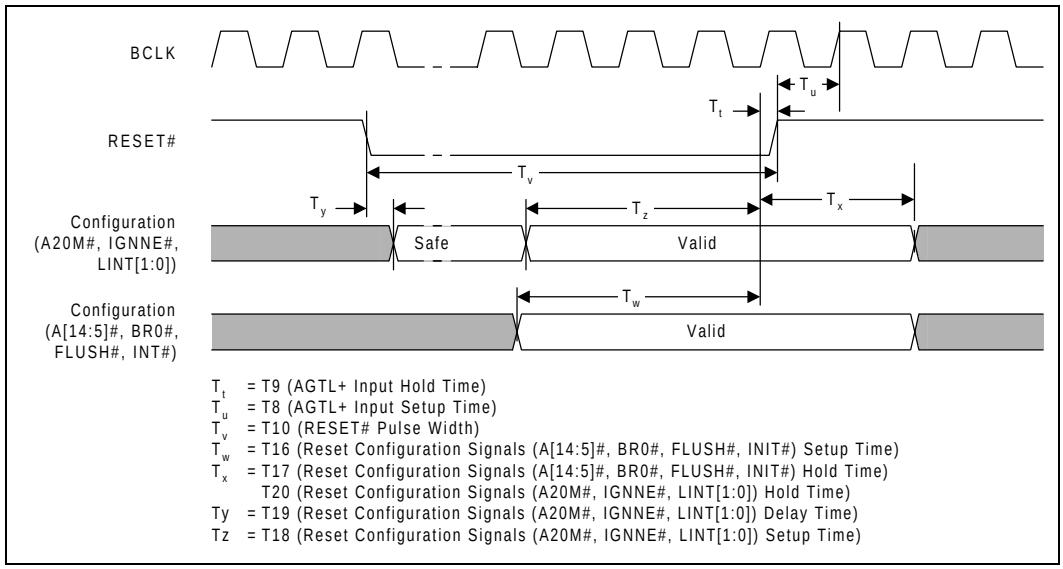


Figure 10. Power-On Reset and Configuration Timings

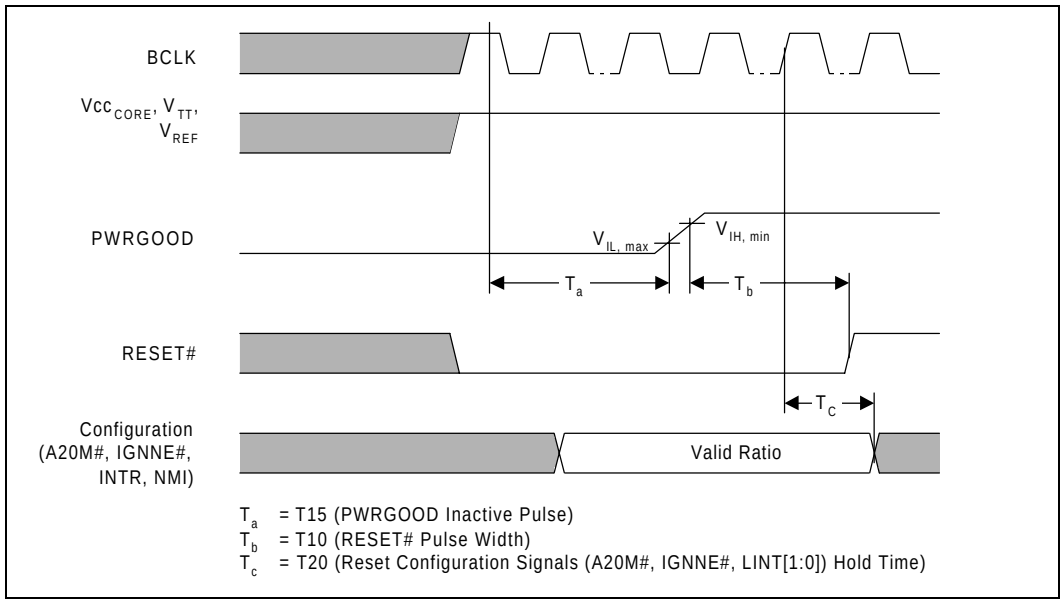
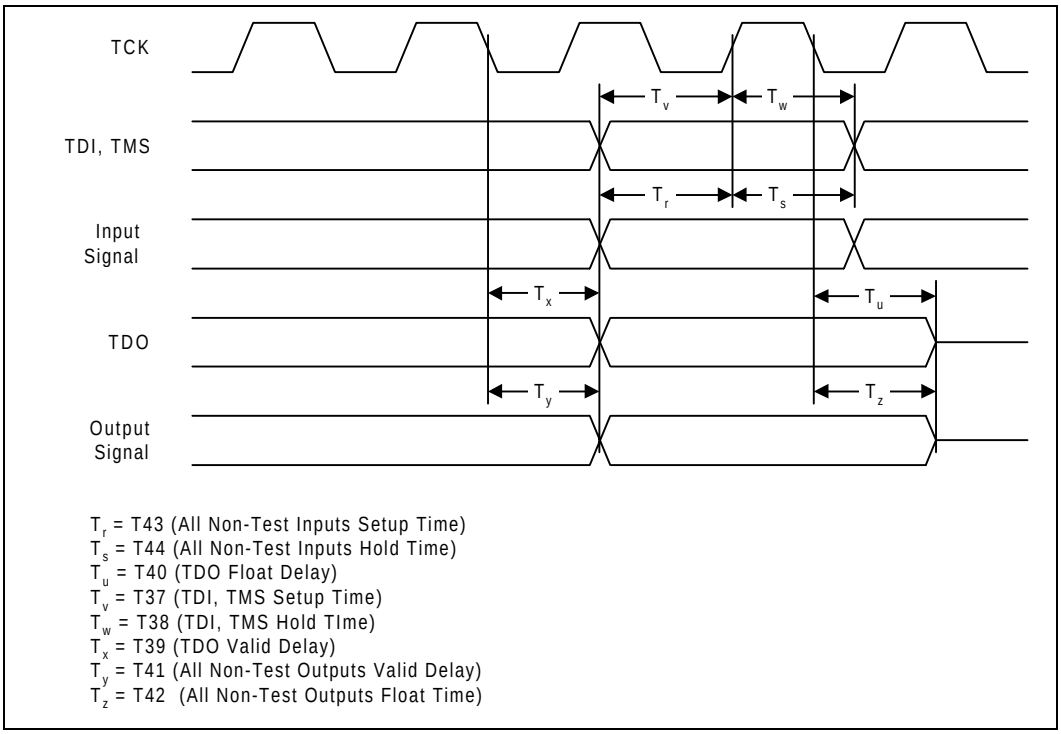
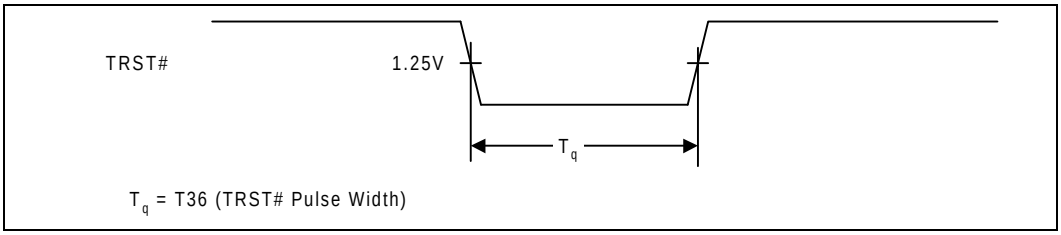


Figure 11. Test Timings (TAP Connection)



T_r = T43 (All Non-Test Inputs Setup Time)
T_s = T44 (All Non-Test Inputs Hold Time)
T_u = T40 (TDO Float Delay)
T_v = T37 (TDI, TMS Setup Time)
T_w = T38 (TDI, TMS Hold TIme)
T_x = T39 (TDO Valid Delay)
T_y = T41 (All Non-Test Outputs Valid Delay)
T_z = T42 (All Non-Test Outputs Float Time)

Figure 12. Test Reset Timings



T_q = T36 (TRST# Pulse Width)

3.0 Signal Quality Specifications

Signals driven on the processor system bus should meet signal quality specifications to ensure that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. Specifications are provided for simulation at the processor pins. Meeting the specifications at the processor pins in Table 17, Table 18, and Table 22 ensures that signal quality effects will not adversely affect processor operation.

3.1 BCLK and PICCLK Signal Quality Specifications and Measurement Guidelines

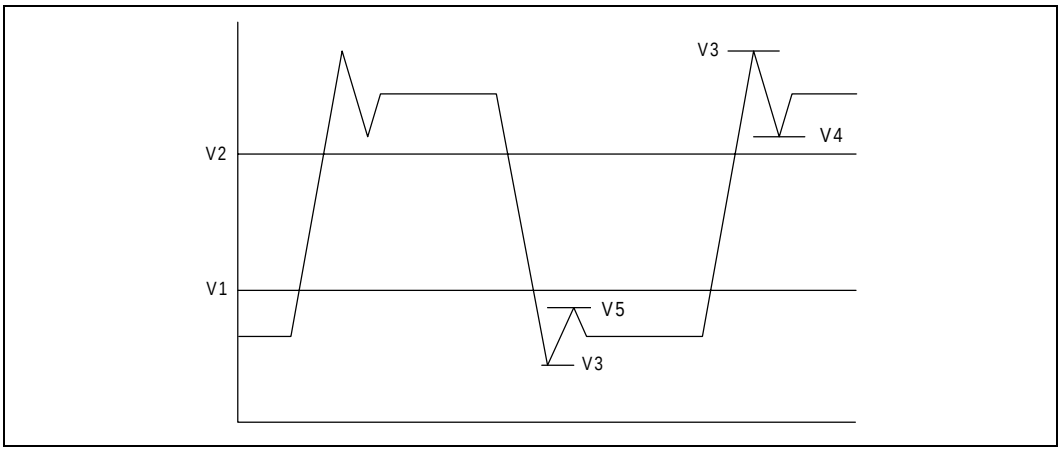
Table 17 describes the signal quality specifications at the processor pins for the processor system bus clock (BCLK) and APIC clock (PICCLK) signals. Figure 13 describes the signal quality waveform for the system bus clock at the processor pins.

Table 17. BCLK/PICCLK Signal Quality Specifications for Simulation at the Processor Pins [1]

T# Parameter	Min	Nom	Max	Unit	Figure	Notes
V1: BCLK V_{IL}			0.500	V	13	
V1: PICCLK V_{IL}			0.700	V	13	
V2: BCLK V_{IH}	2.000			V	13	
V2 PICCLK V_{IH}	2.000			V	13	
V3: V_{IN} Absolute Voltage Range	–0.58		3.18	V	13	
V4: BCLK Rising Edge Ringback	2.000			V	13	2
V4: PICCLK Rising Edge Ringback	2.000			V	13	2
V5: BCLK Falling Edge Ringback			0.500	V	13	2
V5: PICCLK Falling Edge Ringback			0.700	V	13	2

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processors frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK/PICCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 13. BCLK, PICCLK Generic Clock Waveform at the Processor Pins



3.2 AGTL+ Signal Quality Specifications and Measurement Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in the appropriate platform design guide. Refer to the *Intel® Pentium® II Processor Developer's Manual* (Order Number 243502) for the AGTL+ buffer specification.

Table 18 provides the AGTL+ signal quality specifications for the processor for use in simulating signal quality at the processor pins.

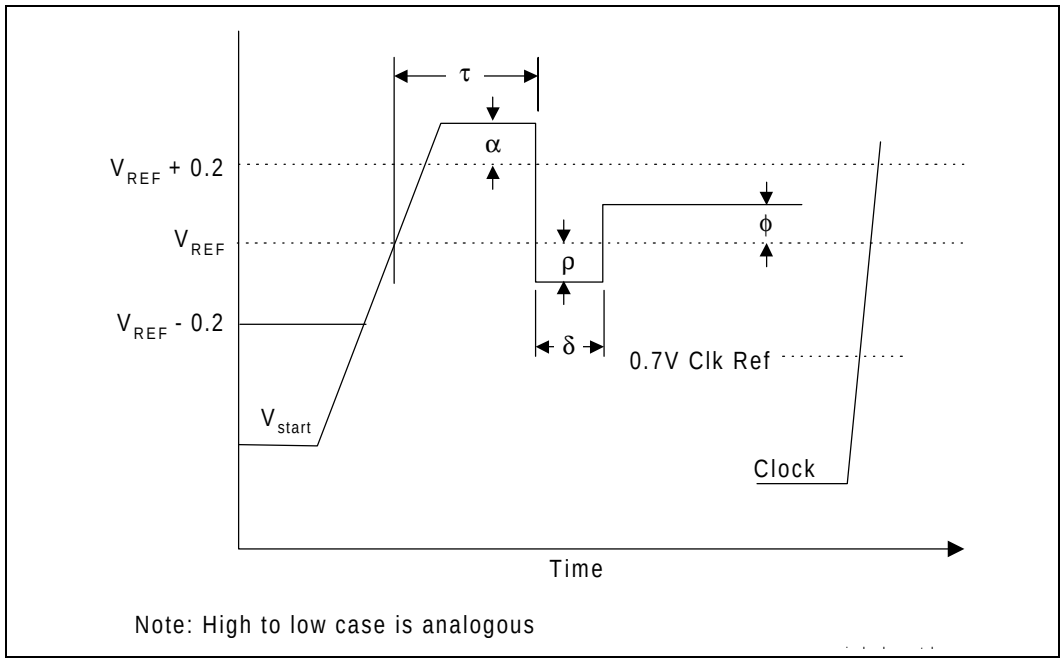
The Pentium III processor for the PGA370 socket maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 20 through Table 21. Figure 14 shows the AGTL+ ringback tolerance and Figure 15 shows the overshoot/undershoot waveform.

Table 18. AGTL+ Signal Groups Ringback Tolerance Specifications at the Processor Pins [1, 2, 3]

T# Parameter	Min	Unit	Figure	Notes
α: Overshoot	100	mV	14	4, 8
τ: Minimum Time at High	0.50	ns	14	
ρ: Amplitude of Ringback	–200	mV	14	5, 6, 7, 8
ϕ: Final Settling Voltage	200	mV	14	8
δ: Duration of Squarewave Ringback	N/A	ns	14	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processors frequencies.
2. Specifications are for the edge rate of 0.3 - 0.8V/ns. See Figure 14 for the generic waveform.
3. All values specified by design characterization.
4. See Table 22 for maximum allowable overshoot.
5. Ringback between V_{REF} + 100 mV and V_{REF} + 200 mV or V_{REF} - 200 mV and V_{REF} - 100 mVs requires the flight time measurements to be adjusted as described in the Intel AGTL+ Specifications (*Intel® Pentium® II Developers Manual*). Ringback below V_{REF} + 100 mV or above V_{REF} - 100 mV is not supported.
6. Intel recommends simulations not exceed a ringback value of V_{REF} ±200 mV to allow margin for other sources of system noise.
7. A negative value for ρ indicates that the amplitude of ringback is above V_{REF}. (i.e., ϕ = -100 mV specifies the signal cannot ringback below V_{REF} + 100 mV).
8. ϕ and ρ: are measured relative to V_{REF}. α: is measured relative to V_{REF} + 200 mV.

Figure 14. Low to High AGTL+ Receiver Ringback Tolerance



3.3 AGTL+ Signal Quality Specifications and Measurement Guidelines

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and overshoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the Pentium III processor performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.3.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level, V_{ss} (overshoot) and V_{TT} (undershoot). While overshoot can be measured relative to V_{ss} using one probe (probe to signal and GND lead to V_{ss}), undershoot must be measured relative to V_{TT}. This could be acomplished by simultaneously measuring the V_{TT} plane while measuring the signal undershoot. Today's oscilloscopes can easily calculate the true undershoot waveform. The true undershoot waveform can also be obtained with the following oscilloscope data file analysis:

$$\text{Converted Undershoot Waveform} = V_{TT} - \text{Signal\_measured}$$

Note: The converted undershoot waveform appears as a positive (overshoot) signal.

Note: Overshoot (rising edge) and undershoot (falling edge) conditions are separate and their impact must be determined independently.

After the true waveform conversion, the undershoot/overshoot specifications shown in Table 20 and Table 22 can be applied to the converted undershoot waveform using the same magnitude and pulse duration specifications used with an overshoot waveform.

Overshoot/undershoot magnitude levels must observe the Absolute Maximum Specifications listed in Table 20 and Table 21. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the Absolute Maximum Specifications (2.18V), the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.3.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/ undershoot reference voltage (Vos_ref = 1.635V). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage can not be substracted from the total overshoot/ undershoot pulse duration.

Note: Multiple Overshoot/Undershoot events occurring within the same clock cycle must be considered together as one event. Using the worst case Overshoot/Undershoot Magnitude, sum together the individual Pulse Duraitons to determine the total Overshoot/Undershoot Pulse Duration for that total event.

3.3.4 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of an AGTL+ or a CMOS signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs EVERY OTHER clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

The specifications provided in Table 20 and Table 21 show the Maximum Pulse Duration allowed for a given Overshoot/Undershoot Magnitude at a specific Activity Factor. Each Table entry is independent of all others, meaning that the Pulse Duration reflects the existence of overshoot/

undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be NO other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note: Activity factor for AGTL+ signals is referenced to BCLK frequency.

Note: Activity factor for CMOS signals is referenced to PICCLK frequency.

3.3.5 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the Pentium III processor for the PGA370 socket is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the junction temperature the processor will be operating at, the width of the overshoot (as measured above 1.635V) and the Activity Factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group that particular signal falls into. If the signal is an AGTL+ signal operating with a 100 MHz system bus, use Table 20 (100 MHz AGTL+ signal group). If the signal is a CMOS signal, use Table 21 (33 MHz CMOS signal group).
2. Determine the maximum junction temperature (Tj) for the range of processors that the system will support (80^oC or 85^oC).
3. Determine the Magnitude of the overshoot (relative to V_{SS})
4. Determine the Activity Factor (how often does this overshoot occur?)
5. From the appropriate Specification table, read off the Maximum Pulse Duration (in ns) allowed.
6. Compare the specified Maximum Pulse Duration to the signal being measured. If the Pulse Duration measured is less than the Pulse Duration shown in the table, then the signal meets the specifications.

The above procedure is similar for undershoots after the undershoot waveform has been converted to look like an overshoot. Undershoot events must be analyzed separately from Overshoot events as they are mutually exclusive.

Table 19 shows an example of how the maximum pulse duration is determined for a given waveform.

Table 19. Example Platform Information

Required Information	Maximum Platform Support	Notes
FSB Signal Group	100 MHz AGTL+	
Max Tj	85 °C	
Overshoot Magnitude	2.13V	Measured Value
Activity Factor (AF)	0.1	Measured overshoot occurs on average every 20 clocks

NOTES:
1. Corresponding Maximum Puse Duration Specification - 3.2 ns
2. Pulse Duration (measured) - 3.0 ns

ExampleGiven the above parameters, and using Table 20 (85°C/AF=0.1 column) the maximum allowed pulse duration is 3.2 ns. Since the measure pulse duration is 3.0ns, this particular 7overshoot event passes the overshoot specifications, although this does not guarantee that the combined overshoot/undershoot events meet the specifications.

3.3.6 Determining if a System meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. Ensure no signal (CMOS or AGTL+) ever exceed the 1.635V OR
2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables OR
3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 20 and Table 21.

NOTES:

1. Overshoot/Undershoot Magnitude = 2.18V is an Absolute value and should never be exceeded
2. Overshoot is measured relative to V_{SS}.
3. Undershoot is measured relative to $V_{TT.}$
4. Overshoot/Undershoot Pulse Duration is measured relative to 1.635V.
5. Rinbacks below V_{TT} can not be subtracted from Overshoots/Undershoots.
6. Lesser Undershoot does not allocate longer or larger Overshoot.
7. Consult the appropriate layout guidelines provided in the specific platform design guide.
8. All values specified by design characterization.

Table 20. 100 MHz AGTL+ Signal Group Overshoot/Undershoot Tolerance at Processor Pins[1,2]

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 85 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	20	2.53	0.25	18.6	1.86	0.18
2.13 V	20	4.93	0.49	20	3.2	0.32
2.08 V	20	9.1	0.91	20	6.1	0.6
2.03 V	20	16.6	1.67	20	11.4	1.1
1.98 V	20	20	3.0	20	20	2
1.93 V	20	20	5.5	20	20	6.6
1.88 V	20	20	10	20	20	20

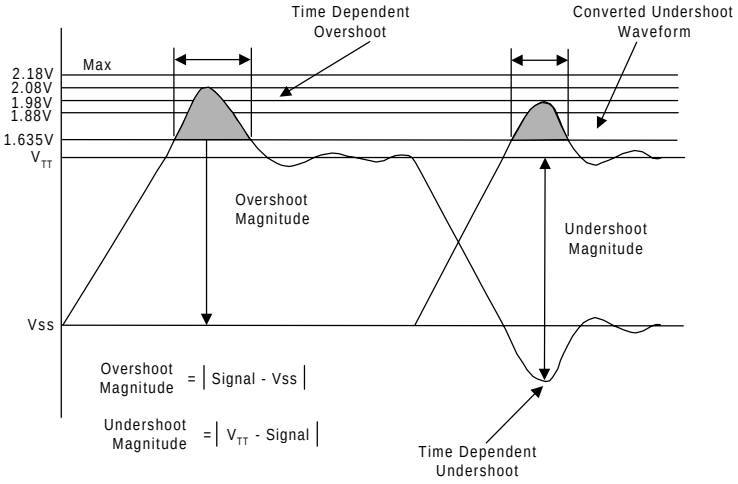
NOTES:
1. BCLK period is 10 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

Table 21. 33 MHz CMOS Signal Group Overshoot/Undershoot Tolerance at Processor Pins[1, 2]

Overshoot/ Undershoot Magnitude	Maximum Pulse Duration at Tj = 80 °C (ns)			Maximum Pulse Duration at Tj = 85 °C (ns)		
	AF = 0.01	AF = 0.1	AF = 1	AF = 0.01	AF = 0.1	AF = 1
2.18 V	60	7.6	0.76	56	5.6	0.56
2.13 V	60	14.8	1.48	60	9.6	0.96
2.08 V	60	27.2	2.7	60	18.4	1.8
2.03 V	60	50	5	60	33	3.3
1.98 V	60	60	9.1	60	60	6
1.93 V	60	60	16.4	60	60	20
1.88 V	60	60	30	60	60	60

NOTES:
1. PICCLK period is 30 ns.
2. Measurements taken at the processor socket pins on the solder-side of the motherboard.

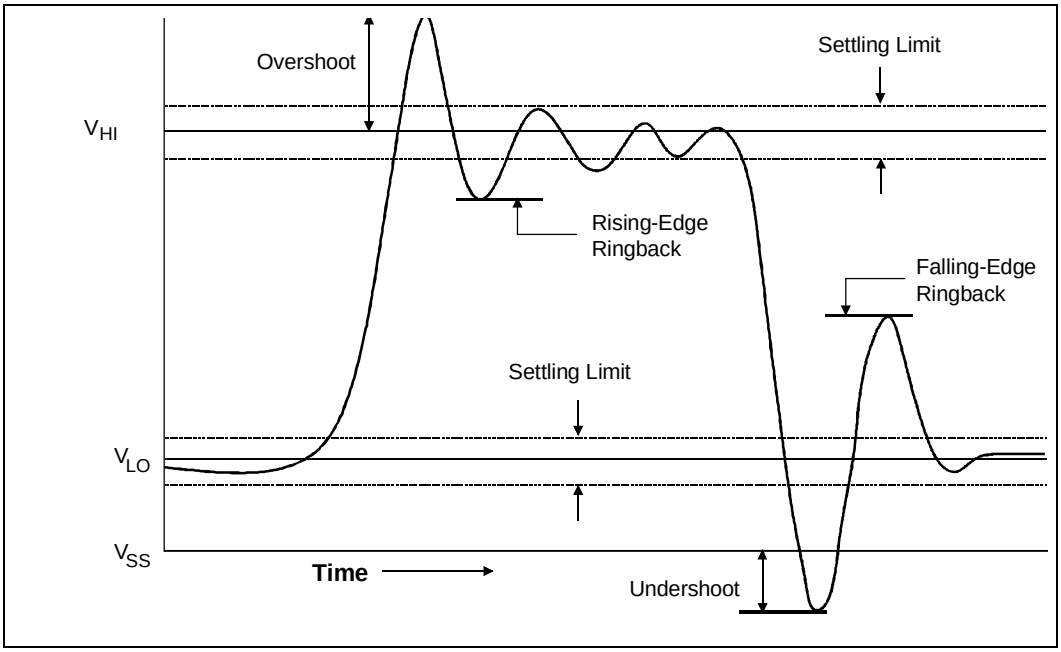
Figure 15. Maximum Acceptable AGTL+ Overshoot/Undershoot Waveform



3.4 Non-AGTL+ Signal Quality Specifications and Measurement Guidelines

There are three signal quality parameters defined for non-AGTL+ signals: overshoot/undershoot, ringback, and settling limit. All three signal quality parameters are shown in Figure 16 for the non-AGTL+ signal group.

Figure 16. Non-AGTL+ Overshoot/Undershoot, Settling Limit, and Ringback [1]



NOTES:
1. V_{HI} = 1.5V for all non-AGTL+ signals except for BCLK, PICCLK, and PWRGOOD. V_{HI} = 2.5 V for BCLK, PICCLK, and PWRGOOD. BCLK and PICCLK signal quality is detailed in Section 3.1.

3.4.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot guideline limits transitions beyond VCC or V_{SS} due to the fast signal edge rates (see Figure 16 for non-AGTL+ signals). The processor can be damaged by repeated overshoot events on 1.5 V or 2.5 V tolerant buffers if the charge is large enough (i.e., if the overshoot is great enough). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult. The overshoot/undershoot guideline is 0.3 V and assumes the absence of diodes on the input. These guidelines should be verified in simulations without the on-chip ESD protection diodes present because the diodes will begin clamping the 1.5 V and 2.5 V tolerant signals beginning at approximately 0.7 V above the appropriate supply and 0.7 V below VSS. If signals are not reaching the clamping voltage, this will not be an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

Note: The undershoot guideline limits transitions exactly as described for the ATGL+ signals. See Figure 15.

3.4.2 Ringback Specification

Ringback refers to the amount of reflection seen after a signal has switched. The ringback specification is the voltage that the signal rings back to after achieving its maximum absolute value. See Figure 16 for an illustration of ringback. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal ringback specification are not allowed under any circumstances for non-AGTL+ signals.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 22 for the signal ringback specifications for non-AGTL+ signals for simulations at the processor pins.

Table 22. Signal Ringback Specifications for Non-AGTL+ Signal Simulation at the Processor Pins [1]

Input Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure
Non-AGTL+ Signals [2]	0 → 1	V_{REF} + 0.200	V	16
Non-AGTL+ Signals [2]	1 → 0	V_{REF} - 0.200	V	16
PWRGOOD	0 → 1	2.00	V	16

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all Pentium III processor frequencies.
2. Non-AGTL+ signals except PWRGOOD.

3.4.3 Settling Limit Guideline

Settling limit defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. The amount allowed is 10% of the total signal swing ($V_{HI} - V_{LO}$) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state or low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify settling limit may be done either with or without the input protection diodes present. Violation of the settling limit guideline is acceptable if simulations of 5 to 10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

4.0 Thermal Specifications and Design Considerations

This chapter provides needed data for designing a thermal solution. However, for the correct thermal measuring processes, refer to AP-905, *Intel® Pentium® III Processor Thermal Design Guidelines* (Order Number 245087). The Pentium III processor uses flip chip pin grid array packaging technology and has a **junction** temperature ($T_{junction}$) specified.

4.1 Thermal Specifications

Table 23 provides the thermal design power dissipation and maximum temperatures for the Pentium III processor for the PGA370 socket. Systems should design for the highest possible processor power, even if a processor with a lower thermal dissipation is planned. A thermal solution should be designed to ensure the junction temperature never exceeds these specifications.

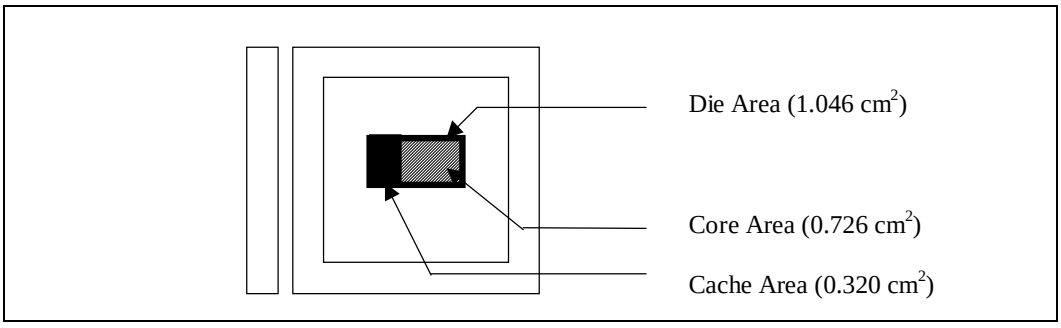
Table 23. Pentium III Processor for the PGA370 Socket Thermal Design Power [1]

Processor	Processor Core Frequency (MHz)	L2 Cache Size (KB)	Processor Power [2] (W)	Processor Core Power [3] (W)	Power Density (W/cm^2)	Maximum $T_{JUNCTION}$ (°C)	$T_{JUNCTION}$ Offset [4, 5] (°C)
500E	500	256	16.0	15.8	22.0[6]	85	2.3
550E	550	256	17.6	17.4	24.2[6]	85	2.6

NOTES:
1. These values are specified at nominal $V_{CC_{CORE}}$ for the processor pins.
2. Processor power includes the power dissipated by the processor core, the L2 cache, and the AGTL + bus termination. The maximum power for each of these components does not occur simultaneously.
3. Processor core power includes only the power dissipated by the core die.
4. $T_{junctionoffset}$ is the worst-case difference between the thermal reading from the on-die thermal diode and the hottest location on the processor's core.
5. $T_{junctionoffset}$ values do not include any thermal diode kit measurement error. Diode kit measurement error must be added to the Tjunctionoffset value from the table, as outlined in the Pentium(r) III Processor Thermal Design Guidelines. Intel has characterized the use of the Analog Devices AD1021 diode measurement kit and found its measurement error to be 1oC.
6. Power density is the maximum power the processor die can dissipate (i.e. processor power) divided by the die area over which the power is generated. Power for these processors is generated of the core area shown in Figure 17.

Figure 17 is a block diagram of the Pentium III processor die layout. The layout differentiates the processor core from the cache die area. In effect, the thermal design power indentified in Table 23 is dissipated entirely from the processor core area. Thermal solution designs should compensate for this smaller heat flux area and not assume that the power is uniformly distributed across the entire die area.

Figure 17. Processor Functional Die Layout



4.1.1 Thermal Diode

The Pentium III processor for the PGA370 socket incorporates an on-die diode that may be used to monitor the die temperature (junction temperature). A thermal sensor located on the motherboard, or a stand-alone measurement kit, may monitor the die temperature of the processor for thermal management or instrumentation purposes. Table 24 and Table 25 provide the diode parameter and interface specifications.

Note: The reading of the thermal sensor connected to the thermal diode will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die at a given point in time, and time based variations in the die temperature measurement. Time based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the $T_{junction}$ temperature can change.

Table 24. Thermal Diode Parameters[1]

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{fw}	Forward Bias Current	5		300	µA	1
n	Diode Ideality Factor	1.0057	1.0080	1.0125		2, 3, 4

NOTES:
1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 100° C with a forward bias current of 5 - 300 µA.
3. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   I_{fw}=Is(e^ ((Vd*q)/(nkT)) - 1), where Is = saturation current, q = electronic charge, Vd = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
4. Not 100% tested. Specified by design characterization.

Table 25. Thermal Diode Interface

Pin Name	PGA370 Socket pin #	Pin Description
THERMDP	AL31	diode anode (p_junction)
THERMDN	AL29	diode cathode (n_junction)

5.0 Mechanical Specifications

The Pentium III processor uses a FC-PGA package technology. Mechanical specifications for the processor are given in this section. See Section 1.1.1 for a complete terminology listing.

The processor utilizes a PGA370 socket for installation into the motherboard. Details on the socket are available in the *370-Pin Socket (PGA370) Design Guidelines*.

Note: For Figure 18, the following apply:

1. Unless otherwise specified, the following drawings are dimensioned in inches.
2. All dimensions provided with tolerances are guaranteed to be met for all normal production product.
3. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
4. Drawings are not to scale.

5.1 FC-PGA Mechanical Specifications

The following figure with package dimensions is provided to aid in the design of heatsink and clip solutions as well as demonstrate where pin-side capacitors will be located on the processor. Table 26 includes the measurements for these dimensions in both inches and millimeters.

Figure 18. Package Dimensions

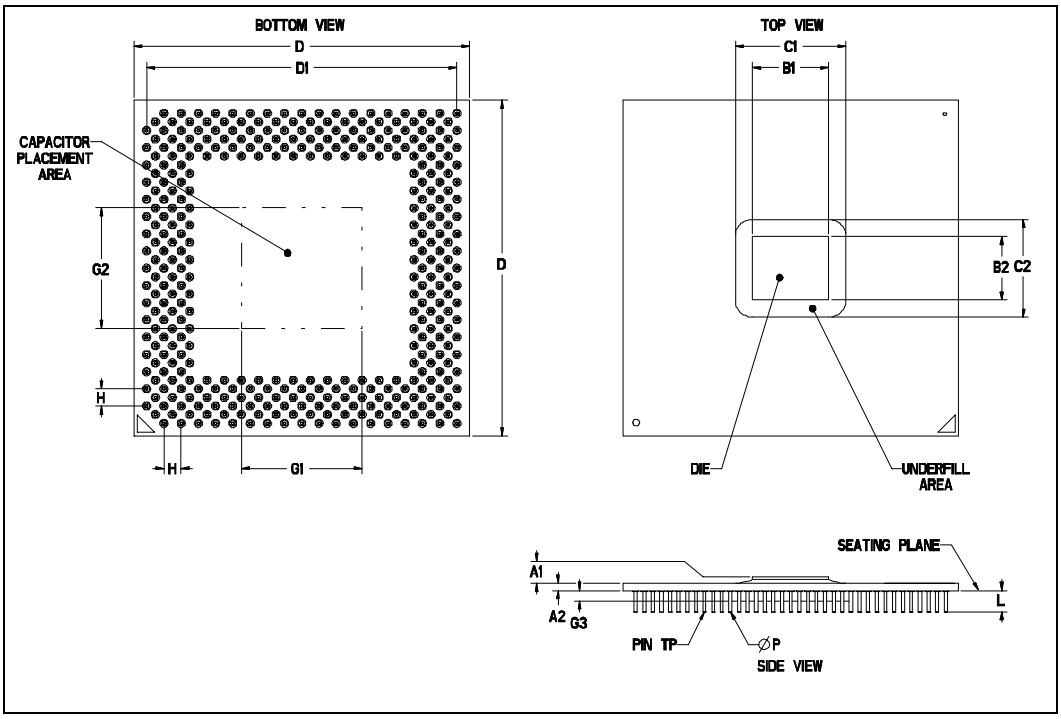


Table 26. Intel® Pentium® III Processor Package Dimensions

Symbol	Millimeters			Inches		
	Minimum	Maximum	Notes	Minimum	Maximum	Notes
A1	0.787	0.889		0.031d	0.035	
A2	1.000	1.200		0.039	0.047	
B1	11.226	11.329		0.442	0.446	
B2	9.296	9.398		0.366	0.370	
C1	23.495 max			0.925 max		
C2	21.590 max			0.850 max		
D	49.428	49.632		1.946	1.954	
D1	45.466	45.974		1.790	1.810	
G1	0.000	17.780		0	0.700	
G2	0.000	17.780		0	0.700	
G3	0.000	0.889		0	0.035	
H	2.540		Nominal	0.100		Nominal
L	3.048	3.302		0.120	0.130	
ΦP	0.431	0.483	Pin Diameter	0.017	0.019	
Pin TP	0.508 Diameteric True Position (Pin-to-Pin)			0.020 Diameteric True Position (Pin-to-Pin)		

NOTES:
1. Capacitors will be placed on the pin-side of the FC-PGA package in the area defined by G1, G2, and G3. This area is a keepout zone for motherboard designers.

The bare processor die has mechanical load limits that should not be exceeded during heat sink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solution must not induce permanent stress into the processor substrate with the exception of a uniform load to maintain the heatsink to the processor thermal interface. The package dynamic and static loading parameters are listed in Table 27.

For Table 27, the following apply:

1. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.
2. Parameters assume uniformly applied loads

Table 27. Processor Die Loading Parameters

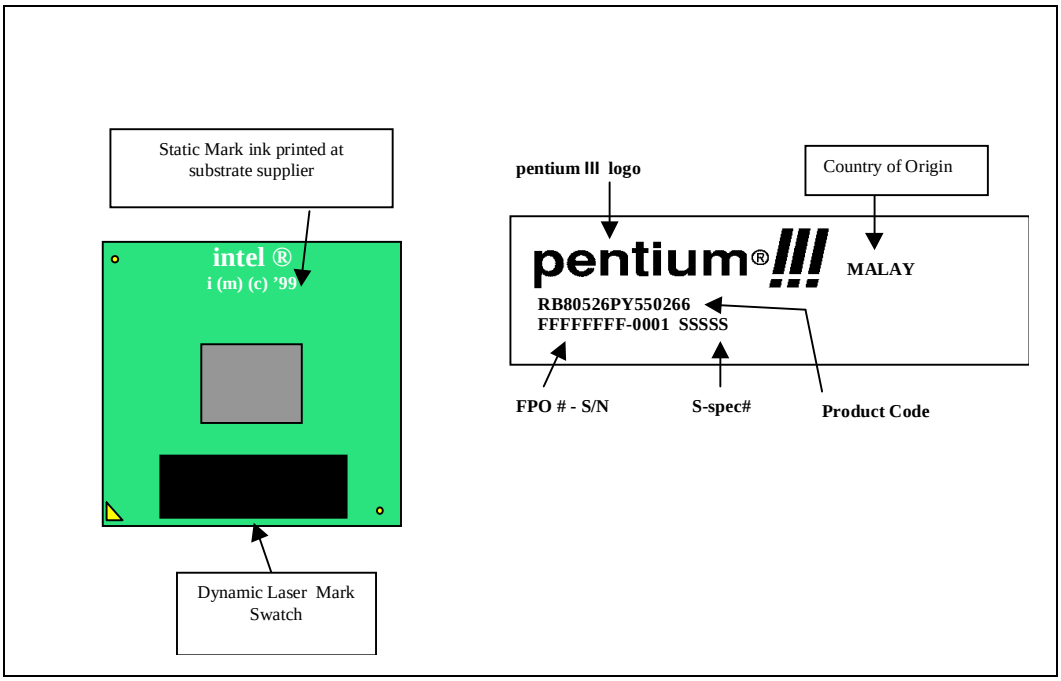
Parameter	Dynamic (max)[1]	Static (max)[2]	Unit
Silicon Die Surface	200	20	lbf
Silicon Die Edge	100	12	lbf

NOTES:
1. This specification applies to a uniform and a non-uniform load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface

5.2 Processor Markings

Figure 19 exemplifies the processor top-side markings and it is provided to aid in the identification of an Pentium III processor for the PGA370 socket. Table 26 lists the measurements for the package dimensions.

Figure 19. Top Side Processor Markings



5.3 Processor Signal Listing

Table 28 and Table 29 provide the processor pin definitions. The signal locations on the PGA370 socket are to be used for signal routing, simulation, and component placement on the baseboard. Figure 20 provides a pin-side view of the Pentium III processor pin-out.

The following notes apply to Table 28 and Table 29:

NOTES:

1. These pins are required for backwards compatibility with other Intel processors. They are not used by the Pentium III processor. Refer to the platform design guide and Section 7.1 for implementation details.
2. RESET# signal must be connected to pins AH4 and X4 for backwards compatibility. Refer to the platform design guide and Section 7.1 for implementation details. If backwards compatibility is not required, then RESET2# (X4) should be connected to GND.
3. $VCC_{1.5}$ must be supplied by the same voltage source supplying the V_{TT} pins.
4. These V_{TT} pins must be left unconnected (N/C) for backwards compatibility with Intel® Celeron™ processors (CPUID 066xh). For designs which do not support the Intel Celeron processors (CPUID 066xh), and for compatibility with future processors, these V_{TT} pins should be connected to the V_{TT} plane. Refer to the platform design guide and Section 7.1 for implementation details.
5. This pin is required for backwards compatibility. If backwards compatibility is not required, this pin may be left connected to VCC_{CORE}. Refer to the platform design guide for implementation details.
6. Previously, PGA370 socket designs defined this pin as a GND. It is now reserved and must be left unconnected (N/C).
7. Previously, PGA370 socket designs defined this pin as a GND. It is now CLKREF.

Figure 20. Intel® Pentium® III Processor Pinout

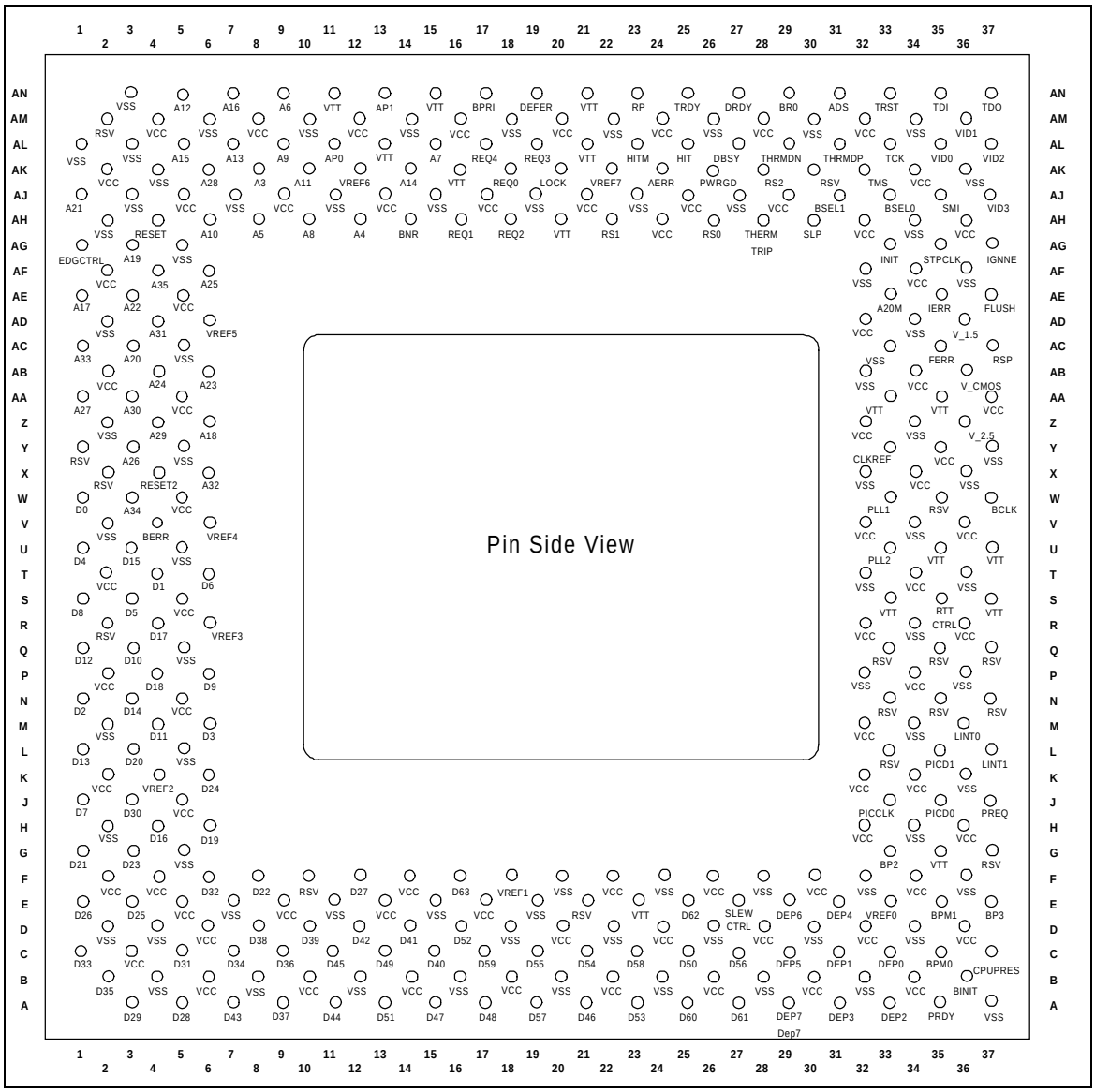


Table 28. Signal Listing in Order by Signal Name

Pin No.	Pin Name	Signal Group
AK8	A3#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AL15	A7#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AL9	A9#	AGTL+ I/O
AH6	A10#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AN5	A12#	AGTL+ I/O
AL7	A13#	AGTL+ I/O
AK14	A14#	AGTL+ I/O
AL5	A15#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AE1	A17#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
AG3	A19#	AGTL+ I/O
AC3	A20#	AGTL+ I/O
AE33	A20M#	CMOS Input
AJ1	A21#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB4	A24#	AGTL+ I/O
AF6	A25#	AGTL+ I/O
Y3	A26#	AGTL+ I/O
AA1	A27#	AGTL+ I/O
AK6	A28#	AGTL+ I/O
Z4	A29#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AD4	A31#	AGTL+ I/O
X6	A32#	AGTL+ I/O
AC1	A33#	AGTL+ I/O
W3	A34#	AGTL+ I/O
AF4	A35#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AK24	AERR#	AGTL+ I/O
AL11	AP0#	AGTL+ I/O
AN13	AP1#	AGTL+ I/O
W37	BCLK	System Bus Clock
V4	BERR#	AGTL+ I/O

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
B36	BINIT#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
G33	BP2#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
C35	BPM0#	AGTL+ I/O
E35	BPM1#	AGTL+ I/O
AN17	BPRI#	AGTL+ Input
AN29	BR0#	AGTL+ I/O
AJ33	BSEL0	Power/Other
AJ31	BSEL1	Power/Other
Y33	CLKREF [7]	Power/Other
C37	CPUPRES#	Power/Other
W1	D0#	AGTL+ I/O
T4	D1#	AGTL+ I/O
N1	D2#	AGTL+ I/O
M6	D3#	AGTL+ I/O
U1	D4#	AGTL+ I/O
S3	D5#	AGTL+ I/O
T6	D6#	AGTL+ I/O
J1	D7#	AGTL+ I/O
S1	D8#	AGTL+ I/O
P6	D9#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
M4	D11#	AGTL+ I/O
Q1	D12#	AGTL+ I/O
L1	D13#	AGTL+ I/O
N3	D14#	AGTL+ I/O
U3	D15#	AGTL+ I/O
H4	D16#	AGTL+ I/O
R4	D17#	AGTL+ I/O
P4	D18#	AGTL+ I/O
H6	D19#	AGTL+ I/O
L3	D20#	AGTL+ I/O
G1	D21#	AGTL+ I/O
F8	D22#	AGTL+ I/O
G3	D23#	AGTL+ I/O
K6	D24#	AGTL+ I/O
E3	D25#	AGTL+ I/O
E1	D26#	AGTL+ I/O
F12	D27#	AGTL+ I/O

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
A5	D28#	AGTL+ I/O
A3	D29#	AGTL+ I/O
J3	D30#	AGTL+ I/O
C5	D31#	AGTL+ I/O
F6	D32#	AGTL+ I/O
C1	D33#	AGTL+ I/O
C7	D34#	AGTL+ I/O
B2	D35#	AGTL+ I/O
C9	D36#	AGTL+ I/O
A9	D37#	AGTL+ I/O
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
C15	D40#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D12	D42#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A11	D44#	AGTL+ I/O
C11	D45#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C25	D50#	AGTL+ I/O
A13	D51#	AGTL+ I/O
D16	D52#	AGTL+ I/O
A23	D53#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C27	D56#	AGTL+ I/O
A19	D57#	AGTL+ I/O
C23	D58#	AGTL+ I/O
C17	D59#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
E25	D62#	AGTL+ I/O
F16	D63#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AN19	DEFER#	AGTL+ Input
C33	DEP0#	AGTL+ I/O
C31	DEP1#	AGTL+ I/O

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
A33	DEP2#	AGTL+ I/O
A31	DEP3#	AGTL+ I/O
E31	DEP4#	AGTL+ I/O
C29	DEP5#	AGTL+ I/O
E29	DEP6#	AGTL+ I/O
A29	DEP7#	AGTL+ I/O
AN27	DRDY#	AGTL+ I/O
AG1	EDGCTRL [5]	Power/Other
AC35	FERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AM22	GND	Power/Other
AM26	GND	Power/Other
AM30	GND	Power/Other
AM34	GND	Power/Other
AM6	GND	Power/Other
AN3	GND	Power/Other
B12	GND	Power/Other
B16	GND	Power/Other
B20	GND	Power/Other
B24	GND	Power/Other
B28	GND	Power/Other
B32	GND	Power/Other
B4	GND	Power/Other
B8	GND	Power/Other
D18	GND	Power/Other
D2	GND	Power/Other
D22	GND	Power/Other
D26	GND	Power/Other
D30	GND	Power/Other
D34	GND	Power/Other
D4	GND	Power/Other
E11	GND	Power/Other
E15	GND	Power/Other
E19	GND	Power/Other
E7	GND	Power/Other
F20	GND	Power/Other
F24	GND	Power/Other
F28	GND	Power/Other
F32	GND	Power/Other
F36	GND	Power/Other

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
G5	GND	Power/Other
H2	GND	Power/Other
H34	GND	Power/Other
K36	GND	Power/Other
L5	GND	Power/Other
M2	GND	Power/Other
M34	GND	Power/Other
P32	GND	Power/Other
P36	GND	Power/Other
A37	GND	Power/Other
AB32	GND	Power/Other
AC33	GND	Power/Other
AC5	GND	Power/Other
AD2	GND	Power/Other
AD34	GND	Power/Other
AF32	GND	Power/Other
AF36	GND	Power/Other
AG5	GND	Power/Other
AH2	GND	Power/Other
AH34	GND	Power/Other
AJ11	GND	Power/Other
AJ15	GND	Power/Other
AJ19	GND	Power/Other
AJ23	GND	Power/Other
AJ27	GND	Power/Other
AJ3	GND	Power/Other
AJ7	GND	Power/Other
AK36	GND	Power/Other
AK4	GND	Power/Other
AL1	GND	Power/Other
AL3	GND	Power/Other
AM10	GND	Power/Other
AM14	GND	Power/Other
AM18	GND	Power/Other
Q5	GND	Power/Other
R34	GND	Power/Other
T32	GND	Power/Other
T36	GND	Power/Other
U5	GND	Power/Other
V2	GND	Power/Other

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
V34	GND	Power/Other
X32	GND	Power/Other
X36	GND	Power/Other
Y37	GND	Power/Other
Y5	GND	Power/Other
Z2	GND	Power/Other
Z34	GND	Power/Other
AL25	HIT#	AGTL+ I/O
AL23	HITM#	AGTL+ I/O
AE35	IERR#	CMOS Output
AG37	IGNNE#	CMOS Input
AG33	INIT#	CMOS Input
M36	LINT0/INTR	CMOS Input
L37	LINT1/NMI	CMOS Input
AK20	LOCK#	AGTL+ I/O
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
L35	PICD1	APIC I/O
W33	PLL1	Power/Other
U33	PLL2	Power/Other
A35	PRDY#	AGTL+ Output
J37	PREQ#	CMOS Input
AK26	PWRGOOD	CMOS Input
AK18	REQ0#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
G37	Reserved	Reserved for future use
L33	Reserved	Reserved for future use
N33	Reserved	Reserved for future use
N35	Reserved	Reserved for future use
N37	Reserved	Reserved for future use
Q33	Reserved	Reserved for future use
Q35	Reserved	Reserved for future use
Q37	Reserved	Reserved for future use
R2	Reserved	Reserved for future use
W35	Reserved	Reserved for future use
Y1	Reserved	Reserved for future use
AK30	Reserved	Reserved for future use

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AM2 [6]	Reserved	Reserved for future use
F10	Reserved	Reserved for future use
X2	Reserved	Reserved for future use
AH4	RESET# [2]	AGTL+ Input
X4	RESET2# [2]	AGTL+ I/O
AN23	RP#	AGTL+ I/O
AH26	RS0#	AGTL + Input
AH22	RS1#	AGTL+ Input
AK28	RS2#	AGTL+ Input
AC37	RSP#	AGTL+ Input
S35	RTTCTRL	Power/Other
E27	SLEWCTRL	Power/Other
AH30	SLP#	CMOS Input
AJ35	SMI#	CMOS Input
AG35	STPCLK#	CMOS Input
AL33	TCK	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AH28	THERMTRIP#	CMOS Output
AK32	TMS	TAP Input
AN25	TRDY#	AGTL+ Input
AN33	TRST#	TAP Input
AD36	$V_{CC1.5}$ [3]	Power/Other
Z36	$V_{CC2.5}$ [1]	Power/Other
AB36	V_{CCCMOS}	Power/Other
AA37	V_{CCCORE}	Power/Other
AA5	V_{CCCORE}	Power/Other
AB2	V_{CCCORE}	Power/Other
AB34	V_{CCCORE}	Power/Other
AD32	V_{CCCORE}	Power/Other
AE5	V_{CCCORE}	Power/Other
E5	V_{CCCORE}	Power/Other
E9	V_{CCCORE}	Power/Other
F14	V_{CCCORE}	Power/Other
F2	V_{CCCORE}	Power/Other
F22	V_{CCCORE}	Power/Other
F26	V_{CCCORE}	Power/Other
F30	V_{CCCORE}	Power/Other

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
F34	V_{CCCORE}	Power/Other
F4	V_{CCCORE}	Power/Other
H32	V_{CCCORE}	Power/Other
H36	V_{CCCORE}	Power/Other
J5	V_{CCCORE}	Power/Other
K2	V_{CCCORE}	Power/Other
K32	V_{CCCORE}	Power/Other
K34	V_{CCCORE}	Power/Other
M32	V_{CCCORE}	Power/Other
N5	V_{CCCORE}	Power/Other
P2	V_{CCCORE}	Power/Other
P34	V_{CCCORE}	Power/Other
R32	V_{CCCORE}	Power/Other
R36	V_{CCCORE}	Power/Other
S5	V_{CCCORE}	Power/Other
T2	V_{CCCORE}	Power/Other
T34	V_{CCCORE}	Power/Other
V32	V_{CCCORE}	Power/Other
V36	V_{CCCORE}	Power/Other
W5	V_{CCCORE}	Power/Other
X34	V_{CCCORE}	Power/Other
Y35	V_{CCCORE}	Power/Other
Z32	V_{CCCORE}	Power/Other
AF2	V_{CCCORE}	Power/Other
AF34	V_{CCCORE}	Power/Other
AH24	V_{CCCORE}	Power/Other
AH32	V_{CCCORE}	Power/Other
AH36	V_{CCCORE}	Power/Other
AJ13	V_{CCCORE}	Power/Other
AJ17	V_{CCCORE}	Power/Other
AJ21	V_{CCCORE}	Power/Other
AJ25	V_{CCCORE}	Power/Other
AJ29	V_{CCCORE}	Power/Other
AJ5	V_{CCCORE}	Power/Other
AK2	V_{CCCORE}	Power/Other
AK34	V_{CCCORE}	Power/Other
AM12	V_{CCCORE}	Power/Other
AM16	V_{CCCORE}	Power/Other
AM20	V_{CCCORE}	Power/Other
AM24	V_{CCCORE}	Power/Other

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AM28	$V_{CC_{CORE}}$	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM4	$V_{CC_{CORE}}$	Power/Other
AM8	$V_{CC_{CORE}}$	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
C3	$V_{CC_{CORE}}$	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
AJ9	$V_{CC_{CORE}}$	Power/Other
E21	$V_{CORE_{DET}}$	Power/Other
AL35	VID0	Power/Other
AM36	VID1	Power/Other

Table 28. Signal Listing in Order by Signal Name (Continued)

Pin No.	Pin Name	Signal Group
AL37	VID2	Power/Other
AJ37	VID3	Power/Other
E33	V_{REF0}	Power/Other
F18	V_{REF1}	Power/Other
K4	V_{REF2}	Power/Other
R6	V_{REF3}	Power/Other
V6	V_{REF4}	Power/Other
AD6	V_{REF5}	Power/Other
AK12	V_{REF6}	Power/Other
AK22	V_{REF7}	Power/Other
AH20	V_{TT}	Power/Other
AK16	V_{TT}	Power/Other
AL13	V_{TT}	Power/Other
AL21	V_{TT}	Power/Other
AN11	V_{TT}	Power/Other
AN15	V_{TT}	Power/Other
G35	V_{TT}	Power/Other
AA33	V_{TT} [4]	Power/Other
AA35	V_{TT} [4]	Power/Other
AN21	V_{TT} [4]	Power/Other
E23	V_{TT} [4]	Power/Other
S33	V_{TT} [4]	Power/Other
S37	V_{TT} [4]	Power/Other
U35	V_{TT} [4]	Power/Other
U37	V_{TT} [4]	Power/Other

Table 29. Signal Listing in Order by Pin Number

Pin No.	Pin Name	Signal Group
A3	D29#	AGTL+ I/O
A5	D28#	AGTL+ I/O
A7	D43#	AGTL+ I/O
A9	D37#	AGTL+ I/O
A11	D44#	AGTL+ I/O
A13	D51#	AGTL+ I/O
A15	D47#	AGTL+ I/O
A17	D48#	AGTL+ I/O
A19	D57#	AGTL+ I/O
A21	D46#	AGTL+ I/O
A23	D53#	AGTL+ I/O
A25	D60#	AGTL+ I/O
A27	D61#	AGTL+ I/O
A29	DEP7#	AGTL+ I/O
A31	DEP3#	AGTL+ I/O
A33	DEP2#	AGTL+ I/O
A35	PRDY#	AGTL+ Output
A37	GND	Power/Other
AA1	A27#	AGTL+ I/O
AA3	A30#	AGTL+ I/O
AA5	$V_{CC_{CORE}}$	Power/Other
AA33	V_{TT} [4]	Power/Other
AA35	V_{TT} [4]	Power/Other
AA37	$V_{CC_{CORE}}$	Power/Other
AB2	$V_{CC_{CORE}}$	Power/Other
AB4	A24#	AGTL+ I/O
AB6	A23#	AGTL+ I/O
AB32	GND	Power/Other
AB34	$V_{CC_{CORE}}$	Power/Other
AB36	$V_{CC_{CMOS}}$	Power/Other
AC1	A33#	AGTL+ I/O
AC3	A20#	AGTL+ I/O
AC5	GND	Power/Other
AC33	GND	Power/Other
AC35	FERR#	CMOS Output
AC37	RSP#	AGTL+ Input
AD2	GND	Power/Other
AD4	A31#	AGTL+ I/O
AD6	V_{REF5}	Power/Other
AD32	$V_{CC_{CORE}}$	Power/Other

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AD34	GND	Power/Other
AD36	$V_{CC_{1.5}}$ [3]	Power/Other
AE1	A17#	AGTL+ I/O
AE3	A22#	AGTL+ I/O
AE5	$V_{CC_{CORE}}$	Power/Other
AE33	A20M#	CMOS Input
AE35	IERR#	CMOS Output
AE37	FLUSH#	CMOS Input
AF2	$V_{CC_{CORE}}$	Power/Other
AF4	A35#	AGTL+ I/O
AF6	A25#	AGTL+ I/O
AF32	GND	Power/Other
AF34	$V_{CC_{CORE}}$	Power/Other
AF36	GND	Power/Other
AG1	EDGCTRL [5]	Power/Other
AG3	A19#	AGTL+ I/O
AG5	GND	Power/Other
AG33	INIT#	CMOS Input
AG35	STPCLK#	CMOS Input
AG37	IGNNE#	CMOS Input
AH2	GND	Power/Other
AH4	RESET# [2]	AGTL+ Input
AH6	A10#	AGTL+ I/O
AH8	A5#	AGTL+ I/O
AH10	A8#	AGTL+ I/O
AH12	A4#	AGTL+ I/O
AH14	BNR#	AGTL+ I/O
AH16	REQ1#	AGTL+ I/O
AH18	REQ2#	AGTL+ I/O
AH20	V_{TT}	Power/Other
AH22	RS1#	AGTL+ Input
AH24	$V_{CC_{CORE}}$	Power/Other
AH26	RS0#	AGTL + Input
AH28	THERMTRIP#	CMOS Output
AH30	SLP#	CMOS Input
AH32	$V_{CC_{CORE}}$	Power/Other
AH34	GND	Power/Other
AH36	$V_{CC_{CORE}}$	Power/Other
AJ1	A21#	AGTL+ I/O
AJ3	GND	Power/Other

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AJ5	$V_{CC_{CORE}}$	Power/Other
AJ7	GND	Power/Other
AJ9	$V_{CC_{CORE}}$	Power/Other
AJ11	GND	Power/Other
AJ13	$V_{CC_{CORE}}$	Power/Other
AJ15	GND	Power/Other
AJ17	$V_{CC_{CORE}}$	Power/Other
AJ19	GND	Power/Other
AJ21	$V_{CC_{CORE}}$	Power/Other
AJ23	GND	Power/Other
AJ25	$V_{CC_{CORE}}$	Power/Other
AJ27	GND	Power/Other
AJ29	$V_{CC_{CORE}}$	Power/Other
AJ31	BSEL1	Power/Other
AJ33	BSEL0	Power/Other
AJ35	SMI#	CMOS Input
AJ37	VID3	Power/Other
AK2	$V_{CC_{CORE}}$	Power/Other
AK4	GND	Power/Other
AK6	A28#	AGTL+ I/O
AK8	A3#	AGTL+ I/O
AK10	A11#	AGTL+ I/O
AK12	V_{REF6}	Power/Other
AK14	A14#	AGTL+ I/O
AK16	V_{TT}	Power/Other
AK18	REQ0#	AGTL+ I/O
AK20	LOCK#	AGTL+ I/O
AK22	V_{REF7}	Power/Other
AK24	AERR#	AGTL+ I/O
AK26	PWRGOOD	CMOS Input
AK28	RS2#	AGTL+ Input
AK30	Reserved	Reserved for future use
AK32	TMS	TAP Input
AK34	$V_{CC_{CORE}}$	Power/Other
AK36	GND	Power/Other
AL1	GND	Power/Other
AL3	GND	Power/Other
AL5	A15#	AGTL+ I/O
AL7	A13#	AGTL+ I/O
AL9	A9#	AGTL+ I/O

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AL11	AP0#	AGTL+ I/O
AL13	V_{TT}	Power/Other
AL15	A7#	AGTL+ I/O
AL17	REQ4#	AGTL+ I/O
AL19	REQ3#	AGTL+ I/O
AL21	V_{TT}	Power/Other
AL23	HITM#	AGTL+ I/O
AL25	HIT#	AGTL+ I/O
AL27	DBSY#	AGTL+ I/O
AL29	THERMDN	Power/Other
AL31	THERMDP	Power/Other
AL33	TCK	TAP Input
AL35	VID0	Power/Other
AL37	VID2	Power/Other
AM2 [6]	Reserved	Reserved for future use
AM4	$V_{CC_{CORE}}$	Power/Other
AM6	GND	Power/Other
AM8	$V_{CC_{CORE}}$	Power/Other
AM10	GND	Power/Other
AM12	$V_{CC_{CORE}}$	Power/Other
AM14	GND	Power/Other
AM16	$V_{CC_{CORE}}$	Power/Other
AM18	GND	Power/Other
AM20	$V_{CC_{CORE}}$	Power/Other
AM22	GND	Power/Other
AM24	$V_{CC_{CORE}}$	Power/Other
AM26	GND	Power/Other
AM28	$V_{CC_{CORE}}$	Power/Other
AM30	GND	Power/Other
AM32	$V_{CC_{CORE}}$	Power/Other
AM34	GND	Power/Other
AM36	VID1	Power/Other
AN3	GND	Power/Other
AN5	A12#	AGTL+ I/O
AN7	A16#	AGTL+ I/O
AN9	A6#	AGTL+ I/O
AN11	V_{TT}	Power/Other
AN13	AP1#	AGTL+ I/O
AN15	V_{TT}	Power/Other
AN17	BPRI#	AGTL+ Input

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
AN19	DEFER#	AGTL+ Input
AN21	V_{TT} [4]	Power/Other
AN23	RP#	AGTL+ I/O
AN25	TRDY#	AGTL+ Input
AN27	DRDY#	AGTL+ I/O
AN29	BR0#	AGTL+ I/O
AN31	ADS#	AGTL+ I/O
AN33	TRST#	TAP Input
AN35	TDI	TAP Input
AN37	TDO	TAP Output
B2	D35#	AGTL+ I/O
B4	GND	Power/Other
B6	$V_{CC_{CORE}}$	Power/Other
B8	GND	Power/Other
B10	$V_{CC_{CORE}}$	Power/Other
B12	GND	Power/Other
B14	$V_{CC_{CORE}}$	Power/Other
B16	GND	Power/Other
B18	$V_{CC_{CORE}}$	Power/Other
B20	GND	Power/Other
B22	$V_{CC_{CORE}}$	Power/Other
B24	GND	Power/Other
B26	$V_{CC_{CORE}}$	Power/Other
B28	GND	Power/Other
B30	$V_{CC_{CORE}}$	Power/Other
B32	GND	Power/Other
B34	$V_{CC_{CORE}}$	Power/Other
B36	BINIT#	AGTL+ I/O
C1	D33#	AGTL+ I/O
C3	$V_{CC_{CORE}}$	Power/Other
C5	D31#	AGTL+ I/O
C7	D34#	AGTL+ I/O
C9	D36#	AGTL+ I/O
C11	D45#	AGTL+ I/O
C13	D49#	AGTL+ I/O
C15	D40#	AGTL+ I/O
C17	D59#	AGTL+ I/O
C19	D55#	AGTL+ I/O
C21	D54#	AGTL+ I/O
C23	D58#	AGTL+ I/O

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
C25	D50#	AGTL+ I/O
C27	D56#	AGTL+ I/O
C29	DEP5#	AGTL+ I/O
C31	DEP1#	AGTL+ I/O
C33	DEP0#	AGTL+ I/O
C35	BPM0#	AGTL+ I/O
C37	CPUPRES#	Power/Other
D2	GND	Power/Other
D4	GND	Power/Other
D6	$V_{CC_{CORE}}$	Power/Other
D8	D38#	AGTL+ I/O
D10	D39#	AGTL+ I/O
D12	D42#	AGTL+ I/O
D14	D41#	AGTL+ I/O
D16	D52#	AGTL+ I/O
D18	GND	Power/Other
D20	$V_{CC_{CORE}}$	Power/Other
D22	GND	Power/Other
D24	$V_{CC_{CORE}}$	Power/Other
D26	GND	Power/Other
D28	$V_{CC_{CORE}}$	Power/Other
D30	GND	Power/Other
D32	$V_{CC_{CORE}}$	Power/Other
D34	GND	Power/Other
D36	$V_{CC_{CORE}}$	Power/Other
E1	D26#	AGTL+ I/O
E3	D25#	AGTL+ I/O
E5	$V_{CC_{CORE}}$	Power/Other
E7	GND	Power/Other
E9	$V_{CC_{CORE}}$	Power/Other
E11	GND	Power/Other
E13	$V_{CC_{CORE}}$	Power/Other
E15	GND	Power/Other
E17	$V_{CC_{CORE}}$	Power/Other
E19	GND	Power/Other
E21	$V_{CORE_{DET}}$	Power/Other
E23	V_{TT} [4]	Power/Other
E25	D62#	AGTL+ I/O
E27	SLEWCTRL	Power/Other
E29	DEP6#	AGTL+ I/O

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
E31	DEP4#	AGTL+ I/O
E33	V_{REF0}	Power/Other
E35	BPM1#	AGTL+ I/O
E37	BP3#	AGTL+ I/O
F2	$V_{CC_{CORE}}$	Power/Other
F4	$V_{CC_{CORE}}$	Power/Other
F6	D32#	AGTL+ I/O
F8	D22#	AGTL+ I/O
F10	Reserved	Reserved for future use
F12	D27#	AGTL+ I/O
F14	$V_{CC_{CORE}}$	Power/Other
F16	D63#	AGTL+ I/O
F18	V_{REF1}	Power/Other
F20	GND	Power/Other
F22	$V_{CC_{CORE}}$	Power/Other
F24	GND	Power/Other
F26	$V_{CC_{CORE}}$	Power/Other
F28	GND	Power/Other
F30	$V_{CC_{CORE}}$	Power/Other
F32	GND	Power/Other
F34	$V_{CC_{CORE}}$	Power/Other
F36	GND	Power/Other
G1	D21#	AGTL+ I/O
G3	D23#	AGTL+ I/O
G5	GND	Power/Other
G33	BP2#	AGTL+ I/O
G35	V_{TT}	Power/Other
G37	Reserved	Reserved for future use
H2	GND	Power/Other
H4	D16#	AGTL+ I/O
H6	D19#	AGTL+ I/O
H32	$V_{CC_{CORE}}$	Power/Other
H34	GND	Power/Other
H36	$V_{CC_{CORE}}$	Power/Other
J1	D7#	AGTL+ I/O
J3	D30#	AGTL+ I/O
J5	$V_{CC_{CORE}}$	Power/Other
J33	PICCLK	APIC Clock Input
J35	PICD0	APIC I/O
J37	PREQ#	CMOS Input

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
K2	$V_{CC_{CORE}}$	Power/Other
K4	VREF2	Power/Other
K6	D24#	AGTL+ I/O
K32	$V_{CC_{CORE}}$	Power/Other
K34	$V_{CC_{CORE}}$	Power/Other
K36	GND	Power/Other
L1	D13#	AGTL+ I/O
L3	D20#	AGTL+ I/O
L5	GND	Power/Other
L33	Reserved	Reserved for future use
L35	PICD1	APIC I/O
L37	LINT1/NMI	CMOS Input
M2	GND	Power/Other
M4	D11#	AGTL+ I/O
M6	D3#	AGTL+ I/O
M32	$V_{CC_{CORE}}$	Power/Other
M34	GND	Power/Other
M36	LINT0/INTR	CMOS Input
N1	D2#	AGTL+ I/O
N3	D14#	AGTL+ I/O
N5	$V_{CC_{CORE}}$	Power/Other
N33	Reserved	Reserved for future use
N35	Reserved	Reserved for future use
N37	Reserved	Reserved for future use
P2	$V_{CC_{CORE}}$	Power/Other
P4	D18#	AGTL+ I/O
P6	D9#	AGTL+ I/O
P32	GND	Power/Other
P34	$V_{CC_{CORE}}$	Power/Other
P36	GND	Power/Other
Q1	D12#	AGTL+ I/O
Q3	D10#	AGTL+ I/O
Q5	GND	Power/Other
Q33	Reserved	Reserved for future use
Q35	Reserved	Reserved for future use
Q37	Reserved	Reserved for future use
R2	Reserved	Reserved for future use
R4	D17#	AGTL+ I/O
R6	V_{REF3}	Power/Other
R32	$V_{CC_{CORE}}$	Power/Other

Table 29. Signal Listing in Order by Pin Number (Continued)

Pin No.	Pin Name	Signal Group
R34	GND	Power/Other
R36	$V_{CC_{CORE}}$	Power/Other
S1	D8#	AGTL+ I/O
S3	D5#	AGTL+ I/O
S5	$V_{CC_{CORE}}$	Power/Other
S33	V_{TT} [4]	Power/Other
S35	RTTCTRL	Power/Other
S37	V_{TT} [4]	Power/Other
T2	$V_{CC_{CORE}}$	Power/Other
T4	D1#	AGTL+ I/O
T6	D6#	AGTL+ I/O
T32	GND	Power/Other
T34	$V_{CC_{CORE}}$	Power/Other
T36	GND	Power/Other
U1	D4#	AGTL+ I/O
U3	D15#	AGTL+ I/O
U5	GND	Power/Other
U33	PLL2	Power/Other
U35	V_{TT} [4]	Power/Other
U37	V_{TT} [4]	Power/Other
V2	GND	Power/Other
V4	BERR#	AGTL+ I/O
V6	V_{REF4}	Power/Other
V32	$V_{CC_{CORE}}$	Power/Other
V34	GND	Power/Other

Table 29. Signal Listing in Order by Pin Number (Continued)

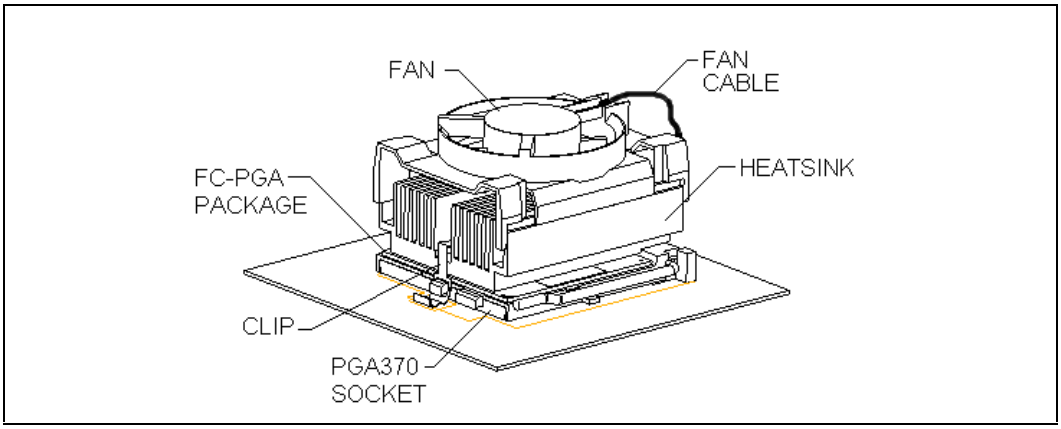
Pin No.	Pin Name	Signal Group
V36	$V_{CC_{CORE}}$	Power/Other
W1	D0#	AGTL+ I/O
W3	A34#	AGTL+ I/O
W5	$V_{CC_{CORE}}$	Power/Other
W33	PLL1	Power/Other
W35	Reserved	Reserved for future use
W37	BCLK	System Bus Clock
X2	Reserved	Reserved for future use
X4	RESET2# [2]	AGTL+ I/O
X6	A32#	AGTL+ I/O
X32	GND	Power/Other
X34	$V_{CC_{CORE}}$	Power/Other
X36	GND	Power/Other
Y1	Reserved	Reserved for future use
Y3	A26#	AGTL+ I/O
Y5	GND	Power/Other
Y33	CLKREF [7]	Power/Other
Y35	$V_{CC_{CORE}}$	Power/Other
Y37	GND	Power/Other
Z2	GND	Power/Other
Z4	A29#	AGTL+ I/O
Z6	A18#	AGTL+ I/O
Z32	$V_{CC_{CORE}}$	Power/Other
Z34	GND	Power/Other
Z36	$V_{CC_{2.5}}$ [1]	Power/Other

6.0 Boxed Processor Specifications

The Pentium III processor for the PGA370 socket is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from motherboards and standard components. The boxed processor will be supplied with an unattached fan heatsink. This section documents motherboard and system requirements for the fan heatsink that will be supplied with the boxed Pentium III processor. This section is particularly important for OEMs that manufacture motherboards for system integrators. Unless otherwise noted, all figures in this section are dimensioned in inches. Figure 21 shows a mechanical representation of the boxed Intel Pentium III processor for the PGA370 socket in the Flip Chip Pin Grid Array (FC-PGA) package.

Note: Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all heatsinks. It is the system designer's responsibility to consider their proprietary solution when designing to the required keep-out zone on their system platform and chassis. Refer to the *Pentium III Processor Enabling Functional Specification* for further guidance. Contact your local Intel Sales Representative for this document.

Figure 21. Conceptual Boxed Intel® Pentium® III Processor



6.1 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor fan heatsink.

6.1.1 Boxed Processor Thermal Cooling Solution Dimensions

The boxed processor ships with an unattached fan heatsink that has an integrated clip. The fan heatsink is designed to allow visibility of the processor markings located on the top of the package. Clearance is required around the fan heatsink to ensure unimpeded airflow for proper cooling. Note that the airflow of the fan heatsink is into the center and out of the sides of the fan heatsink. The dimensions for the boxed processor with integrated fan heatsink are shown in Figure 22 and Figure 23. General spatial specifications are also outlined in Table 30. All dimensions are in inches.

The processor markings are visible after installation of the fan heatsink due to notched sides of the heatsink base (See Figure 24). The boxed processor fan heatsink is also asymmetrical in that the mechanical step feature (specified in Figure 25) must sit over the socket's cam. Note - the step allows the heatsink to securely interface with the processor to meet thermal requirements.

Figure 22. Side View of Space Requirements for the Boxed Processor - View #1

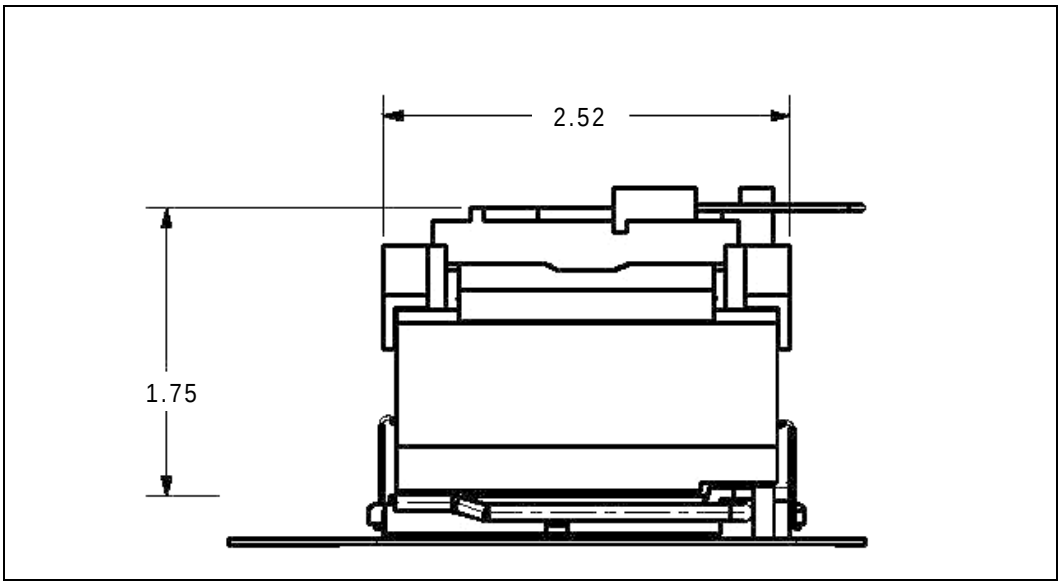


Figure 23. Side View of Space Requirements for the Boxed Processor - View #2

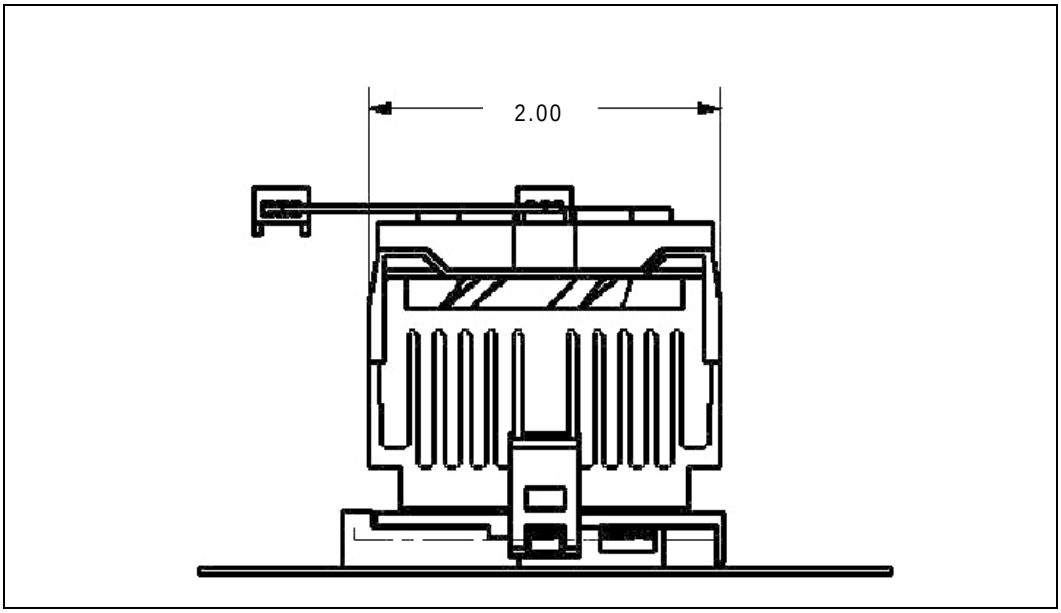


Table 30. Boxed Processor Fan Heatsink Spatial Dimensions

Dimensions (Inches)	Min	Typ	Max
Fan heatsink length			2.52
Fan heatsink height			1.76
Fan heatsink width			2.00
Fan heatsink height above motherboard		0.29	

NOTE: All dimensions in inches.

Figure 24. Dimensions of Notches in Heatsink Base

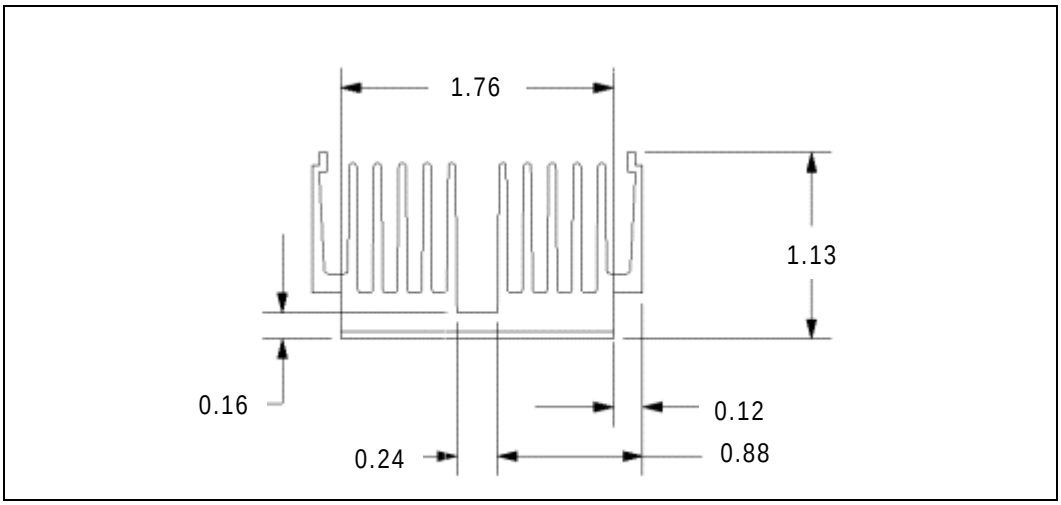
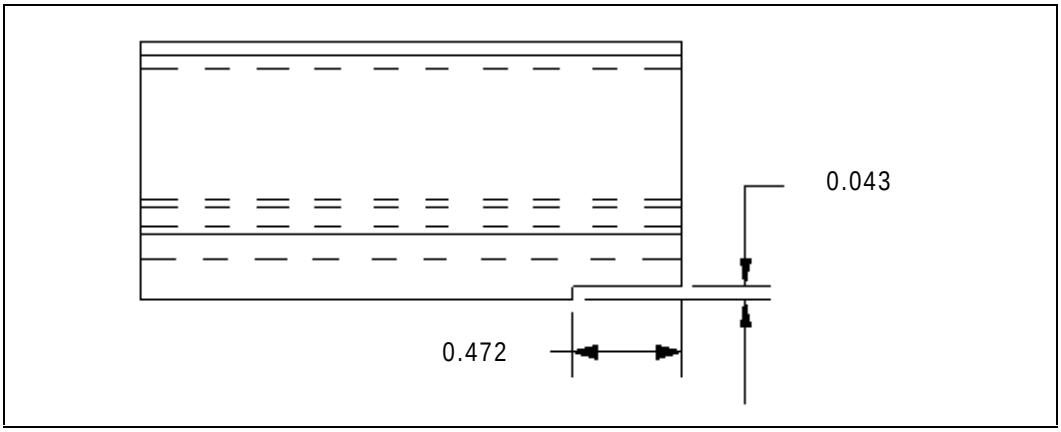


Figure 25. Dimensions of the Mechanical Step Feature in Heatsink Base



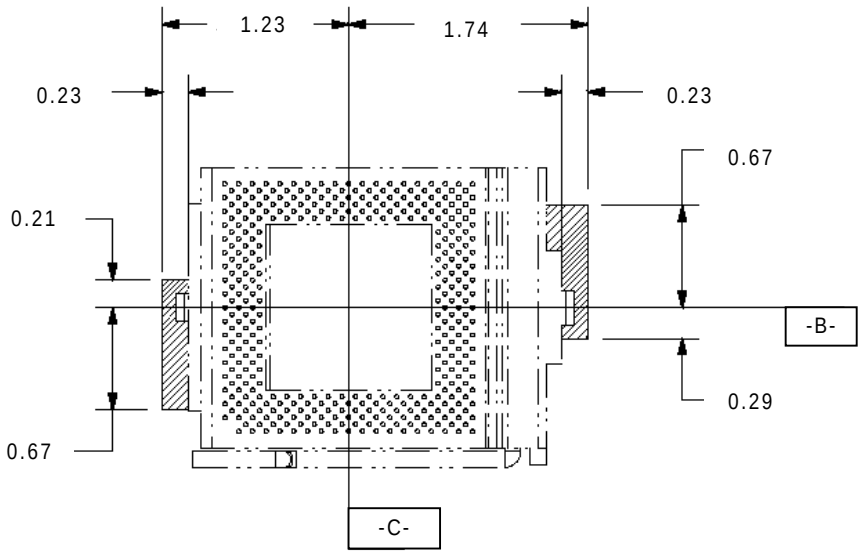
6.1.2 Boxed Processor Heatsink Weight

The boxed processor thermal cooling solution will not weigh more than 180 grams.

6.1.3 Boxed Processor Thermal Cooling Solution Clip

The boxed processor thermal solution requires installation by a system integrator to secure the thermal cooling solution to the processor after it is installed in the PGA370 ZIF socket. Motherboards designed for use by system integrators should take care to consider the implications of clip installation and potential scraping of the motherboard PCB underneath the PGA370 socket attach tabs. Motherboard components should not be placed too close to the PGA370 socket attach tabs in a way that interferes with the installation of the boxed processor thermal cooling solution (see Figure 26 for specifications).

Figure 26. Clip Keepout Requirements for PGA370



Notes: Unless otherwise specified:
1. Motherboard mounted components are not allowed in this area
2. -B- & -C-: Processor package centerlines.
3. -B-: FHS retention clip centerline.

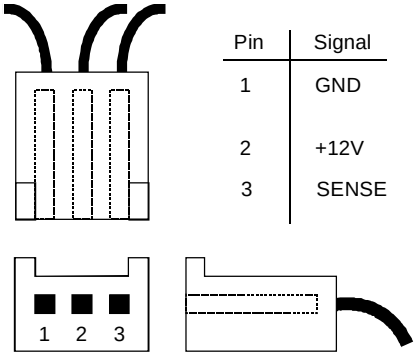
6.2 Boxed Processor Requirements

6.2.1 Fan Heatsink Power Supply

The boxed processor's fan heatsink requires a +12 V power supply. A fan power cable is attached to the fan and will draw power from a power header on the motherboard. The power cable connector and pinout are shown in Figure 27. Motherboards must provide a matched power header to support the boxed processor. Table 31 contains specifications for the input and output signals at the fan heatsink connector. The cable length is 7.0 inches (±0.25"). The fan heatsink outputs a SENSE signal, which is an open-collector output, that pulses at a rate of two pulses per fan revolution. A motherboard pull-up resistor provides VOH to match the motherboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

The power header on the motherboard must be positioned to allow the fan heatsink power cable to reach it. The power header identification and location should be documented in the motherboard documentation or on the motherboard. Figure 28 shows the recommended location of the fan power connector relative to the PGA370 socket. The motherboard power header should be positioned within 4.00 inches from the center of the PGA370 socket.

Figure 27. Boxed Processor Fan Heatsink Power Cable Connector Description



Pin	Signal
1	GND
2	+12V
3	SENSE

Straight square pin, 3-pin terminal housing with polarizing ribs and friction locking ramp.

0.100" pin pitch, 0.025" square pin width.

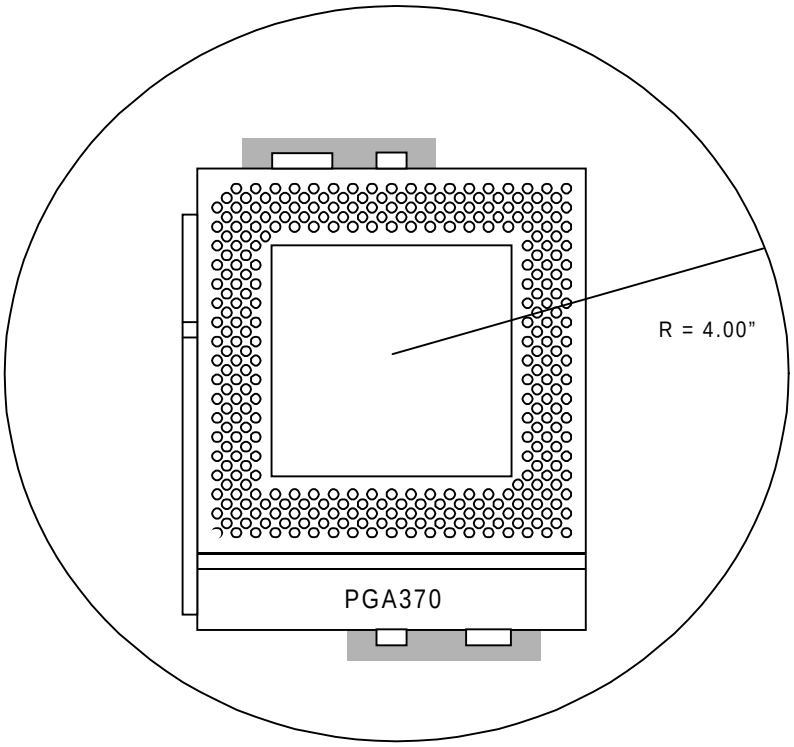
Waldom/Molex P/N 22-01-3037 or equivalent.

Match with straight pin, friction lock header on motherboard Waldom/Molex P/N 22-23-2031, AMP P/N 640456-3, or equivalent.

Table 31. Fan Heatsink Power and Signal Specifications

Description	Min	Typ	Max
+12 V: 12 volt fan power supply	7 V	12 V	13.8 V
IC: Fan current draw			100 mA
SENSE: SENSE frequency (motherboard should pull this pin up to appropriate V_{CC} with resistor)		2 pulses per fan revolution	

Figure 28. Motherboard Power Header Placement Relative to the Processor



6.3 Thermal Specifications

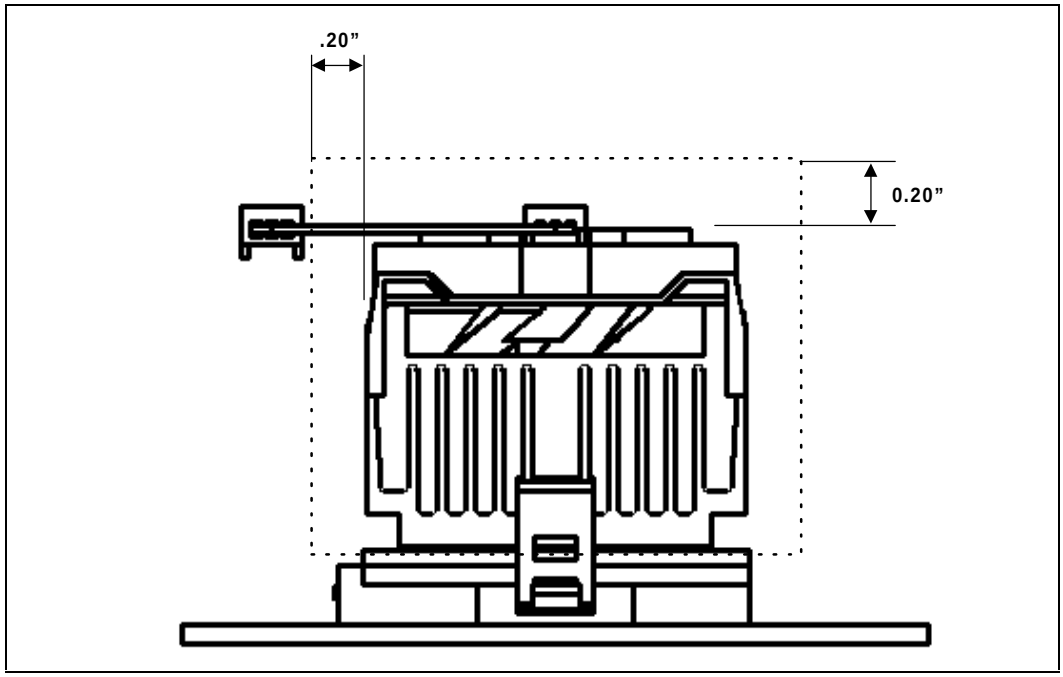
This section describes the cooling requirements of the thermal cooling solution utilized by the boxed processor.

6.3.1 Boxed Processor Cooling Requirements

The boxed processor is cooled with a fan heatsink. The boxed processor fan heatsink will keep the processor core at the specified Tjunction (see Table 23), provided airflow through the fan heatsink is unimpeded. It is recommended that the air temperature entering the fan inlet is below 45 °C (measured at 0.3 inches above the fan hub).

Airspace is required around the fan to ensure that the airflow through the fan heatsink is not blocked. Blocking the airflow to the fan heatsink reduces the cooling efficiency and decreases fan life. Figure 29 shows the specification for the boxed Pentium III processor fan heatsink as 0.20” clearance in all directions.

Figure 29. Thermal Airspace Requirement for the Boxed Processor Fan Heatsink



7.0 Processor Signal Description

This section provides an alphabetical listing of all the Pentium III processor signals. The tables at the end of this section summarize the signals by direction: output, input, and I/O.

7.1 Alphabetical Signals Reference

Table 32. Signal Description (Sheet 1 of 7)

Name	Type	Description
A[35:3]#	I/O	The A[35:3]# (Address) signals define a 2^{36}-byte physical memory address space. When ADS# is active, these pins transmit the address of a transaction; when ADS# is inactive, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor system bus. The A[35:24]# signals are parity-protected by the AP1# parity signal, and the A[23:3]# signals are parity-protected by the AP0# parity signal. On the active-to-inactive transition of RESET#, the processors sample the A[35:3]# pins to determine their power-on configuration. See the Intel® *Pentium® II Processor Developer's Manual* for details.
A20M#	I	If the A20M# (Address-20 Mask) input signal is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
ADS#	I/O	The ADS# (Address Strobe) signal is asserted to indicate the validity of the transaction address on the A[35:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor system bus agents.
AERR#	I/O	The AERR# (Address Parity Error) signal is observed and driven by all processor system bus agents, and if used, must connect the appropriate pins on all processor system bus agents. AERR# observation is optionally enabled during power-on configuration; if enabled, a valid assertion of AERR# aborts the current transaction. If AERR# observation is disabled during power-on configuration, a central agent may handle an assertion of AERR# as appropriate to the error handling architecture of the system.
AP[1:0]#	I/O	The AP[1:0]# (Address Parity) signals are driven by the request initiator along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#, and AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all processor system bus agents.
BCLK	I	The BCLK (Bus Clock) signal determines the bus frequency. All processor system bus agents must receive this signal to drive their outputs and latch their inputs on the BCLK rising edge. All external timing parameters are specified with respect to the BCLK signal.

Table 32. Signal Description (Sheet 2 of 7)

Name	Type	Description
BERR#	I/O	The BERR# (Bus Error) signal is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents, and must connect the appropriate pins of all such agents, if used. However, Pentium III processors do not observe assertions of the BERR# signal. BERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: • Enabled or disabled. • Asserted optionally for internal errors along with IERR#. • Asserted optionally by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction.
BINIT#	I/O	The BINIT# (Bus Initialization) signal may be observed and driven by all processor system bus agents, and if used must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset and any data which was in transit is lost. All agents reset their rotating ID for bus arbitration to the state after Reset, and internal count information is lost. The L1 and L2 caches are not affected. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	The BNR# (Block Next Request) signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BP[3:2]#	I/O	The BP[3:2]# (Breakpoint) signals are outputs from the processor that indicate the status of breakpoints.
BPM[1:0]#	I/O	The BPM[1:0]# (Breakpoint Monitor) signals are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance.
BPRI#	I	The BPRI# (Bus Priority Request) signal is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	I/O	The BR0# (Bus Request) pin drives the BREQ0# signals in the system. During power-up configuration, the central agent must assert the BR0# bus signal in the system to assign the symmetric agent ID to the processor. The processor samples it's BR0# pin on the active-to-inactive transition of RESET# to obtain it's symmetric agent ID. The processor asserts BR0# to request the system bus.

Table 32. Signal Description (Sheet 3 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BSEL[1:0]</td><td>I/O</td><td>These signals are used to select the system bus frequency. A BSEL[1:0] = “01” will select a 100 MHz system bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All system bus agents must operate at the same frequency. Individual processors will only operate at their specified front side bus (FSB) frequency.
On motherboards which support operation at either 66 MHz or 100 MHz, a BSEL[1:0] = “x0” will select a 66 Mhz system bus frequency. 66 MHz operation is not support by the Pentium III processor for the PGA370 socket, therefore BSEL0 is ignored.
These signals must be pulled up to 2.5 V with 1KΩ resistors and provided as a frequency selection signal to the clock driver/synthesizer. See Section 2.8.2 for implementation examples.</td></tr>
<tr><td>CLKREF</td><td>I</td><td>The CLKREF input is a filtered 1.25V supply voltage for the processor PLL. A voltage divider and decoupling solution is provided by the motherboard. See the design guide for implementation details.</td></tr>
<tr><td>CPUPRES#</td><td>O</td><td>The CPUPRES# signal is defined to allow a system design to detect the presence of a terminator device or processor in a PGA370 socket. Combined with the VID combination of VID[3:0]= 1111 (see Section 2.6), a system can determine if a socket is occupied, and whether a processor core is present. See the table below for states and values for determining the presence of a device.

PGA370 Socket Occupation Truth Table
<table>
<tr><th>Signal</th><th>Value</th><th>Status</th></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
Anything other than ‘1111’</td><td>Processor core installed in the PGA370 socket.</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>0
1111</td><td>Terminator device installed in the PGA370 socket (i.e., no core present).</td></tr>
<tr><td>CPUPRES#
VID[3:0]</td><td>1
Any value</td><td>PGA370 socket not occupied.</td></tr>
</table></td></tr>
<tr><td>D[63:0]#</td><td>I/O</td><td>The D[63:0]# (Data) signals are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</td></tr>
<tr><td>DBSY#</td><td>I/O</td><td>The DBSY# (Data Bus Busy) signal is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>I</td><td>The DEFER# signal is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DEP[7:0]#</td><td>I/O</td><td>The DEP[7:0]# (Data Bus ECC Protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all processor system bus agents which use them. The DEP[7:0]# signals are enabled or disabled for ECC protection during power on configuration.</td></tr>
<tr><td>DRDY#</td><td>I/O</td><td>The DRDY# (Data Ready) signal is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-cycle data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
</table>

Table 32. Signal Description (Sheet 4 of 7)

Name	Type	Description
EDGCTRL	O	The EDGCTRL input adjusts the edge rate of AGTL+ output buffers for previous processors and should be pulled up to Vcc_{CORE} with a 51Ω ±5% resistor. See the platform design guide for implementation details. This signal is not used by the Pentium III processor.
FERR#	O	The FERR# (Floating-point Error) signal is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting.
FLUSH#	I	When the FLUSH# input signal is asserted, processors write back all data in the Modified state from their internal caches and invalidate all internal cache lines. At the completion of this operation, the processor issues a Flush Acknowledge transaction. The processor does not cache any new data while the FLUSH# signal remains asserted. FLUSH# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction. On the active-to-inactive transition of RESET#, each processor samples FLUSH# to determine its power-on configuration. See the *P6 Family of Processors Hardware Developer's Manual* for details.
HIT# HITM#	I/O I/O	The HIT# (Snoop Hit) and HITM# (Hit Modified) signals convey transaction snoop operation results, and must connect the appropriate pins of all processor system bus agents. Any such agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	The IERR# (Internal Error) signal is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	The IGNNE# (Ignore Numeric Error) signal is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O Write bus transaction.
INIT#	I	The INIT# (Initialization) signal, when asserted, resets integer registers inside all processors without affecting their internal (L1 or L2) caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT[1:0]	I	The LINT[1:0] (Local APIC Interrupt) signals must connect the appropriate pins of all APIC Bus agents, including all processors and the core logic or I/O APIC component. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Intel® Pentium® processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.

Table 32. Signal Description (Sheet 5 of 7)

Name	Type	Description
LOCK#	I/O	The LOCK# signal indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
PICCLK	I	The PICCLK (APIC Clock) signal is an input clock to the processor and core logic or I/O APIC which is required for operation of all processors, core logic, and I/O APIC components on the APIC bus.
PICD[1:0]	I/O	The PICD[1:0] (APIC Data) signals are used for bidirectional serial message passing on the APIC bus, and must connect the appropriate pins of all processors and core logic or I/O APIC components on the APIC bus.
PLL1, PLL2	I	All Pentium III processors have an internal analog PLL clock generator that requires a quiet power supply. PLL1 and PLL2 are inputs to this PLL and must be connected to $V_{CC_{CORE}}$ through a low pass filter that minimizes jitter. See the platform design guide for implementation details.
PRDY#	O	The PRDY (Probe Ready) signal is a processor output used by debug tools to determine processor debug readiness.
PREQ#	I	The PREQ# (Probe Request) signal is used by debug tools to request debug operation of the processors.
PWRGOOD	I	The PWRGOOD (Power Good) signal is processor input. The processor requires this signal to be a clean indication that the clocks and power supplies ($V_{CC_{CORE}}$, etc.) are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The figure below illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 13, and be followed by a 1 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	The REQ[4:0]# (Request Command) signals must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner over two clock cycles to define the currently active transaction type.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their L1 and L2 caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after $V_{CC_{CORE}}$ and CLK have reached their proper specifications. On observing active RESET#, all processor system bus agents will deassert their outputs within two clocks. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the *P6 Family of Processors Hardware Developer's Manual* for details. The processor may have its outputs tristated via power-on configuration. Otherwise, if INIT# is sampled active during the active-to-inactive transition of RESET#, the processor will execute its Built-in Self-Test (BIST). Whether or not BIST is executed, the processor will begin program execution at the power on Reset vector (default 0_FFFF_FFF0h). RESET# must connect the appropriate pins of all processor system bus agents.
RESET2#	I	The RESET2# pin is provided for compatibility with other Intel Architecture processors. The Pentium III processor does not use the RESET2# pin. Refer to the platform design guide for the proper connections of this signal.

Table 32. Signal Description (Sheet 6 of 7)

Name	Type	Description
RP#	I/O	The RP# (Request Parity) signal is driven by the request initiator, and provides parity protection on ADS# and REQ[4:0]#. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.
RS[2:0]#	I	The RS[2:0]# (Response Status) signals are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	I	The RSP# (Response Parity) signal is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
RTTCTRL	I	The RTTCTRL input signal provides AGTL+ termination control. The Pentium III processor samples this input to sense the presence of motherboard AGTL+ termination. See the platform design guide for implementation details.
SLEWCTRL	I	The SLEWCTRL input signal provides AGTL+ slew rate control. The Pentium III processor samples this input to determine the slew rate for AGTL+ signals when it is the driving agent. See the platform design guide for implementation details.
SLP#	I	The SLP# (Sleep) signal, when asserted in Stop-Grant state, causes processors to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertions of the SLP#, STPCLK#, and RESET# signals while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and APIC processor core units.
SMI#	I	The SMI# (System Management Interrupt) signal is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.
STPCLK#	I	The STPCLK# (Stop Clock) signal, when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the bus and APIC units. The processor continues to snoop bus transactions and latch interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units, services pending interrupts while in the Stop-Grant state, and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	The TCK (Test Clock) signal provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	The TDI (Test Data In) signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	The TDO (Test Data Out) signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
THERMDN	O	Thermal Diode Cathode. Used to calculate core (junction) temperature. See Section 4.1.
THERMDP	I	Thermal Diode Anode. Used to calculate core (junction) temperature. See Section 4.1.

Table 32. Signal Description (Sheet 7 of 7)

Name	Type	Description
THERMTRIP#	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 135 °C. This is signaled to the system by the THERMTRIP# (Thermal Trip) pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself; as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped below the trip level, the processor will continue to drive THERMTRIP# and remain stopped.
TMS	I	The TMS (Test Mode Select) signal is a JTAG specification support signal used by debug tools.
TRDY#	I	The TRDY# (Target Ready) signal is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all processor system bus agents.
TRST#	I	The TRST# (Test Reset) signal resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VID[3:0]	O	The VID[3:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages. These pins are not signals, but are either an open circuit or a short circuit to V_{SS} on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support voltage specification variations on processors. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
$VCORE_{DET}$	O	The $VCORE_{DET}$ pin indicate the type of processor core present. This pin will float for 2.0V VccCORE based processor and will be shorted to Vss for the Pentium III processor.
$VCC_{1.5}$	I	The $VCC_{1.5}$ input pin provides the termination voltage for CMOS signals interfacing to the processor. The Pentium III processor reroutes the 1.5V input to the VCC_{CMOS} output via the package. The supply for $VCC_{1.5}$ must be the same one used to supply $V_{TT.}$
$VCC_{2.5}$	I	The $VCC_{2.5}$ input pin provides the termination voltage for CMOS signals interfacing to processors which require 2.5V termination on the CMOS signals. This signal is not used by the Pentium III processor.
VCC_{CMOS}	O	The VCC_{CMOS} pin provides the CMOS voltage for use by the platform and is used for terminating CMOS signals that interface to the processor.
V_{REF}	I	The V_{REF} input pins supply the AGTL+ reference voltage, which is typically 2/3 of V_{TT}. V_{REF} is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1.

7.2 Signal Summaries

Table 33 through Table 36 list attributes of the processor output, input, and I/O signals.

Table 33. Output Signals

Name	Active Level	Clock	Signal Group
CPUPRES#	Low	Asynch	Power/Other
EDGCTRL	N/A	Asynch	Power/Other
FERR#	Low	Asynch	CMOS Output
IERR#	Low	Asynch	CMOS Output
PRDY#	Low	BCLK	AGTL+ Output
TDO	High	TCK	TAP Output
THERMTRIP#	Low	Asynch	CMOS Output
$VCORE_{DET}$	N/A	Asynch	Power/Other
VID[3:0]	N/A	Asynch	Power/Other

Table 34. Input Signals

Name	Active Level	Clock	Signal Group	Qualified
A20M#	Low	Asynch	CMOS Input	Always[1]
BCLK	High	—	System Bus Clock	Always
BPRI#	Low	BCLK	AGTL+ Input	Always
DEFER#	Low	BCLK	AGTL+ Input	Always
FLUSH#	Low	Asynch	CMOS Input	Always[1]
IGNNE#	Low	Asynch	CMOS Input	Always[1]
INIT#	Low	Asynch	CMOS Input	Always[1]
INTR	High	Asynch	CMOS Input	APIC disabled mode
LINT[1:0]	High	Asynch	CMOS Input	APIC enabled mode
NMI	High	Asynch	CMOS Input	APIC disabled mode
PICCLK	High	—	APIC Clock	Always
PREQ#	Low	Asynch	CMOS Input	Always
PWRGOOD	High	Asynch	CMOS Input	Always
RESET#	Low	BCLK	AGTL+ Input	Always
RS[2:0]#	Low	BCLK	AGTL+ Input	Always
RSP#	Low	BCLK	AGTL+ Input	Always
RTTCTRL	N/A	Asynch	Power/Other	
SLEWCTRL	N/A	Asynch	Power/Other	
SLP#	Low	Asynch	CMOS Input	During Stop-Grant state
SMI#	Low	Asynch	CMOS Input	
STPCLK#	Low	Asynch	CMOS Input	
TCK	High	—	TAP Input	
TDI	High	TCK	TAP Input	
TMS	High	TCK	TAP Input	
TRST#	Low	Asynch	TAP Input	
TRDY#	Low	BCLK	AGTL+ Input	

NOTE:
1. Synchronous assertion with active TDRY# ensures synchronization.

Table 35. Input/Output Signals (Single Driver)

Name	Active Level	Clock	Signal Group	Qualified
A[35:3]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
ADS#	Low	BCLK	AGTL+ I/O	Always
AP[1:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
BP[3:2]#	Low	BCLK	AGTL+ I/O	Always
BPM[1:0]#	Low	BCLK	AGTL+ I/O	Always
BR0#	Low	BCLK	AGTL+ I/O	Always
BSEL[1:0]	High	Asynch	Power/Other	Always
D[63:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DBSY#	Low	BCLK	AGTL+ I/O	Always
DEP[7:0]#	Low	BCLK	AGTL+ I/O	DRDY#
DRDY#	Low	BCLK	AGTL+ I/O	Always
LOCK#	Low	BCLK	AGTL+ I/O	Always
REQ[4:0]#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1
RP#	Low	BCLK	AGTL+ I/O	ADS#, ADS#+1

Table 36. Input/Output Signals (Multiple Driver)

Name	Active Level	Clock	Signal Group	Qualified
AERR#	Low	BCLK	AGTL+ I/O	ADS#+3
BERR#	Low	BCLK	AGTL+ I/O	Always
BINIT#	Low	BCLK	AGTL+ I/O	Always
BNR#	Low	BCLK	AGTL+ I/O	Always
HIT#	Low	BCLK	AGTL+ I/O	Always
HITM#	Low	BCLK	AGTL+ I/O	Always
PICD[1:0]	High	PICCLK	APIC I/O	Always