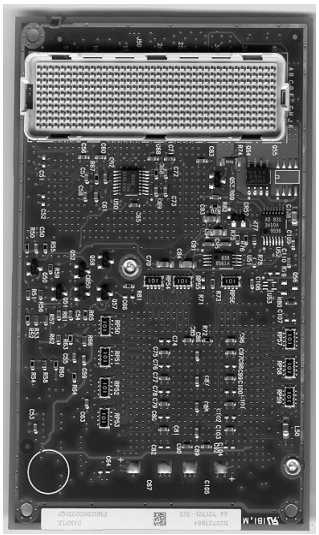
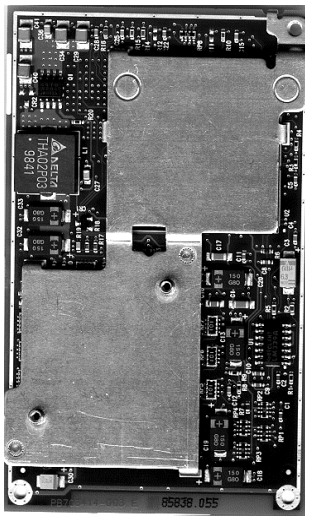
Pentium® II Processor with On-Die Cache – Low-Power Module

Datasheet

Product Features

- Processor core frequency of 333 MHz
- 256 Kbytes of on-die level 2 cache
- 66-MHz processor system bus speed
- Processor core voltage regulation supports input voltages from 5 V to 21 V
  - —Above 80 percent peak efficiency
- Integrated Active Thermal Feedback (ATF) system
  - —ACPI Specification Rev. 1.0 compliant
  - —Internal A/D – digital signaling (SMBus) across the module interface
  - —Programmable trip point interrupt or poll mode for temperature reading
- Supports a single AGP 66-MHz, 3.3 V device
- Intel® 82443BX Host Bridge/Controller
  - —DRAM controller supports EDO and SDRAM at 3.3 V
  - —Supports PCI CLKRUN# protocol
  - —SDRAM clock support and self-refresh of EDO or SDRAM during Suspend mode
  - —3.3 V only PCI bus control, Rev 2.1 compliant
- Thermal transfer plate on the processor and the 82443BX Host Bridge/Controller for heat dissipation





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Datasheet

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Revision History

Revision	Date	Description
001	June 1999	First release of this document.

1.0 Introduction

This document provides the technical information for integrating the Intel® Pentium® II Processor with On-Die Cache – Low-Power Module into the latest applied computing systems.

Building around this design gives the system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards.
- Provides an upgrade path from previous Intel modules using a standard interface.

2.0 Architecture Overview

A highly integrated assembly, the Low-Power Module contains the Pentium II Processor with On-Die Cache – Low Power core and its immediate system-level support. The Low-Power Module is offered with a core speed of 333 MHz. All processor speeds have a 66-MHz processor system bus (PSB) speed.

The PIIX4E PCI/ISA IDE Xcelerator bridge is one of two large-scale integrated devices of the Intel® 440BX AGPset. A design's system electronics must include a PIIX4E device to connect to the Low-Power Module. The PIIX4E provides extensive power management capabilities and supports the Intel® 82443BX Host Bridge/Controller, the second integrated device. Key features of the 82443BX Host Bridge/Controller include the DRAM controller, which supports EDO at 3.3 V with a burst read at 7-2-2-2 (60 nanoseconds) or SDRAM at 3.3 V with a burst read at 8-1-1-1 (66 MHz, CL=2). The 82443BX Host Bridge/Controller also provides a PCI CLKRUN# signal to request the PIIX4E to regulate the PCI clock on the PCI bus. The 82443BX clock enables Self Refresh mode of EDO or SDRAM during Suspend mode and is compatible with SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management. E_SMRAM mode supports write-back cacheable SMRAM up to 1 Mbyte.

A thermal transfer plate (TTP) on the 82443BX Host Bridge/Controller and the processor provides heat dissipation and a thermal attach point for the system manufacturer's thermal solution.

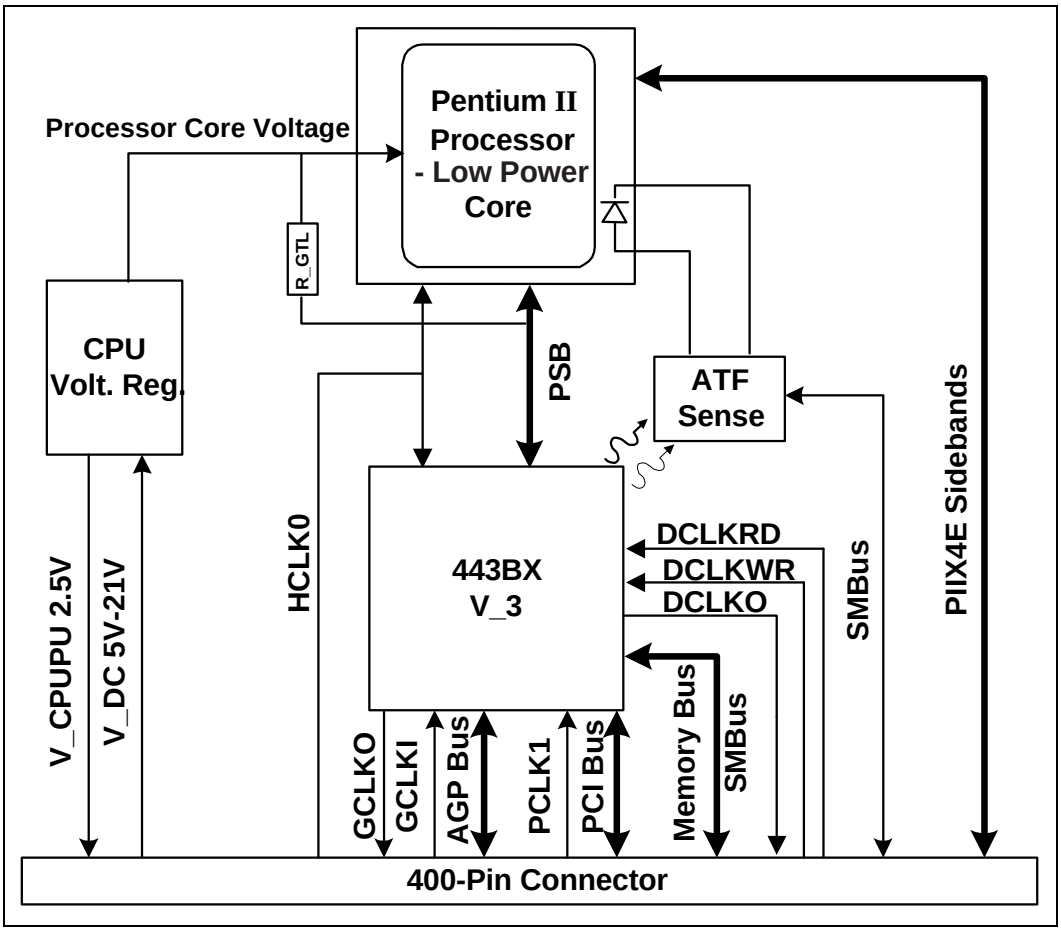
An on-board voltage regulator converts the system DC voltage to the processor's core and I/O voltage. Isolating the processor voltage requirements allows the system manufacturer to incorporate different processor variants into a single system.

Supporting input voltages from 5 V to 21 V, the processor core voltage regulation enables an above 80 percent peak efficiency and decouples processor voltage requirements from the system.

The Low-Power Module also incorporates Active Thermal Feedback (ATF) sensing, compliant to the *ACPI Specification Rev 1.0*. A system management bus (SMBus) supports the internal and external temperature sensing with programmable trip points.

Figure 1 illustrates the block diagram of the module.

Figure 1. Block Diagram of the Low-Power Module



3.0 Connector Interface

This section provides information on the signal groups and the corresponding pin information. The signals are defined for compatibility with future modules.

3.1 Signal Definitions

Table 1 provides a list of signals by category and the corresponding number of signals in each category. For proper signal termination, see the *Pentium® II Processor – Low Power Module Design Guide* (order number 273212).

Table 1. Connector Signal Summary

Signal Group	Number of Pins
Memory	109
AGP	60
PCI	58
Processor/PIIX4E Sideband	8
Geyserville Technology	4
Power Management	7
Clocks	9
Voltage: V_DC	20
Voltage: V_3S	9
Voltage: V_5	3
Voltage: V_3	16
Voltage: VCCAGP	4
Voltage: V_CPUPU	1
Voltage: V_CLK	1
ITP/JTAG	9
Module ID	4
Ground	45
Reserved	33
Total	**400**

3.1.1 Signal List

The following notations are used to denote signal type:

I	Input pin
O	Output pin
O D	Open-drain output pin requiring a pullup resistor
I D	Open-drain input pin requiring a pullup resistor
I/O D	Input/Open-drain output pin requiring a pullup resistor
I/O	Bidirectional input/output pin

The signal description also includes the type of buffer used for a particular signal:

GTL+	Open-drain GTL+ interface signal
PCI	PCI bus interface signals
AGP	AGP bus interface signals
CMOS	The CMOS buffers are low voltage TTL compatible signals with 3.3-V outputs with 5.0-V tolerant inputs.

3.1.2 Memory (109 Signals)

Table 2 lists the memory interface signals.

Table 2. Memory Signal Descriptions

Name	Type	Voltage	Description
MECC[7:0]	I/O CMOS	V_3	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. These pins are implemented by design but not tested on the module.
RASA[5:0]# or CSA[5:0]#	O CMOS	V_3	**Row Address Strobe (EDO):** These pins select the DRAM row. **Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
CASA[7:0]# or DQMA[7:0]	O CMOS	V_3	**Column Address Strobe (EDO):** These pins select the DRAM column. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10] MAB[12:11]# MAB[13]	O CMOS	V_3	**Memory Address (EDO/SDRAM):** This is the row and column address for DRAM. The 82443BX Host Bridge/Controller has two identical sets of address lines (MAA and MAB#). The module supports only the MAB set of address lines. For additional addressing features, please refer to the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.
MWEA#	O CMOS	V_3	**Memory Write Enable (EDO/SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	V_3	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCASA#	O CMOS	V_3	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock. This signal also allows Column access.
CKE[5:0]	O CMOS	V_3	**SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are deasserted, SDRAM enters power-down mode. Each row is individually controlled by its own clock enable.
MD[63:0]	I/O CMOS	V_3	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the module.

3.1.3 AGP (60 Signals)

Table 3 lists the AGP interface signals.

Table 3. AGP Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
GAD[31:0]	I/O AGP	V_3	**AGP Address/Data:** The standard AGP address and data lines. This bus functions in the same way as the PCI AD[31:0] bus. The address is driven with FRAME# assertion and data is driven or received in following clocks.
GC/BE[3:0]#	I/O AGP	V_3	**AGP Command/Byte Enable:** This bus carries the command information during AGP cycles when PIPE# is used. During an AGP write, this bus contains byte enable information. The command is driven with FRAME# assertion and byte enables corresponding to supplied or requested data are driven on the following clocks.
GFRAME#	I/O AGP	V_3	**AGP Frame:** Not used during AGP transactions. Remains deasserted by an internal pullup resistor. Assertion indicates the address phase of a PCI transfer. Negation indicates that the cycle initiator desires one more data transfer.
GDEVSEL#	I/O AGP	V_3	**AGP Device Select:** Same function as PCI DEVSEL#. It is not used during AGP transactions. The 82443BX Host Bridge/Controller drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
GIRDY#	I/O AGP	V_3	**AGP Initiator Ready:** Indicates the AGP compliant target is ready to provide *all* write data for the current transaction. Asserted when the initiator is ready for a data transfer.
GTRDY#	I/O AGP	V_3	**AGP Target Ready:** Indicates the AGP compliant master is ready to provide *all* write data for the current transaction. Asserted when the target is ready for a data transfer.
GSTOP#	I/O AGP	V_3	**AGP Stop:** Same function as PCI STOP#. It is not used during AGP transactions. Asserted by the target to request the master to stop the current transaction.
GREQ#	I AGP	V_3	**AGP Request:** AGP master requests for AGP.
GGNT#	O AGP	V_3	**AGP Grant:** Same function as on PCI. Additional information is provided on the ST[2:0] bus. PCI Grant: Permission is given to the master to use PCI.
GPAR	I/O AGP	V_3	**AGP Parity:** A single parity bit is provided over GAD[31:0] and GC/BE[3:0]. This signal is not used during AGP transactions.
PIPE#	I AGP	V_3	**Pipelined Request:** Asserted by the current master to indicate a full width address that is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted.
SBA[7:0]	I AGP	V_3	**Sideband Address:** This bus provides an additional conduit to pass address and commands to the 82443BX Host Bridge/Controller from the AGP master.
RBF#	I AGP	V_3	**Read Buffer Full:** Indicates if the master is ready to accept previously requested, low-priority read data.

Table 3. AGP Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
ST[2:0]	O AGP	V_3	**Status Bus:** Provides information from the arbiter to an AGP Master on what it may do. These bits only have meaning when GGNT is asserted.
ADSTB[B:A]	I/O AGP	V_3	**AD Bus Strobes:** Provide timing for double-clocked data on the GAD bus. The agent providing data drives these signals. These are identical copies of each other.
SBSTB	I AGP	V_3	**Sideband Strobe:** Provides timing for a sideband bus. The SBA[7:0] (AGP master) drives the sideband strobe.

3.1.4 PCI (58 Signals)

Table 4 lists the PCI interface signals.

Table 4. PCI Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
AD[31:0]	I/O PCI	V_3	**Address/Data:** The standard PCI address and data lines. The address is driven with FRAME# assertion and data is driven or received in the following clocks.
C/BE[3:0]#	I/O PCI	V_3	**Command/Byte Enable:** The command is driven with FRAME# assertion and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	V_3	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that the cycle initiator desires one more data transfer.
DEVSEL#	I/O PCI	V_3	**Device Select:** the 82443BX Host Bridge/Controller drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	V_3	**Initiator Ready:** Asserted when the initiator is ready for data transfer.
TRDY#	I/O PCI	V_3	**Target Ready:** Asserted when the target is ready for a data transfer.
STOP#	I/O PCI	V_3	**Stop:** Asserted by the target to request the master to stop the current transaction.
PLOCK#	I/O PCI	V_3	**Lock:** Indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, nonexclusive transactions may proceed. The 82443BX supports lock for processor initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	V_3	**PCI Request:** PCI master requests for PCI.
GNT[4:0]#	O PCI	V_3	**PCI Grant:** Permission is given to the master to use PCI.

Table 4. PCI Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
PHOLD#	I PCI	V_3	**PCI Hold:** This signal comes from the expansion bridge; it is the bridge request for PCI. The 82443BX Host Bridge/Controller will drain the DRAM write buffers, drain the processor-to-PCI posting buffers, and acquire the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	V_3	**PCI Hold Acknowledge:** This signal is driven by the 82443BX Host Bridge/Controller to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O PCI	V_3	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	I/O PCI	V_3	**System Error:** The 82443BX asserts this signal to indicate an error condition. Refer to the *Intel® 440BX AGPset: Host Bridge/Controller* datasheet for further information.
CLKRUN#	I/O D PCI	V_3	**Clock Run:** An open-drain output and input. The 82443BX Host Bridge/Controller requests the central resource (PIIX4E) to start or maintain the PCI clock by asserting CLKRUN#. The 82443BX Host Bridge/Controller three-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	V_3	**Reset:** When asserted, this signal asynchronously resets the 82443BX Host Bridge. The PCI signals also three-state, compliant with *PCI Rev 2.1 Specifications*.

3.1.5 Geyserville (4 Signals)

Table 5 lists the Geyserville signal definitions. The module does not support Geyserville technology. This section is included for those wishing to design for compatibility with future modules.

Table 5. Geyserville Descriptions

Name	Type	Voltage	Description
G_LO/HI#	I CMOS	V_3	**Geyserville State Transition**: Generated by the PIIX4E, this signal defines a Geyserville state change to the Geyserville state machine. This signal is not implemented on the module.
G_CPU_STP#	I CMOS	V_3	**Geyserville CPU_STP#**: The CPU_STP# signal gated by the Geyserville state machine becomes G_CPU_STP#. This signal is not implemented on the module.
VRCHGNG#	O CMOS	V_3	**Voltage Changing**: A Geyserville state machine signal that indicates that the actual state change is in progress – the VR setpoint has changed and the VR is settling. When this signal deasserts, the new state is sent to the processor. The system electronics will use this signal to generate an SCI to force a transition out of deep sleep. This signal is not implemented on the module.
G_SUS_STAT1#	O CMOS	V_3	**G_SUS_STAT1#:** The SUS_STAT1# signal gated by the Geyserville control logic. G_SUS_STAT1# should be used in place of the SUS_STAT1# signal in the system electronics design. This signal is not implemented on the module.

3.1.6 Processor/PIIX4E Sideband (8 Signals)

Table 6 lists the signals for the processor and the PIIX4E sideband signals. The voltage level for these signals is determined by V_CPUPU.

Table 6. Processor/PIIX4E Sideband Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
FERR#	O CMOS	V_CPUPU	**Numeric Coprocessor Error:** This pin functions as a FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is driven by the processor to the PIIX4E.
IGNNE#	I D CMOS	V_CPUPU	**Ignore Error:** This open-drain signal is connected to the Ignore Error pin on the processor and is driven by the PIIX4E.
INIT#	I D CMOS	V_CPUPU	**Initialization:** INIT# is asserted by the PIIX4E to the processor for system initialization. This signal is an open-drain.
INTR	I D CMOS	V_CPUPU	**Processor Interrupt:** INTR is driven by the PIIX4E to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open-drain.
NMI	I D CMOS	V_CPUPU	**Non-maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4E ISA bridge generates a NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open-drain.

Table 6. Processor/PIIX4E Sideband Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
A20M#	I D CMOS	V_CPUPU	**Address Bit 20 Mask:** When enabled, this open-drain signal causes the processor to emulate the address wraparound at one MB, which occurs on the Intel 8086 processor.
SMI#	I D CMOS	V_CPUPU	**System Management Interrupt:** SMI# is an active low synchronous output from the PIIX4E that is asserted in response to one of many enabled hardware or software events. The SMI# open-drain signal can be an asynchronous input to the processor. However, in this chip set SMI# is synchronous to PCLK.
STPCLK#	I D CMOS	V_CPUPU	**Stop Clock:** STPCLK# is an active low synchronous open-drain output from the PIIX4E that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted, it responds by entering a low power state (Quick Start). The processor will only exit this mode when this signal is deasserted.

3.1.7 Power Management (7 Signals)

Table 7 lists the power management signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface. Although this interface is currently used solely for the digital thermal sensor, the SMBus contains reserved serial addresses for future use. See “Thermal Sensor Configuration Register” on page 41 for more details.

Table 7. Power Management Signal Descriptions

Name	Type	Voltage	Description
SUS_STAT1#	I CMOS	V_3ALWAY†	**Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4E. It provides information on host clock status and is asserted during all suspend states.
VR_ON	I CMOS	V_3	**VR_ON:** Voltage regulator ON. This 3.3V (5V tolerant) signal controls the operation of the voltage regulator. VR_ON should be generated as a function of the PIIX4E SUSB# signal which is used for controlling the “Suspend State B” voltage planes. This signal should be driven by a digital signal with a rise/fall time of less than or equal to 1 µs. Refer to “Voltage Signal Definition and Sequencing” on page 33. (VIL (max)=0.4V, VIH (min)=3.0V).
VR_PWRGD	O	V_3	**VR_PWRGD:** This signal is driven high by the module to indicate that the voltage regulator is stable. The signal is pulled low using a 100 KΩ resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
BXPWROK	I CMOS	V_3	**Power OK to BX:** This signal must go active 1 ms after the V_3 power rail is stable, and 1 ms prior to deassertion of PCIRST#.
SM_CLK	I/O D CMOS	V_3	**Serial Clock:** This clock signal is used on the SMBus interface to the digital thermal sensor.
SM_DATA	I/O D CMOS	V_3	**Serial Data:** Open-drain data signal on the SMBus interface to the digital thermal sensor.
ATF_INT#	O D CMOS	V_3	**ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor.

† V_3ALWAYS: 3.3 V supply. It is generated whenever V_DC is available and supplied to PIIX4E resume well.

3.1.8 Clock (9 Signals)

Table 8 lists the clock signals.

Table 8. Clock Signal Descriptions

Name	Type	Voltage	Description
PCLK	I PCI	V_3	**PCI Clock In:** PCLK is an input to the module and is one of the system's PCI clocks. This clock is used by all of the 82443BX Host Bridge/Controller logic in the PCI clock domain. This clock is stopped when the PIIX4E PCI_STP# signal is asserted and/or during all suspend states.
HCLK[1:0]	I CMOS	V_CLK	**Host Clock In:** These clocks are inputs to the module from the CK97-M clock source. The processor and the 82443BX Host Bridge/Controller use HCLK[0]. This clock is stopped when the PIIX4E CPU_STP# signal is asserted and/or during all suspend states.
DCLKO	O CMOS	V_3	**SDRAM Clock Out:** A 66-MHz SDRAM clock reference generated internally by the 82443BX Host Bridge/Controller onboard PLL. It feeds an external buffer that produces multiple copies for the SO-DIMMs.
DCLKRD	I CMOS	V_CLK	**SDRAM Read Clock:** Feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge/Controller uses this clock when reading data from the SDRAM array. This signal is not implemented on the module.
DCLKWR	I CMOS	V_CLK	**SDRAM Write Clock:** Feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge/Controller uses this clock when writing data to the SDRAM array.
GCLKIN	I CMOS	V_3	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKO signal.
GCLKO	O CMOS	V_3	**AGP Clock Out:** This signal is generated by the 82443BX Host Bridge/Controller onboard PLL from the HCLK0 host clock reference. The frequency of GCLKO is 66 MHz. The GCLKO output is used to feed both the PLL reference input pins on the 82443BX Host Bridge/Controller and the AGP device. The board layout must maintain complete symmetry on loading and trace geometry to minimize AGP clock skew.
FQS	O CMOS	V_CLK	**Frequency Select:** This output signal provides the status of the host clock frequency to the system electronics. This signal is static and is pulled either low or high to the V_CLK voltage supply through a 10-KΩ resistor. This module is designed for the 66-MHz strapping option shown below. FQS=0 indicates 66 MHz FQS=1 indicates 100 MHz (for future modules)

3.1.9 Voltages (54 Signals)

Table 9 lists the voltage signal definitions.

Table 9. Voltage Descriptions

Name	Type	Number of Pins	Description
V_DC	I	20	**DC Input:** 5 V-21 V
V_3S	I	9	**SUSB# controlled 3.3 V:** This rail is not used on the module. It is a power managed 3.3 V supply. An output of the voltage regulator on the system electronics. This rail is off during STR, STD, and SOff.
V_5	I	3	**SUSC# controlled 5 V:** Power managed 5 V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and SOff.
V_3	I	16	**SUSC# controlled 3.3 V:** Power managed 3.3 V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and SOff.
VCCAGP	I	4	**AGP I/O Voltage**: This voltage rail is not implemented on module. Intel recommends that this voltage rail be connected to V_3 on the system electronics.
V_CPUPU	O	1	**Processor I/O Ring:** Driven by the module to power processor interface signals such as the PIIX4E open-drain pullups for the processor/PIIX4E sideband signals.
V_CLK	O	1	**Processor Clock Rail:** Driven by the module to power CK100-M VDDCPU rail.

3.1.10 ITP/JTAG (9 Signals)

Table 10 lists the ITP/JTAG signals, which the system manufacturer can use to implement a JTAG chain and an ITP port if desired.

Table 10. ITP/JTAG Pins

Name	Type	Voltage	Description
TDO	O	V_CPUPU	**JTAG Test Data Out:** Serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	V_CPUPU	**JTAG Test Data In:** Serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_CPUPU	**JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	V_CPUPU	**JTAG Test Clock:** Testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_CPUPU	**JTAG Test Reset:** Asynchronously resets the TAP controller in the processor.
FS_RESET#	O	GTL+	**Processor Reset:** Processor reset status to the ITP.
VTT	O	V_CORE	**GTL+ Termination Voltage:** Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON pin is pulled up using a 1-KΩ resistor to VTT.
FS_PREQ#	I	V_CPUPU	**Debug Mode Request:** Driven by the ITP and makes request to enter debug mode.
FS_PRDY#	O	GTL+	**Debug Mode Ready:** Driven by the processor and informs the ITP that the processor is in debug mode.

NOTE: DBREST# (reset target system) on the ITP debug port can be “logically ANDed” with VR_PWRGD TO PIIX4E’s PWROK

3.1.11 Miscellaneous (82 Signals)

Table 11 lists the miscellaneous signal pins.

Table 11. Miscellaneous Pins

Name	Type	Number	Description
Module ID[3:0]	O CMOS	4	**Module Revision ID**: These pins track the revision level of the module. A 100-KΩ pullup resistor to V_3S must be placed on the system electronics for these signals. See “Labeling Information” on page 49 for more information.
Ground	I	45	Ground.
Reserved	RSVD	33	Unallocated Reserved pins and should not be connected.

3.2 Connector Pin Assignments

Table 12 and Table 13 list the signals for each pin of the connector to the system electronics. Refer to “Pin and Pad Assignments” on page 21 for the pin assignments of the pads on the connector.

Table 12. Connector Pin Assignments – Rows A Through E (Sheet 1 of 2)

Pin Number	Row A	Row B	Row C	Row D	Row E
1	SBA5	ADSTBB	GND	GAD31	SBA7
2	GAD25	GAD24	SBA6	SBA4	SBA0
3	GAD30	GAD29	GAD26	GAD27	GND
4	GND	VCCAGP	GAD4	GAD6	GAD8
5	RBF#	GAD1	GAD3	GAD5	GC/BE0#
6	BXPWROK	Reserved	GAD2	ADSTBA	GND
7	MD0	MD1	V_3	CLKRUN#	GAD7
8	MD2	MD33	GND	MD32	GAD0
9	MD36	MD4	MD3	MD35	MD34
10	MD7	MD38	MD37	MD6	MD5
11	MD41	MD42	MD40	MD39	MD8
12	MD43	MD11	GND	MD10	MD9
13	MD14	MD45	MD44	MD13	MD12
14	MECC4	MECC0	MD15	MD47	MD46
15	SCASA#	MWEA#	MECC5	Reserved	GND
16	GND	MID1	DQMA0	DQMA1	Reserved
17	V_3	DQMA4	MID0	DQMA5	CSA0#
18	CSA1#	CSA2#	CSA4#	CSA3#	GND
19	SRASA#	CSA5#	MAB0#	MAB1#	Reserved
20	Reserved	Reserved	MAB2#	Reserved	MAB3#
21	Reserved	MAB4#	GND	Reserved	MAB6#
22	Reserved	Reserved	MAB5#	Reserved	MAB7#

Table 12. Connector Pin Assignments – Rows A Through E (Sheet 2 of 2)

Pin Number	Row A	Row B	Row C	Row D	Row E
23	MAB8#	Reserved	Reserved	MAB9#	MAB10
24	Reserved	MAB11#	MAB12#	Reserved	DCLKO
25	MAB13	V_3	GND	CKE0	DCLKRD
26	CKE1	MID2	CKE3	CKE4	GND
27	CKE5	CKE2	MID3	G_CPU_STP#	VRCHGNG#
28	Reserved	G_LO/HI#	DQMA2	DCLKWR	GND
29	GND	VTT	Reserved	FS_PREQ#	DQMA3
30	FS_RESET#	V_3	MD26	GND	MD25
31	FS_PRDY#	GND	MD58	MD57	MD60
32	G_SUS_STAT1#	SMCLK	TDO	TCLK	FERR#
33	Reserved	SMDAT	TDI	TMS	IGNNE#
34	Reserved	FQS	Reserved	TRST#	ATF_INT#
35	Reserved	V_5	V_3S	V_3S	V_3S
36	V_CPUPU	V_5	V_3S	V_3S	V_3S
37	V_CLK	V_5	V_3S	V_3S	V_3S
38	Reserved	Reserved	Reserved	Reserved	Reserved
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

Table 13. Connector Pin Assignments – Rows F Through K (Sheet 1 of 2)

Pin Number	Row F	Row G	Row H	Row J	Row K
1	GREQ#	GND	PIPE#	SBA3	GND
2	ST0	ST1	SBA1	SBSTB	GCLKI
3	GGNT#	ST2	SBA2	GND	GCLKO
4	GAD13	GSTOP#	GAD16	GAD20	GAD23
5	GAD12	GPAR	GAD18	GAD17	GC/BE3#
6	GAD10	GAD15	GFRAME#	GND	GAD22
7	GAD11	GC/BE1#	GTRDY#	GC/BE2#	GAD21
8	GAD9	GAD14	GDEVSEL#	GIRDY#	GAD19
9	GND	VCCAGP	GND	VCCAGP	GAD28
10	AD0	AD4	AD2	AD3	AD1
11	GND	C/BE0#	AD6	GND	AD5
12	VCCAGP	AD10	AD7	AD8	AD9
13	MECC1	AD13	GND	AD12	AD11
14	SERR#	PAR	AD15	C/BE1#	AD14
15	AD16	TRDY#	STOP#	DEVSEL#	PLOCK#
16	AD19	GND	AD17	GND	AD18

Table 13. Connector Pin Assignments – Rows F Through K (Sheet 2 of 2)

Pin Number	Row F	Row G	Row H	Row J	Row K
17	AD23	AD30	AD24	C/BE2#	AD21
18	AD27	AD22	C/BE3#	AD26	PCLK
19	PCI_RST#	GND	AD20	AD28	GND
20	Reserved	PHOLD#	AD31	AD29	AD25
21	IRDY#	FRAME#	GND	REQ1#	REQ0#
22	GND	GNT2#	REQ2#	REQ3#	GNT3#
23	GNT1#	GNT4#	GNT0#	REQ4#	GND
24	GND	PHLDA#	GND	V_3	MD59
25	DQMA6	MECC7	MD50	MD51	MD54
26	MECC2	MD48	MD18	MD52	MD24
27	DQMA7	MD16	MD19	GND	MD23
28	MECC6	MD17	MD21	MD53	MD55
29	MECC3	MD49	MD20	MD22	MD56
30	MD27	MD28	GND	MD62	MD63
31	GND	MD29	MD61	MD30	MD31
32	SMI#	INTR	VR_ON	GND	GND
33	NMI	SUS_STAT1#	VR_PWRGD	GND	HCLK0
34	A20M#	STPCLK#	INIT#	GND	GND
35	V_3	V_3	V_3	GND	HCLK1
36	V_3	V_3	V_3	GND	GND
37	V_3	V_3	V_3	V_3	V_3
38	Reserved	Reserved	Reserved	Reserved	Reserved
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

3.3 Pin and Pad Assignments

The module connector has 400 pins, a 1.27-millimeter pitch, and a BGA-style surface mount. Refer to *"Height Restrictions" on page 44* for connector size information. Figure 2 shows the pad assignments of the module connector.

Figure 2. 400-Pin Connector Footprint Pad Numbers

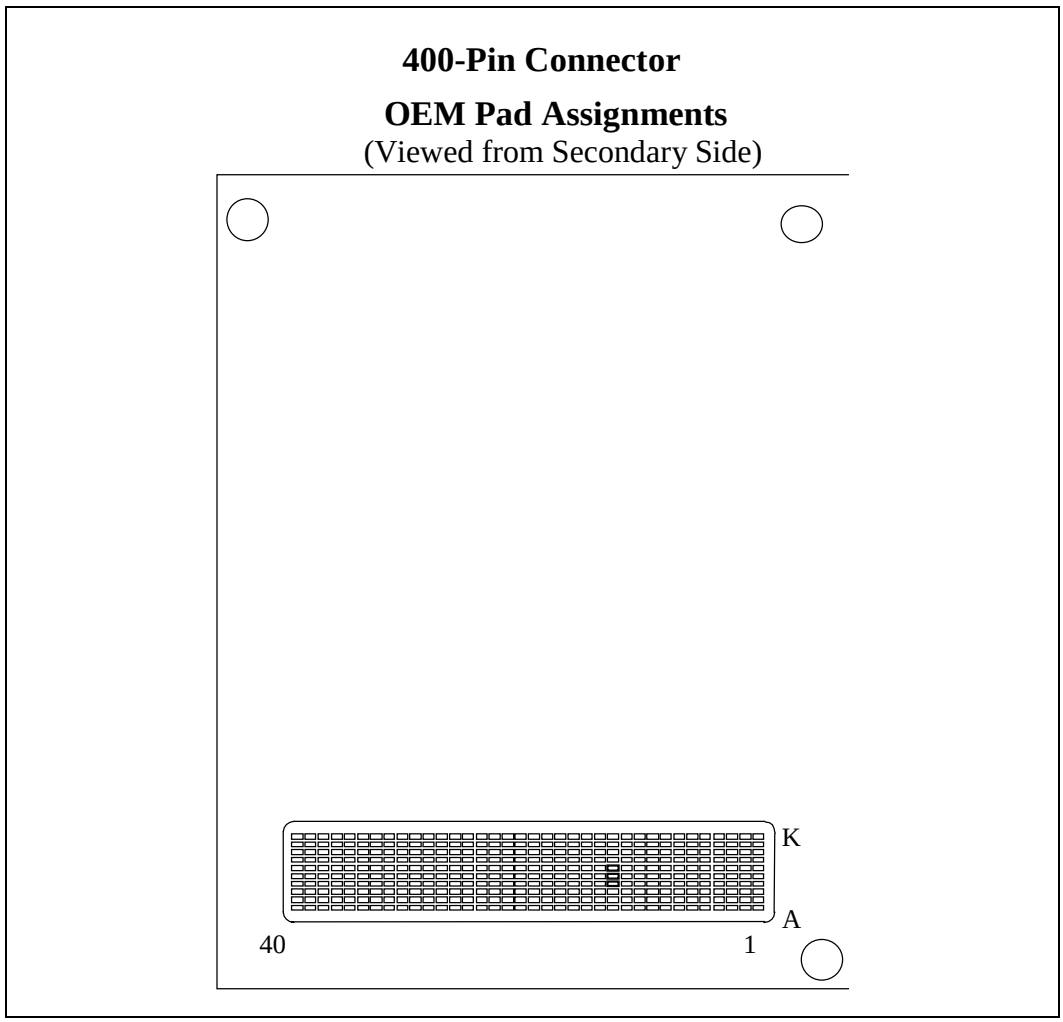


Table 14 summarizes some of the key specifications for the connector.

Table 14. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Copper Alloy
	Housing	Thermo Plastic Molded Compound: LCP
Electrical	Current	0.5 A
	Voltage	50 VAC
	Insulation Resistance	100 MΩ minimum at 500 VDC
	Termination Resistance	10 mΩ maximum
	Capacitance	5 pF maximum per contact
Mechanical	Mating Cycles	50 cycles
	Connector Mating Force	2.0 oz maximum per contact
	Contact Unmating Force	1.5 oz minimum per contact

4.0 Functional Description

4.1 Pentium® II Processor With On-Die Cache – Low-Power Module

The module is offered at a core speed of 333 MHz, with a 66-MHz processor system bus speed.

4.2 L2 Cache

The on-die L2 cache is 256 Kbytes, is four-way set associative, and runs at the speed of the processor core.

4.3 The 82443BX Host Bridge/Controller

Intel's 82443BX Host Bridge/Controller is a highly integrated device that combines the bus controller, the DRAM controller, and the PCI bus controller into one component. The 82443BX Host Bridge/Controller has multiple power management features designed specifically for low-power systems such as:

- CLKRUN#, a feature that enables controlling of the PCI clock on or off.
- The 82443BX Host Bridge/Controller suspend modes, which include Suspend-to-RAM (STR), Suspend-to-Disk (STD), and Power-On-Suspend (POS).
- System Management RAM (SMRAM) power management modes, which include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets. E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1 Mbyte. To minimize power

consumption while the system is idle, the internal 82443BX Host Bridge/Controller clock is turned off (gated off) when there is no processor and PCI activity. This is accomplished by setting the G_CLK enable bit in the power management register in the 82443BX through the system BIOS.

4.3.1 Memory Organization

The memory interface of the 82443BX Host Bridge/Controller is available at connector. This allows for the following:

- One set of memory control signals, sufficient to support up to three SO-DIMM sockets and six banks of SDRAM at 66 MHz.
- One CKE signal for each bank.

Memory features not supported by the 82443BX Host Bridge/Controller standard mode are:

- Support for eight banks of memory.
- Second set of memory address lines (MAA[13:0]).

DRAM technologies supported by the 82443BX Host Bridge/Controller include EDO and SDRAM. These memory types may not be mixed in the system, so that all DRAM in all rows (RAS[5:0]#) must be of the same technology. The 82443BX Host Bridge/Controller targets 60 nanoseconds EDO DRAMs and 66-MHz SDRAMs.

The module's clocking architecture supports the use of SDRAM. Tight timing requirements of the 66-MHz SDRAM clocks allow all host and SDRAM clocks to be generated from the same clocking architecture. For complete details about using SDRAM memory, and for trace length guidelines, see the *Pentium® II Processor – Low Power Module at 266 MHz 66 MHz SDRAM DIMM Routing Guidelines* (order number 273230). Refer to the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet for details on memory device support, organization, size, and addressing.

4.3.2 Reset Strap Options

Several strap options on the memory address bus define the behavior of the module after reset. Other straps can override the default settings. Table 15 shows the straps and their implementation.

Table 15. Configuration Straps for the 82443BX Host Bridge/Controller

Signal	Function	Module Default Setting	Optional Override on System Electronics
MAB[12]#	Host Frequency Select	No strap–66 MHz default.	None
MAB[11]#	In Order Queue Depth	No strap–maximum queue depth is set, i.e., 8.	None
MAB[10]	Quick Start Select	Strapped high on the module for Quick Start mode.	None
MAB[9]#	AGP disable	No strap–AGP is enabled.	Pull up this signal to disable the AGP interface.
MAB[7]#	MM Config	No strap-standard mode.	None
MAB[6]#	Host Bus Buffer Mode Select	Strapped high on the module for PSB buffers.	None

4.3.3 PCI Interface

The PCI interface of the 82443BX Host Bridge/Controller is available at the connector. The 82443BX Host Bridge/Controller supports the PCI Clockrun protocol for PCI bus power management. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface.

The 82443BX Host Bridge/Controller is responsible for arbitrating the PCI bus. With the module connector, the 82443BX Host Bridge/Controller can support up to five PCI bus masters. There are five PCI Request/Grant pairs, REQ[4:0]# and GNT[4:0]#, available on the connector to the manufacturer's system electronics.

Note: The PCI interface on the module connector is 3.3 V only. 5 V PCI devices are not supported such as all devices that drive outputs to a 5_{Vt} nominal V_{oh} level.

The 82443BX Host Bridge/Controller is compliant with the PCI Rev. 2.1 specification, which improves the worst case PCI bus access latency from earlier PCI specifications. The 82443BX Host Bridge/Controller supports only Mechanism #1 for accessing PCI configuration space, as detailed in the PCI specification. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 82443BX Host Bridge/Controller is always device #0, AD11 will never be asserted during PCI configuration cycles as an IDSEL. The 82443BX reserves AD12 for the AGPbus. Thus, AD13 is the first available address line usable as an IDSEL. Intel recommends that AD18 be used by the PIIX4E.

4.3.4 AGP Interface

The 82443BX Host Bridge/Controller is compliant with the AGP Interface Specification Rev 1.0, which supports an asynchronous AGP interface coupling to the 82443BX core frequency. The AGP interface can achieve real data throughput in excess of 500 Mbytes/s using an AGP 2X graphics device. Actual bandwidth may vary depending on specific hardware and software implementations.

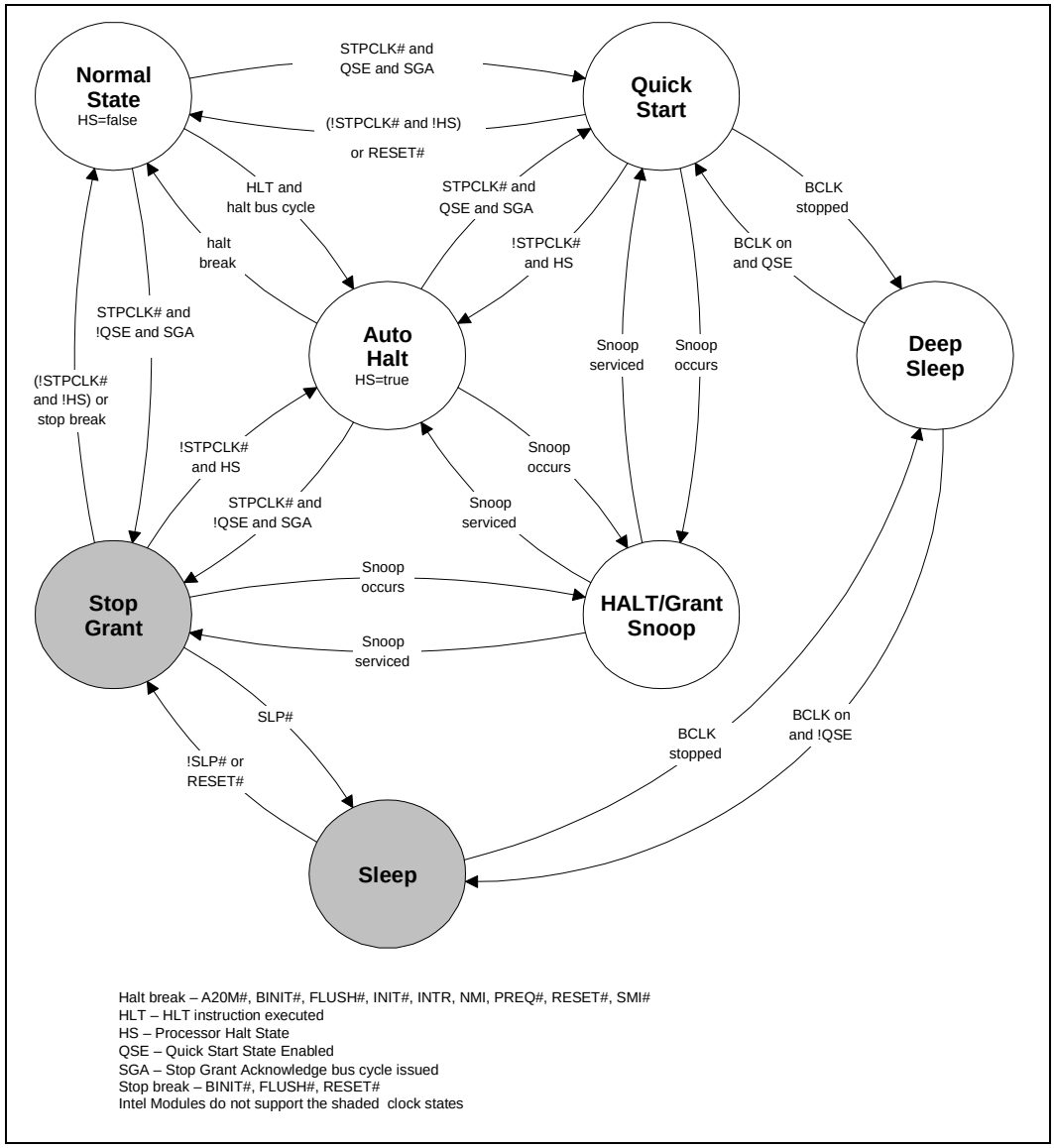
4.4 Power Management

4.4.1 Clock Control Architecture

The clock control architecture is optimal for low-power designs. The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep states. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low-power, low-exit latency clock state that can be used for hardware controlled "idle" states. The Deep Sleep State provides an extremely low power state that can be used for "Power-on Suspend" states, which is an alternative to shutting off the processor's power. The exit latency of the Deep Sleep State has been reduced to 30 µs. The Stop Grant and Sleep states are not available on the module since these states are intended for desktop or server systems. The Stop Grant state and the Quick Start clock state are mutually exclusive. For example, a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. Strapping the A15# signal enables the Quick Start state to ground at Reset. Otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state. The Stop Grant state is useful for SMP platforms and is not supported on the module. The Quick Start state is available on the module and provides a significantly lower power level.

Figure 3 provides an illustration of the clock control architecture. State transitions not shown in Figure 3 are neither recommended nor supported

Figure 3. Clock Control States



4.4.2 Normal State

This is the normal operating mode where the processor's core clock is running and the processor is actively executing instructions.

4.4.3 Auto Halt State

This is a low power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state will cause the processor to transition to the Stop Grant state or the Quick Start state, where a Stop Grant Acknowledge bus cycle will be issued. Deasserting STPCLK# will cause the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# (System Management Interrupt) is recognized in the Auto Halt state. The return from the SMI handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information. No Halt bus cycle is issued when returning to the Auto Halt state from System Management Mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After flushing the on-chip, the processor will return to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

4.4.4 Stop Grant State

Important: This state is not available on the module.

The processor enters this mode with the assertion of the STPCLK# signal when it is configured for Stop Grant state (via the A15# strapping option). The processor is still able to respond to snoop requests and latch interrupts. Latched interrupts will be serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event will be latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal, or the occurrence of a stop break event (a BINIT#, FLUSH#, or RESET# assertion).

The processor will return to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion will cause the processor to immediately initialize itself. However, the processor will stay in the Stop Grant state after initialization until STPCLK# is deasserted. If the FLUSH# signal is asserted, the processor will flush the on-chip caches and return to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of SMI#, INIT#, INTR, and NMI (or LINT[1:0]) will be latched by the processor. These latched events will not be serviced until the processor returns to the Normal state. Only one of each event will be recognized upon return to the Normal state.

4.4.5 Quick Start State

This is a mode entered by the processor with the assertion of the STPCLK# signal when it is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state the processor is only capable of acting on snoop transactions generated by the PSB priority device. Because of its snooping behavior, Quick Start can only be used in single processor configurations.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# and BINIT# assertions. In the Quick Start state, the processor will not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion will cause the processor to immediately initialize itself, but the processor will stay in the Quick Start state after initialization until STPCLK# is deasserted.

4.4.6 HALT/Grant Snoop State

The processor will respond to snoop transactions on the PSB while in the Auto Halt, Stop Grant, or Quick Start state. When a snoop transaction is presented on the system bus, the processor will enter the HALT/Grant Snoop state. The processor will remain in this state until the snoop has been serviced and the PSB is quiet. After the snoop has been serviced, the processor will return to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state (except for those signal transitions that are required to perform the snoop).

4.4.7 Sleep State

Important: This state is not available on the module.

The Sleep state is a very low power state in which the processor maintains its context and the phase locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal state or the Auto Halt state.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state, then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in the Sleep state or transitioning into or out of the Sleep state. Input signal changes at these times will cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state the processor can enter its lowest power state, the Deep Sleep state. Removing the processor's input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

4.4.8 Deep Sleep State

The Deep Sleep state is the lowest power mode the processor can enter while maintaining its context. Stopping the BCLK input to the processor enters the Deep Sleep state, while it is in the Sleep state or the Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

The processor will return to the Sleep state or the Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a 30-ms delay after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on when transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion will result in unpredictable behavior.

Table 16. Clock State Characteristics

Clock State	Exit Latency	Processor Power	Snooping	System Uses
Normal	N/A	Varies	Yes	Normal program execution.
Auto Halt	Approximately 10 bus clocks	1.2 W	Yes	S/W controlled entry idle mode.
Stop Grant[1]	10 bus clocks	1.2 W	Yes	H/W controlled entry/exit throttling.
Quick Start	**Through snoop**, to HALT/Grant Snoop state: immediate **Through STPCLK#**, to Normal state: 10 bus clocks	0.5 W	Yes	H/W controlled entry/exit throttling.
HALT/Grant Snoop	A few bus clocks after the end of snoop activity.	Not specified	Yes	Supports snooping in the low power states.
Sleep[1]	To Stop Grant state 10 bus clocks	0.5 W	No	H/W controlled entry/exit desktop idle mode support.
Deep Sleep	30 ms	150 mW	No	H/W controlled entry/exit powered-on suspend support.

NOTES:
1. The module does not support the Sleep and Stop Grant clock control states.
2. Not 100% tested. Specified at 50° C by design/characterization.

4.5 Typical POS/STR Power

Table 17 shows the typical POS/STR power values.

Table 17. POS/STR Power

State	Typical Module Power
POS	0.475 W
STR	0.018 W

NOTE: These are average values of measurement and are guidelines only.

4.6 Electrical Requirements

The following section provides information on the electrical requirements for the module.

4.6.1 DC Requirements

Table 18 provides DC power supply design criteria.

Table 18. Power Supply Design Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{DC}	DC Input Voltage	5.0	12.0	21.0	V	
I_{DC}[1,2]	DC Input Current	0.1	0.9	3.5	A	
$I_{DC\text{-}Surge}$	Maximum Surge Current for V_{DC}			17.3	A	
$I_{DC\text{-}Leakage}$[3]	Typical Leakage Current for V_{DC}		4.0		µA	(At 25° C)
V_5	Power Managed 5V Voltage Supply	4.75	5.0	5.25	V	
I_5	Power Managed 5V Current	17	32	60	mA	
$I_{5\text{-}Surge}$	Maximum Surge Current for V_5			0.6	A	
$I_{5\text{-}Leakage}$	Typical Leakage Current for V_5		1.0		µA	
V_3	Power Managed 3.3V Voltage Supply	3.135	3.3	3.465	V	
I_3	Power Managed 3.3V Current	0.8	1.2	2.0	A	
$I_{3\text{-}Surge}$	Maximum Surge Current for V_3			2.8	A	
$I_{3\text{-}Leakage}$	Typical Leakage Current for V_3		1.1		mA	
V_{CPUPU}	Processor I/O Ring Voltage	2.375	2.5	2.625	V	± 0.125
I_{CPUPU}[4]	Processor I/O Ring Current	0	10	20	mA	
V_{CLK}	Processor Clock Rail Voltage	2.375	2.5	2.625	V	± 0.125
I_{CLK}[4]	Processor Clock Rail Current	24.0	35.0	80	mA	

NOTES:
1. V_DC is set for 12 V in order to determine typical V_DC current.
2. V_DC is set for 5 V in order to determine maximum V_DC current.
3. Leakage current that can be expected when VR_ON is deactivated and V_DC is still applied.
4. These values are system dependent.

4.6.2 AC Requirements

Table 19 shows the BCLK AC requirements.

Table 19. AC Specifications at the Processor Core Pins

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1,2]
PSB Frequency[3]		66.67		MHz		All processor core frequencies
T1: BCLK Period[3,4]		15.0		ns		
T2: BCLK Period Stability[5,6,7]			±250	ps		
T3: BCLK High Time	5.3			ns		At >1.8 V
T4: BCLK Low Time	5.3			ns		At <0.7V
T5: BCLK Rise Time[7]	0.175		0.875	ns		(0.9 V-1.6 V)
T6: BCLK Fall Time[7]	0.175		0.875	ns		(1.6 V–0.9 V)

NOTES:
1. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
2. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
3. The internal core clock frequency is derived from the PSB clock. The PSB clock to core clock ratio is determined during initialization as described and is predetermined by the module.
4. The BCLK period allows a +0.5 ns tolerance for clock driver variation. See the *CK97 Clock Synthesizer/Driver Specification* for further information.
5. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
6. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The -20 dB attenuation point, as measured into a 10 pF to a 20 pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CK97 Clock Synthesizer/Driver Specification* for further details.
7. Not 100% tested. Specified by design characterization as a clock driver requirement.

4.6.2.1 PSB Clock Signal Quality Specifications and Measurement Guidelines

Table 20 describes the signal quality specifications at the processor core for the processor system bus (PSB) clock (BCLK) signal.

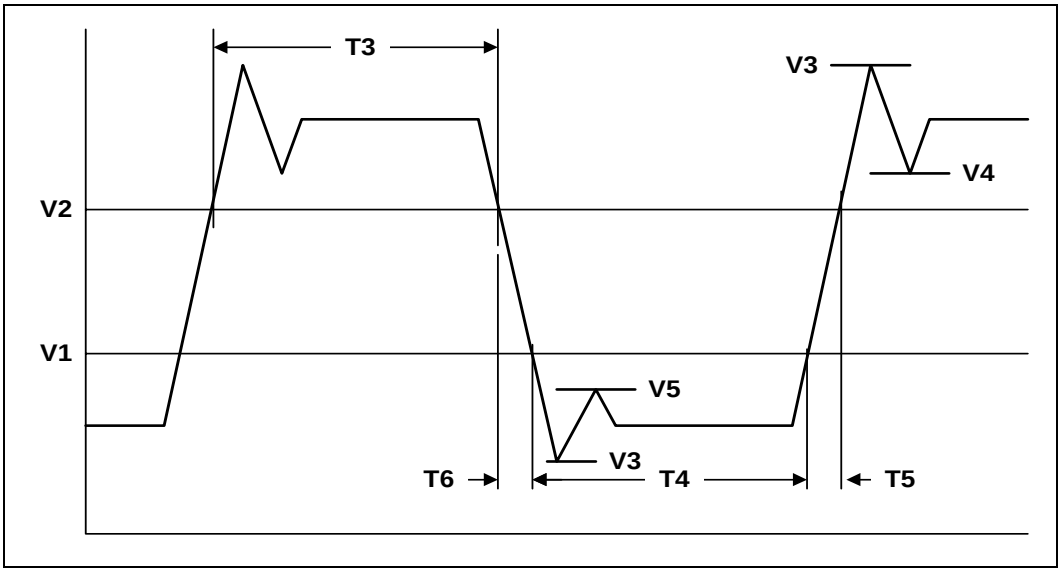
Figure 4 describes the signal quality waveform for the PSB clock at the processor core pins.

Table 20. BCLK Signal Quality Specifications at the Processor Core

T# Parameter[1,5]	Min	Nom	Max	Unit
V1: BCLK V_{IL}[2]			0.7	V
V2: BCLK V_{IH}[2]	1.8			V
V3: V_{IN} Absolute Voltage Range[3]	–0.8		3.5	V
V4: Rising Edge Ringback[4]	1.8			V
V5: Falling Edge Ringback[4]			0.7	V
BCLK rising/falling slew rate	0.8		4	V/ns

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all modules.
2. BCLK must rise/fall monotonically between $V_{IL,BCLK}$ and $V_{IH,\ BCLK}$.
3. This is the processor PSB clock overshoot and undershoot specification for a 66-MHz PSB operation.
4. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits.
5. For proper signal termination, refer to the *Pentium® II Processor – Low Power Module at 266 MHz Design Guide* (order number 273212).

Figure 4. BCLK, TCK, PICCLK Generic Clock Waveform at the Processor Core Pins



4.7 Voltage Regulator

The DC voltage regulator (DC/DC converter) provides the appropriate core voltage, the I/O ring voltage, and the sideband signal pullup voltage for the module. The voltage range is 5 V to 21 V.

4.7.1 Voltage Regulator Efficiency

Table 21 lists the voltage regulator efficiencies.

Table 21. Typical Voltage Regulator Efficiency

Icore, A[3]	V_DC, V	I_DC, A[2]	Efficiency[1]
1	5.0	0.370	82.8%
2	5.0	0.702	88.8%
3	5.0	1.044	89.8%
4	5.0	1.404	89.7%
5	5.0	1.762	88.1%
6	5.0	2.144	86.4%
7	5.0	2.528	85.0%
1	12.0	0.159	79.7%
2	12.0	0.295	87.0%
3	12.0	0.438	87.8%
4	12.0	0.584	87.3%
5	12.0	0.736	86.1%
6	12.0	0.890	84.9%
7	12.0	1.043	83.8%
1	21.0	0.091	79.3%
2	21.0	0.170	86.0%
3	21.0	0.253	87.3%
4	21.0	0.340	85.3%
5	21.0	0.429	84.1%
6	21.0	0.519	82.9%
7	21.0	0.617	80.7%

NOTES:
1. These efficiencies will change with future voltage regulators that accommodate wider ranges of input voltages.
2. With V_DC applied and the voltage regulator off, typical leakage is 0.3 mA with a maximum of 0.7 mA.
3. Icore indicates the CPU core current being drawn during test and measurement.

4.7.2 Control of the Voltage Regulator

The VR_ON pin turns the DC voltage regulator on or off. The VR_ON pin should be controlled as a function of the SUSB#, which controls the system's power planes. VR_ON should switch high only when the following conditions are met: V_5(s) ≥ 4.5 V and V_DC ≥ 4.75 V.

Caution: Turning on VR_ON prior to meeting these conditions will severely damage the module**.**

The VR_PWRGD signal indicates that the voltage regulator power is operating at a stable voltage level. Use VR_PWRGD on the system electronics to control power inputs and to gate PWROK to the PIIX4E.

Table 22 lists the voltage signal definitions and sequences, and Figure 5 shows the signal sequencing and the voltage planes sequencing required for normal operation of the module.

4.7.2.1 Voltage Signal Definition and Sequencing

Table 22. Voltage Signal Definitions and Sequences

Signal	Source	Definitions and Sequences
V_DC	System Electronics	V_DC is required to be between 5 V and 21 V DC and is driven by the system electronics' power supply. V_DC powers the module's DC-to-DC converter for the processor core and I/O voltages. The module cannot be hot inserted or removed while V_DC is powered on.
V_3	System Electronics	V_3 is supplied by the system electronics for the 82443BX.
V_5	System Electronics	V_5 is supplied by the system electronics for the 82443BX's 5 V reference voltage and the module's voltage regulator.
VR_ON	System Electronics	VR_ON is a 3.3 V (5 V tolerant) signal that enables the module's voltage regulator circuit. When driven active high the voltage regulator circuit is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 µs. (V_{IL} (max)=0.4V, V_{IH} (min)=3.0V).
V_CORE (also a host bus GTL+ termination voltage VTT)	Module	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the module and is driven to the core voltage of the processor. It is also used as the host bus GTL+ termination voltage, known as VTT.
VR_PWRGD	Module	Upon sampling the voltage level of V_CORE (minus tolerances for ripple), VR_PWRGD is driven active high. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON, then the system electronics should deassert VR_ON. After V_CORE is stabilized, VR_PWRGD will assert to logic high (3.3V). This signal *must not be pulled up* by the system electronics. VR_PWRGD should be "ANDed" with V_3s to generate the PIIX4E input signal, PWROK. The system electronics should monitor VR_PWRGD to verify it is asserted high prior to the active high assertion of PIIX4E PWROK.
V_CPUPU	Module	V_CPUPU is 2.5 V. The system electronics use this voltage to power the PIIX4E-to-processor interface circuitry.
V_CLK	Module	V_CLK is 2.5 V. The system electronics use this voltage to power the HCLK[0:1] drivers for the processor clock.

The following list provides additional specifications and clarifications of the power sequence timing and Figure 5 provides an illustration.

- The VR_ON signal *may only be* asserted to a logical high by a digital signal *after* V_DC ≥ 4.7 volts, V_5 ≥ 4.5 volts, and V_3 ≥ 3.0 volts.
- The Rise Time and Fall Time of VR_ON *must* be less than or equal to *1 microsecond* when it goes through its V_{IL} to V_{IH}.
- VR_ON has its V_{IL} (max) = +0.4 volts and V_{IH} (min) = +3.0 volts.
- The VR_PWRGD will get asserted to logic high (3.3 volts) after V_CORE is stabilized and V_DC reaches 5.0 volts. This signal should not and can not be pulled up by the system electronics.
- In the power-on process, Intel recommends to raise the higher voltage power plane first (V_DC), followed by the lower power planes (V_5, V_3), and finally assert VR_ON after above voltage levels are met on all rails. The power-off process should be the reverse process, i.e., VR_ON gets deasserted, followed by the lower power planes, and finally the higher power planes.
- VR_ON must monotonically rise through its V_{IL} to V_{IH} and fall through its V_{IH} to V_{IL} points. The sign of slope can not change between V_{IL} and V_{IH} in rising and V_{IH} and V_{IL} in falling.
- VR_ON must provide an instantaneous in-rush current to the module with the following values as listed in Table 23.

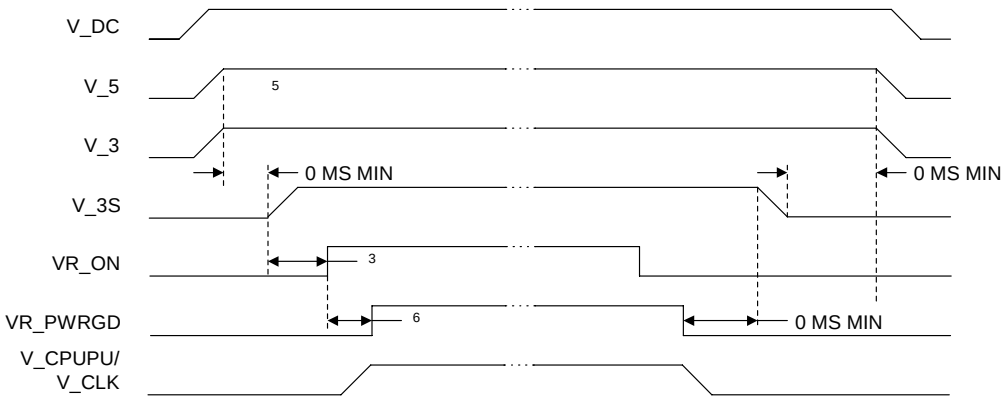
Table 23. VR_ON In-rush Current

	Instantaneous	DC Operating
MAX	41.0 mA	0.1 µA
TYP	0.2 mA	0.0 µA

NOTE: These values are based on a 3.3V VR_ON signal.

- VR_ON Valid-Low Time: This specifies how long VR_ON needs to be low for a valid off before VR_ON can be turned back on again. In going from a valid on to off and then back on, the following conditions must be met to prevent damage to the OEM system or the module:
- VR_ON must be low for 1 millisecond.
- The original voltage level requirements for turn-on must be met before assertion of VR_ON (i.e., V_DC ≥ 4.7 volts, V_5 ≥ 4.5 volts, and V_3 ≥ 3.0 volts).

Figure 5. Power-on Sequence Timing



POWER SEQUENCE TIMING

1. PWROK on I/O board should be active on when VR_PWRGD is active and V_3S is good.
2. CPU_RST from I/O board should be active for a minimum of 6 ms after PWROK is active and PLL_STP# and CPU_STP# are inactive. Note that PLL_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4E/M.
3. V_DC >= 4.7V, V_5>=4.5V, V_3S>=3.0V.
4. V_CPUPU and V_CLK are generated on the Intel Module.
5. This is the 5V power supplied to the processor module connector. This should be the first 5V plane to power up.
6. VR_PWRGD is specified to its associated high/active by the module regulator within less than or equal to 6 ms max. after the assertion of VR_ON.

4.7.3 Power Planes: Bulk Capacitance Requirements

In order to provide adequate filtering and in-rush current protection for any system design, bulk capacitance is required. A small amount of bulk capacitance is supplied on the module. However, in order to achieve proper filtering, additional capacitance should be placed on the system electronics.

Table 24 details the bulk capacitance requirements for the system electronics.

Table 24. Capacitance Requirement per Power Plane

Power Plane	Capacitance Requirements	ESR	Ripple Current	Rating
V_DC	100 µF, 0.1 µF, 0.01 µF[1]	20 mΩ	1 A-3.5 A[3]	20% tolerance at 35 V
V_5	100 µF, 0.1 µF, 0.01 µF[1]	100 mΩ	1 A	20% tolerance at 10 V
V_3	470 µF, 0.1 µF, 0.01 µF[1]	100 mΩ	1 A	20% tolerance at 6 V
V_3S	100 µF, 0.1 µF, 0.01 µF[1]	100 mΩ	N/A	20% tolerance at 6 V
VCC_AGP	22 µF, 0.1 µF, 0.01 µF[1]	100 mΩ	1 A	20% tolerance at 6 V
V_CPUPU	2.2 µF, 8200 pF[1]	N/A	N/A	20% tolerance at 6 V
V_CLK2	10 µF, 8200 pF[2]	N/A	N/A	20% tolerance at 6 V

NOTES:
1. Placement of above capacitance requirements should be located near the connector.
2. V_CLK filtering should be located next to the system clock synthesizer.
3. Ripple current specification depends on V_DC input. For 5.0 V V_DC, a 3.5 A device is required. For V_DC at 18 V or higher, 1 A is sufficient.

4.7.4 Surge Current Guidelines

This section provides the results of a worst case, surge current analysis. The analysis determines the maximum amount of surge current that the module can manage.

In the analysis, the module has two 4.7 µF with an ESR of 0.15 Ω each. The module is approximately 30.0 mΩ of series resistance, for a total series resistance of 0.18 Ω. If powering the system with the A/C adapter (18 V), the amount of surge current on the module would be approximately 100 A. This information is also used to develop I/O bulk capacitance requirements. See Table 24 for more information.

Note: Depending on the system electronics design, different impedances may yield different results. A thorough analysis should be performed to understand the implications of surge current on their system.

Figure 6 shows an electrical model used when analyzing instantaneous in-rush conditions, and Figure 7 illustrates the results with a SPICE simulation.

Figure 6. Instantaneous In-rush Current Model

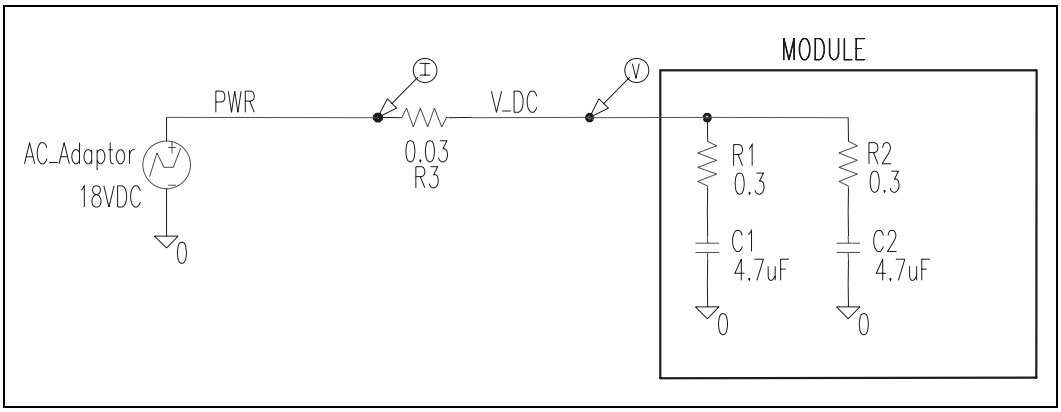
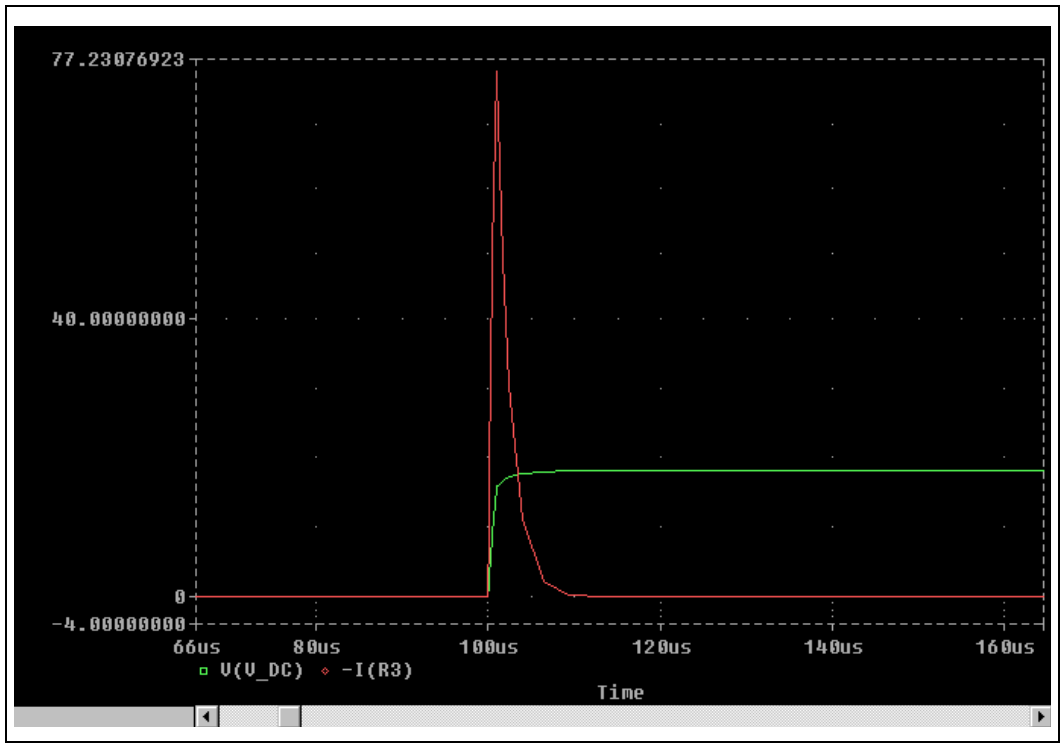
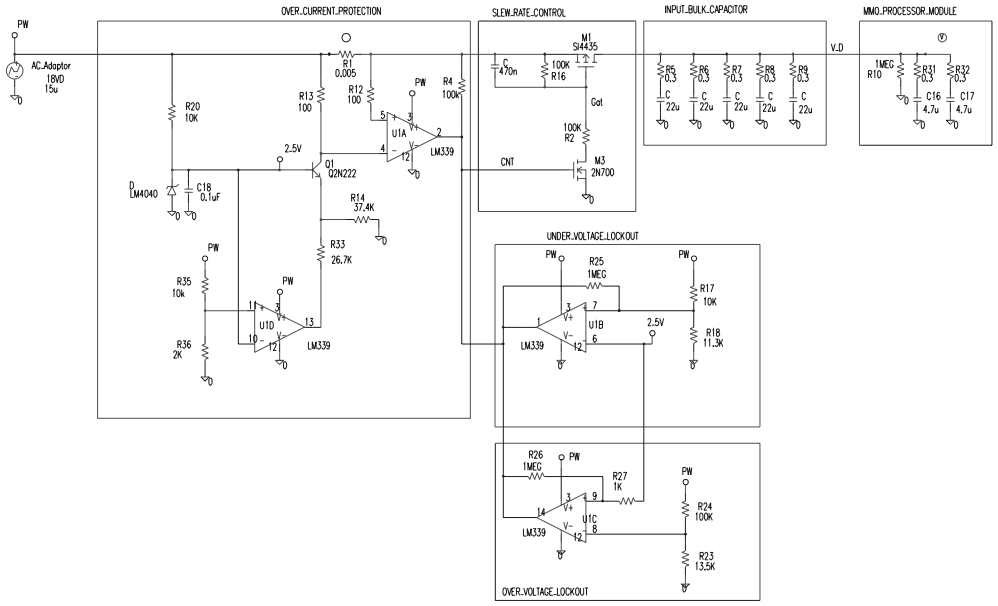


Figure 7. Instantaneous In-rush Current SPICE Simulation



Due to component height requirements (≤ 4 millimeters) of the module, Polymerized Organic Semiconductor capacitors must be used as input bulk capacitance in the voltage regulator circuit. Because of the capacitor's susceptibility to high in-rush current, special care must be taken. One way to soften the in-rush current and provide overvoltage and overcurrent protection is to ramp up V_DC slowly using a circuit similar to the one shown in Figure 8.

Figure 8. Overcurrent Protection Circuit



NOTE: Values shown are for reference only.

4.7.4.1 Slew-rate Control: Circuit Description

In Figure 8, PWR is the voltage generated by applying the AC Adaptor or Battery. M1 is a low RDS (on) P-Channel MOSFET such as a Siliconix* SI4435DY. When the voltage on PWR is applied and increased to over 4.75 V, the UNDER_VOLTAGE_LOCKOUT circuit allows R4 to pull up the gate of M3 to start a turn-on sequence. M3 pulls its drain toward ground forcing current to flow through R2. M1 will not start to source any current until after t_delay with t_delay defined as:

$$t\_delay := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vt}{Vpwr - Vgs\_max}\right)$$

$$Vgs\_max = \frac{R16}{R16\ R2} \cdot \quad Vpwr$$

The system manufacturer's Vgs_max specification of 20 V must never be exceeded. However, Vgs_max must be high enough to keep the RDS (on) of the device as low as possible. After the initial t_delay, M1 will begin to source current and V_DC will start to ramp up. The ramp up time, t_ramp, is defined as:

$$t\_ramp := -R2 \cdot C9 \cdot \ln\left(1 - \frac{Vsat}{Vgs\_max}\right) - t\_delay$$

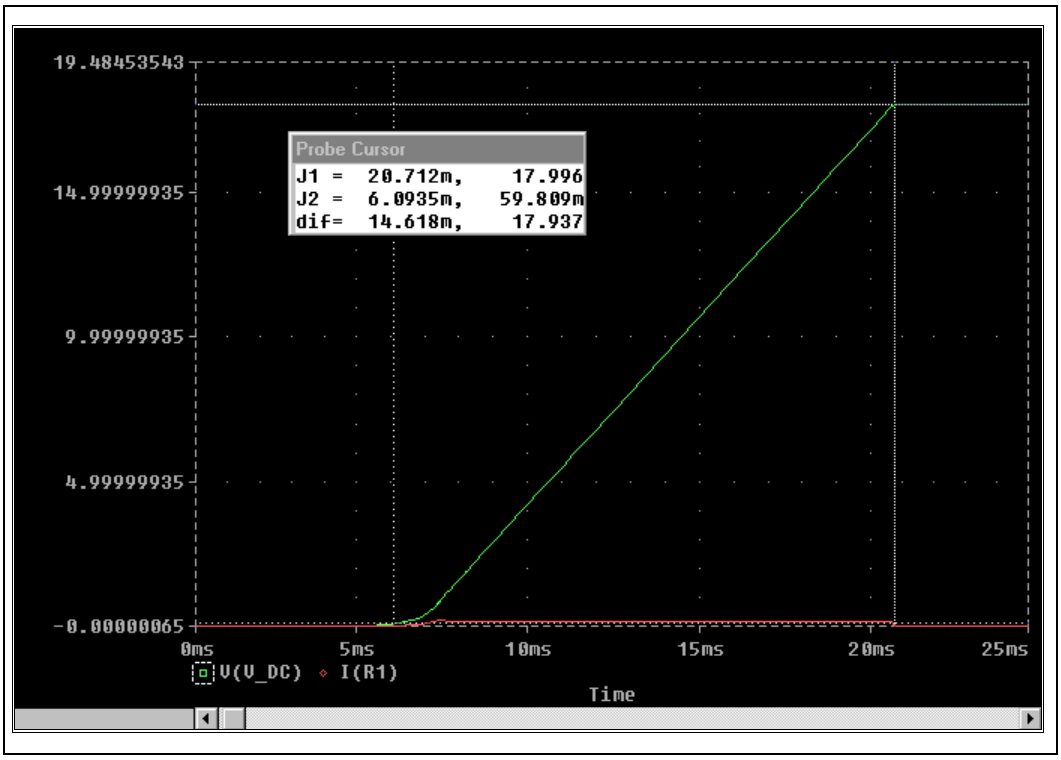
Maximum current during the voltage ramping is:

$$I = Ctotal \frac{Vpwr}{t\_ramp}$$

With the circuit shown in Figure 8: t_delay = 5.53 ms; t_tran = 14.0 ms; and I_max = 146 mA.

Figure 9 shows a SPICE simulation of the circuit in Figure 8. To increase the reliability of tantalum capacitors, use a slew-rate control circuit described in Figure 8 and voltage derate the capacitor about 50 percent. That is, for a maximum input voltage of 18.0 V, use a 35.0-V, low ESR capacitor with high ripple current capability. Place five, 22-µF/35-V capacitors on the baseboard, directly at the V_DC pins of the processor module connector. Finally, the slew-rate control circuit should be applied to every input power source to the system V_DC to provide the most protection. A potential problem still exists if all power sources are “logically OR’ed” together at the PWR node. For example, the system will immediately source current to the PWR node and V_DC if a 3X3 Li-Ion battery pack is powering the system (12.0 V at PWR) and the AC Adaptor (18.0 V) is plugged into the system. This is because the slew-rate control is already on. Therefore, the slew-rate control must be applied to every input power source to provide the most protection.

Figure 9. Spice Simulation Using In-rush Protection (Example ONLY))



4.7.4.2 Undervoltage Lockout: Circuit Description (V_uv_lockout)

The circuit shown in Figure 8 provides an undervoltage protection and locks out the applied voltage to the module to prevent an accidental turn-on at low voltage. The output of this circuit, pin 1 of the LM339 comparator, is an open collector output. It is low when the applied voltage at PWR is less than 4.75 V. This voltage can be calculated with the following equation with the voltage across D7 as 2.5 V (D7 is a 2.5-V reference generator).

$$V\_uv\_lockout := Vref \cdot \left[1 + \frac{R17}{\left(\frac{R18 \cdot R25}{R18 + R25} \right)} \right]$$

$$V\_uv\_lockout = 4.757 \cdot volt$$

4.7.4.3 Overvoltage Lockout: Circuit Description (V_ov_lockout)

The module operates with a maximum input voltage of 21 V. This circuit locks out the input voltage if it exceeds the maximum 21 V. The output of this circuit, Pin 14 of the LM339 comparator, is an open-collector output. It is low when the applied voltage at PWR is more than 21 V. This voltage can be calculated with the following equation:

$$V\_ov\_lockout := Vref \cdot \left(\frac{R26}{R26 + R27} \right) \cdot \left(1 + \frac{R24}{R23} \right)$$

$$V\_ov\_lockout = 20.998 \cdot volt$$

4.7.4.4 Overcurrent Protection: Circuit Description

Figure 8 shows that the circuit detects an overcurrent condition and cuts off the input voltage applied to the module. This circuit has two different current limit trip points, which accounts for the different maximum current drain by the module at different input voltages. Assuming the AC Adaptor is 18.0 V and the battery is a 3x3 Li-Ion configuration with a minimum voltage of 7.5 V, the maximum current for the above circuit can be calculated using the following expression:

With AC Adaptor (I_wAdaptor):

$$I\_wAdaptor := \frac{Vref - Vbe\_Q1}{R14} \cdot \frac{R13}{R1}$$

I_wAdaptor = 0.989 • amp

Without AC Adaptor (I_woAdaptor):

$$I\_woAdaptor := \frac{Vref - Vbe\_Q1}{\left(\frac{R14 \cdot R33}{R14 + R33} \right)} \cdot \frac{R13}{R1}$$

I_woAdaptor = 2.375 • amp

4.8 Active Thermal Feedback

Table 25 identifies the address allocated for the SMBus thermal sensor used on the module.

Table 25. Thermal Sensor SMBus Address Table

Function	Fixed Address AD Bits (6:4)	Selectable Address AD Bits (3:0)
Thermal Sensor	100	1110
Reserved	010	1010
Reserved	010	1011

NOTE: The thermal sensor used is compliant with SMBus addressing. Please refer to the *Pentium® II processor Thermal Sensor Interface Specification.*

4.9 Thermal Sensor Configuration Register

The configuration register of the thermal sensor controls the operating mode (Auto Convert vs. Standby) of the device. Since the processor temperature varies dynamically during normal operation, Auto Convert mode should be used exclusively to monitor processor temperature. Table 26 shows the format of the configuration register. If the RUN/STOP bit is low, then the thermal sensor enters auto-conversion mode. If the RUN/STOP bit is set high, then the thermal sensor immediately stops converting and enters the Standby mode. The thermal sensor will still perform temperature conversions in Standby mode when it receives a one-shot command. However, the result of a one-shot command during Auto Convert mode is not guaranteed. Intel does not recommend using the one-shot command to monitor temperature when the processor is active, only Auto Convert mode should be used.

Table 26. Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 MSB	MASK	0	Masks SMBALERT# when high.
6	RUN/STOP	0	Standby mode control bit. If low, the device enters auto-convert mode. If high, the device immediately stops converting, and enters standby mode where the one-shot command can be performed.
5 – 0	RFU	0	Reserved for future use.

NOTE: All RFU bits should be written as “0” and read as “don’t care” for programming purposes.

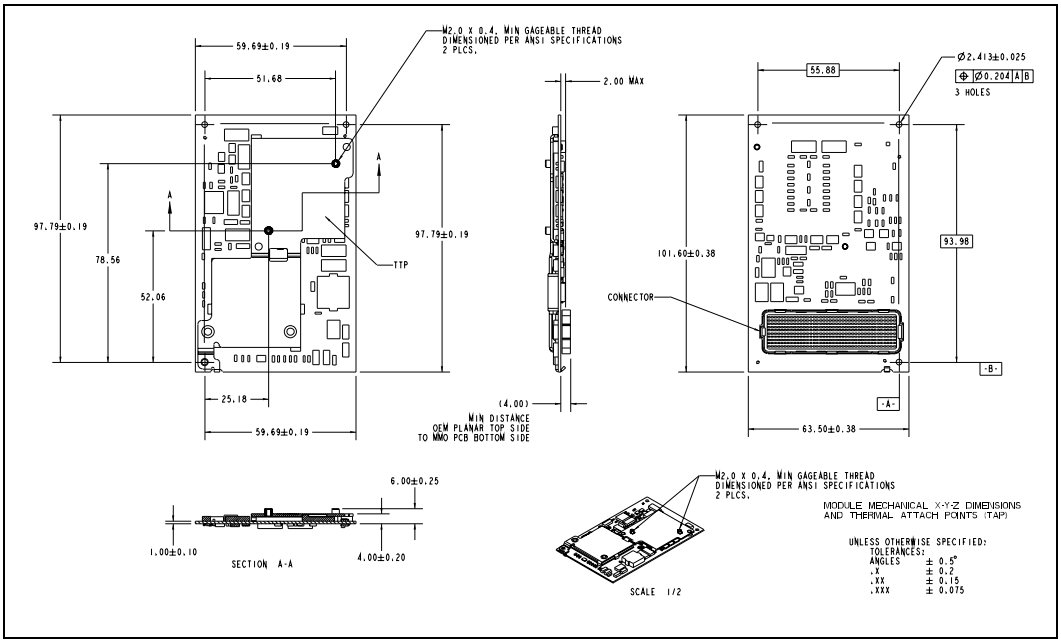
5.0 Mechanical Specification

This section provides the physical dimensions for the module.

5.1 Module Dimensions

Figure 10 shows the board dimensions and the connector orientation.

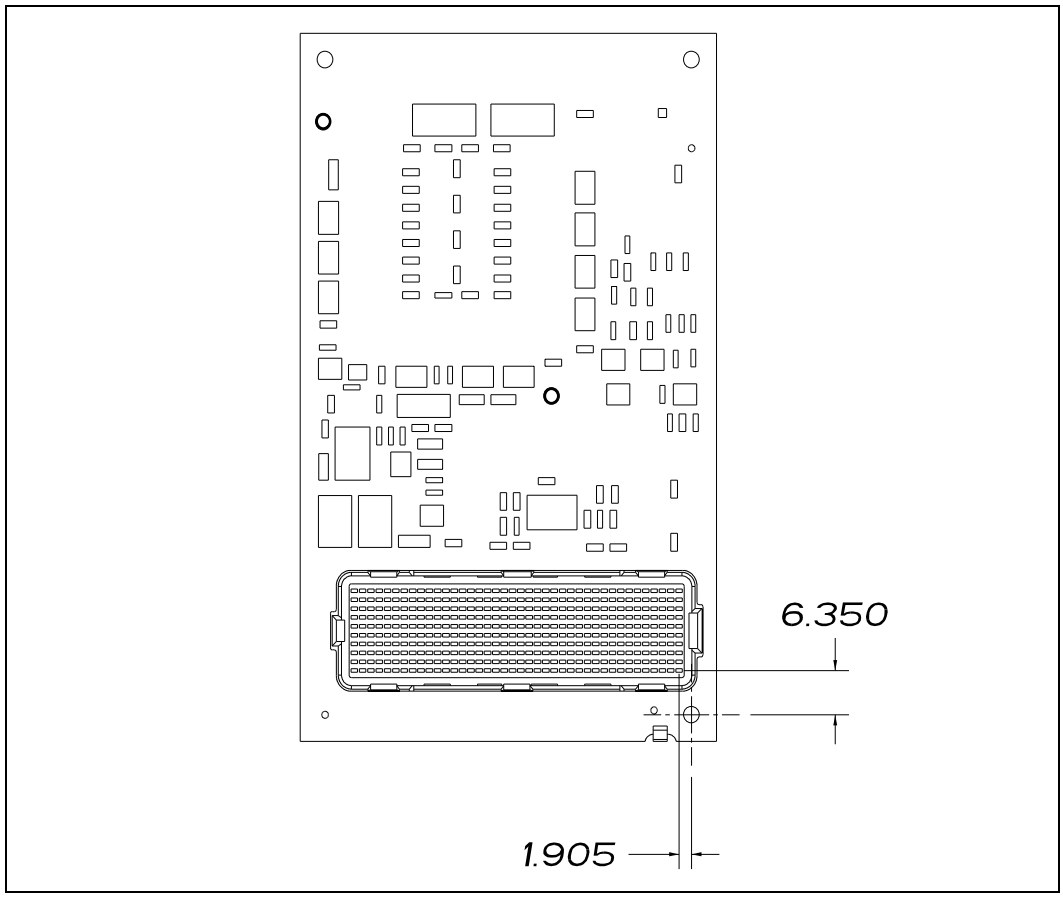
Figure 10. Board Dimensions with 400-Pin Connector Orientation



5.1.1 Pin 1 Location of the 400-pin Connector

Figure 11 shows the location of pin 1 of the 400-pin connector as referenced to the adjacent mounting hole.

Figure 11. Board Dimensions with 400-Pin Connector- Pin 1 Orientation

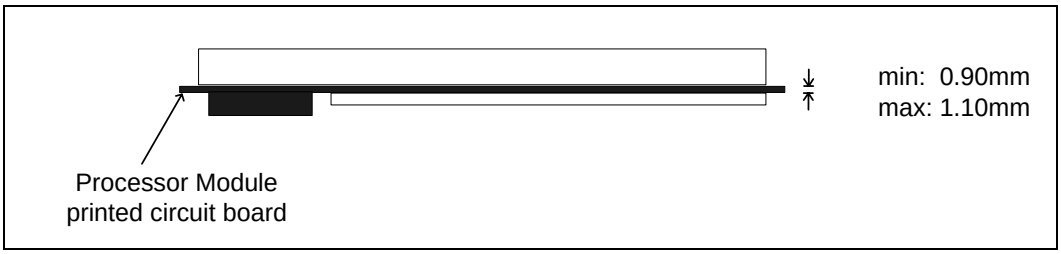


5.1.2 Printed Circuit Board Thickness

Figure 12 shows the minimum and maximum thickness of the printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with current and future modules.

Note: The system manufacturer must ensure that the mechanical restraining method and/or system-level EMI contacts are able to support this range of PCB for compatibility with future modules.

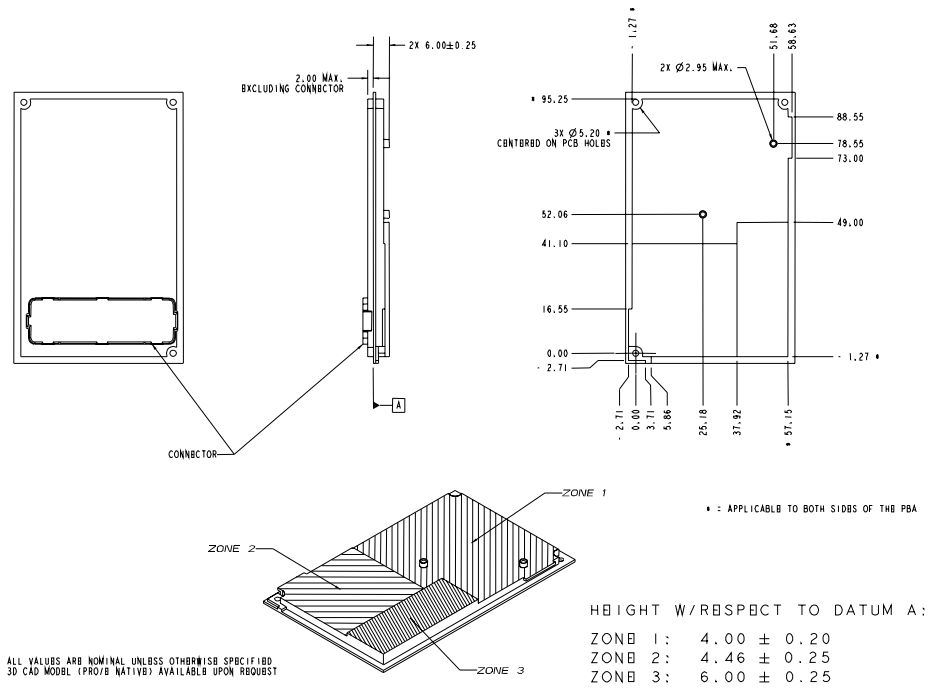
Figure 12. Printed Circuit Board Thickness



5.1.3 Height Restrictions

Figure 13 shows the mechanical stack-up and associated component clearance requirements. This is the module keep-out zone and should not be entered. The system manufacturer establishes board-to-board clearance between the module and the system electronics by selecting one of three mating connectors. The connector sizes available are 4 millimeters, 6 millimeters, and 8 millimeters. The three sizes provide flexibility in choosing the system electronics components between the two boards. Information on these connectors can be obtained from Berg Electronics (part number 74291-002).

Figure 13. Keep-out Zone



NOTE: The topside component clearance is independent of the PCB thickness.

5.2 Thermal Transfer Plate

The TTP on the processor and the 82443BX provides heat dissipation and a thermal attach point where a system manufacturer can attach a heat pipe, a heat spreader plate, or a thermal solution to transfer heat through the system. See Figure 14 and Figure 15 for attachment dimensions from the thermal interface block to the TTP.

When attaching the mating block to the TTP, a thermal elastomer or thermal grease should be used. This material reduces the thermal resistance. The OEM thermal interface block should be secured with 2.0-mm screws using a maximum torque of 1.5 Kg*cm to 2.0 Kg*cm (equivalent to 0.147 N*m to 0.197 N*m). The thread length of the 2.00-mm screws should be 2.25-mm gaugeable thread (2.25-mm minimum to 2.80-mm maximum).

The system manufacturer should use the exact dimensions for maximum contact area to the TTP to ensure that no warpage of the TTP occurs. If warpage occurs, the thermal resistance of the module could be adversely affected.

The TTP thermal resistance between the processor core to the system interface (top of the TTP) is less than 1° C/W.

Figure 14. Thermal Transfer Plate (A)

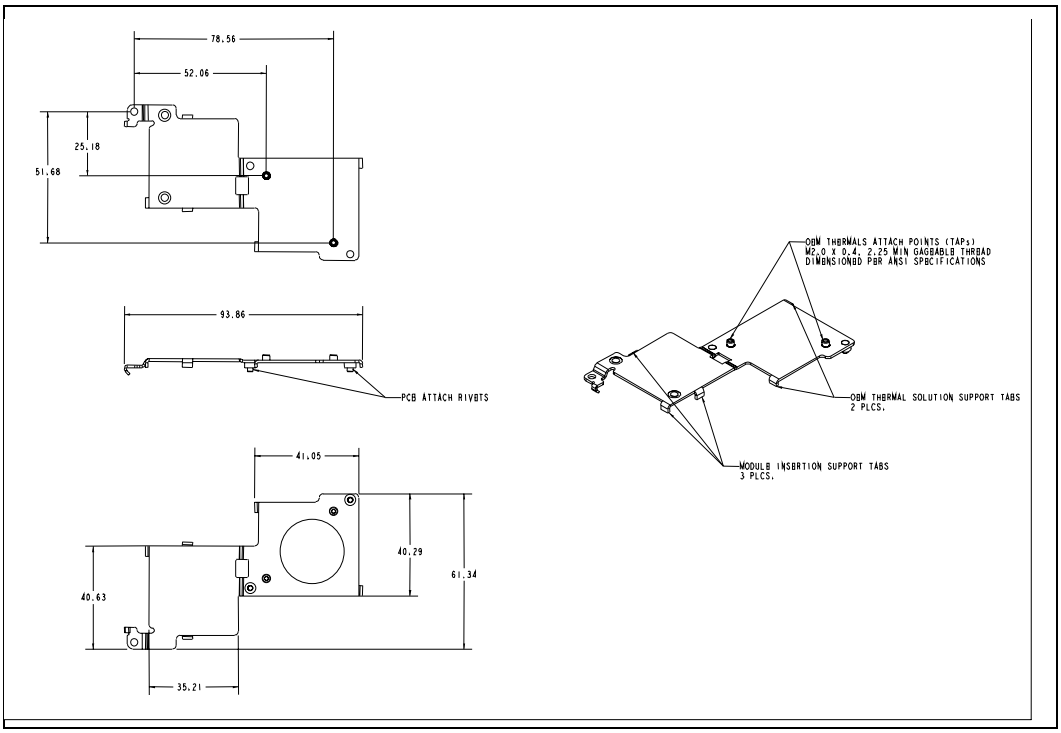
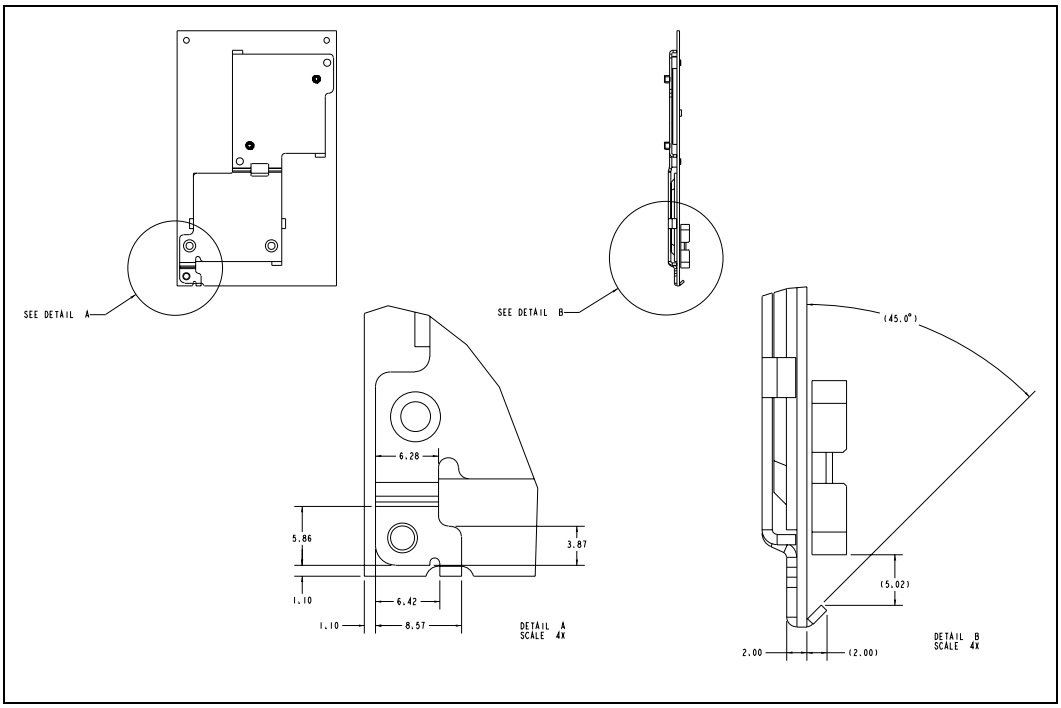


Figure 15. Thermal Transfer Plate (B)



5.3 Module Physical Support

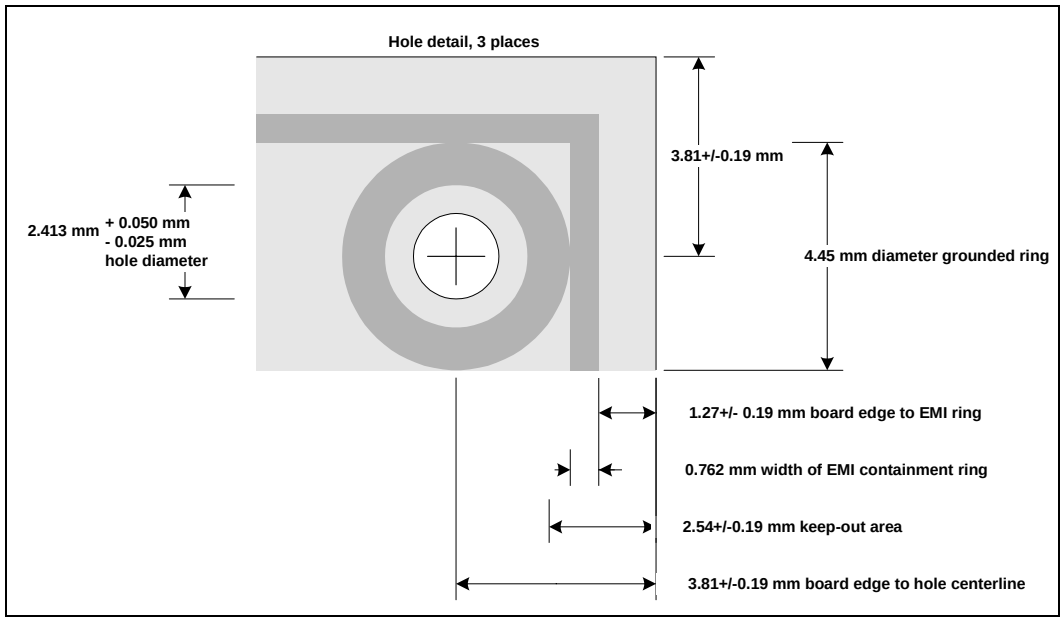
5.3.1 Module Mounting Requirements

Three mounting holes are available for securing the module to the system base. See Figure 10 for mounting hole locations. These hole locations and board edge clearances will remain fixed for all modules. All three mounting holes should be used to ensure long term mechanical reliability and EMI integrity of the system. The board edge clearance includes a 0.762-mm (0.030 inches) wide EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. On the surface of the module, the metal is exposed for EMI shielding purposes. The hole patterns also have a plated surrounding ring to use a metal standoff for EMI shielding purposes.

Standoffs should be used to provide support for the installed module. The distance from the bottom of the module PCB to the top of the system electronics board with the connectors mated is 4.0 millimeters + 0.16 mm / -0.13 mm. However, the warpage of the baseboard can vary and should be calculated into the final dimensions of the standoffs used.

Figure 16 shows the standoff support hole patterns, the board edge clearance, and the dimensions of the EMI containment ring. No components are placed on the board in the keep-out area.

Figure 16. Standoff Holes, Board Edge Clearance, and EMI Containment Ring



5.3.2 Module Weight

The module weighs approximately 50 g.

6.0 Thermal Specification

6.1 Thermal Design Power

The power handling capability of the system thermal solution may be reduced to less than the recommended typical thermal design power (TDP) with the implementation of firmware/software control or “throttling,” which reduces the processor power consumption and dissipation. The typical TDP is the typical power dissipation under normal operating conditions at nominal V_CORE (CPU power supply) while executing the worst case power instruction mix. This includes the power dissipated by *all* of the relevant components.

During all operating environments, the processor junction temperature, T_J, must be within the specified range of 0° C to 100° C.

6.2 Thermal Sensor Setpoint

The thermal sensor implements the SMBALERT# signal described in the SMBus specification. SMBALERT# is always asserted when the temperature of the processor core thermal diode or the thermal sensor internal temperature exceeds either the upper or lower temperature thresholds. SMBALERT# may also be asserted if the measured temperature equals either the upper or the lower threshold.

Table 27. Thermal Design Power Specification

Symbol	Parameter	Typical	Notes
TDP_{module}	Module Thermal Design Power	11.5 W	Module TDP = core, 82443BX, and voltage regulator

NOTES:
1. During all operating environments, the processor temperature, T_J must be within the specified range of 0° C to 100° C.
2. TDP_{module} is a thermal solution design reference point for OEM thermal solution readiness for total module power.

7.0 Labeling Information

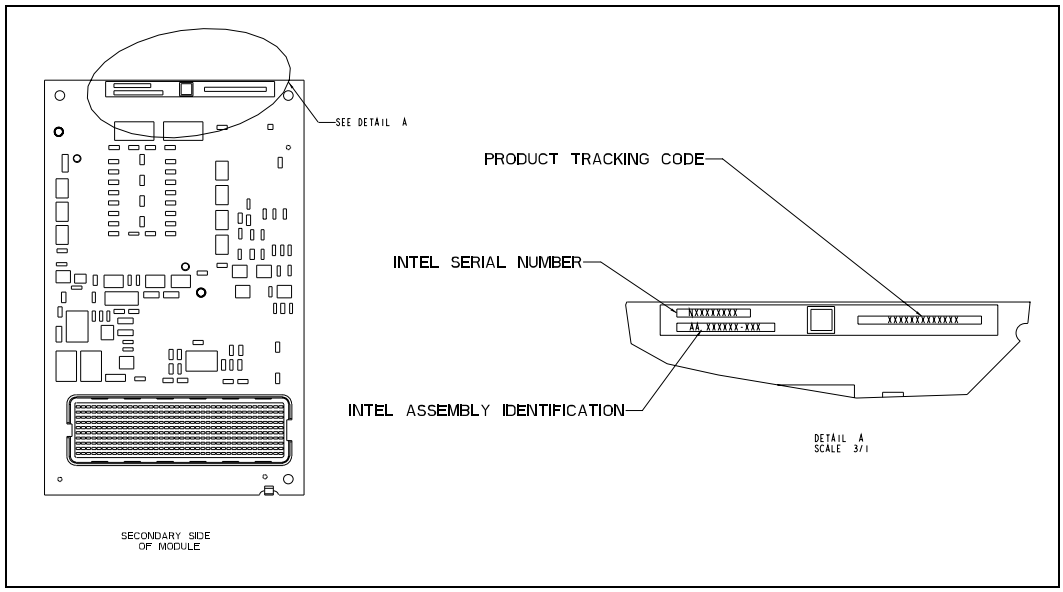
All modules are tracked in two ways. The first is by the Product Tracking Code (PTC). Intel uses the PTC label to determine the assembly level of the module. The PTC contains 13 characters as shown below.

AABCCCDDEEEFF

where

Code	Description (Low-Power Module markings)
AA	Processor Module (PM)
B	Low-Power Module (G)
CCC	Speed Identity (333)
DD	Cache Size = (02 = 256Kbyte)
EEE	Notifiable Design Revision (Start at 001)
FF	Notifiable Processor Revision (Start at AA)

Figure 17. Product Tracking Information



The second tracking method is by an OEM generated software utility. Four strapping resistors located on the module determine its production level. If connected and terminated properly, up to 16 module-revision levels can be determined. An OEM generated software utility can then read these ID bits with CPU IDs and stepping IDs to provide a complete module manufacturing revision level.

8.0 Environmental Standards

The environmental standards are defined in Table 28.

Table 28. Environmental Standards

Parameter	Condition	Specification
Temperature	Non-operating	-40° C to 85° C
Cycle	Operating	0° C to 55° C
Humidity	Unbiased	85% relative humidity at 55° C
Voltage	V_5	5 V ± 5%
	V_3	3.3 V ± 5%
Shock	Non-operating	Half Sine, 2 G, 11 ms
	Unpackaged	Trapezoidal, 50 G, 11 ms
	Packaged	Inclined Impact at 5.7 ft/s
	Packaged	Half Sine, 2 ms at 36 in Simulated Free Fall
Vibration	Unpackaged	5 Hz to 500 Hz 2.2 gRMS random
	Packaged	10 Hz to 500 Hz 1.0 gRMS
	Packaged	11,800 impacts 2 Hz to 5 Hz (low frequency)
ESD Damage	Human Body Model	Non-powered test of the module only for non-catastrophic failure. The module is tested at 2 KV and then inserted in a system for functional test.