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News Release

INTEL PRESENTS P6 MICROARCHITECTURE DETAILS

Technical Paper Highlights "Dynamic Execution" Design

SAN FRANCISCO, Calif., Feb. 16, 1995 -- Intel Corporation today disclosed details of the first fruit of a parallel engineering effort, the next-generation P6 microprocessor, at an engineering conference here. The presentation of technical details follows the delivery of first working samples to OEMs.

The 5.5-million transistor chip will deliver the highest level of processor performance for the Intel Architecture when systems using the chip begin to ship in the second half of this year. P6 will achieve this performance using a unique combination of technologies known as Dynamic Execution.

P6 microarchitecture details were presented by Intel at the IEEE International Solid State Circuits Conference (ISSCC), an annual industry gathering where technical innovations are showcased and discussed. Details on P6's unique approach to high-performance processing, described collectively as Dynamic Execution, were presented by Dr. Robert Colwell, P6 architecture manager, at ISSCC.

Colwell explained that this architectural enhancement is the next step beyond the superscalar advance implemented in the Pentium® processor. Dynamic Execution is a combination of technologies -- multiple branch prediction, data flow analysis and speculative execution -- that is constantly feeding P6's data-crunching units. Intel engineers were able to implement Dynamic Execution by analyzing how billions of lines of code in software programs are typically executed by processors. Collectively, these technologies allow the P6 to operate as an efficient information factory.

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Multiple branch prediction increases the amount of work available for the microprocessor to execute. Data flow analysis schedules the instructions to be executed when ready, independent of the original program order. Speculative execution allows the P6 to keep its superscalar engine as busy as possible by executing instructions that are likely to be needed.

With these technologies, the P6 can efficiently analyze much larger sections of incoming program flow than any previous PC processor, swiftly allocate internal resources, and intelligently optimize work that can be done in parallel. Consequently, more data can be processed in a given time period.

Parallel Design Teams Learn From Each Other

The concept of P6's Dynamic Execution engine began in 1990, when today's mainstream Pentium processor was still just a software simulation.

"Intel's use of parallel engineering teams for chip design has compressed delivery cycles of new generations of chips, cutting the time about in half," said Albert Yu, senior vice president and general manager, Microprocessor Products Group. "As a result, computer users will have some of the most powerful, low-cost engines at hand to enrich the desktop with software and other capabilities we only imagined five years ago," he said.

Yu said the Oregon-based P6 design team, building on the knowledge gained from the Pentium processor design, embarked on an innovative system-level solution to the next-generation processor involving the processor, cache (high-speed supporting memory), and bus (the transport mechanism that keeps data flowing into and out of the processor). "This approach will ensure that computers built around P6 will be able to take advantage of the chip's processing power when it is introduced as a commercial product later this year," he said.

The system-level approach means the P6 will be the first high-volume microprocessor with two die in a single package. A dual-cavity, standard PGA package contains a P6 die and a companion level two (L2) cache die. The two chips communicate using a highly-optimized bus which contributes to high performance by tightly-coupling the processor to its primary data source.

Additional Features

In addition to providing new levels of performance, the P6 will contain new features which will greatly simplify the design of multiprocessor systems and improve overall system

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reliability. Among applications that will benefit greatly from this processing power are: desktop applications such as image processing, speech recognition, software-only videoconferencing and multimedia authoring, and server applications such as transaction and database processing.

At introduction in the second half of this year, the P6 processor will operate at 133 MHz and will use a power supply of 2.9 volts. The low voltage also contributes to low power dissipation, which is expected to be only about 14 watts, typically, for the processor and L2 cache combined. Complete performance and power dissipation information will also be available at that time, although estimated performance has been measured at more than 200 SPECint92 on a prototype system, twice the performance of today's fastest Pentium processor.

P6 Information Available on the Internet

Comprehensive information about the P6 ISSCC paper is also available at Intel's World Wide Web service on the Internet. The information is part of this week's debut of Intel's new WWW home page at URL HTTP://www.intel.com/. Users will be able to obtain a copy of the actual P6 technical paper presented at ISSCC, a simplified explanation of the technical information, and view a die photo of the P6 as well.

Intel, the world's largest chip maker, is also a leading manufacturer of personal computer, networking and communications products.

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