Intel® Celeron™ Processor for Embedded Applications

PRODUCT HIGHLIGHTS

High Performance

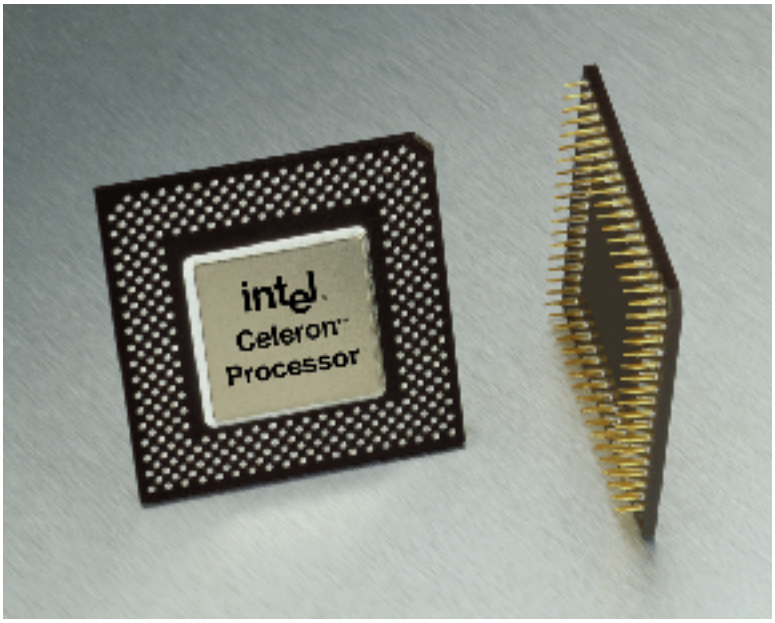
- **Integrated L2 cache 128 Kbytes**
- **Dynamic execution technology**
- **MMX™ technology**
- **66 MHz multi-transaction system bus with L2 cache interface**
- **16K code and 16K data caches**
- **High-performance floating-point unit**
- **Enhanced 64-bit data bus**
- **Branch prediction feature**
- **440 BX chipset support**

Data Integrity Features

- **ECC memory control with 440 BX chipset**
- **Built-in Self Test (BIST)**
- **IEEE 1149.1 Standard test access port and boundary scan mechanism**

Small Form Factor

- **370-pin PPGA package**
- **Socketable solution**



PRODUCT DESCRIPTION

The 300A and 366 MHz Celeron™ processors with MMX™ technology have joined the family of Intel® processors for embedded applications. Now that Intel supports these products in the embedded product roadmap, designers will benefit from both embedded life cycle support and a scalable path for high-performance requirements, ideal for embedded applications.

The Celeron processor provides high performance in a small package for value conscious developers. In addition to featuring the dynamic execution of the P6 micro-architecture the Celeron processor further enhances performance by integrating a 128K on-chip L2 cache.

PERFORMANCE

The 300A and 366 MHz Celeron processors' 128-Kbyte unified, non-blocking level two cache can improve performance by reducing the average memory access time and provides fast access to recently used instructions and data. The large on-chip cache can help reduce the traffic across the main memory bus. The large cache frees memory bandwidth for networking or graphics traffic, giving the Celeron processor the performance that many telecommunications, data communications, transaction terminals and industrial PC application designers look for.

The Intel Celeron processors utilize the Intel P6 micro-architecture's multi-transaction system bus. The 300A and 366 MHz processors incorporate an internal full speed L2 cache interface supporting the Dual Independent Bus architecture of the Pentium® II processor. Having two

separate buses allows simultaneous access to both the L2 cache bus and the system bus. The combination of the L2 cache bus and the processor-to-main-memory system bus can increase peak overall bandwidth availability and performance over single-bus processors.

The Celeron processors also feature Intel MMX Media enhancement technology. This technology includes instructions and data types that can help many applications achieve new levels of performance.

Applying MMX technology to networking software stacks can help dramatically improve the performance of telecommunications and data communications applications. The imaging features accelerated by MMX technology can help enable exciting new capabilities for transaction terminals including the incorporation of JPEG images and motion video.

iCOMP® INDEX 2-0*

Compares the relative performance of Intel microprocessors

Processors	iCOMP® Index 2.0 Rating
166 MHz Pentium® processor with MMX™ technology	160
200 MHz Pentium processor with MMX technology	182
233 MHz Pentium processor with MMX technology	203
300A Celeron™ processor with MMX technology	296
366 Celeron processor with MMX technology	N/A

*This graph was taken from the Intel benchmark report 2.0

DATA INTEGRITY FEATURES

The Celeron processors also feature Built-in Self Test (BIST), providing single stuck-at fault coverage of the microcode and large logic arrays, as well as testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs) and ROMs.

The IEEE 1149.1 Standard Test Access Port and Boundary Scan mechanism, enables testing of the Intel® Celeron processor and system connections through a standard interface.

CHIPSET SUPPORT FOR EMBEDDED APPLICATIONS

The Celeron processor with MMX technology is supported by the Intel 440BX chipset, which is also on Intel's embedded roadmap for embedded lifecycle support.

The 440 BX chipset incorporates ECC memory control providing a high level of data integrity, critical for maintaining uptime in applications. The chipset also features Intel's Quad Port Acceleration to help improve bandwidth between the Celeron processors, the accelerated graphics port, 66 MHz SDRAM and the PCI bus. QPA combines enhanced bus arbitration, deeper buffers, open page memory architecture and ECC memory control. All of these features combine to help enhance value and performance of the product.

PACKAGING

The Celeron processor is available in the plastic pin grid array (PPGA) package. The PPGA package is compatible with the 370-pin socket and provides flexibility to design low cost systems by enabling lower profile and smaller systems. The PPGA package also provides the potential for reusing costs of processor retention and cooling solutions.

The PPGA package is outstanding wherever high performance and value conscious applications are required. By enabling low profile and small systems, the PPGA package provides flexibility to design low cost systems.

INTEL® CELERON™ PROCESSOR FOR EMBEDDED APPLICATIONS LINECARD

Product	Speed	External Bus	Bus/core	Active power	Voltage (nominal)	Tcase	Package
FV80524RX300128	300A	66	2/9	17.5W	2.0v	0-85°C	370 pin PPGA
FV80524RX366128	366	66	2/11	21.4W	2.0v	0-85°C	370 pin PPGA

INTEL® PCISETS LINECARD

NAME	PRODUCT	COMPONENTS	FEATURES
Intel® 440BX PCIset for embedded applications	FW, 82443BX FW,82371EB	1 X 492 BGA 1X P114XE 324 BA	-AGPset enables “world class” multimedia -Supports 66 MHz system and memory bus designs -ACPI compliant power management -ECC parity for application-critical environments

INTEL® CELERON™ PROCESSOR FOR EMBEDDED APPLICATIONS

Features	Benefits
■ 128K integrated L2 cache	**Higher Performance:** Improves performance by reducing the average memory access time and provides fast access to recently used instructions and data
■ Multiple branch prediction	**Higher Performance:** Accelerates the flow of work to the processor by predicting program execution through several branches
■ Dataflow analysis	**Higher Performance:** Creates an optimized, reordered schedule of instructions by analyzing data dependencies between instructions
■ Speculative execution: Carries out instructions speculatively	**Higher Performance:** Ensures that the processors superscalar execution units remain busy, boosting overall performance
■ Intel P6 microarchitecture multi-transaction system bus at 66 MHz with the addition of the L2 cache interface	**Higher Performance:** The combination of the L2 cache bus and the processor-to-main-memory system bus increases bandwidth and performance over single-bus processors
Intel® MMX™ media enhancement technology ■ Single Instruction Multiple Data (SIMD) technique ■ 57 new instructions ■ Eight 64-bit wide MMX technology registers ■ Four new data types	**Higher Performance:** Includes instructions and data types that can help many applications achieve new levels of performance. Accelerates imaging features to enable new capabilities for applications such as transaction terminals including the incorporation of JPEG images and motion video
■ 370-lead plastic pin grid array package	**Lower System Cost:** Compatible with the 370-pin socket. Provides flexibility to design low cost systems
■ BIST - Built in Self Test	**Data Integrity:** Provides single stuck-at fault coverage of the microcode and large logic arrays, as well as testing of the instruction cache, data cache, Translation Lookaside Buffers (TLB's) and ROMs
■ IEEE 1149.1 Standard self test port and boundary scan mechanism	**Data Integrity:** Enables testing of the Intel® Celeron™ processor and system connections through a standard interface
■ 440BX chipset	**Design Flexibility:** One chipset for both 66 MHz and 100 MHz system designs

INTEL® 440BX CHIPSET

Features	Benefits
■ Features Intel's Quad Port Acceleration (QPA) combines enhanced bus arbitration, deeper buffers, open page memory architecture and ECC memory control	**Higher performance:** Improves performance by increasing the bandwidth of the system bus
■ Incorporates Error Correction Code (ECC) memory control	**Data Integrity:** Maintains uptime in critical applications

Intel Reference Numbers	
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