# Intel® Celeron™ Processor (PPGA) with the Intel® 440ZX-66 AGPset

## Design Guide

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## Revision History

| Date | Revision | Description |
|---|---|---|
| 3/99 | -001 | Initial Release. |

# 1

# Introduction

# Introduction 1

The Intel® Celeron™ processor line includes processors that can be installed in a 370-pin socket. The intent of this document is to organize any special design recommendations and concerns that exist for creating an Intel Celeron processor (PPGA) / Intel® 440ZX-66 AGPset based system. Likely design issues have been identified and included here in a checklist format to alleviate problems during the design and debug phases. The information contained in this document should be used in conjunction with the *Intel® 440BX AGPset Design Guide*, which covers Intel® 440BX AGPset designs with the Pentium® II processor. Exceptions to the *Intel® 440BX AGPset Design Guide* are listed in this document. For topics not covered in this document, refer to the *Intel® 440BX AGPset Design Guide*.

## 1.1 Overview

This document contains information necessary for implementing an Intel Celeron processor (PPGA) / Intel 440ZX-66 AGPset platform design. Throughout the document references to the "processor" refer to the Intel Celeron processor (PPGA) or future 2.0 V processors that are designed to fit in the 370-pin socket. Design guidelines that are unchanged from the *Intel® 440BX AGPset Design Guide* are not covered in this document.

## 1.2 Reference Documents And Information Sources

| Document Name or Information Source | Available From |
|---|---|
| Intel® 82443ZX Host Bridge / Controller | Intel Website |
| Intel® 82371AB PCI-to-ISA / IDE Xcelerator (PIIX4) | Intel Website |
| Intel® 440BX AGPset Design Guide | Intel Website |
| Intel® 440BX AGPset Design Guide Update | Intel Website |
| 82443BX Application Notes | Intel Field Sales Representative |
| Intel® 440BX AGPset 82443BX Host Bridge / Controller Specification Update | Intel Website |
| Intel® 82371EB (PIIX4E) Specification Update | Intel Website |
| Intel® Celeron™ Processor Datasheet | Intel Website |
| Intel® Celeron™ Processor Specification Update | Intel Website |
| VRM 8.2 DC-DC Converter Design Guidelines | Intel Website |

# 1.3 Design Features

## 1.3.1 Intel® Celeron™ Processor (PPGA)

The Intel Celeron processor (PPGA) is the latest addition to the Intel Celeron processor product line. The Intel Celeron processor (PPGA), like the Intel Celeron processor in the Single-Edge Processor Package (S.E.P. Package), implements a Dynamic Execution microarchitecture and executes MMX™ media technology instructions for enhanced media and communication performance. The Intel Celeron processor (PPGA) also uses the same multi-transaction system bus used in the Intel Pentium® II processor. The Intel Celeron processor (PPGA) supports multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel Celeron processor (PPGA) is based on the P6 core (like the S.E.P. Package) but is provided in a Plastic Pin Grid Array (PPGA) package for use in low cost systems in the Value PC market segment. The Intel Celeron processor (PPGA) utilizes the AGTL+ system bus used by the Pentium II processor with support limited to single processor-based systems. Support for multi-processor-based systems is not provided with the Intel Celeron processor (PPGA). Pentium II processors should be used for multi-processor system designs. The Intel Celeron processor (PPGA) includes an integrated 128 KB level-two cache with a separate 16 KB instruction and 16 KB data level-one caches. The level-two cache is capable of caching 4 GB of system memory address space.

## 1.3.2 Intel® 440ZX-66 AGPset

This information is being provided to Intel customers to begin developing a design with the 82443ZX. The 82443ZX is a Value PC solution for an Intel Celeron processor-based platform.

The 82443ZX has the following features:

- Maximum of 256 MB SDRAM memory or 256 MB EDO memory
- Maximum of 4 PCI slots (4 PREQx#/PGNTx# pairs support 4 PCI masters. PHOLD# and PHLDA# continue to support the PIIX4E as another bus master. There is support for a total of 5 PCI masters including the PIIX4E. Four PCI slots means 4 bus masters using the available 4 PREQx#/PGNTx# pairs. The physical location of these 4 PCI bus masters may be in cards inserted in the 4 PCI slots, or in cards inserted in 3 PCI slots together with one PCI bus master down on the motherboard, or in cards inserted in 2 PCI slots together with two PCI masters down on the motherboard, etc.)
- 66 MHz-only system bus / DRAM bus frequency
- No ECC
- Single processor support only (no I/O APIC support)

# 1.4 General Design Recommendations

## 1.4.1 Voltage Definitions

For the purposes of this document the following nominal voltage definitions are used:

| | |
|---|---|
| $V_{CC}$ | 5.0V |
| $V_{CC_{3.3}}$ | 3.3V |
| $V_{CC_{CORE}}$ | Voltage is dependent on the four bit VID setting |
| $V_{CC_{2.5}}$ | 2.5V |
| $V_{CC_{CORE}}$ | 2.0V |
| $V_{CC_{1.5}}$ | 1.5V |
| $V_{TT}$ | 1.5V |
| $V_{REF}$ | 1.0V |
| $AGPV_{REF}$ | 1.32V |

## 1.4.2 General Design Recommendations

1. Intel recommends using a widely available, programmable Voltage Regulator Module (VRM) installed in a VRM header or an onboard programmable voltage regulator. Please see the *VRM 8.2 DC-DC Converter Design Guidelines*.
2. Motherboard designs targeted for system integrators should design to the boxed processor electrical, mechanical, and thermal specifications provided in the boxed processor section of the *Intel® Celeron™ Processor* Datasheet. The most notable items are the required fan power header and fan/heatsink physical clearance on the motherboard.

# 1.5 Transitioning From an Intel® Pentium® II Processor/ Intel® 440BX AGPset Design

## 1.5.1 AGTL+ Termination

AGTL+ termination is no longer provided on the processor and must be implemented on the system board. Intel recommends 56 ± 5% ohm resistors for AGTL+ termination. In addition, high frequency $V_{TT}$ decoupling is also required on the system board. Intel recommends one 0.1 µF capacitor in the 0603 package for every two resistor packs.

## 1.5.2 VREF Inputs

$V_{REF}$ ($^2/_3$ $V_{TT}$) must be supplied to the processor through each of the eight $V_{REF}$ inputs. Intel recommends using one 75 ± 1% and 150 ± 1% ohm resistor divider of the $V_{TT}$ supply to generate $V_{REF}$. Intel also recommends placing four 0.1 µF capacitors, in the 0603 package, within 500 mils of the processor's $V_{REF}$ pins.

### 1.5.3 System Bus Clock

Due to the change in system bus trace lengths in the PPGA package, chipset, and processor clocks must be ganged to minimize pin-to-pin clock skew. Implementation details are provided in the AGTL+ section of this document.

It is also recommended that a capacitor site be placed near the processor BCLK input to allow the clock skew to be minimized through tuning. This can be done by changing the value at the capacitor site to compensate for the actual motherboard trace lengths.

### 1.5.4 CMOS Compatibility with Future Processors

All processor CMOS outputs are open drain and require a pull-up to drive to external logic. The Intel Celeron processor's (PPGA) CMOS signals are 2.5 V-compatible. Since there are no plans for the Intel 440ZX-66 AGPset to support future processors based on a 1.5 V core, Intel recommends the CMOS design guidelines listed below.

Intel has defined three new pins for the Intel Celeron processor (PPGA):

- $V_{CC_{2.5}}$: This pin should be connected to the system's 2.5 V supply.
- $V_{CC_{1.5}}$: This pin should be left open (recommended configuration).
- $V_{CC_{CMOS}}$: This pin should be used as the system CMOS pull-up voltage. A 0.1 µF decoupling capacitor is recommended.

On a 2.0 V-core Intel Celeron processor (PPGA), $V_{CC_{CMOS}}$ will be tied to the $V_{CC_{2.5}}$ pin, thereby providing 2.5 V to system CMOS pull-ups.

These pins have been defined to permit a maximum current of 500 mA.

### 1.5.5 Processor Core Voltage Decoupling

High frequency decoupling for the processor core voltage is no longer provided on the processor as in previous generation processors. As a result, the system board must implement these capacitors. Intel recommends ten or more 4.7 µF capacitors in the 1206 package (ceramic X5R or better material) as well as nineteen or more 1.0 µF capacitors in the 0805 package to be placed within the socket cavity. Placement of the capacitors should be such that overall inductance between $V_{CC}$ / $V_{SS}$ power pins is minimized. Meeting these guidelines will insure system compatibility with future Intel® Celeron™ processors (PPGA) with a 2.0 V-core. Implementation details are provided later in this document.

### 1.5.6 VID[4]

VID[4] is not available on the processor. Therefore, according to the *VRM 8.2 DC-DC Converter Guidelines*, VID[4] must be connected to ground on the voltage regulator in order to provide the correct VID[3:0] for 1.30 V to 2.05 V Voltage ID encoding.

## 1.5.7 PHASE LOCK LOOP (PLL) Power

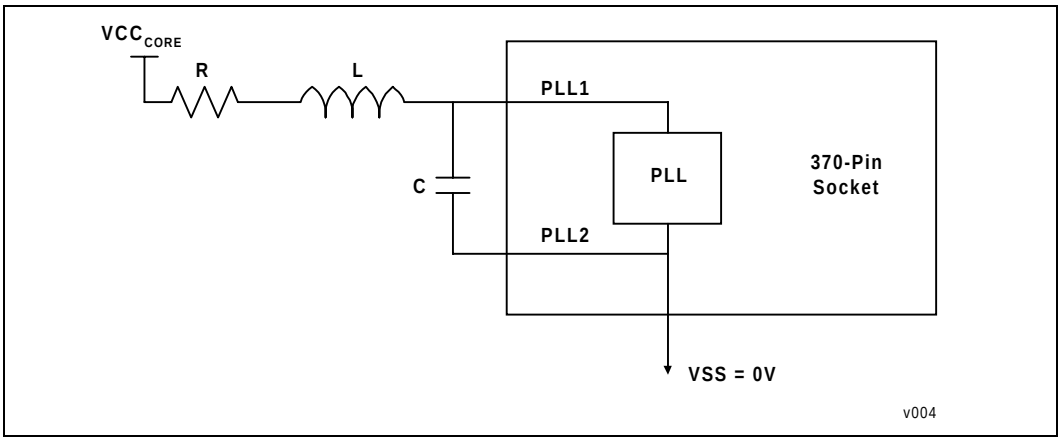
### 1.5.7.1 Processor PLL Filter Recommendation

All Intel Celeron processors have internal PLL clock generators which are analog and require quiet power supplies to minimize jitter.

### 1.5.7.2 Topology

The general desired topology is shown in Figure 1-1. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

**Figure 1-1. Filter Topology**



### 1.5.7.3 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. In general, the low-pass description forms an adequate description for the filter.

The low-pass specification, with input at $V_{CC_{CORE}}$ and output measured across the capacitor, is as follows:

< 0.2 dB gain in pass band

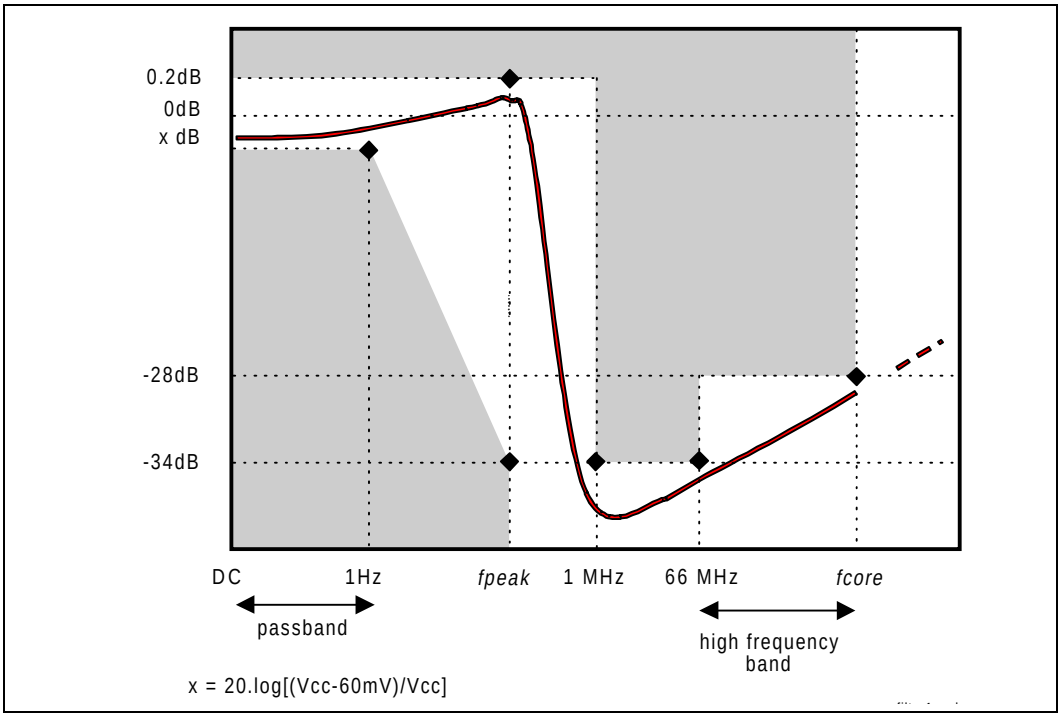
< 0.5 dB attenuation in pass band (see DC drop in next set of requirements)

> 34 dB attenuation from 1 MHz to 66 MHz

> 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 1-2.

**Figure 1-2. Filter Specification**




**NOTES:**
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak*, if it exists, it should be less than 0.05 MHz.

Other requirements:

- Filter should support DC current > 30 mA.
- Shielded type inductor to minimize magnetic pickup.
- DC voltage drop from $V_{CC}$ to PLL1 should be < 60 mV, which in practice implies series R < 2 ohm; also means pass band (from DC to 1 Hz) attenuation < 0.5 dB for $V_{CC}$ = 1.1 V, and < 0.35 dB for $V_{CC}$ = 1.5 V.

### 1.5.7.4 Recommendation for Intel Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in the topology presented in Figure 1-1.

**Table 1-1. Inductor**

| Part Number | Value | Tol | SRF | Rated I | DCR |
|---|---|---|---|---|---|
| TDK MLF2012A4R7KT | 4.7 uH | 10% | 35 MHz | 30 mA | 0.56 ohm |
| Murata LQG21N4R7K00T1 | 4.7 uH | 10% | 47 MHz | 30 mA | 0.70 ohm |
| Murata LQG21C4R7N00 | 4.7 uH | 30% | 35 MHz | 30 mA | 0.30 ohm |

**Table 1-2. Capacitor**

| Part Number | Value | Tolerance | ESL | ESR |
|---|---|---|---|---|
| Kemet T495D336M016AS | 33 uF | 20% | 2.5 nH | 0.225 ohm |
| AVX TPSD336M020S0200 | 33 uF | 20% | TBD | 0.200 ohm |

**Table 1-3. Resistor**

| Value | Tolerance | Power | Note |
|---|---|---|---|
| 1 ohm | 10% | $^1/_{16}$ W | Resistor may be implemented with trace resistance, in which discrete R is not needed |

To satisfy damping requirements, total series resistance in the filter (from $V_{CC_{CORE}}$ to the top plate of the capacitor) must be at least 0.35 ohm. This resistor can be in the form of a discrete component, or routing, or both. For example, if the selected inductor has a minimum DCR of 0.25 ohm, then a routing resistance of at least 0.10 ohm is required. Be careful not to exceed the maximum resistance rule (2 ohm). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9 ohm, which precludes using some inductors.

Other routing requirements:

- C should be close to PLL1 and PLL2 pins, < 0.1 ohm per route. These routes do not count towards the minimum damping R requirement.
- PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- L should be close to C; any routing resistance should be inserted between $V_{CC_{CORE}}$ and L.
- Any discrete R should be inserted between $V_{CC_{CORE}}$ and L.

**Figure 1-3. Using Discrete R**

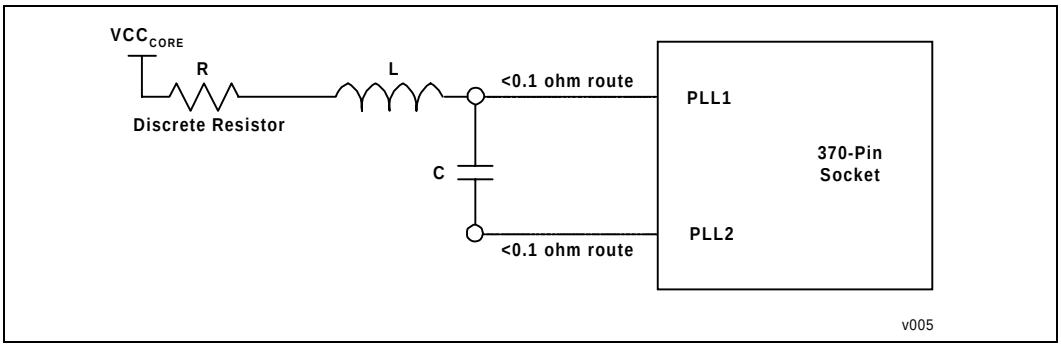
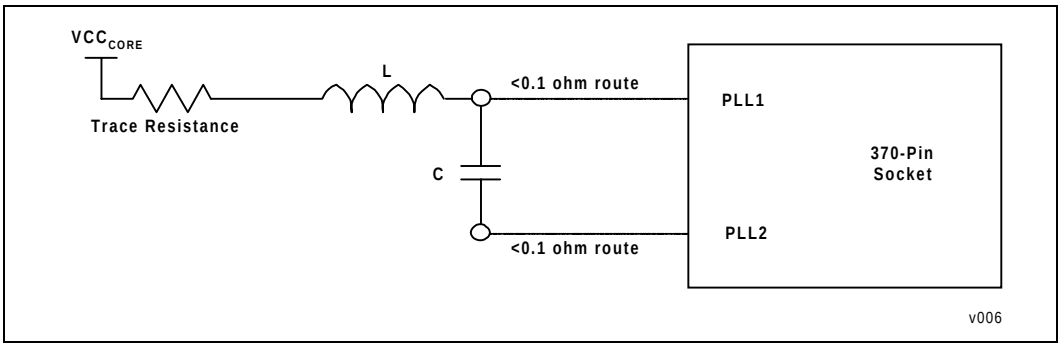


Figure 1-4. No Discrete R




## 1.5.8 Bus Frequency Selection

The BSEL pin on the Intel Celeron processor (PPGA) is used to select the system bus frequency. A logic-low on BSEL is defined as 66 MHz. BSEL should be implemented as discussed in Table 3-2.

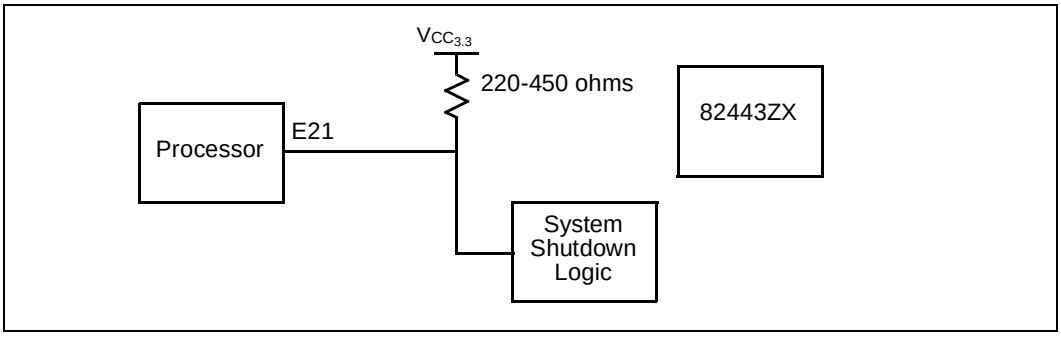
## 1.5.9 EDGCTRL

A new pin that is required for correct operation of the processor, EDGCTRL, requires a 51 ± 5% ohm pull-up to $V_{CC_{CORE}}$.

## 1.5.10 $VCORE_{DET}$

There are no current plans for the Intel 440ZX-66 AGPset to support future processors based on a 1.5 V core. Therefore, the $V_{CORE_{DET}}$ pin can be used by external motherboard logic to shutdown the platform if a 1.5 V-core processor is installed. This is because the $V_{CORE_{DET}}$ pin is tied to $V_{SS}$ on the package for 1.5 V-core processors and is a no-connect (floating) for 2.0 V-core processors. Refer to Figure 1-6 as an example.

Figure 1-5. $VCORE_{DET}$ Not Supported Using 440ZX-66 AGPset



# 2

# Motherboard Design

# Motherboard Layout and Routing Guidelines 2

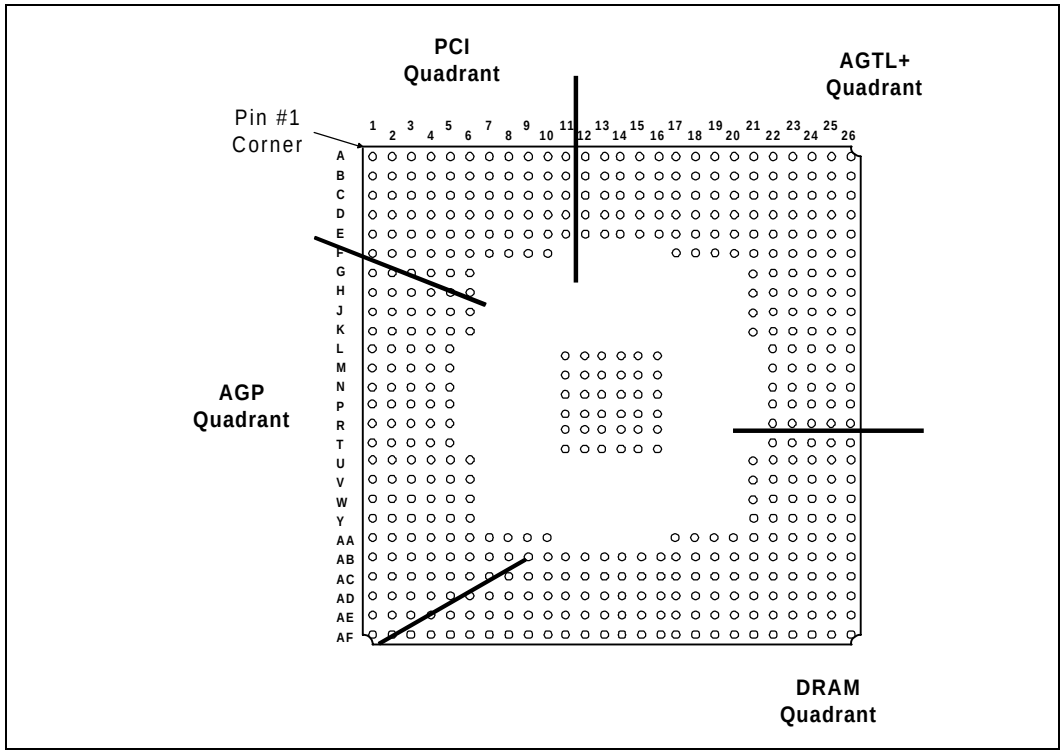
This section describes layout and routing recommendations to insure a robust design. Follow these guidelines as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

## 2.1 BGA Quadrant Assignment

Intel assigned pins on the 82443ZX to simplify routing and keep board fab costs down, this by permitting a motherboard to be routed in 4-layers. Figure 2-1 shows the 4 signal quadrants of the 82443ZX. The component placement on the motherboard should be done with this general flow in mind. This simplifies routing and minimizes the number of signals which must cross. The individual signals within the respective groups have also been optimized in order to be routed using only 2 PCB layers.

The 82443ZX datasheet contains a complete list of signals and ball assignments.

**Figure 2-1. Major Signal Sections (82443ZX Top View)**



## 2.2 Intel® Celeron™ Processor (PPGA) Signal Quadrants

**Figure 2-2. Intel® Celeron™ Processor (PPGA) Quadrants**

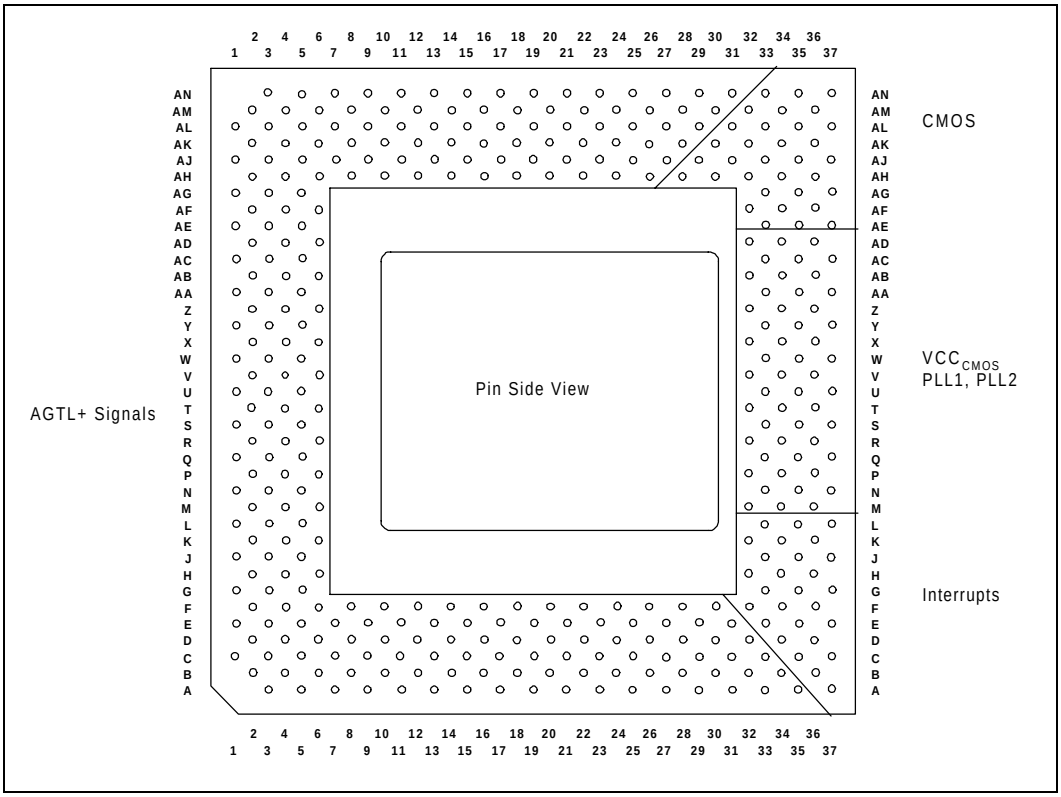
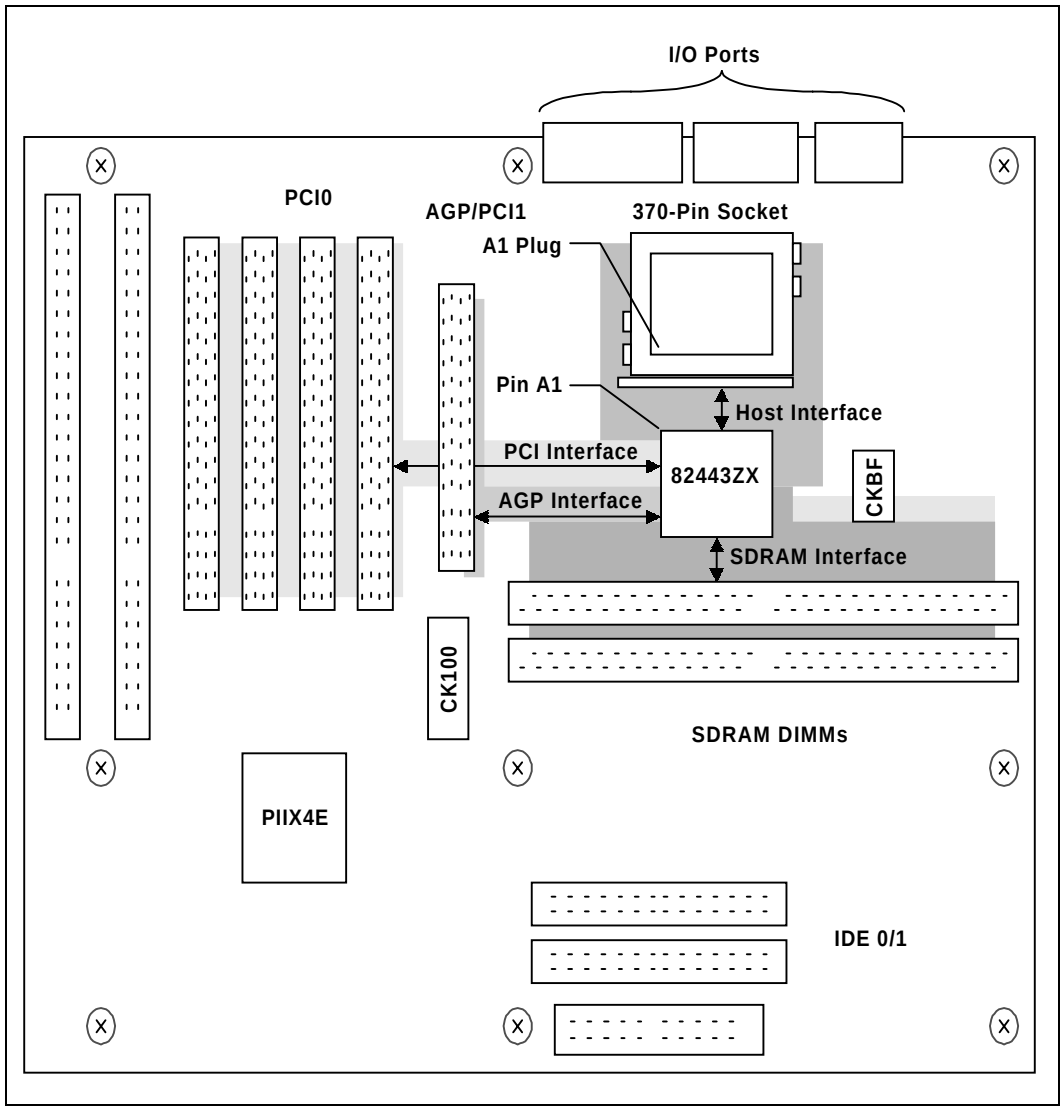



Figure 2-2 indicates the signal quadrants for the Intel Celeron™ processor (PPGA). These quadrants were defined to facilitate layout and placement and show the proposed component placement for an Intel Celeron™ processor (PPGA) for both ATX and NLX form factor designs.

**ATX Form Factor:**

1. The ATX placement and layout below is recommended for an Intel® Celeron™ processor (PPGA) / Intel® 440ZX-66 AGPset system design.
2. The example placement below shows 4 PCI slots, 2 ISA slots, 2 DIMM sockets, and one AGP connector.
3. For an ATX form factor design, the AGP compliant graphics device can be either on the motherboard (device down option) or on an AGP connector (up option).
4. The trace length limitation between critical connections will be addressed later in this document.
5. Figure 2-3 is for ***reference only*** and the trade-off between the number of PCI and ISA slots, number of DIMM sockets, and other motherboard peripherals needs to be evaluated for each design.

**Figure 2-3. Example ATX Placement for an Intel® Celeron™ Processor (PPGA) / Intel® 440ZX-66 AGPset Design**

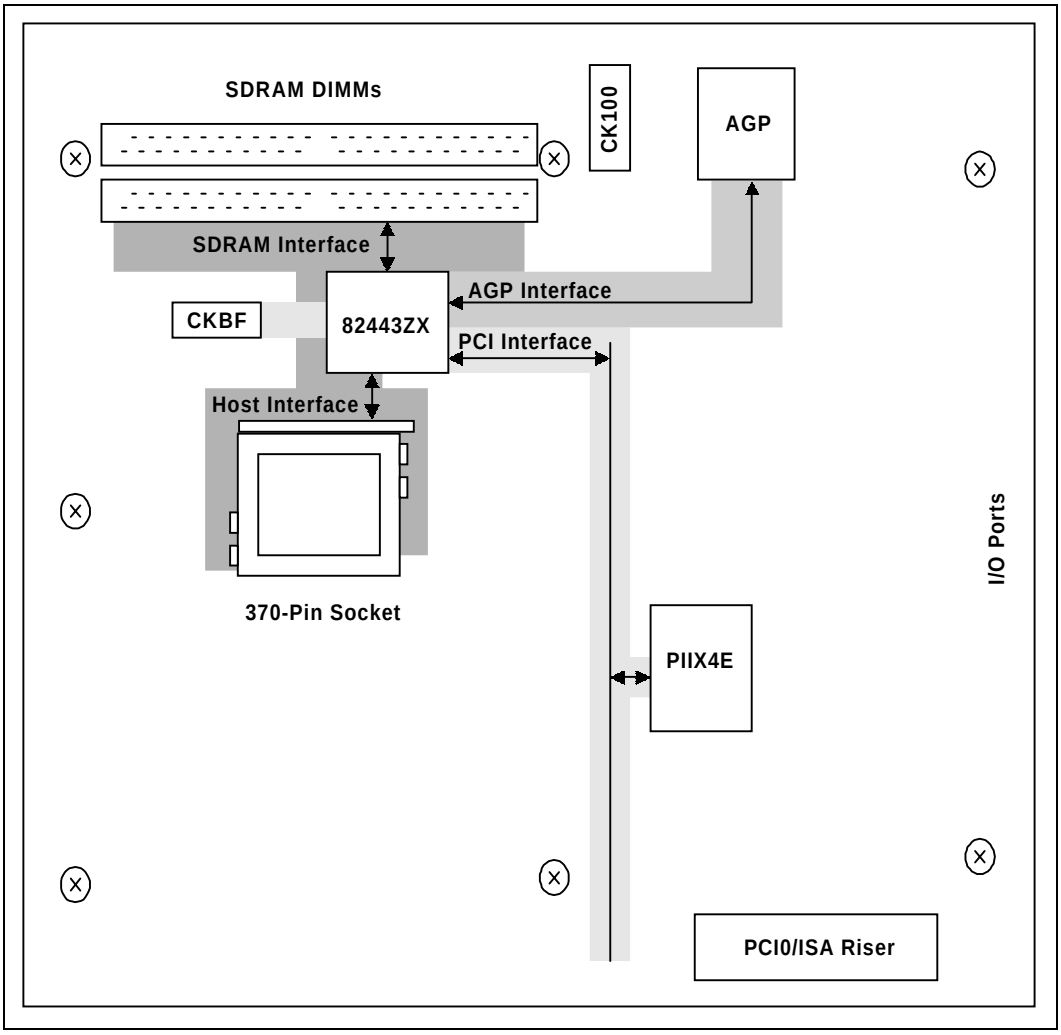


**NLX Form Factor:**

The NLX placement and layout below is recommended for a Intel® Celeron™ processor (PPGA) / Intel® 440ZX-66 AGPset system design.

1. The example placement below shows 2 DIMM sockets and an AGP compliant device down on the motherboard.
2. For an NLX form factor design, the AGP compliant graphics device may readily be integrated on the motherboard (device down option).
3. The trace length limitation between critical connections will be addressed later in this document.
4. Figure 2-4 is for ***reference only*** and the trade-off between the number of DIMM sockets and other motherboard peripherals needs to be evaluated for each design.

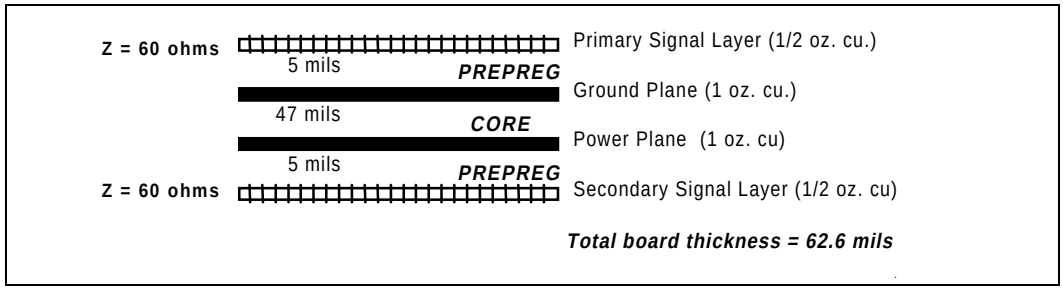
**Figure 2-4. Example NLX Placement for an Intel® Celeron™ Processor (PPGA) / Intel® 440ZX-66 AGPset Design**



## 2.3 Board Description

A 4-layer stack-up arrangement is recommended for the system board. An example of a 4-layer stack up is shown in Figure 2-5. The impedance of all the signal layers are to be between 55 and 75 ohms. Lower trace impedance will reduce signal edge rates, overshoot, and undershoot, and have less crosstalk than a higher trace impedance. Higher trace impedance will increase edge rates and may slightly decrease signal flight times.

**Figure 2-5. Four Layer Board Stack-up Example**




Note that the top and bottom routing layers specify $^{1}/_{2}$ oz. cu. However, by the time the board is plated, the traces will be about 1 oz. cu. Check with your fab vendor on the exact value and insure that any signal simulation accounts for this.

***Note:*** A thicker core may help reduce board warpage issues.

Additional guidelines on board stackup, placement, and layout include:

- Single-ended termination is recommended for AGTL+ signals. This requires one termination resistor present for each AGTL+ signal. The trace lengths should be controlled to 1.6” minimum and 4.3” maximum.
- The termination resistors on the AGTL+ bus should be 56 ± 5% ohms.
- The board impedance (Z) should be between 55 and 75 ohms (65 ± 15% ohms is recommended).
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power or ground plane, then it should be routed on a $V_{CC}$ plane, not the ground plane.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

## 2.4 Routing Guidelines

This section lists guidelines to be followed when routing the signal traces during board design. The order of which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. If the guidelines listed here are not followed, it is important that your design is simulated, especially on the AGTL+ signals. Even when the guidelines are followed, it is still a good idea to simulate as many signals as possible for proper signal integrity, flight time, and crosstalk.

### 2.4.1 AGTL+ Description

AGTL+ is the electrical bus technology used for both the Pentium® II processor and Intel® Celeron™ processor host buses. AGTL+ is a low output swing, incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at the end of the bus. The AGTL+ specification is contained in the *Intel® P6 Family Processor Developer's Manual*.

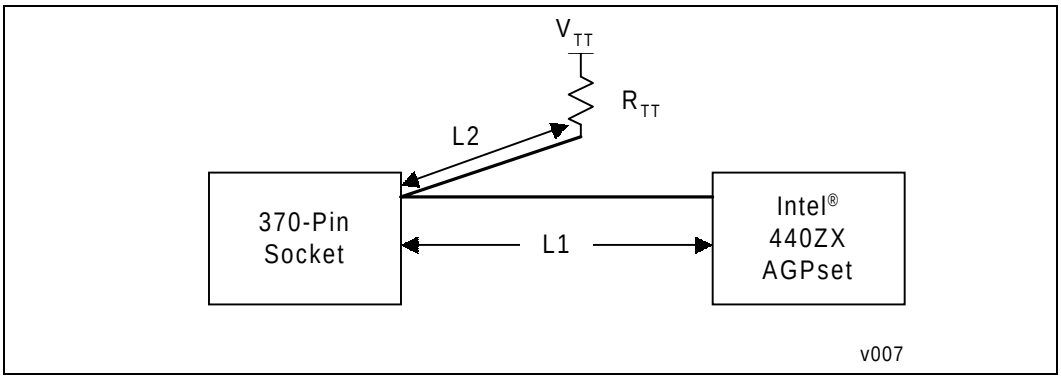
## 2.5 AGTL+ Layout Recommendations

This section contains the layout recommendations for the AGTL+ signals. The layout recommendations are derived from pre-layout simulations that Intel has performed.

### 2.5.1 Network Topology and Conditions

The recommended topology for single processor systems is shown in Figure 2-6. A termination resistor is placed on the system board. The recommended value for the termination resistor is 56 ± 5% ohms.

**Figure 2-6. Recommended Topology**




### 2.5.2 Recommended Trace Lengths

Trace length recommendations are summarized Table 2-1. The recommended lengths are derived from the parametric sweeps and Monte Carlo analysis.

**Table 2-1. Recommended Trace Lengths**

| Trace | Minimum Length | Maximum Length |
|---|---|---|
| L1 | 1.6” | 4.3” |
| L2 | 0.5” | 2.0” |

Intel recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design. Simulation will confirm that the design adheres to the guidelines.

#### 2.5.2.1 Single Processor Simulation Results

**Parametric Sweeps**

The values for interconnect parameter values that were used in all parametric sweeps are summarized in Table 2-2.

**Table 2-2. Model M Parameter Values For Interconnect SImulations**

| Component | Parameter | Fast | Typical | Slow |
|---|---|---|---|---|
| PPGA | $Z_0$ [Ω] | 74.75 | 65.00 | 55.25 |
| | $S_0$ [ns/ft] | 1.6 (µstrip)<br>1.8 (stripline & emb µstrip) | 1.8 (µstrip)<br>2.0 (stripline & emb µstrip) | 2.0 (µstrip)<br>2.2 (stripline & emb µstrip) |
| | length [in] | 2.0 | | 3.0 |
| Motherboard | $Z_0$ [Ω] | 74.75 | 65.00 | 55.25 |
| | $S_0$ [ns/ft] | 1.8 | 2.0 | 2.2 |
| Connector | $Z_0$ [Ω] | 75 | 65 | 50 |
| | $T_d$ [ps] | 30 | 100 | 120 |
| Termination | $R_{TT}$ [Ω] | 56 ± 5% | 56 | 56 ± 5% |
| | $V_{TT}$ [V] | 1.5 + 9% | 1.5 | 1.5 - 9% |

***Note:*** For simulation purposes, the socket connector can be modeled as a transmission line. The length of the line and the propagation speed must be selected such that they give a total delay of 120 ps in the slow case and 30 ps in the fast case.

## 2.5.3 Additional Guidelines

### 2.5.3.1 For More Information on AGTL+

The general rules for minimizing the impact of crosstalk and other practical considerations in the design of a high speed AGTL+ bus are discussed in the *Intel® 440BX AGPset Design Guide* document.

## 2.5.4 Performance Requirements

Prior to performing interconnect simulations, establish the minimum and maximum flight time requirements. Setup and hold requirements determine the flight time bounds for the system bus. The bus contains two paths which must be considered:

- the processor driving an AGPset component
- the AGPset component driving a processor

Table 2-3 provides recommended flight time specifications. Flight times are measured at the processor pins.

**Table 2-3. Recommended 66 MHz System Flight Time Targets**

| Driver | Receiver | $T_{flight,min}$ [ns] | $T_{flight,max}$ [ns] |
|---|---|---|---|
| Processor | AGPset | 0.20 | 1.82 |
| AGPset | Processor | 0.25 | 2.52 |

### 2.5.5 Topology Definition

As described in Section 2.5.1, AGTL+ is sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. AGTL+ signals should be connected in a daisy chain, keeping transmission line stubs to the processor under 2.0 inches.

### 2.5.6 Pre-Layout Simulation (Sensitivity Analysis)

After an initial timing analysis has been completed, simulations should be performed to determine the bounds on system layout. AGTL+ interconnect simulations using transmission line models are recommended to determine signal quality and flight times for proposed layouts. Recommended parameter values shown in Table 2-2 should be used for simulation. The recommended values in Table 2-2 may be replaced if your supplier's specific capabilities are known. The corner values should comprehend the full range of manufacturing variation. The Intel® Celeron™ processor (PPGA) models include the I/O buffer models, core package parasitics, package trace length, impedance, and velocity. Intel® 440ZX-66 AGPset models are available and include the I/O buffers and package traces. Termination resistors should be controlled to within ± 5%.

## 2.6 Post-Layout Simulation

Following layout, extract the traces and run simulations to verify that the layout meets timing and noise requirements. A small amount of trace "tuning" may be required, but experience at Intel has shown that a sensitivity analysis dramatically reduces the amount of tuning required.

The post layout simulations should take into account the expected variation for all interconnect parameters. For timing simulations, use a $V_{REF}$ of $^2/_3$ $V_{TT}$ ± 2% for both the processor and Intel® 440ZX-66 AGPset components. Flight times measured from the processor pins to other system components use the normal flight time method.

### 2.6.1 Crosstalk and the Multi-Bit Adjustment Factor

Coupled lines should be included in the post-layout simulations. The flight times listed in Table 2-3 apply to single bit simulations only. They do not include an allowance for crosstalk. Crosstalk effects are accounted for separately, as part of the multi-bit timing adjustment factor ($T_{adj}$) that is defined in Table 2-5. The recommended timing budget includes 300 ps for the adjustment factor.

Use caution in applying $T_{adj}$ to coupled simulations. This adjustment factor encompasses other effects besides board coupling, such as processor and package crosstalk, and ground return inductances. In general, the additional delay introduced by coupled simulations should be less than 300 ps.

## 2.7 Timing Analysis

To determine the available flight time window, perform an initial timing analysis. Analysis of setup and hold conditions will determine the minimum and maximum flight time bounds for the system bus. Use the following equations to establish the system flight time limits.

**Table 2-4. Intel® Celeron™ Processor and Intel® 440ZX-66 AGPset System Timing Equations**

| Driver | Receiver | Equation |
|---|---|---|
| processor | AGPset | $T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} + T_{skew,SKT}$ |
| | | $T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{skew,SKT} - T_{jit} - T_{adj}$ |
| AGPset | processor | $T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} + T_{skew,SKT}$ |
| | | $T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{skew,SKT} - T_{jit} - T_{adj}$ |

The terms used in the equations are described below.

**Table 2-5. Intel® Celeron™ Processor and Intel® 440ZX-66 AGPset System Timing Terms**

| Term | Description |
|---|---|
| $T_{cycle}$ | System cycle time, defined as the reciprocal of the frequency |
| $T_{flight,min}$ | Minimum system flight time. |
| $T_{flight,max}$ | Maximum system flight time. |
| $T_{co,max}$ | Maximum driver delay from input clock to output data. |
| $T_{co,min}$ | Minimum driver delay from input clock to output data. |
| $T_{su}$ | Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock. |
| $T_{h}$ | Minimum hold time. Defined as the time for which the input data must remain valid after the input clock. |
| $T_{skew,CLK}$ | Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator. |
| $T_{skew,PCB}$ | PCB skew. Defined as the maximum delay variation between clock signals due to system board variation and Intel® 440ZX-66 AGPset loading variation. |
| $T_{skew,SKT}$ | Skew due to delay in the 370-pin socket. |
| $T_{jit}$ | Clock jitter. Defined as the maximum edge to edge variation in a given clock signal. |
| $T_{adj}$ | Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise. |

Component timings for the Intel® Celeron™ processor are available in the *Intel® Celeron™ Processor* Datasheet.

Recommended values for system timings are contained in Table 2-6. Skew and jitter values for the clock generator device come from the clock driver vendor's datasheet. The PCB skew specification is based on the results of extensive simulations at Intel. The $T_{adj}$ value is based on Intel's experience with systems that use the Intel® Pentium® Pro and Intel® Pentium® II processors.

**Table 2-6. Recommended 66 MHz System Timing Parameters**

| Timing Term | Value |
|---|---|
| $T_{skew,CLK}$ [ns] | 0.00 |
| $T_{skew,SKT}$ [ns] | 0.05 |
| $T_{skew,PCB}$ [ns] | 0.15 |
| $T_{jit}$ [ns] | 0.25 |
| $T_{adj}$ [ns] | 0.30 |

The flight time requirements that result from using the component timing specifications and recommended system timings are summarized in Table 2-3. All component values should be verified against the latest specifications before proceeding with analysis.

# 2.8 82443ZX Layout and Routing Guidelines

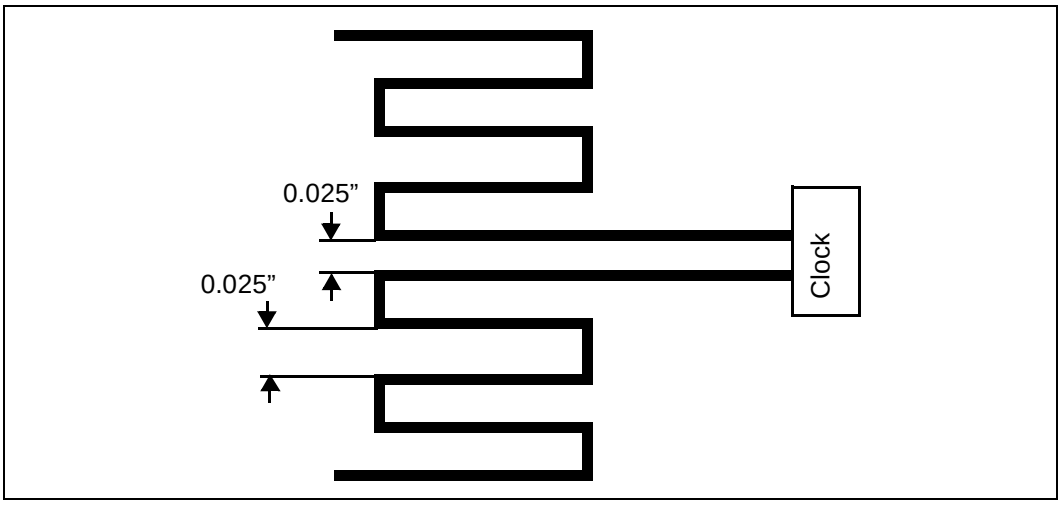
## 2.8.1 82443ZX Clock Layout Recommendations

### 2.8.1.1 Clock Routing Spacing

The Intel® Celeron™ / Intel® 440ZX-66 AGPset platform requires a clock synthesizer for supplying 66 MHz system bus clocks, PCI clocks, APIC clocks, SDRAM clocks, and 14 MHz clocks.

To minimize the impact of crosstalk, a minimum of 0.025" spacing should be maintained between the clock traces and other traces. A minimum spacing of 0.025" is also recommended for serpentines.

**Figure 2-7. Clock Trace Spacing Guidelines**



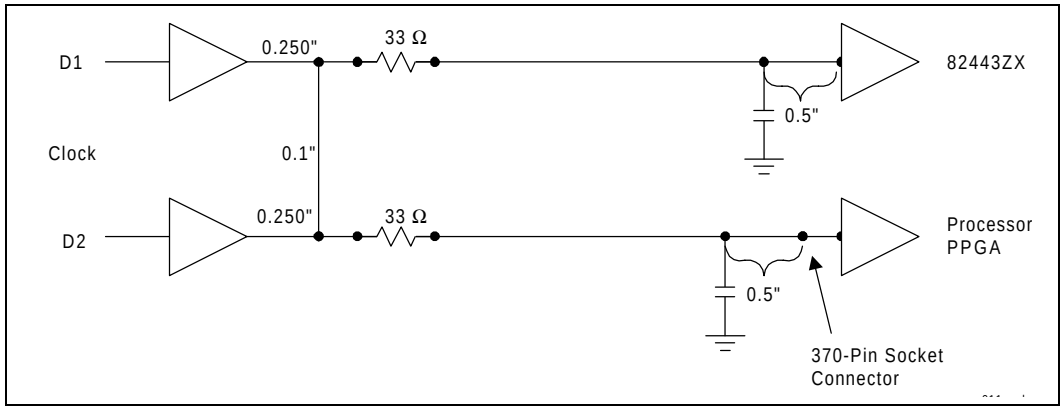
### 2.8.1.2 System Clock Layout

Intel recommends 33 ohm series termination for all system bus clocks. The pin-to-pin skew of the clock generator can be reduced by tying the clock driver pins together at the clock chip. The recommended topology is defined below (See Figure 2-8).

Note that the trace lengths to the processor socket and the 82443ZX are not specified. They are system dependent and it is up to the system designer to determine what length is best for their motherboard. Two items that need to be considered when determining the clock lengths are the additional delay due to the socket (30 ps - 120 ps) and loading differences between the 82443ZX and the processor. Also, the maximum trace length should not exceed 9.0". It is recommended that the clock skew be kept to less than 200 ps in order to avoid affecting the timing budget.

Tuning capacitors are recommended on each clock signal. They involve placing 0603 package capacitor sites within 0.5" of both the socket connector and 82443ZX ball. Each capacitor site should have a pad placed on the clock trace itself, avoiding the creation of a stub which can affect signal integrity on the clock line. The capacitor site is there to allow the system designer the flexibility of adjusting the slew rate of each clock (adjusting the load), thereby minimizing the skew between them.

**Figure 2-8. Host Clock Topology**




### 2.8.1.3 Other Busses

Busses not mentioned in the previous sections should adhere to the recommendations set forth in the *Intel® 440BX AGPset Design Guide* document.

# 3

# Design Checklist

# Design Checklist 3

## 3.1 Overview

The following checklist is intended to be used for schematic reviews of Intel® 440ZX-66 AGPset desktop designs. It will be revised as new information is available.

## 3.2 Pull-up and Pull-down Resistor Values

Pull-up and pull-down values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc.. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, overshoot/undershoot, and other considerations.

A simplistic DC calculation for a pull-up value is:

$$R_{MAX} = (V_{CC_{PU}}\ MIN - V_{IH}\ MIN) / I_{LEAKAGE}\ MAX$$

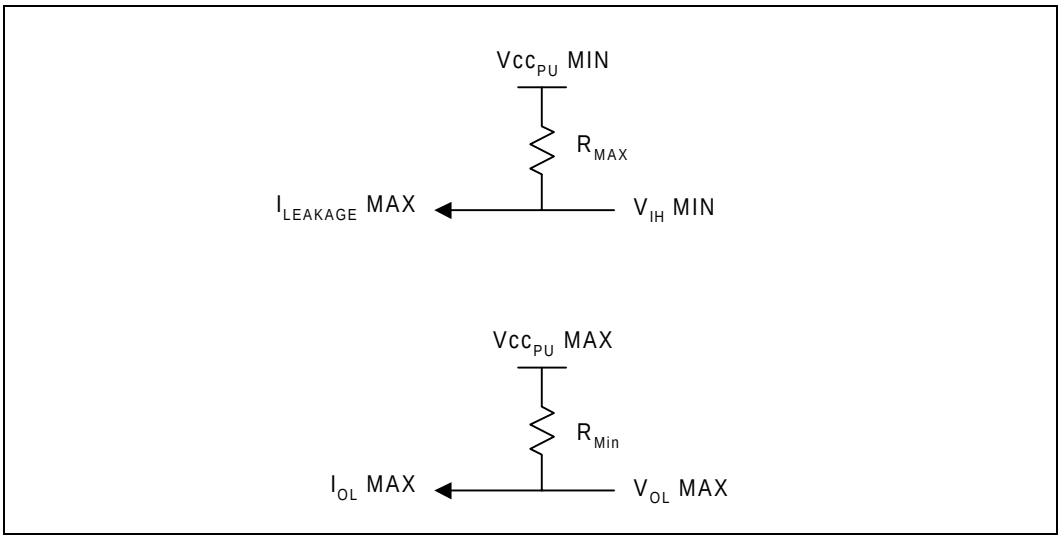
$$R_{MIN} = (V_{CC_{PU}}\ MAX - V_{OL}\ MAX) / I_{OL}\ MAX$$

Since $I_{LEAKAGE}$ MAX is normally very small, $R_{MAX}$ may not be meaningful. $R_{MAX}$ is also determined by the maximum allowable rise time. The following calculation allows for t (maximum allowable rise time) and C (total load capacitance in the circuit, including input capacitance of the devices to be driven, output capacitance of the driver, and line capacitance). This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / ( C * \ln ( 1 - ( V_{IH}\ MIN / V_{CC_{PU}}\ MIN ) ) )$$

It is recommended that a SPICE or equivalent simulation be run to determine the proper values.

**Figure 3-1. Pull-up Resistor Example**




# 3.3 Processor Checklist

## 3.3.1 Intel® Celeron™ Processor

**Table 3-1. AGTL+ Connectivity (Sheet 1 of 2)**

| CPU Pin | Pin Connection |
|---|---|
| A[31:3] | Terminate to VTT / Connect to 82443ZX PAC |
| ADS# | Terminate to VTT / Connect to 82443ZX PAC |
| BNR# | Terminate to VTT / Connect to 82443ZX PAC |
| BP[3:2]# | Leave as NO CONNECT<br>Optional Debug:<br>If used, terminate to VTT |
| BPM[1:0] | Leave as NO CONNECT<br>Optional Debug:<br>If used, terminate to VTT |
| BPRI# | Terminate to VTT / Connect to 82443ZX PAC |
| BR[0]# | Terminate to VTT / Connect to 82443ZX PAC pin BREQ#<br>Optional: connect to ground with a 10 - 450 ohm resistor |
| D[63:0]# | Terminate to VTT / Connect to 82443ZX PAC |
| DBSY# | Terminate to VTT / Connect to 82443ZX PAC |
| DEFER# | Terminate to VTT / Connect to 82443ZX PAC |
| DRDY# | Terminate to VTT / Connect to 82443ZX PAC |
| HIT# | Terminate to VTT / Connect to 82443ZX PAC |
| HITM# | Terminate to VTT / Connect to 82443ZX PAC |
| LOCK# | Terminate to VTT / Connect to 82443ZX PAC |

### Table 3-1. AGTL+ Connectivity (Sheet 2 of 2)

| CPU Pin | Pin Connection |
|---|---|
| PRDY# | Leave as NO CONNECT<br>Optional Debug:<br>Terminate to $V_{TT}$ / 240 ohm series resistor to ITP connector |
| REQ[4:0]# | Terminate to $V_{TT}$ / Connect to 82443ZX PAC |
| RESET# | Terminate to $V_{TT}$ / Connect to 82443ZX PAC,<br>Optional Debug:<br>240 ohm series resistor to ITP connector |
| RS[2:0]# | Terminate to $V_{TT}$ / Connect to 82443ZX PAC |
| TRDY# | Terminate to $V_{TT}$ / Connect to 82443ZX PAC |

### Table 3-2. CMOS Connectivity

| CPU Pin | Pin Connection |
|---|---|
| A20M# | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| BSEL | Pull-up to $V_{CC_{2.5}}$ with a 200 ohm resistor. Connect to 82443ZX PAC. |
| FERR# | Pull-up to $V_{CC_{CMOS}}$ with a 150 - 10K ohm resistor. Connect to PIIX4E. |
| FLUSH# | Leave as NO CONNECT |
| IERR# | Leave as NO CONNECT<br>Optional:<br>Pull-up to $V_{CC_{CMOS}}$ and connect to error logic |
| IGNNE# | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| INIT# | Pull-up to $V_{CC_{CMOS}}$ with a 300 - 10K ohm resistor. Connect to PIIX4E. |
| LINT[1:0] | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| PICD[1:0] | Pull-up to $V_{CC_{CMOS}}$ with a 150 ohm resistor. |
| PREQ# | Pull up to $V_{CC_{CMOS}}$ with a 150 - 5K ohm resistor. Optional debug; connect to ITP. |
| PWRGOOD | Pull-up to $V_{CC_{2.5}}$ with a 50 - 5K ohm resistor. Connect to power sense logic. |
| SLP# | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| SMI# | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| STPCLK# | Pull-up to $V_{CC_{CMOS}}$ with a 650 - 5K ohm resistor. Connect to PIIX4E. |
| THERMTRIP# | NO CONNECT. Optional: pull-up to $V_{CC_{CMOS}}$ with a 150 - 10K ohm resistor and connect to error logic. |

### Table 3-3. TAP Connectivity (optional)

| CPU Pin | Pin Connection |
|---|---|
| TCK | 150 - 6.75K ohm pull-up to $V_{CC_{CMOS}}$. 47 ohm series resistor to processor. |
| TDO | Connected to ITP/processor. 150 - 900 ohm pull-up to $V_{CC_{CMOS}}$. |
| TDI | Connected to ITP/processor. 150 - 500 ohm pull-up to $V_{CC_{CMOS}}$. |
| TMS | 150 - 6.75K ohm pull-up to $V_{CC_{CMOS}}$. 47 ohm series resistor to processor. |
| TRST# | Connect to ITP/processor. 150 - 5K ohm pull-down. |

**NOTE:** If not used, connect TCK, TD1, TMS, and TRST# to valid logic level; do not leave floating.

**Table 3-4. Miscellaneous Connectivity**

| CPU Pin | Pin Connection |
|---|---|
| BCLK | Connect to CK3D. Gang with PAC HCLK, 33 ohm series resistor |
| CPUPRES# | Tie to GND. Optionally pull-up for external logic. |
| EDGCTRL | Pull-up to $V_{CC_{CORE}}$ with a 51 ± 5% ohm resistor |
| PICCLK | Connect to CK3D. 33 ohm series resistor. |
| PLL1 & PLL2 | See Section 1.5.7. for inductor and capacitor values |
| THERMDN | NO CONNECT if not used |
| THERMDP | NO CONNECT if not used |
| $V_{CC_{1.5}}$ | Leave as NO CONNECT |
| $V_{CC_{2.5}}$ | Connect to 2.5 V supply |
| $V_{CC_{CMOS}}$ | Use for system CMOS pull-up voltage. Provide 0.1 µF decoupling |
| $V_{CC_{CORE}}$ | Connect to VRM output/<br>Decoupling Guidelines:<br>10 each (min) 4.7 µF in 1206 package / 19 each (min) 1.0 µF in 0805 package |
| $V_{CORE_{DET}}$ | Pull-up to $V_{CC_{3.3}}$ with a 220 - 450 ohm resistor. Connect to system shutdown logic. |
| VID[3:0] | 10K ohm pull-up to 5 V; connect to VRM. |
| VID[4] | Not on processor, Connect VRM controller pin to ground |
| $V_{REF}$[7:0] | Connect to $V_{REF}$ voltage divider made up of 75 ± 1% and 150 ± 1% ohm resistors connected to $V_{TT}$/<br>Decoupling Guidelines:<br>4 ea. (min) 0.1 µF in 0603 package |
| $V_{SS}$ | Tie to GND |
| $V_{TT}$ | Decoupling Guidelines:<br>14 each (min) 0.1 µF in 0603 package |
| Reserved | Leave as NO CONNECT. |

## 3.3.2 GND & Power Pin Definition

Refer to the *Intel® Celeron™ Processor* and *Intel® 440ZX AGPset* Datasheets for this information.

## 3.3.3 Processor Clocks

- PICCLK must be driven by a clock even if an I/O APIC is not being used. This clock can be as high as 33.3 MHz in a UP system.

### 3.3.4 Processor Signals

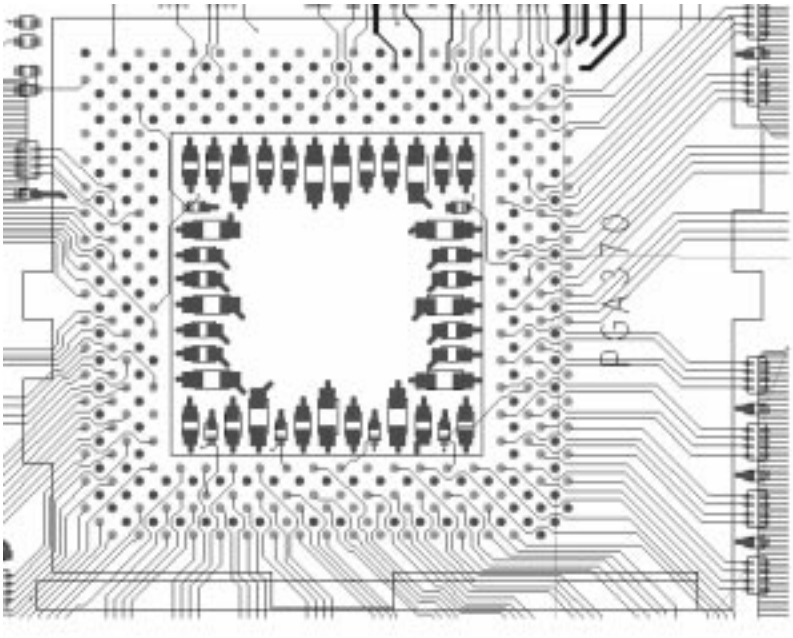
- THERMTRIP# must be pulled-up to $V_{CC_{CMOS}}$ (150 ohm - 10K ohm) if used by system logic. The signal may be wire-OR'ed and does not require an external gate. It may be left as NO CONNECT if it is not used.
- The FERR# output must be pulled up to $V_{CC_{CMOS}}$ (150 ohm - 10K ohm) and connected to the PIIX4E. Please see the reference schematics.
- PICD[1:0]# must have 150 ohm pull-ups to $V_{CC_{CMOS}}$ even if an I/O APIC is not being used.
- All CMOS inputs should be pulled up to $V_{CC_{CMOS}}$ with appropriate resistor value.
- Be sure the processor inputs are not being driven by 3.3 V or 5 V logic. Logic translation of 3.3 V or 5 V signals may be accomplished by using open-drain drivers pulled-up to $V_{CC_{CMOS}}$.
- The PWRGOOD input should be driven to the appropriate level from the active-high "AND" of the "Power Good" signals from the 5 V, 3.3 V, and $V_{CC_{CORE}}$ supplies. The output of any logic used to drive PWRGOOD should be a 2.5 V level to the processor.
- $V_{REF}$ should be generated for the processor. Intel recommends using a 75 ± 1% and 150 ± 1% ohm resistor divider with $V_{TT}$ for generating $V_{REF}$. $V_{REF}$ is not locally generated on the processor as on the S.E.P. Package.
- $V_{TT}$ must have adequate bulk decoupling based on the reaction time of the regulator used to generate $V_{TT}$. It must provide for a current ramp of up to 8 A/mS while maintaining the voltage tolerance defined in the *Intel® Celeron™ Processor* Datasheet. In addition, $V_{TT}$ must have adequate high frequency decoupling on the system board. See decoupling guidelines.
- If an onboard voltage regulator is used instead of a VRM, $V_{CC_{CORE}}$ must have adequate bulk decoupling based on the reaction time of the regulator used to generate $V_{CC_{CORE}}$. It must provide for a current ramp of up to 240 A/mS while maintaining the *VRM 8.2 DC-DC Converter Specification*.
- The VID lines should have pull-up resistors on them ONLY if they are required by the Voltage Regulator Module or on board regulator that you have chosen. The pull-up voltage used should be to the regulator input voltage (5 V or 12 V), however, if 12 V is used, a resistor divider should be utilized to lower the VID signal to CMOS/TTL levels. A pull-up is not required unless the VID signals are used by other logic requiring CMOS/TTL logic levels. The VID lines on the processor are 5 V tolerant.
- The JTAG port must be properly terminated even if it is not used.
- TRST# must be driven low during reset to all components with TRST# pins. Connecting a pull-down resistor to TRST# will accomplish the reset of the port. See figures in the Integration Tools chapter of the *Pentium® II processor Developer's Manual (order number 243502)*.
- A single $V_{TT}$ regulator may be used. A simplistic, single ended termination, calculation for maximum worst case current is 3.6 A. This takes into consideration that some signals are not used by the Intel® 440ZX-66 AGPset.
- Motherboards planning to support the boxed processor must provide a matched power header for the boxed processor fan/heatsink power cable connector. Consult the *Intel® Celeron™ Processor* datasheet for specifications of the fan power cable connector. The power header must be positioned within close proximity to the 370-pin socket.
- The CPUPRES# signal is a ground on the processor. The presence of a CPU core can be determined with this pin if it is pulled up on the system board. If not used, connect to ground to provide additional support to the processor.
- DBRESET (ITP Reset signal) requires a 240 ohm pull-up to $V_{CC_{3.3}}$.
- The system board should connect BR0# of the processor to the 82443ZX's BREQ0# signal. This will assign an agent ID of 0 to the processor. Optionally, this signal may be grounded with a 10 - 450 ohm resistor.

## 3.3.5 Processor Decoupling Capacitors

### 3.3.5.1 Core Voltage High Frequency Decoupling

- Intel recommends ten or more 4.7 µF in a 1206 package and nineteen or more 1.0 µF in a 0805 package. All capacitors should be placed within the socket cavity and mounted directly on the primary side of the motherboard. The capacitors should be arranged to minimize the overall inductance between $V_{CC}$ / $V_{SS}$ power pins (See Figure 3-2). These recommendations are adequate for future Intel Celeron processors with $V_{CC_{CORE}}$ of 2.0 V, and $I_{CC_{CORE}}$ of 0.8 A to 15.2 A.

**Figure 3-2. Capacitor Placement Study**



- Contact your regulator vendor for bulk decoupling recommendations that will meet the *VRM 8.2 DC-DC Converter Guidelines.*
- Decoupling capacitor traces should be as short and wide as possible.
- The VRM 8.2 regulator provides the Flexible Motherboard guidelines for processor voltage and current.

## 3.4 Thermals / Cooling Solutions

- For the Intel® Celeron™ processor, an adequate heat sink and air ventilation must be provided to ensure that the TCASE specification documented in the *Intel® Celeron™ Processor* datasheet is met. Please see the *Pentium® II Processor Power Distribution Guidelines*, and *Pentium II Processor Thermal Design Guidelines* for thermal design information.
- The Flexible Motherboard guidelines for processor power dissipation is 30 W at a TCASE of 70 °C.
- Verify that all major components, including the 82443ZX can be cooled the way they are placed.

### 3.4.1 Design Considerations:

- Could anything block the air flow to or from the processor (I/O cards, VRM etc.)?
- Is there anything between the processor and the air intake that may preheat the air flowing into the fan/heatsink?
- If a system fan (other than the power supply fan) is used, have all recirculation paths been eliminated?
- What is the air flow through the PSU/system fan?
- What is the maximum ambient operation temperature of the system?

## 3.5 Mechanicals

- For the processor: The physical space requirements of the processor must be met. See the *Intel® Celeron™ Processor* Datasheet for details. In addition the physical space requirements of your heatsink must be met.
- For the boxed processor: The physical space requirements of the boxed processor fan/heatsink must be met. See the *Intel® Celeron™ Processor* Datasheet for details.

# 3.6 Electricals

## 3.6.1 Design Considerations

- It is recommended that simulations be performed on the AGTL+ bus to ensure that proper bus timings and signal integrity are met, especially if the layout guideline recommendations in this document are not followed.
- It is recommended that simulations be performed to ensure proper timings and signal integrity is met, especially if the non-AGTL+ (CMOS) layout guideline recommendations in this document are not followed.
- Verify the voltage range and tolerance of your VRM or onboard regulator adequately cover the $V_{CC_{CORE}}$ requirements of the processor is supported.
- Verify the maximum current value your VRM or onboard regulator can support at $V_{CC_{CORE}}$. This should meet the value specified by the *VRM 8.2 DC-DC Converter Guidelines*.
- Verify the voltage tolerance of your VRM or onboard regulator at $V_{CC_{CORE}}$. This should meet the value specified by the *VRM 8.2 DC-DC Converter Guidelines.*
- Adequate 5 V and/or 3.3 V decoupling should be provided for all components.
- $V_{REF}$ for the AGPset should be decoupled to $V_{TT}$ with 0.001 µF capacitors at each voltage divider. It should be decoupled to ground, to ensure an even better solution.
- It is recommended that AC/DC analysis be performed to determine proper pull-up and pull-down values.

# 4

# Debug Recommendations

# Debug Recommendations 4

This section provides tool and model information.

## 4.1 Debug/Simulation Tools

### 4.1.1 Logic Analyzer Interface (LAI)

**Table 4-1. Third-Party LAIs & Logic Analyzer Software**

| Vendor | Phone Number/ Web address | Revision | Available | Price |
|---|---|---|---|---|
| Hewlett Packard Co. | 1-800-452-4844<br>www.tmo.hp.com/tmo | Contact Vendor | Contact Vendor | Contact Vendor |
| American Arium | 714-731-1661<br>www.arium.com | Contact Vendor | Contact Vendor | Contact Vendor |
| Tektronix Inc. | 503-627-1922<br>www.tek.com/Measurement | Contact Vendor | Contact Vendor | Contact Vendor |

***Note:*** Contact the respective tool vendor for details. Certain products are available only under RS-NDA and license agreement. Contact your Intel Field Sales representative.

### 4.1.2 In-Target Probe (ITP)

The ITP32A provides a software debug capability allowing the setting/clearing of hardware/ software breakpoints, assembly/disassembly of code, display/modification of the processor register set, display/modification of system memory, display/modification of I/O space and includes a macro language for custom debug procedure creation, etc. Contact your local Field Sales representative for availability of this tool from Intel.

### Table 4-2. Intel In-Target Probe (ITP) Debuggers

| Part Number | Supported Processors | Revision | Available | Price |
|---|---|---|---|---|
| ITP32A | P6 family processors | 1.5 | Yes | Note 2 |
| ITP32AUP | P6 family processors | 1.5 | Yes | Note 2 |
| ITP565UPGFR560 | P6 family processors | 1.5 | Yes | Note 2 |

**NOTES:**
1. For ITP technical support: Call 1-800-628-8686 and ask for help with an “XTG tool”.
2. Contact your local Intel Field Sales representative.

### Table 4-3. Third-Party ITP-like Debuggers and Run Control Solutions

| Tool Vendor | Phone Number/ Web address | Revision | Available | Price |
|---|---|---|---|---|
| American Arium | 714-731-1661<br>www.arium.com | Contact Vendor | Contact Vendor | Contact Vendor |
| Hewlett-Packard Co. | 1-800-452-4844<br>www.tmo.hp.com/tmo | Contact Vendor | Contact Vendor | Contact Vendor |

**NOTES:**
1. Contact the respective tool vendor for details. Certain products are available only under RS-NDA and license agreement.

Contact your local Intel Field Sales representative to complete the proper software license agreement and non-disclosure agreement required to receive the ITP.

## 4.1.3 I/O Buffer Models

IBIS Models are available from Intel for:

1. Intel® Celeron™ Processor (QUAD XTK only)
2. 82443ZX IBIS Models
3. PIIX4E PCI-to-ISA IDE Xcelerator IBIS Models

Contact your local Intel Field Sales representative for a copy of these models and to complete the appropriate non-disclosure agreements.

# 5

# Third Party Vendors

# Third-Party Vendor Information 5

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This section refers to listings of various third-party vendors who provide products to support the Intel® Celeron™ Processor and the Intel® 440ZX-66 AGPset. The lists of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing, and compatibility.

## 5.1 Voltage Regulator Control Silicon

Intel's *Developer* web site lists vendors who offer DC-DC converter silicon and reference designs for Celeron processor voltage and current requirements per the *VRM 8.2 DC-DC Converter Design Guidelines*.

http://developer.intel.com/design/celeron/components/#POWER.

## 5.2 Clock Drivers

Intel's *Developer* web site lists vendors who offer clock drivers for the Celeron processor and Intel® 440ZX-66 AGPset.

http://developer.intel.com/design/celeron/components/#CLOCK.

## 5.3 370-Pin Socket

The *370-pin Socket Guidelines* document can be obtained from:

http://developer.intel.com/desgin/celeron/applnots/244410.htm

# A

# Reference Design Schematics

# Intel(R) Celeron(tm) Processor/440ZX AGPset Uniprocessor Customer Reference Schematics

## Revision 1.3

**** Please note that these schematics are subject to change.**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Title
Intel(R) Celeron(tm) processor/440ZX AGPset Uni-Processor Cover Sheet

| Size | Document Number | Rev |
|---|---|---|
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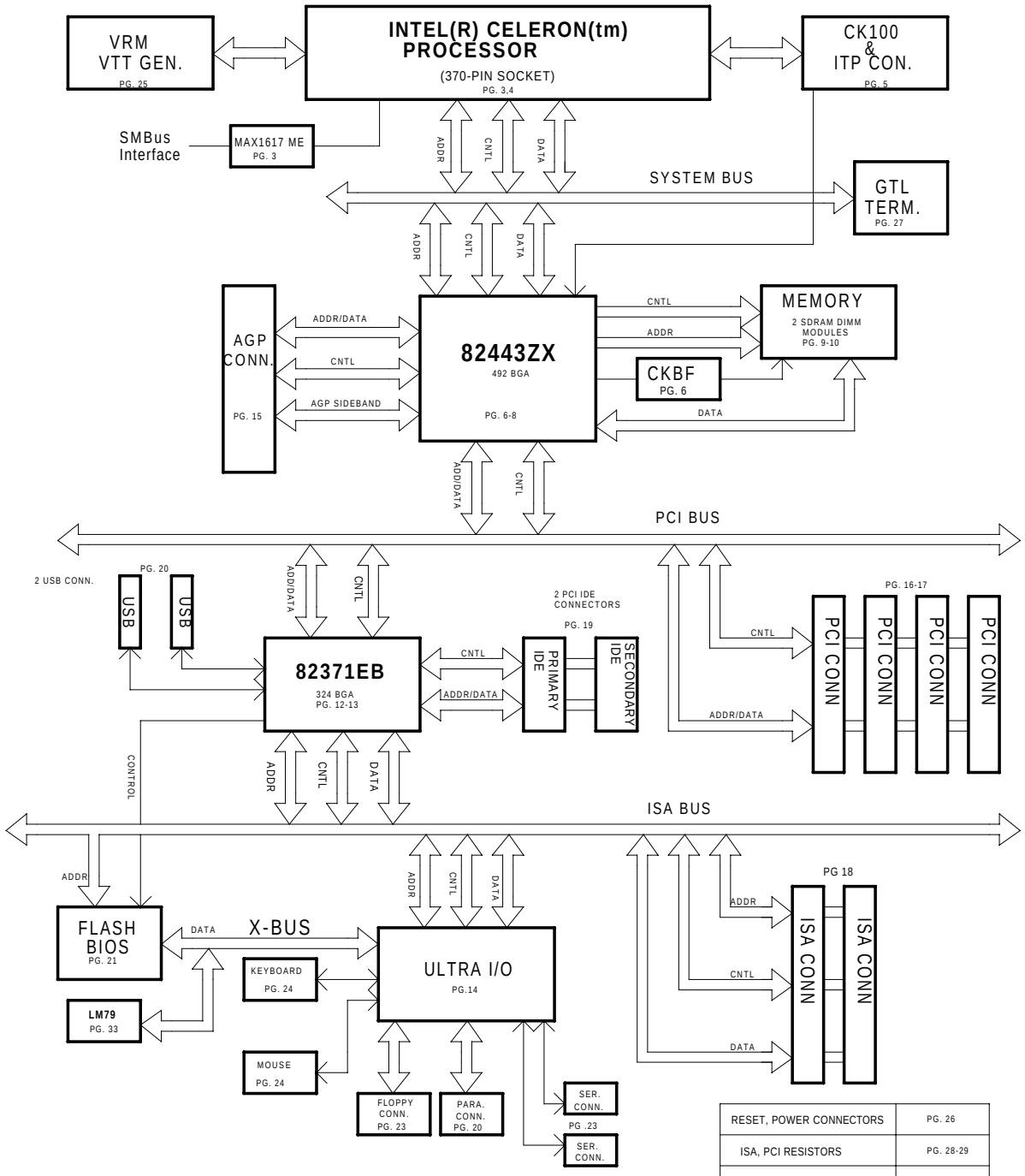


| | |
|---|---|
| RESET, POWER CONNECTORS | PG. 26 |
| ISA, PCI RESISTORS | PG. 28-29 |
| DECOUPLING CAPACITORS | PG. 30-32 |

THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AN END USER PRODUCT. iNTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

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| 370 PIN SOCKET | J33 A,B | 3,4 |
| AGP Connector | J32 | 15 |
| PCI Connectors | J34-37 | 16,17 |
| | | |
| BLM31A700S | L1-L6,L7-L13 | 20,24 |
| | | |
| CK100 | U1 | 5 |
| 74LVC14 **3VSB** | U5 A,B,C,D,E,F | 13,26 |
| FDC37C932FR | U6 | 14 |
| 74AS07 | U7 A,B,C,D,E,F | 15,26,29 |
| 74HCT14 | U8 A,B,C,D,E,F | 21,25,26 |
| E28F002BC-T(FLASH) | U9 | 21 |
| 74F07 | U12 A,B,C,D,E,F | 25,26,29 |
| 74LVC3244 | U13 | 25 |
| | | |
| 74ALS08 | U16 A,B,C,D | 26,29 |
| 74HC10 **5VSB** | U17 A,B,C | 13,26,29 |
| 82443ZX | U19-1,2,3 | 6,7,8 |
| CKBF | U20 | 6 |
| LM79 | U21 | 33 |
| 74F07 **5VSB** | U28 A,B,C,D,E,F | 13,26,29 |
| 82371EB (PIIX4E) | U23 A,B | 12,13 |
| MAX1617 ME | U24 | 3 |
| 74HC112 | U27 A,B | 13 |
| | | |
| LT1585 | VR1 | 25 |
| LT1575 | VR2 | 25 |
| | | |
| Crystal (14.318MHz) | Y1 | 5 |
| Crystal(32.768KHz) | Y2 | 13 |


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Title: INTEL(R) Celeron(tm) processor/440ZX AGPset Block Diagram

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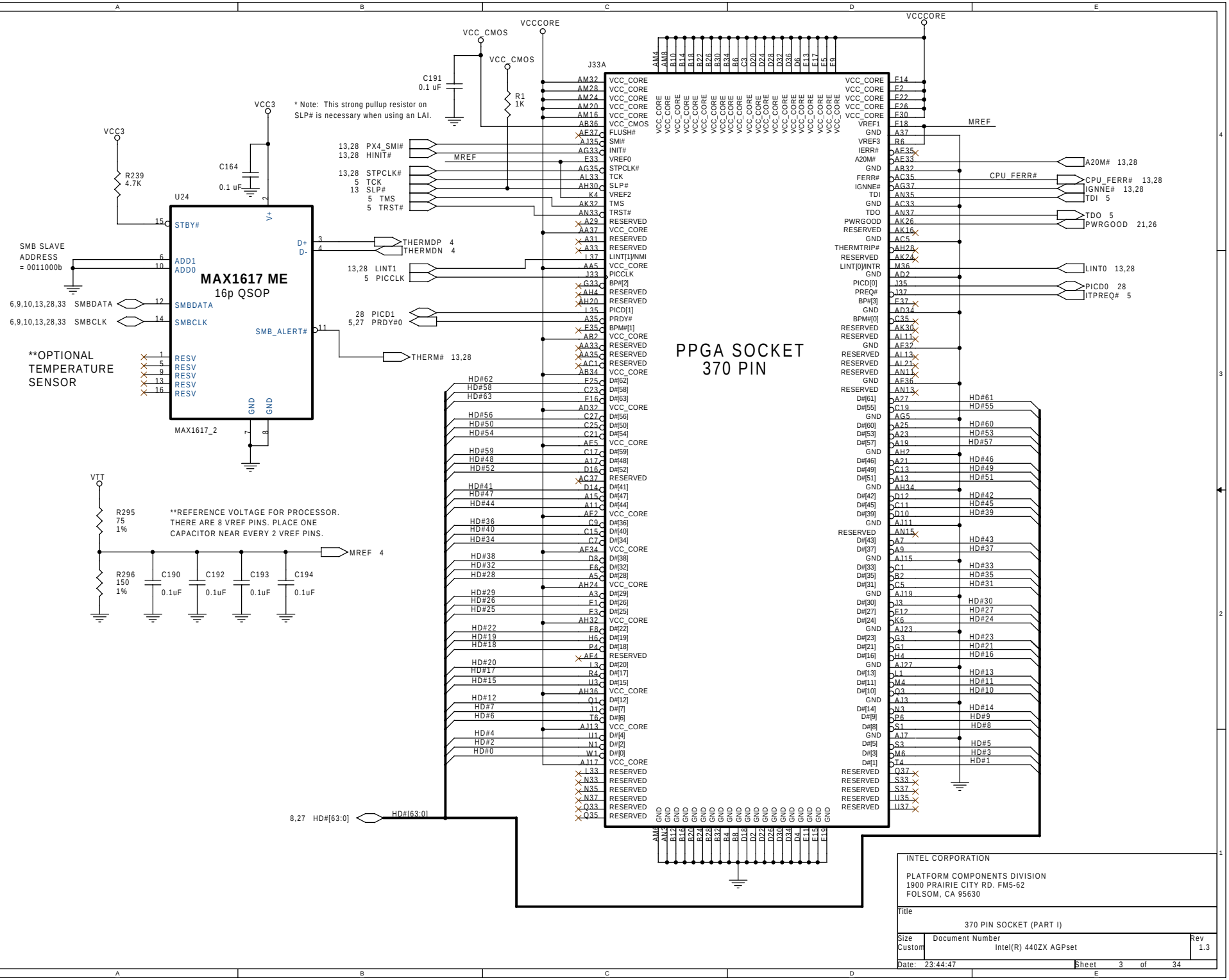
VCCCORE
VCC_CMOS
C191
0.1 uF
R1
1K
J33A
PPGA SOCKET
370 PIN
* Note: This strong pullup resistor on SLP# is necessary when using an LAI.
VCC3
R239
4.7K
C164
0.1 uF
U24
MAX1617 ME
16p QSOP
STBY#
V+
D+
D-
ADD1
ADD0
SMBDATA
SMBCLK
SMB_ALERT#
GND
MAX1617_2
SMB SLAVE
ADDRESS
= 0011000b
**OPTIONAL
TEMPERATURE
SENSOR
RESV
THERMDP 4
THERMDN 4
LINT1
PICCLK
PICD1
PRDY#0
THERM# 13,28
VTT
R295
75
1%
R296
150
1%
C190
C192
C193
C194
0.1uF
**REFERENCE VOLTAGE FOR PROCESSOR.
THERE ARE 8 VREF PINS. PLACE ONE
CAPACITOR NEAR EVERY 2 VREF PINS.
MREF 4
HD#[63:0]
8,27 HD#[63:0]
PX4_SMI#
HINIT#
STPCLK#
TCK
SLP#
TMS
TRST#
FLUSH#
SMI#
INT#
VREF0
VREF2
VREF1
VREF3
IERR#
A20M#
FERR#
IGNNE#
TDI
TDO
PWRGOOD
THERMTRIP#
PICD[0]
PREQ#
BP#[3]
BPM#[0]
BPM#[1]
BP#[2]
PICD[1]
PRDY#
D#[63:0]
A20M# 13,28
CPU_FERR#
FERR# 13,28
IGNNE# 13,28
TDI 5
TDO 5
PWRGOOD 21,26
LINT0 13,28
PICD0 28
ITPREQ# 5
INTEL CORPORATION
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Title
370 PIN SOCKET (PART I)
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Custom
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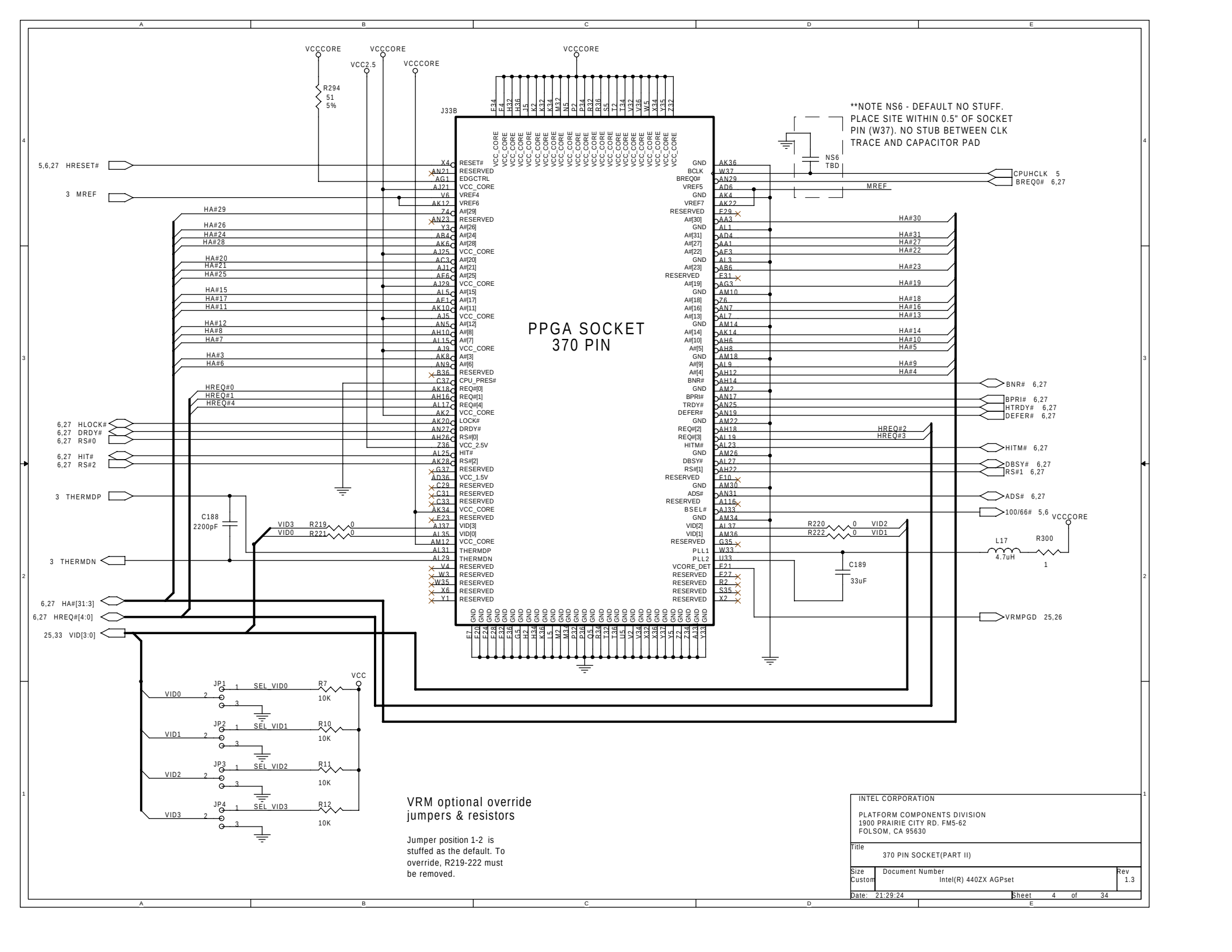
PPGA SOCKET
370 PIN
J33B
**NOTE NS6 - DEFAULT NO STUFF.
PLACE SITE WITHIN 0.5" OF SOCKET
PIN (W37). NO STUB BETWEEN CLK
TRACE AND CAPACITOR PAD
NS6
TBD
MREF
VCCCORE
VCC2.5
R294
51
5%
5,6,27 HRESET#
3 MREF
3 THERMDP
3 THERMDN
6,27 HLOCK#
6,27 DRDY#
6,27 RS#0
6,27 HIT#
6,27 RS#2
6,27 HA#[31:3]
6,27 HREQ#[4:0]
25,33 VID[3:0]
C188
2200pF
C189
33uF
L17
4.7uH
R300
1
R219
R221
R220
R222
VID3
VID0
VID2
VID1
CPUHCLK 5
BREQ0# 6,27
BNR# 6,27
BPRI# 6,27
HTRDY# 6,27
DEFER# 6,27
HITM# 6,27
DBSY# 6,27
RS#1 6,27
ADS# 6,27
100/66# 5,6
VRMPGD 25,26
JP1
JP2
JP3
JP4
SEL_VID0
SEL_VID1
SEL_VID2
SEL_VID3
R7
R10
R11
R12
10K
VCC
VRM optional override
jumpers & resistors
Jumper position 1-2 is
stuffed as the default. To
override, R219-222 must
be removed.
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370 PIN SOCKET(PART II)
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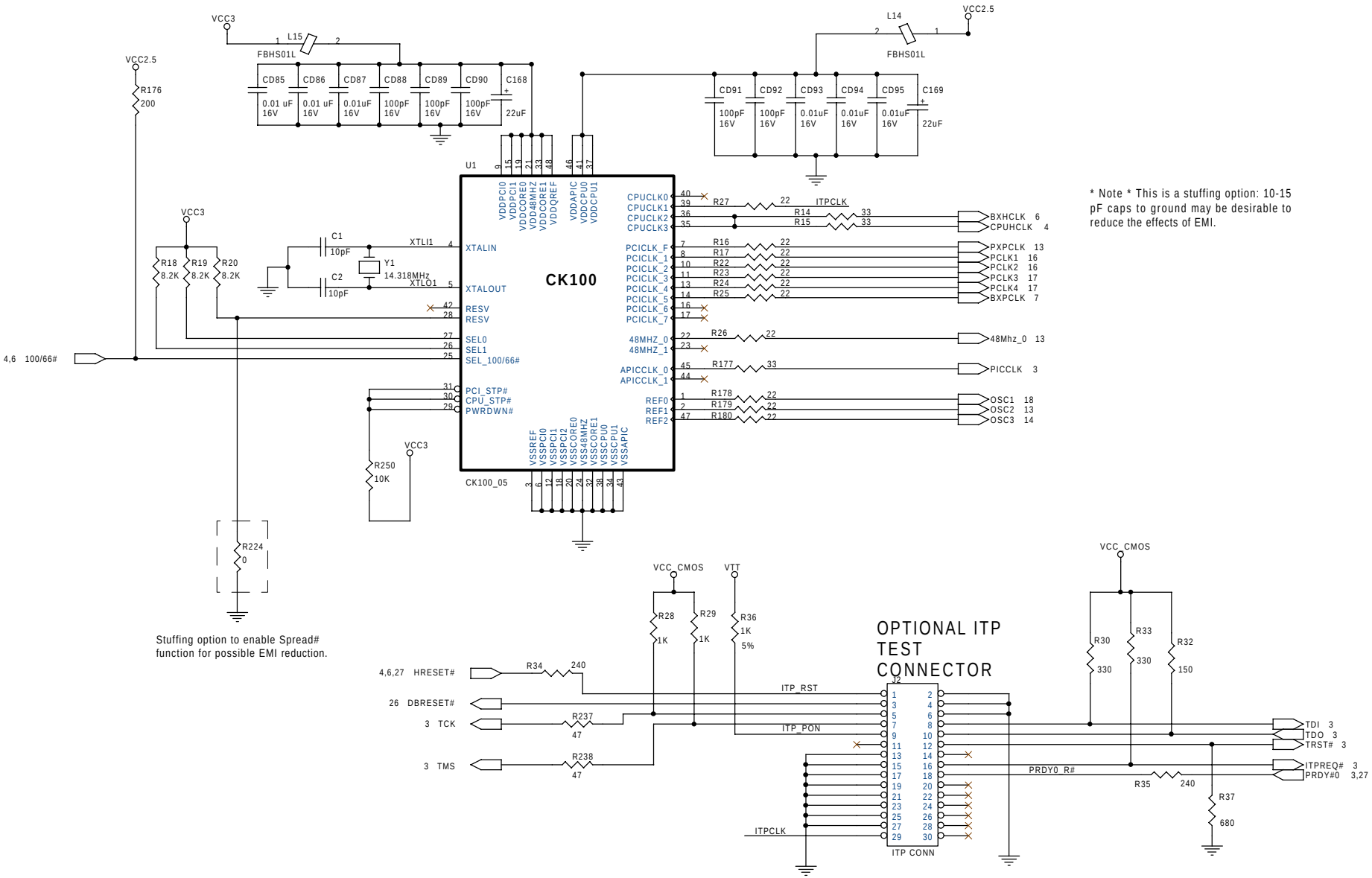
# CLOCK SYNTHESIZER

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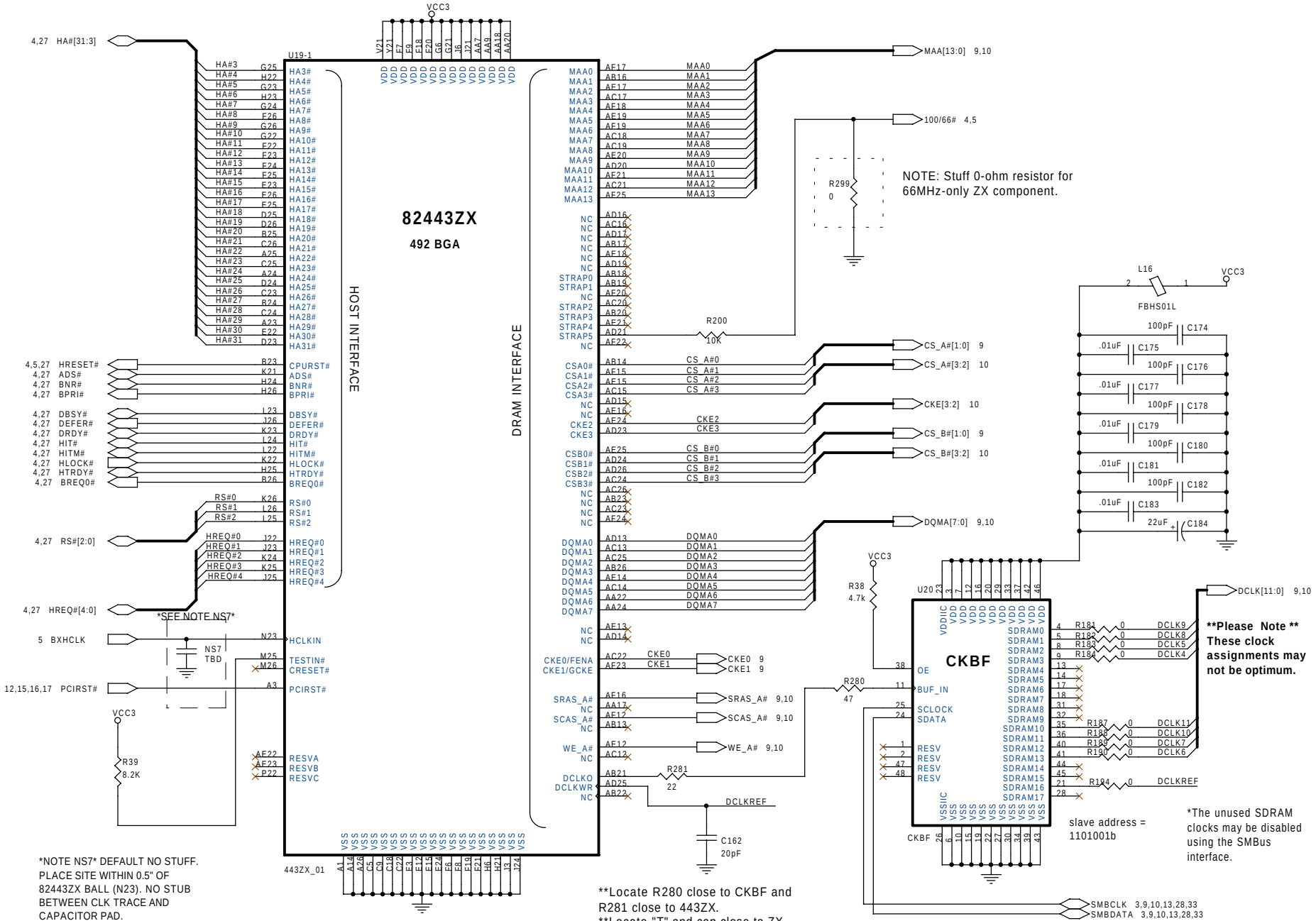


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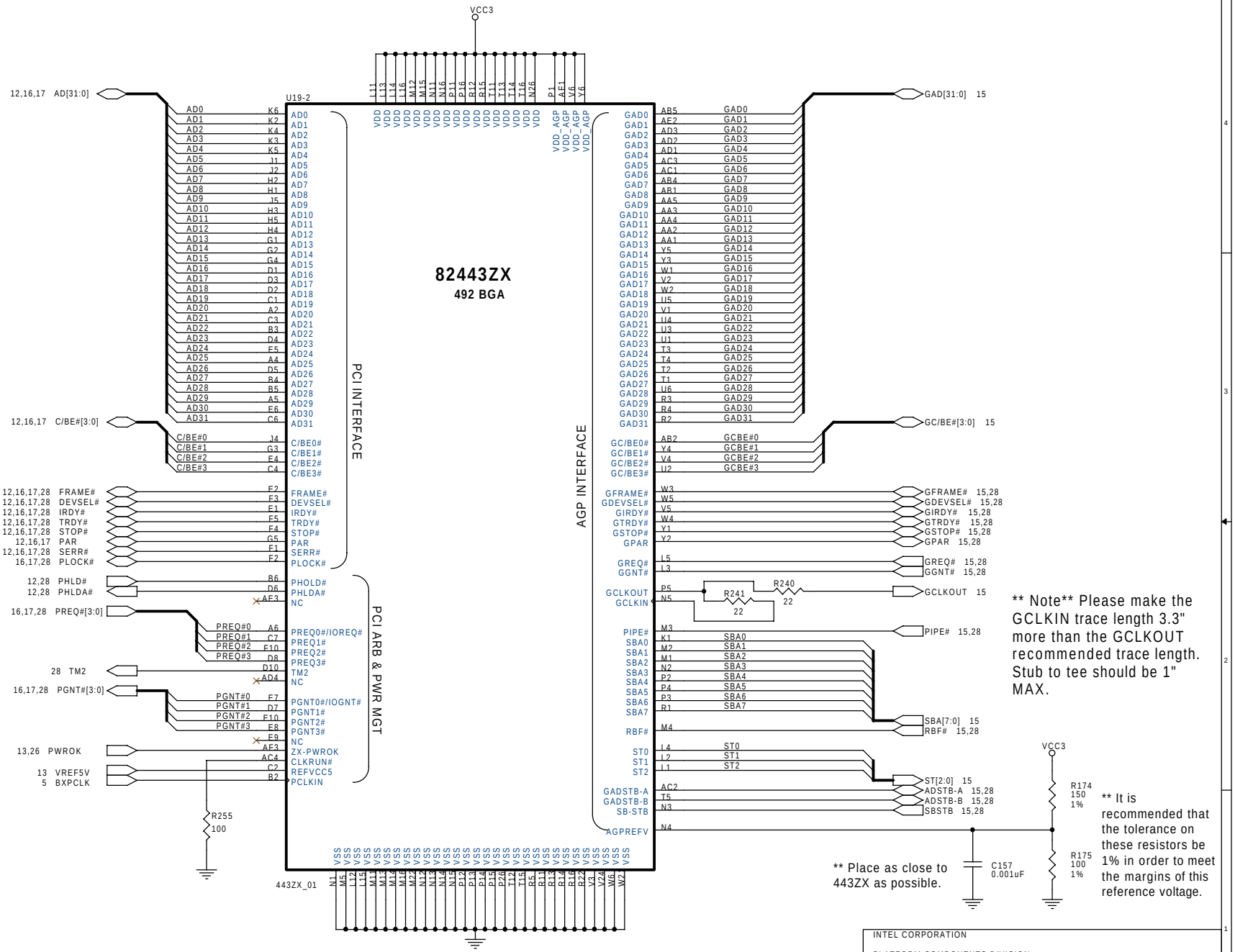


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| Title: 82443ZX PCI AND AGP INTERFACES | | |
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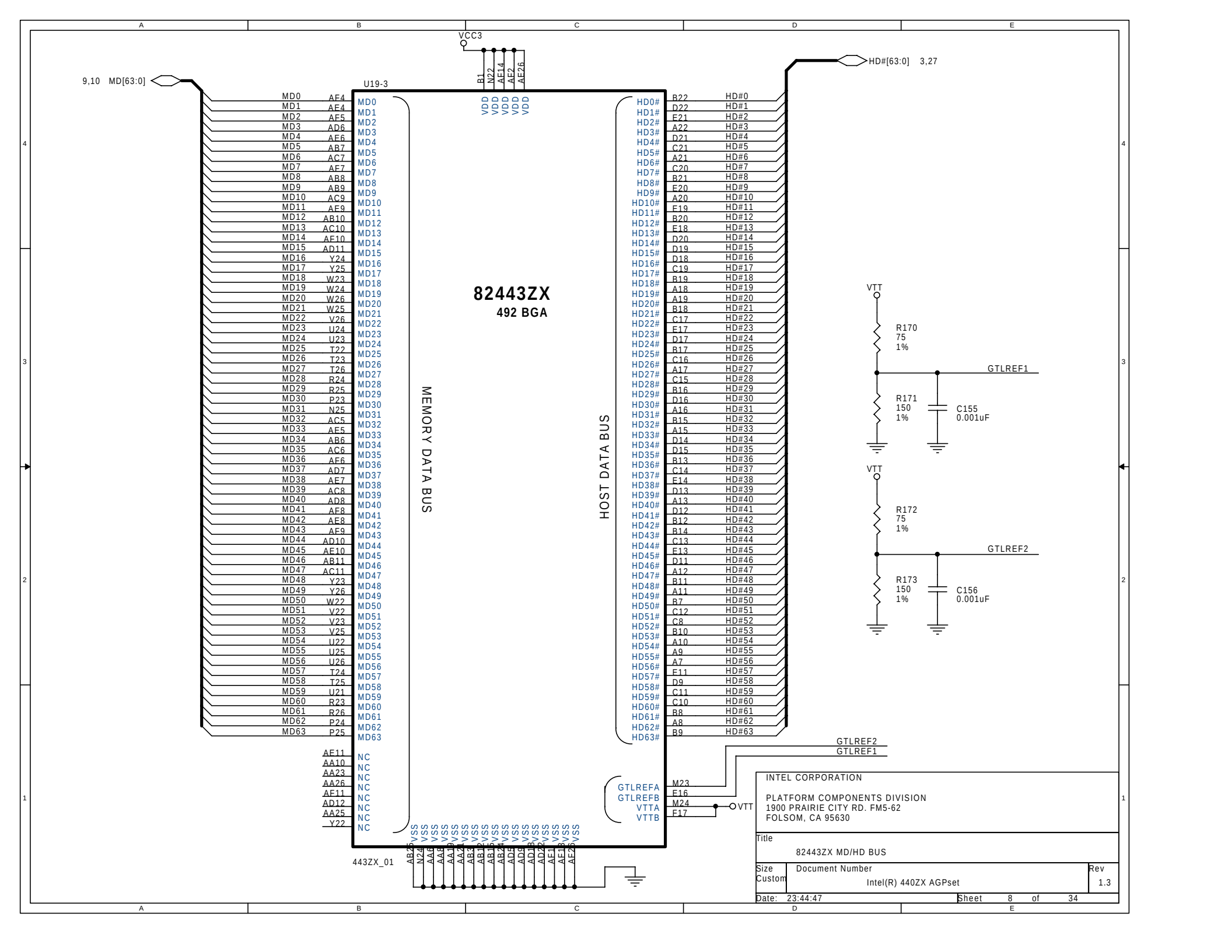
9,10 MD[63:0]
HD#[63:0] 3,27
VCC3
U19-3
82443ZX
492 BGA
MEMORY DATA BUS
HOST DATA BUS
443ZX_01
MD0 AF4
MD1 AE4
MD2 AF5
MD3 AD6
MD4 AE6
MD5 AB7
MD6 AC7
MD7 AF7
MD8 AB8
MD9 AB9
MD10 AC9
MD11 AE9
MD12 AB10
MD13 AC10
MD14 AF10
MD15 AD11
MD16 Y24
MD17 Y25
MD18 W23
MD19 W24
MD20 W26
MD21 W25
MD22 V26
MD23 U24
MD24 U23
MD25 T22
MD26 T23
MD27 T26
MD28 R24
MD29 R25
MD30 P23
MD31 N25
MD32 AC5
MD33 AE5
MD34 AB6
MD35 AC6
MD36 AF6
MD37 AD7
MD38 AE7
MD39 AC8
MD40 AD8
MD41 AF8
MD42 AE8
MD43 AF9
MD44 AD10
MD45 AE10
MD46 AB11
MD47 AC11
MD48 Y23
MD49 Y26
MD50 W22
MD51 V22
MD52 V23
MD53 V25
MD54 U22
MD55 U25
MD56 U26
MD57 T24
MD58 T25
MD59 U21
MD60 R23
MD61 R26
MD62 P24
MD63 P25
AE11 NC
AA10 NC
AA23 NC
AA26 NC
AE11 NC
AD12 NC
AA25 NC
Y22 NC
B1 N22 AE14 AE2 AE26 VDD
AB25 N24 AA6 AA8 AA10 AA12 AA14 AA16 AB13 AB15 AB17 AB19 AD5 AD7 AD9 AD11 AD22 AE1 AE18 AE25 VSS
HD0# B22 HD#0
HD1# D22 HD#1
HD2# E21 HD#2
HD3# A22 HD#3
HD4# D21 HD#4
HD5# C21 HD#5
HD6# A21 HD#6
HD7# C20 HD#7
HD8# B21 HD#8
HD9# E20 HD#9
HD10# A20 HD#10
HD11# E19 HD#11
HD12# B20 HD#12
HD13# E18 HD#13
HD14# D20 HD#14
HD15# D19 HD#15
HD16# D18 HD#16
HD17# C19 HD#17
HD18# B19 HD#18
HD19# A18 HD#19
HD20# A19 HD#20
HD21# B18 HD#21
HD22# C17 HD#22
HD23# E17 HD#23
HD24# D17 HD#24
HD25# B17 HD#25
HD26# C16 HD#26
HD27# A17 HD#27
HD28# C15 HD#28
HD29# B16 HD#29
HD30# D16 HD#30
HD31# A16 HD#31
HD32# B15 HD#32
HD33# A15 HD#33
HD34# D14 HD#34
HD35# D15 HD#35
HD36# B13 HD#36
HD37# C14 HD#37
HD38# E14 HD#38
HD39# D13 HD#39
HD40# A13 HD#40
HD41# D12 HD#41
HD42# B12 HD#42
HD43# B14 HD#43
HD44# C13 HD#44
HD45# E13 HD#45
HD46# D11 HD#46
HD47# A12 HD#47
HD48# B11 HD#48
HD49# A11 HD#49
HD50# B7 HD#50
HD51# C12 HD#51
HD52# C8 HD#52
HD53# B10 HD#53
HD54# A10 HD#54
HD55# A9 HD#55
HD56# A7 HD#56
HD57# E11 HD#57
HD58# D9 HD#58
HD59# C11 HD#59
HD60# C10 HD#60
HD61# B8 HD#61
HD62# A8 HD#62
HD63# B9 HD#63
GTLREFA M23
GTLREFB E16
VTTA M24
VTTB F17
VTT
GTLREF2
GTLREF1
VTT
R170 75 1%
GTLREF1
R171 150 1%
C155 0.001uF
VTT
R172 75 1%
GTLREF2
R173 150 1%
C156 0.001uF
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82443ZX MD/HD BUS
Size Custom
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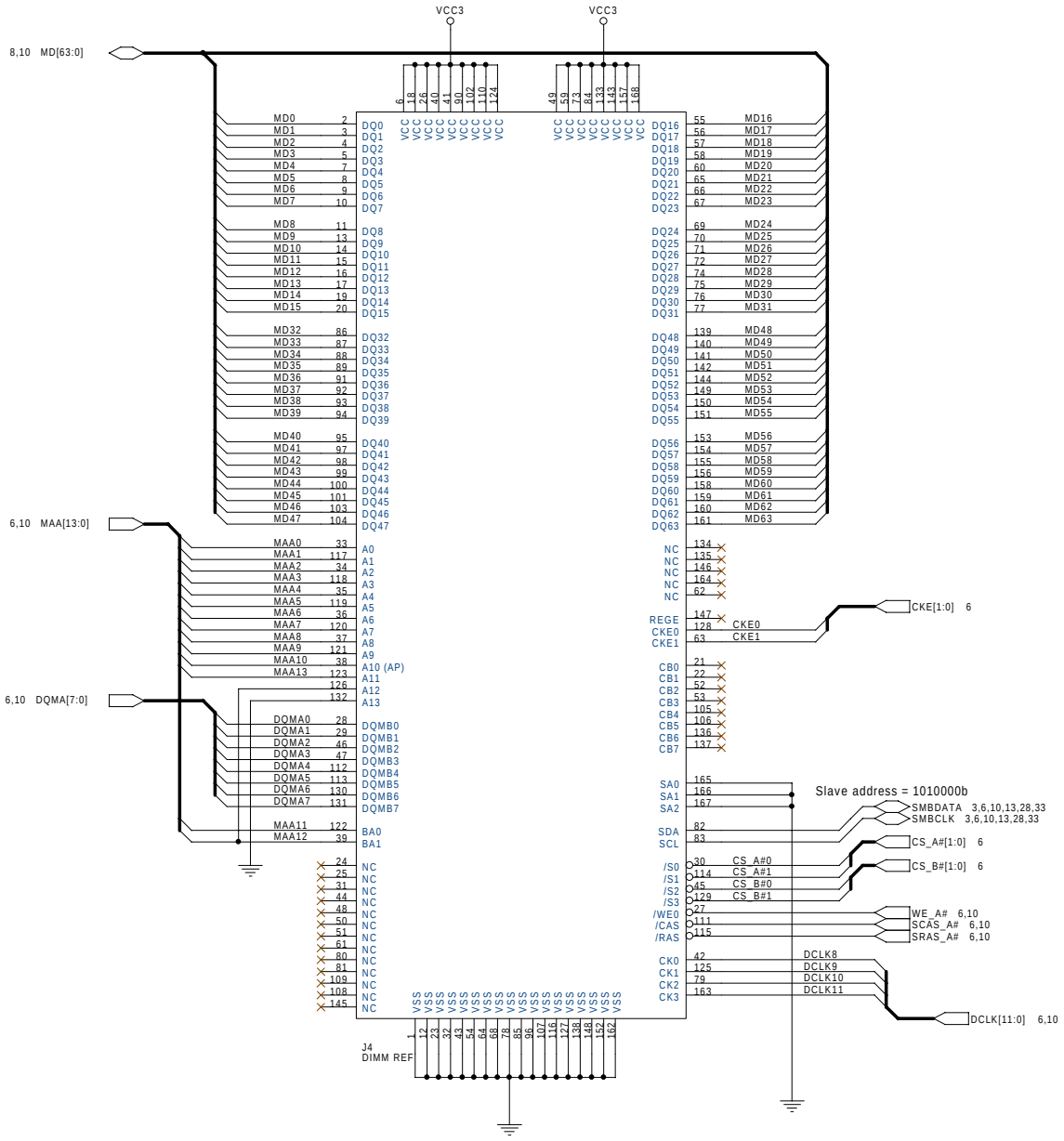
# DIMM SOCKET 0

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| Title: DIMM SOCKET 0 | |
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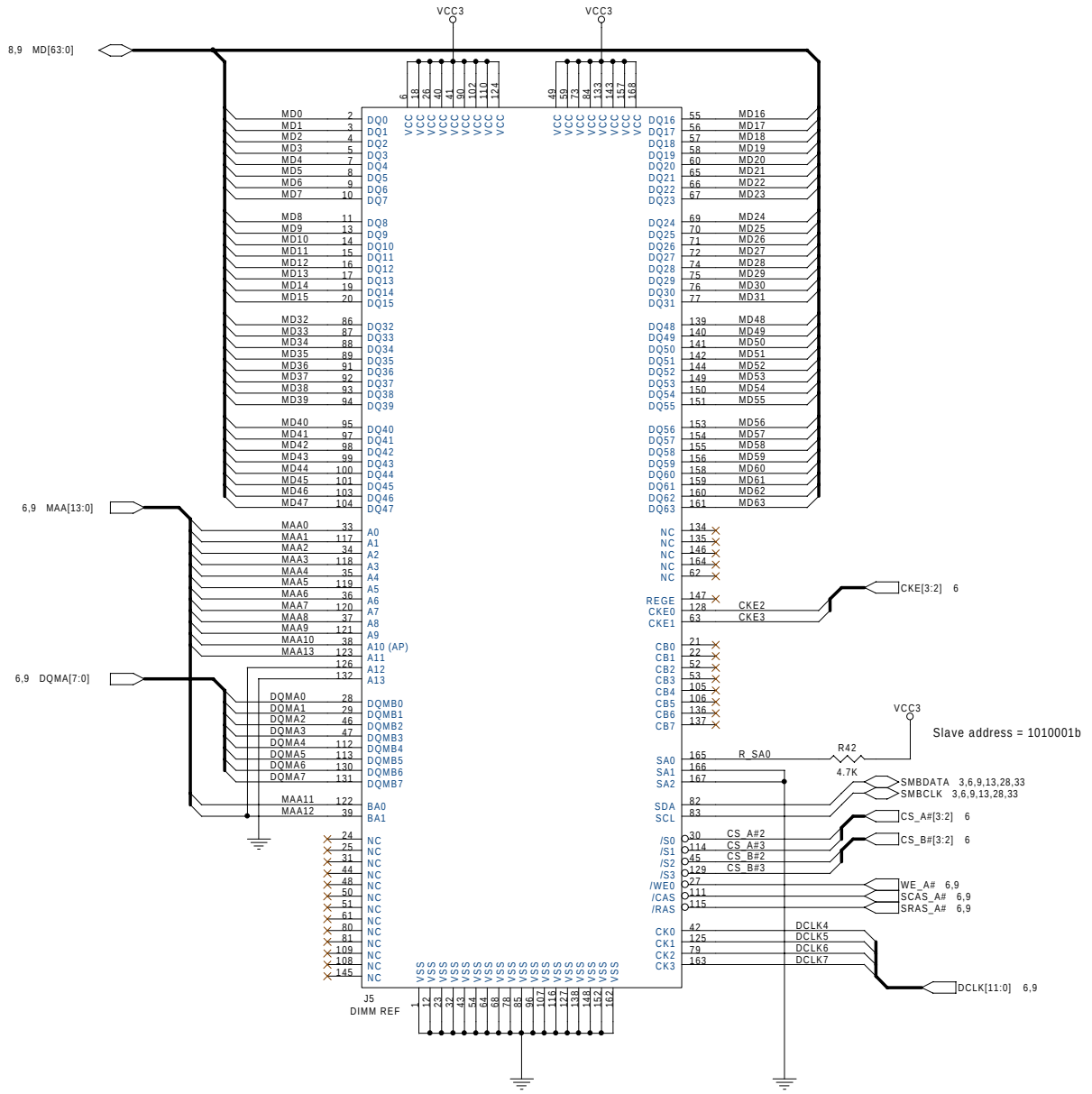
# DIMM SOCKET 1

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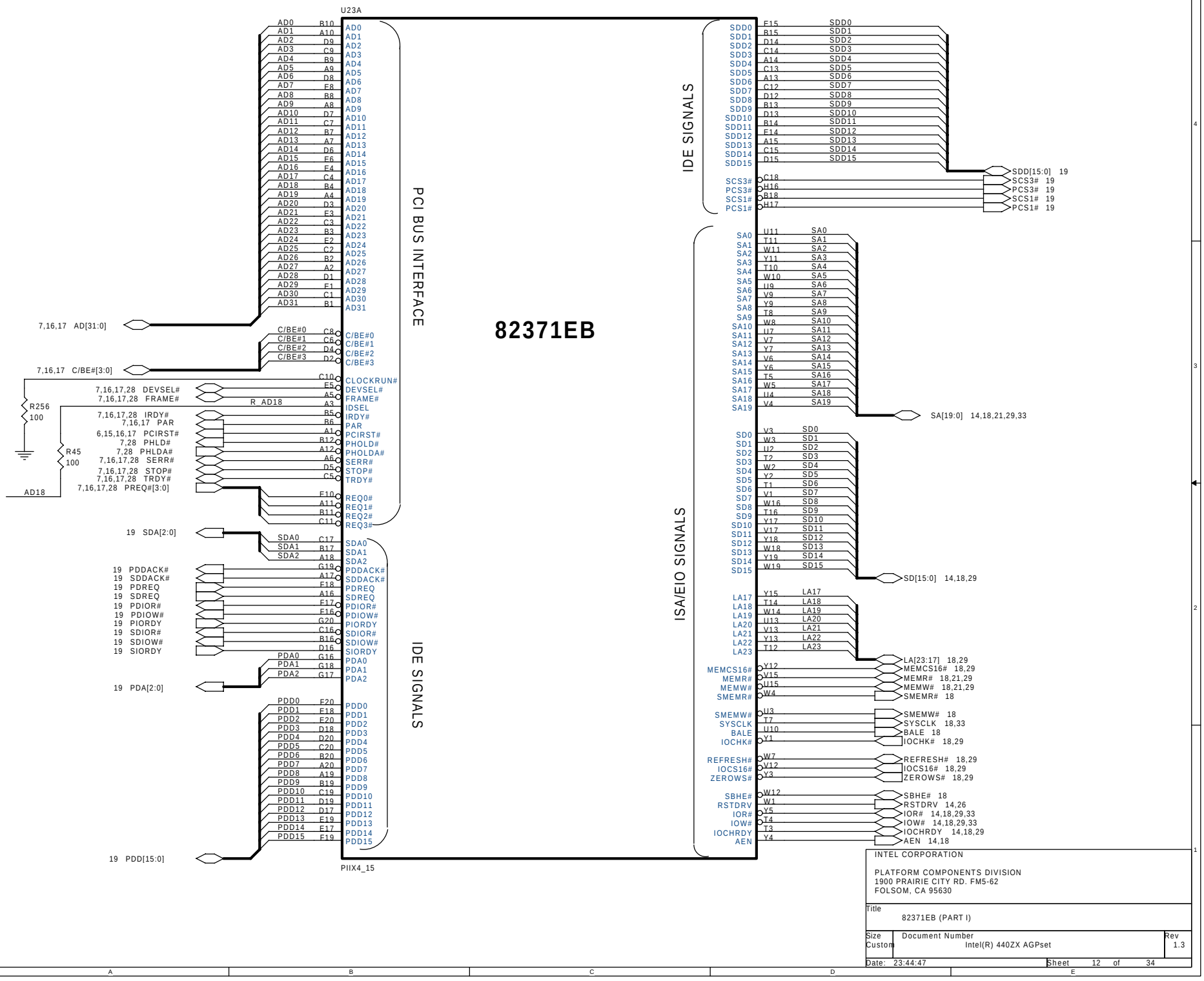
U23A
82371EB
PCI BUS INTERFACE
IDE SIGNALS
ISA/EIO SIGNALS
PIIX4_15
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
7,16,17 AD[31:0]
C/BE#0 C/BE#1 C/BE#2 C/BE#3
7,16,17 C/BE#[3:0]
CLOCKRUN# DEVSEL# FRAME# IDSEL IRDY# PAR PCIRST# PHOLD# PHOLDA# SERR# STOP# TRDY# REQ0# REQ1# REQ2# REQ3#
7,16,17,28 DEVSEL#
7,16,17,28 FRAME#
R_AD18
7,16,17,28 IRDY#
7,16,17 PAR
6,15,16,17 PCIRST#
7,28 PHLD#
7,28 PHLDA#
7,16,17,28 SERR#
7,16,17,28 STOP#
7,16,17,28 TRDY#
7,16,17,28 PREQ#[3:0]
R256 100
R45 100
AD18
19 SDA[2:0]
SDA0 SDA1 SDA2
19 PDDACK#
19 SDDACK#
19 PDREQ
19 SDREQ
19 PDIOR#
19 PDIOW#
19 PIORDY
19 SDIOR#
19 SDIOW#
19 SIORDY
PDA0 PDA1 PDA2
19 PDA[2:0]
PDD0 PDD1 PDD2 PDD3 PDD4 PDD5 PDD6 PDD7 PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15
19 PDD[15:0]
SDD0 SDD1 SDD2 SDD3 SDD4 SDD5 SDD6 SDD7 SDD8 SDD9 SDD10 SDD11 SDD12 SDD13 SDD14 SDD15
SDD[15:0] 19
SCS3# PCS3# SCS1# PCS1#
SCS3# 19
PCS3# 19
SCS1# 19
PCS1# 19
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SA18 SA19
SA[19:0] 14,18,21,29,33
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15
SD[15:0] 14,18,29
LA17 LA18 LA19 LA20 LA21 LA22 LA23
LA[23:17] 18,29
MEMCS16#
MEMR#
MEMW#
SMEMR#
MEMCS16# 18,29
MEMR# 18,21,29
MEMW# 18,21,29
SMEMR# 18
SMEMW#
SYSCLK
BALE
IOCHK#
SMEMW# 18
SYSCLK 18,33
BALE 18
IOCHK# 18,29
REFRESH#
IOCS16#
ZEROWS#
REFRESH# 18,29
IOCS16# 18,29
ZEROWS# 18,29
SBHE#
RSTDRV
IOR#
IOW#
IOCHRDY
AEN
SBHE# 18
RSTDRV 14,26
IOR# 14,18,29,33
IOW# 14,18,29,33
IOCHRDY 14,18,29
AEN 14,18
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Title
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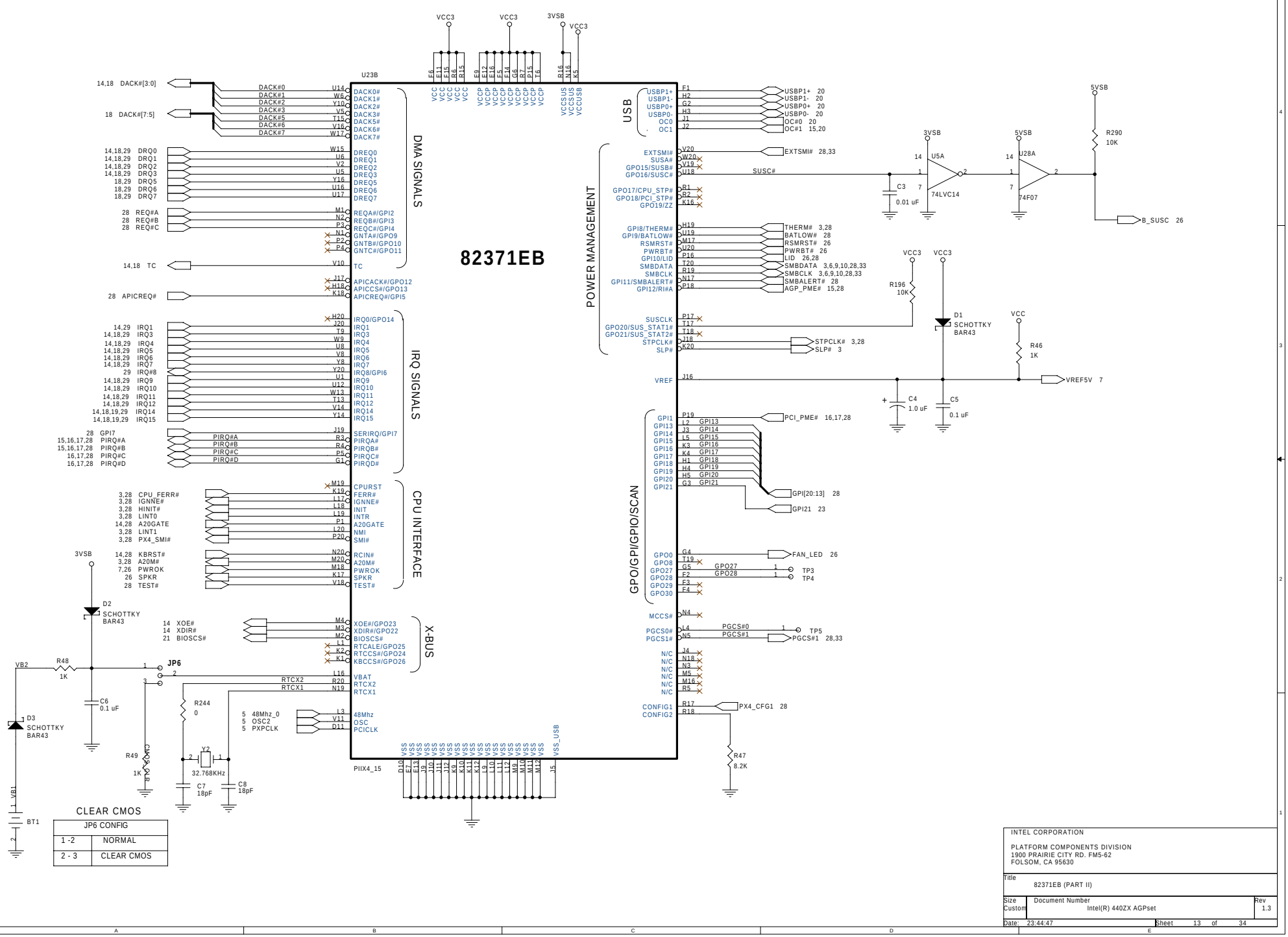
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U23B
DMA SIGNALS
IRQ SIGNALS
CPU INTERFACE
X-BUS
USB
POWER MANAGEMENT
GPO/GPI/GPIO/SCAN
PIIX4_15
DACK#0
DACK#1
DACK#2
DACK#3
DACK#5
DACK#6
DACK#7
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
REQA#/GPI2
REQB#/GPI3
REQC#/GPI4
GNTA#/GPO9
GNTB#/GPO10
GNTC#/GPO11
TC
APICACK#/GPO12
APICCS#/GPO13
APICREQ#/GPI5
IRQ0/GPO14
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8/GPI6
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
SERIRQ/GPI7
PIRQA#
PIRQB#
PIRQC#
PIRQD#
CPURST
FERR#
IGNNE#
INIT
INTR
A20GATE
NMI
SMI#
RCIN#
A20M#
PWROK
SPKR
TEST#
XOE#/GPO23
XDIR#/GPO22
BIOSCS#
RTCALE/GPO25
RTCCS#/GPO24
KBCCS#/GPO26
VBAT
RTCX2
RTCX1
48Mhz
OSC
PCICLK
USBP1+
USBP1-
USBP0+
USBP0-
OC0
OC1
EXTSMI#
SUSA#
GPO15/SUSB#
GPO16/SUSC#
GPO17/CPU_STP#
GPO18/PCI_STP#
GPO19/ZZ
GPI8/THERM#
GPI9/BATLOW#
RSMRST#
PWRBT#
GPI10/LID
SMBDATA
SMBCLK
GPI11/SMBALERT#
GPI12/RI#A
SUSCLK
GPO20/SUS_STAT1#
GPO21/SUS_STAT2#
STPCLK#
SLP#
VREF
GPI1
GPI13
GPI14
GPI15
GPI16
GPI17
GPI18
GPI19
GPI20
GPI21
GPO0
GPO8
GPO27
GPO28
GPO29
GPO30
MCCS#
PGCS0#
PGCS1#
N/C
CONFIG1
CONFIG2
VCC3
3VSB
5VSB
VSS
VSS_USB
14,18 DACK#[3:0]
18 DACK#[7:5]
14,18,29 DRQ0
14,18,29 DRQ1
14,18,29 DRQ2
14,18,29 DRQ3
18,29 DRQ5
18,29 DRQ6
18,29 DRQ7
28 REQ#A
28 REQ#B
28 REQ#C
14,18 TC
28 APICREQ#
14,29 IRQ1
14,18,29 IRQ3
14,18,29 IRQ4
14,18,29 IRQ5
14,18,29 IRQ6
14,18,29 IRQ7
29 IRQ#8
14,18,29 IRQ9
14,18,29 IRQ10
14,18,29 IRQ11
14,18,29 IRQ12
14,18,19,29 IRQ14
14,18,19,29 IRQ15
28 GPI7
15,16,17,28 PIRQ#A
15,16,17,28 PIRQ#B
16,17,28 PIRQ#C
16,17,28 PIRQ#D
3,28 CPU_FERR#
3,28 IGNNE#
3,28 HINIT#
3,28 LINT0
14,28 A20GATE
3,28 LINT1
3,28 PX4_SMI#
14,28 KBRST#
3,28 A20M#
7,26 PWROK
26 SPKR
28 TEST#
14 XOE#
14 XDIR#
21 BIOSCS#
5 48Mhz_0
5 OSC2
5 PXPCLK
USBP1+ 20
USBP1- 20
USBP0+ 20
USBP0- 20
OC#0 20
OC#1 15,20
EXTSMI# 28,33
SUSC#
THERM# 3,28
BATLOW# 28
RSMRST# 26
PWRBT# 26
LID 26,28
SMBDATA 3,6,9,10,28,33
SMBCLK 3,6,9,10,28,33
SMBALERT# 28
AGP_PME# 15,28
STPCLK# 3,28
SLP# 3
PCI_PME# 16,17,28
GPI[20:13] 28
GPI21 23
FAN_LED 26
GPO27
GPO28
TP3
TP4
PGCS#0
PGCS#1
PGCS#1 28,33
TP5
PX4_CFG1 28
B_SUSC 26
VREF5V 7
U5A
74LVC14
U28A
74F07
R290 10K
R196 10K
R46 1K
R47 8.2K
C3 0.01 uF
C4 1.0 uF
C5 0.1 uF
C6 0.1 uF
C7 18pF
C8 18pF
R244 0
R48 1K
R49 1K
Y2 32.768KHz
D1 SCHOTTKY BAR43
D2 SCHOTTKY BAR43
D3 SCHOTTKY BAR43
JP6
BT1
VB1
VB2
CLEAR CMOS
JP6 CONFIG
1 -2 NORMAL
2 - 3 CLEAR CMOS
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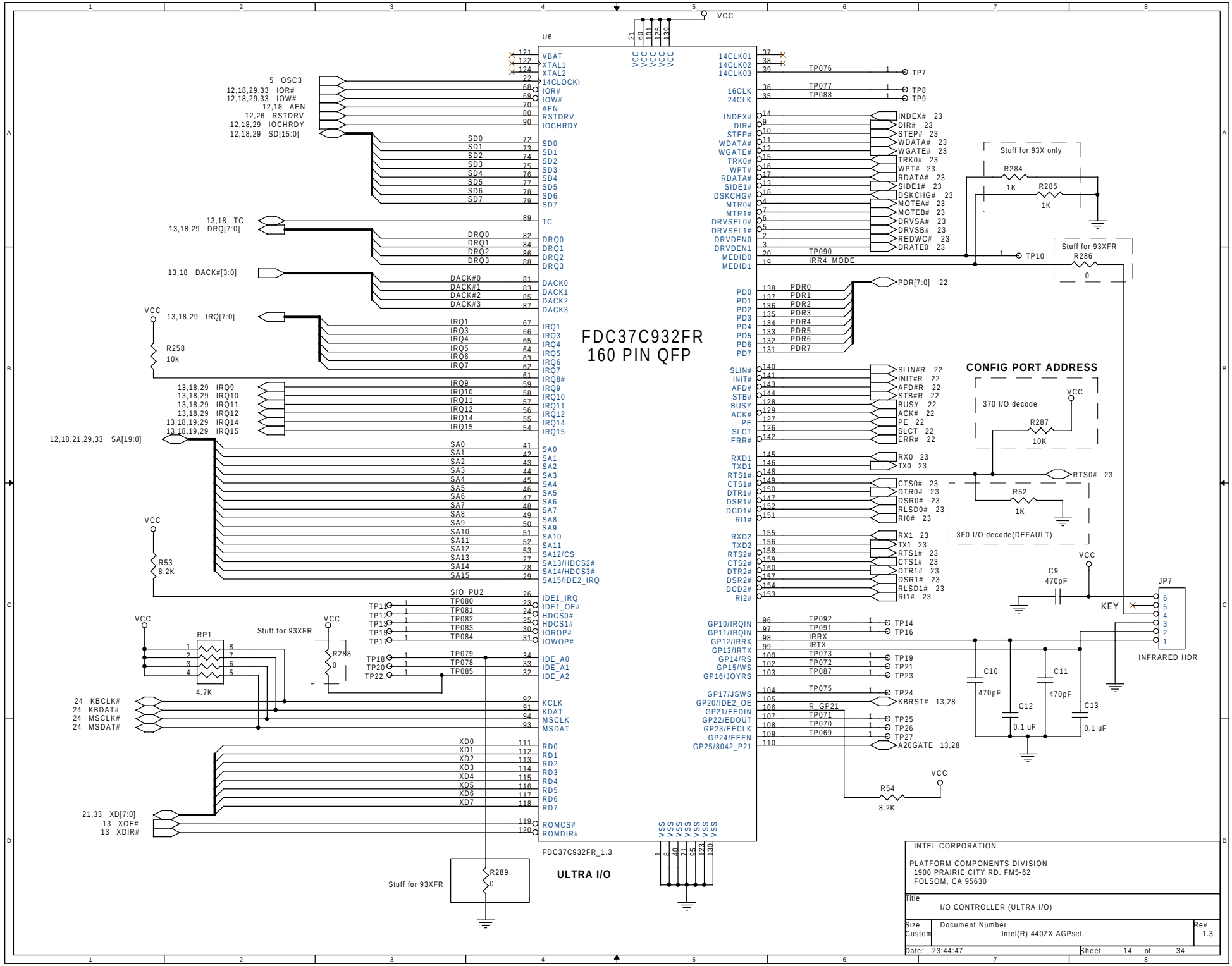
U6
FDC37C932FR
160 PIN QFP
FDC37C932FR_1.3
ULTRA I/O
VCC
5 OSC3
12,18,29,33 IOR#
12,18,29,33 IOW#
12,18 AEN
12,26 RSTDRV
12,18,29 IOCHRDY
12,18,29 SD[15:0]
13,18 TC
13,18,29 DRQ[7:0]
13,18 DACK#[3:0]
13,18,29 IRQ[7:0]
13,18,29 IRQ9
13,18,29 IRQ10
13,18,29 IRQ11
13,18,29 IRQ12
13,18,19,29 IRQ14
13,18,19,29 IRQ15
12,18,21,29,33 SA[19:0]
R258
10k
R53
8.2K
RP1
4.7K
Stuff for 93XFR
R288
0
24 KBCLK#
24 KBDAT#
24 MSCLK#
24 MSDAT#
21,33 XD[7:0]
13 XOE#
13 XDIR#
R289
0
TP076
TP077
TP088
TP090
TP092
TP091
TP073
TP072
TP087
TP075
TP071
TP070
TP069
TP080
TP081
TP082
TP083
TP084
TP079
TP078
TP085
INDEX# 23
DIR# 23
STEP# 23
WDATA# 23
WGATE# 23
TRK0# 23
WPT# 23
RDATA# 23
SIDE1# 23
DSKCHG# 23
MOTEA# 23
MOTEB# 23
DRVSA# 23
DRVSB# 23
REDWC# 23
DRATE0 23
IRR4_MODE
PDR[7:0] 22
SLIN#R 22
INIT#R 22
AFD#R 22
STB#R 22
BUSY 22
ACK# 22
PE 22
SLCT 22
ERR# 22
RX0 23
TX0 23
RTS0# 23
CTS0# 23
DTR0# 23
DSR0# 23
RLSD0# 23
RI0# 23
RX1 23
TX1 23
RTS1# 23
CTS1# 23
DTR1# 23
DSR1# 23
RLSD1# 23
RI1# 23
KBRST# 13,28
A20GATE 13,28
R_GP21
R54
8.2K
Stuff for 93X only
R284
1K
R285
1K
Stuff for 93XFR
R286
0
CONFIG PORT ADDRESS
370 I/O decode
R287
10K
R52
1K
3F0 I/O decode(DEFAULT)
C9
470pF
KEY
JP7
INFRARED HDR
C10
470pF
C11
470pF
C12
0.1 uF
C13
0.1 uF
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FOLSOM, CA 95630
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Size
Custom
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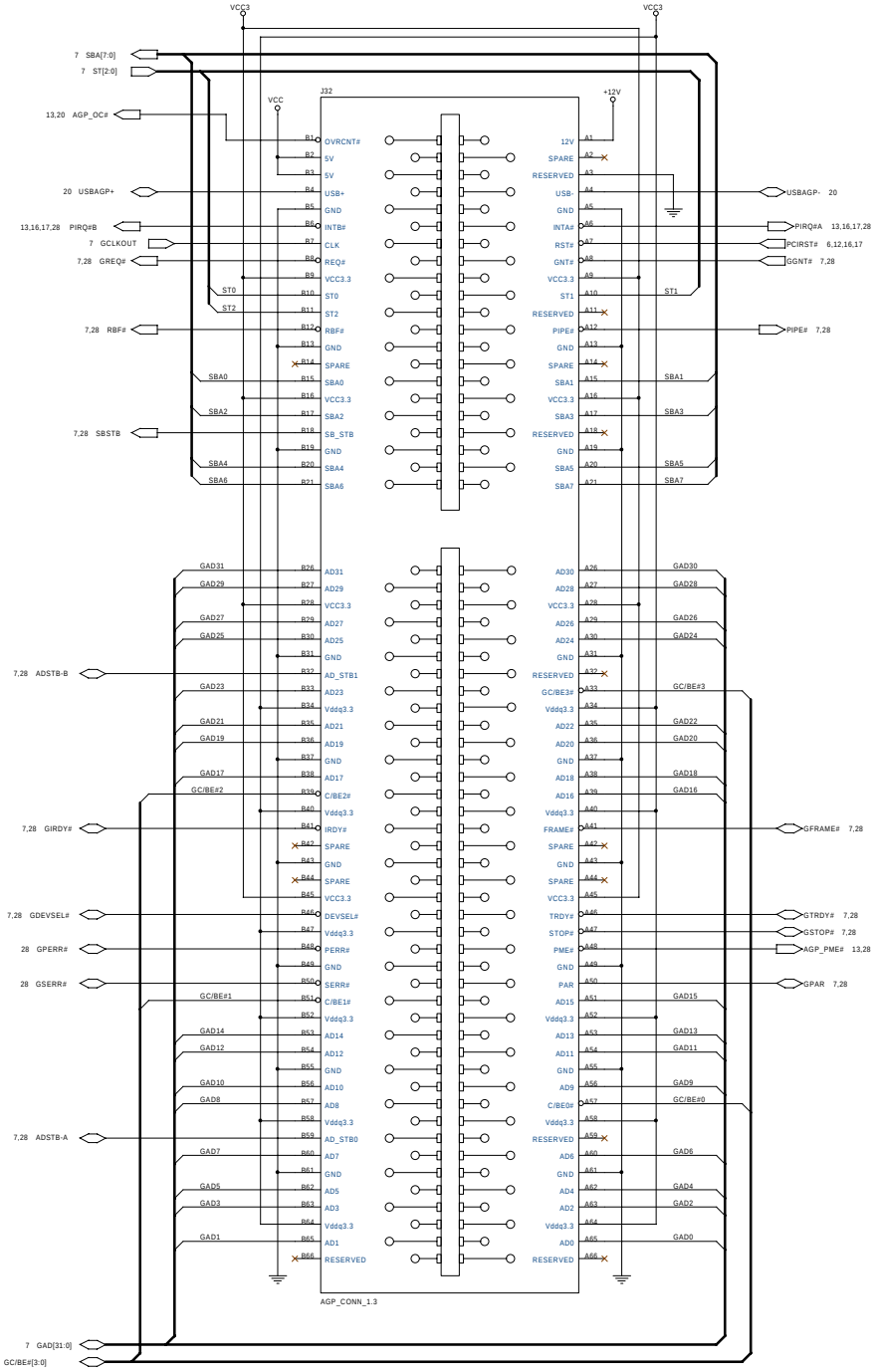
# AGP CONNECTOR





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Title: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR

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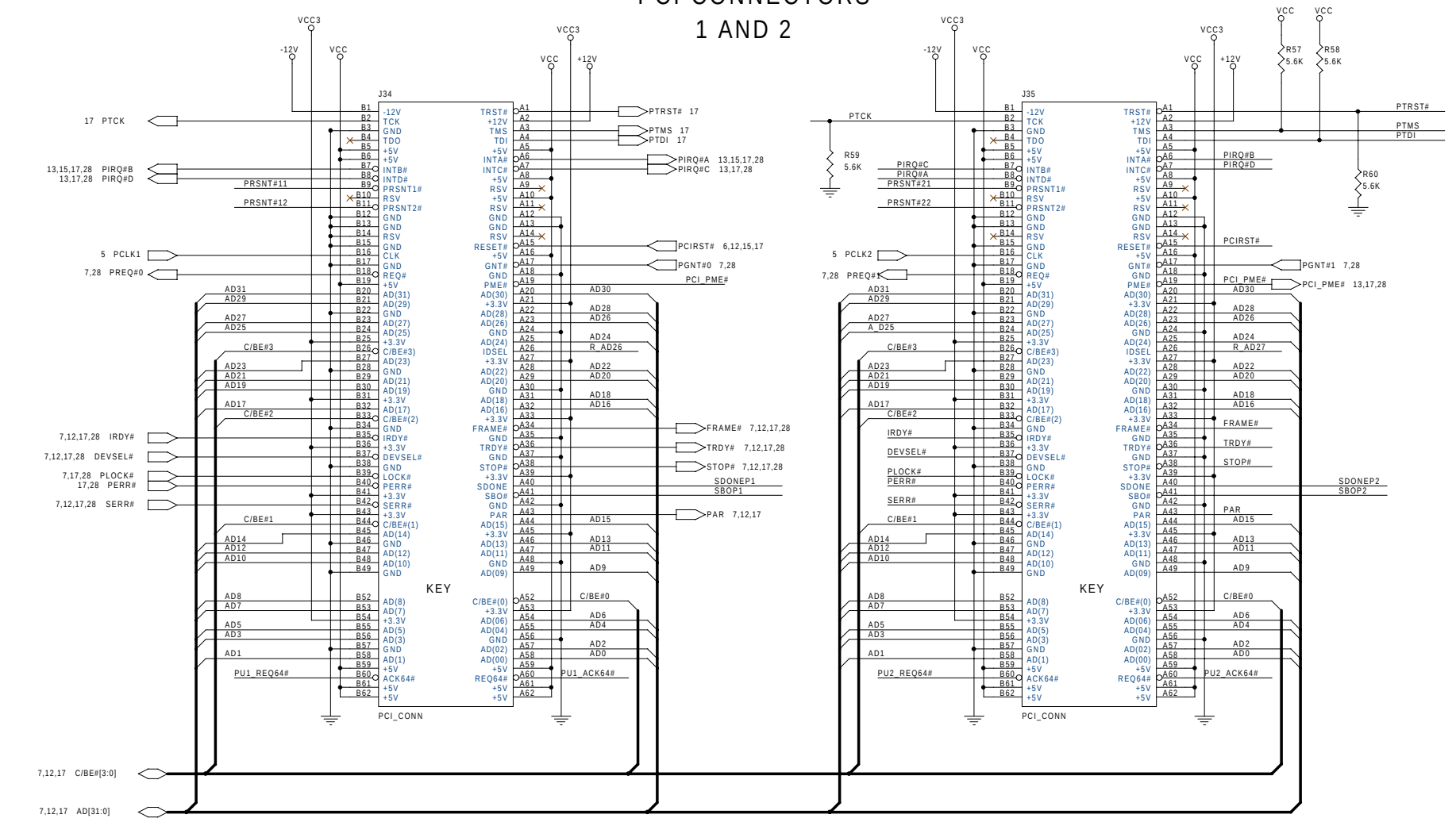
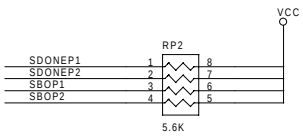
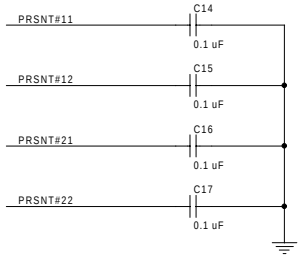
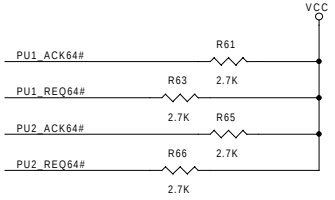
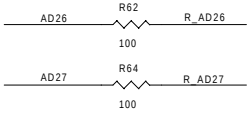
# PCI CONNECTORS 1 AND 2




| | |
|---|---|
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| Title: PCI CONNECTORS 1 & 2 | |
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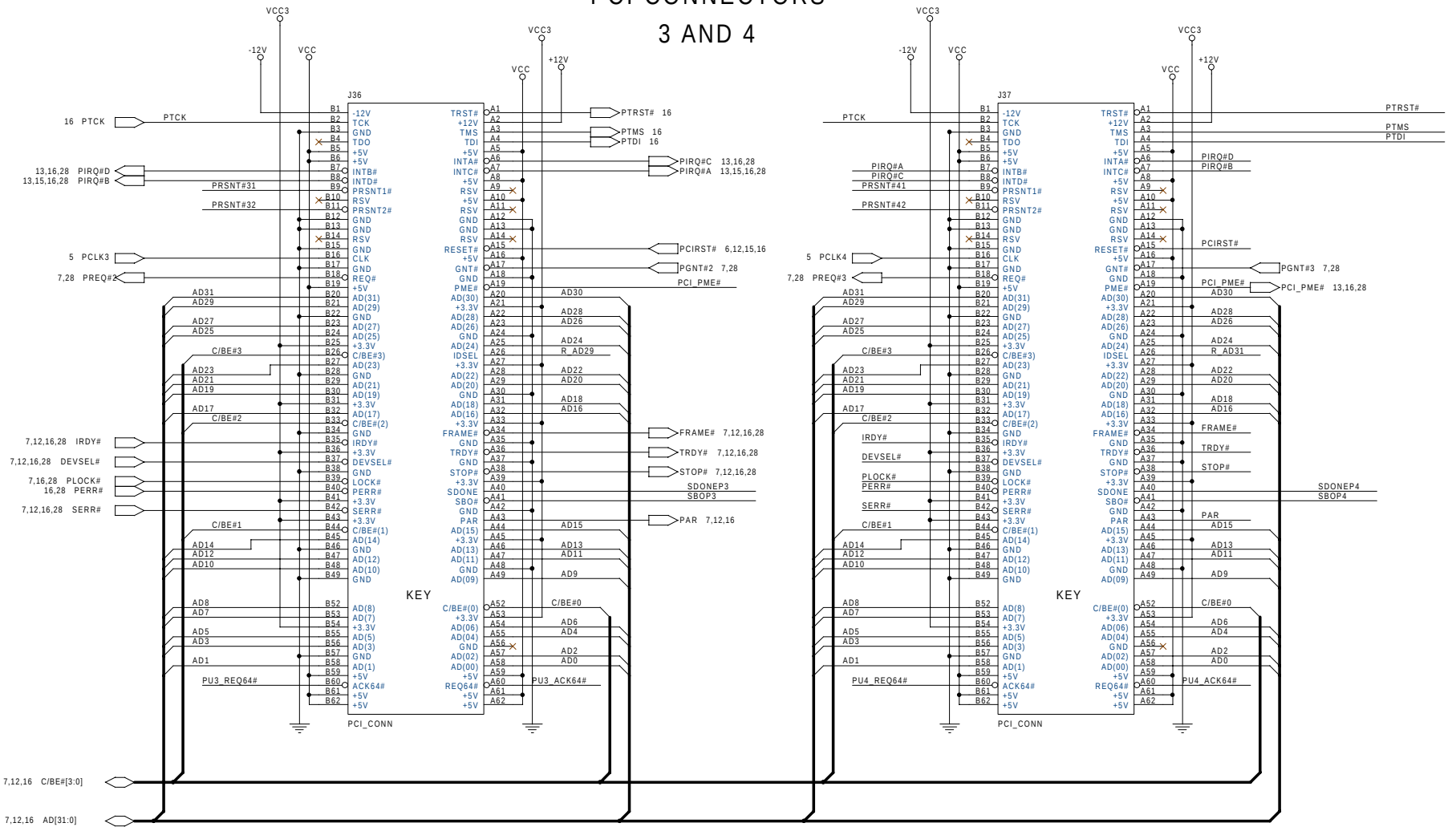
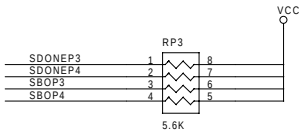
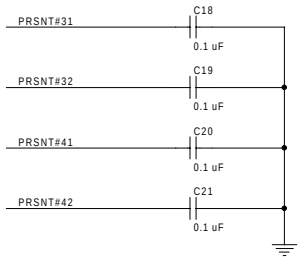
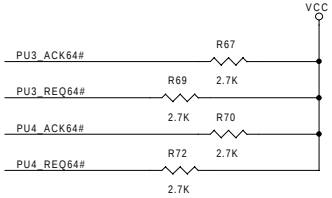
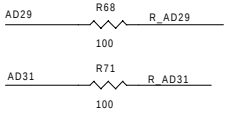
# PCI CONNECTORS
# 3 AND 4

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| Title: PCI CONNECTORS 3 & 4 | | |
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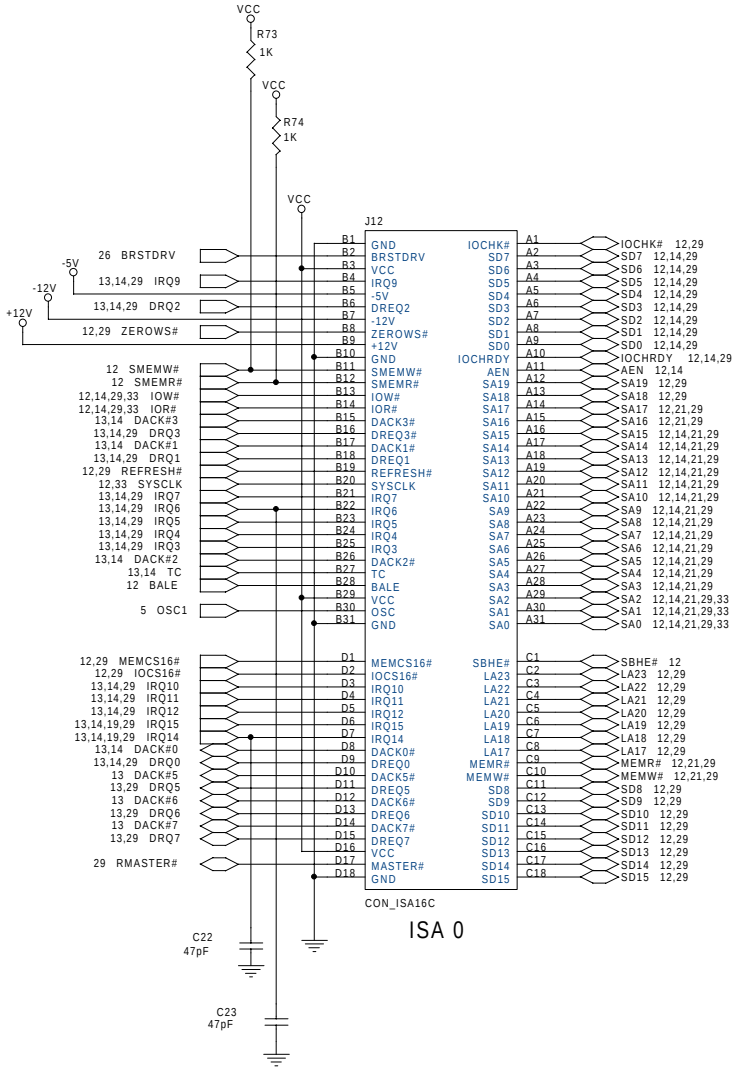
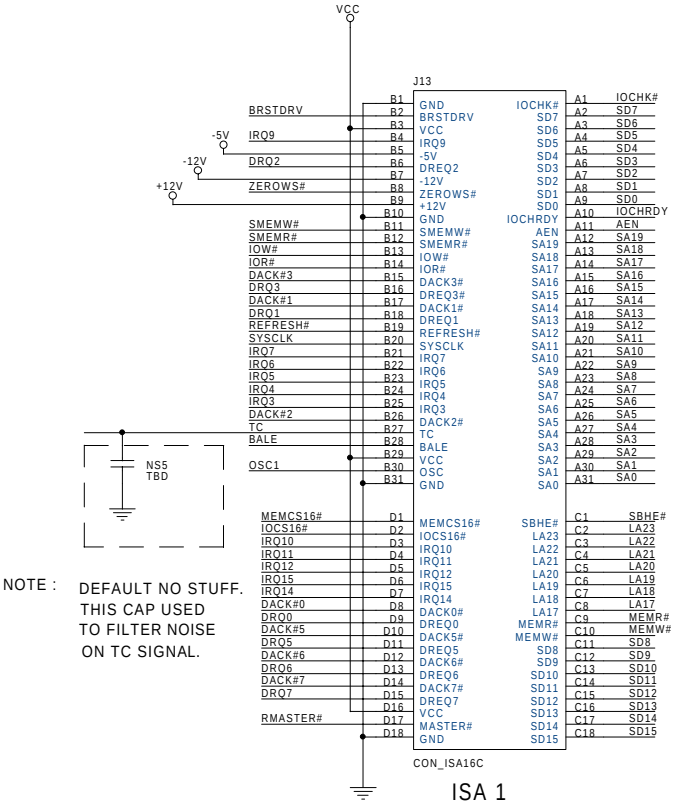
# ISA SLOTS




ISA 0




ISA 1

NOTE : DEFAULT NO STUFF. THIS CAP USED TO FILTER NOISE ON TC SIGNAL.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| | | |
|---|---|---|
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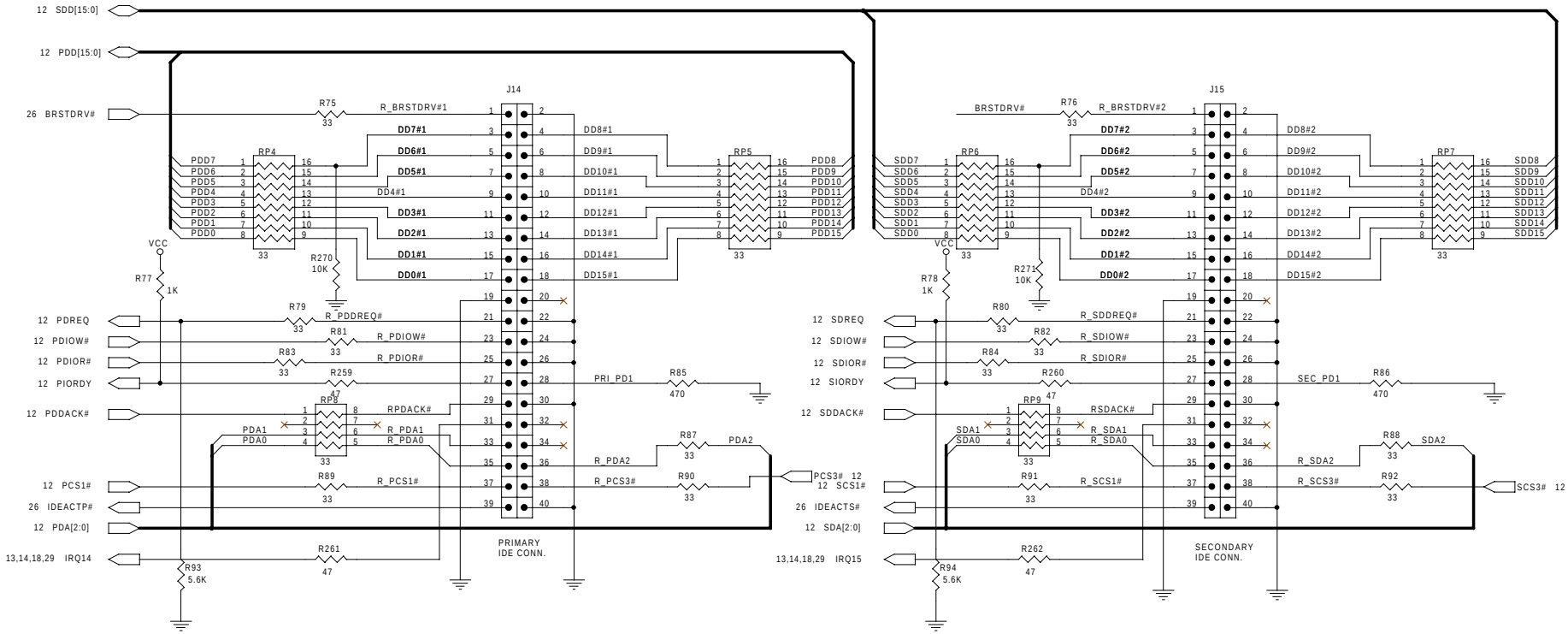
# IDE CONNECTORS

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| Title: PCI IDE CONNECTORS | | |
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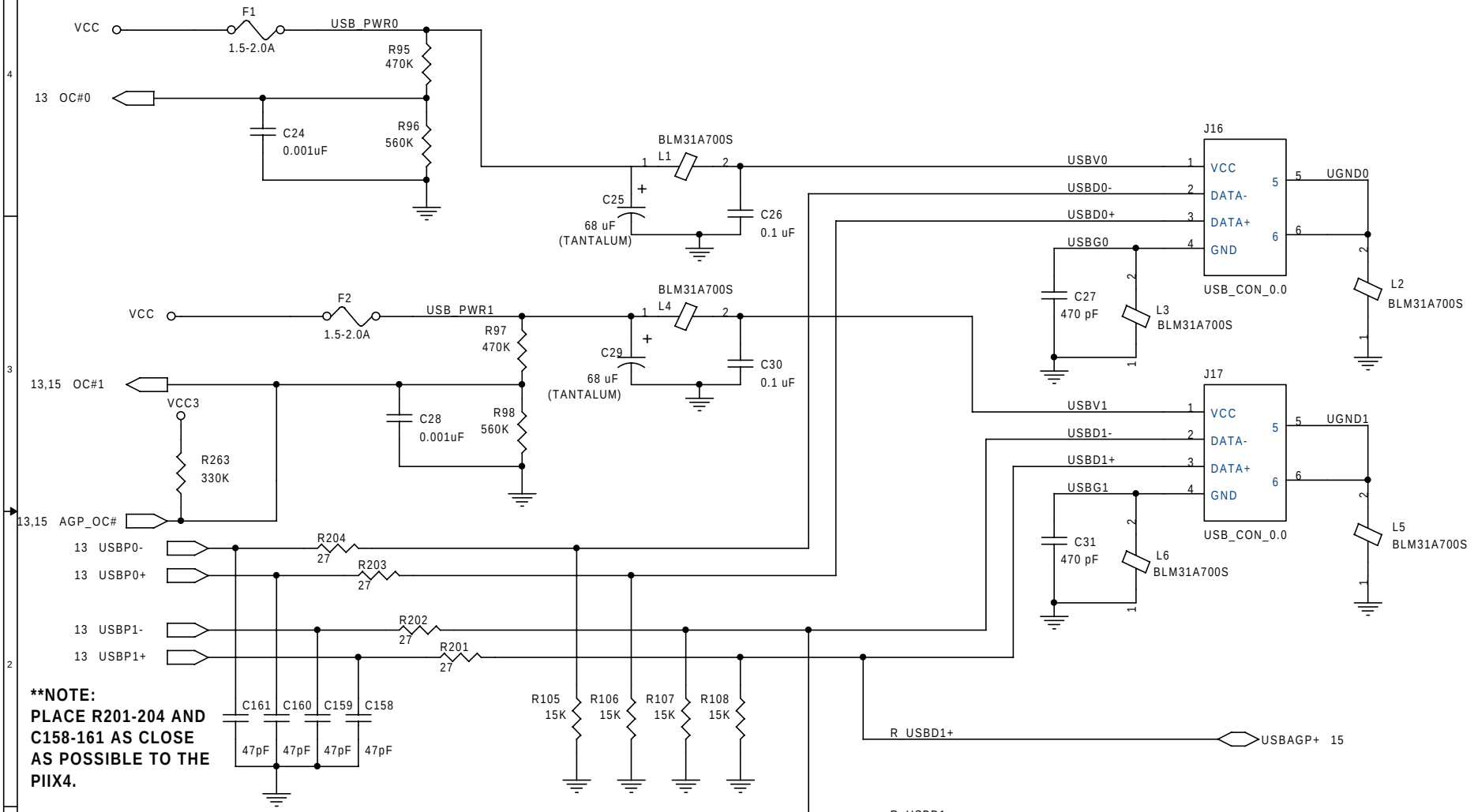
# USB CONNECTORS




****NOTE:**
**PLACE R201-204 AND C158-161 AS CLOSE AS POSSIBLE TO THE PIIX4.**

NOTE:
USE PIIX4 APPLICATION NOTE FOR LAYOUT GUIDELINES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| | | |
|---|---|---|
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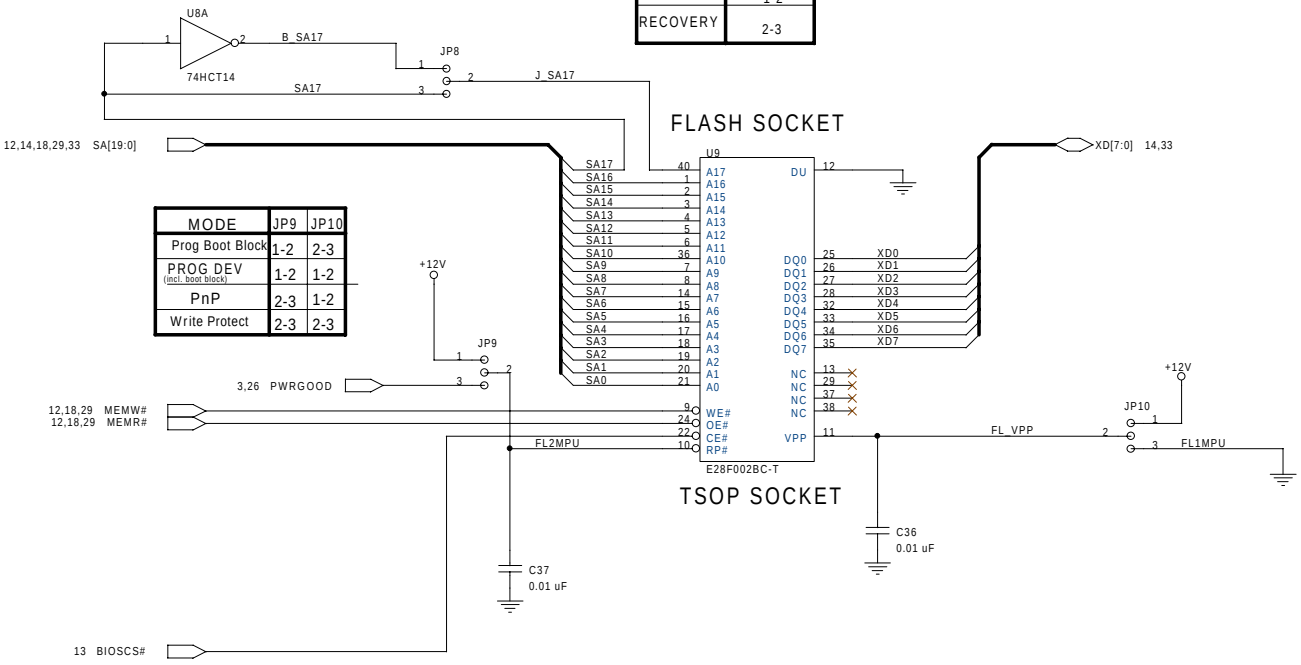
# SYSTEM ROM

| MODE | JP8 |
|---|---|
| NORMAL | 1-2 |
| RECOVERY | 2-3 |




| MODE | JP9 | JP10 |
|---|---|---|
| Prog Boot Block | 1-2 | 2-3 |
| PROG DEV (incl. boot block) | 1-2 | 1-2 |
| PnP | 2-3 | 1-2 |
| Write Protect | 2-3 | 2-3 |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Title: SYSTEM ROM

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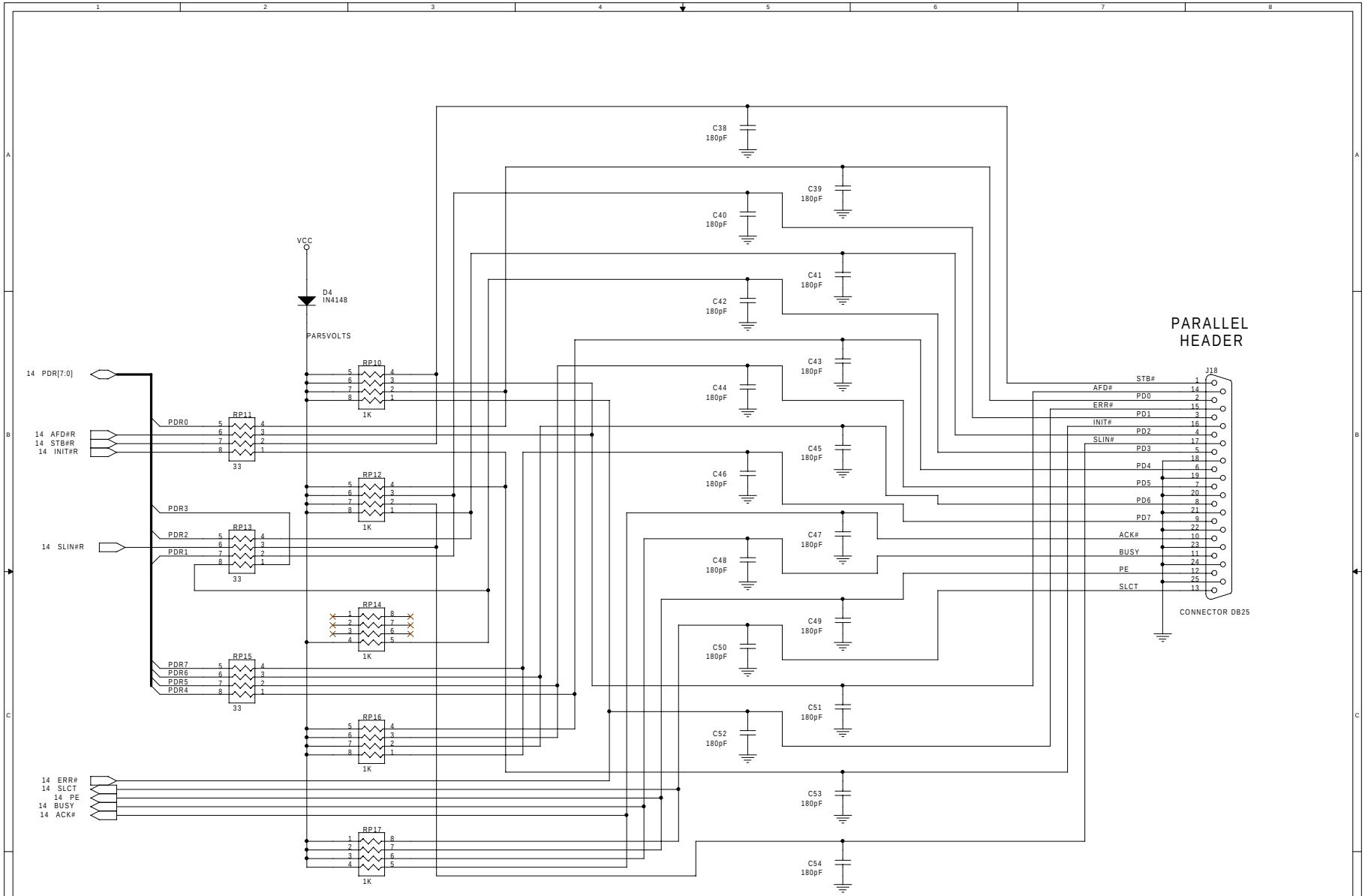


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Title: PARALLEL PORT

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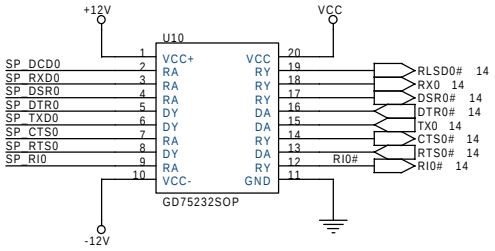
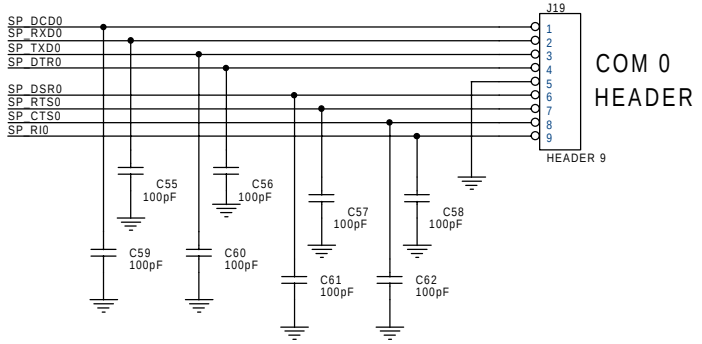
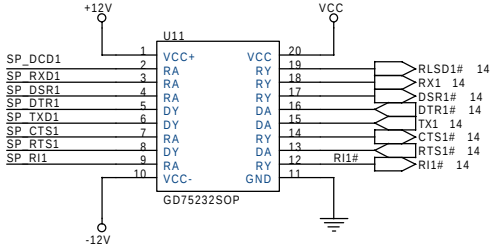
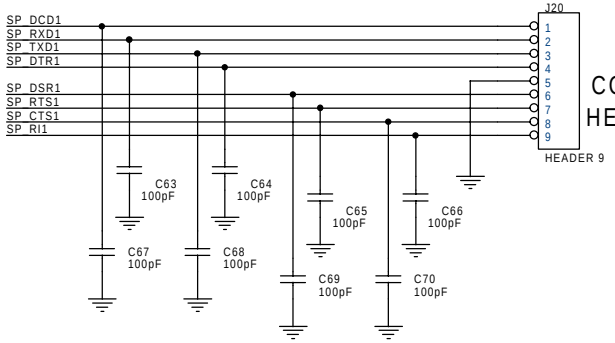


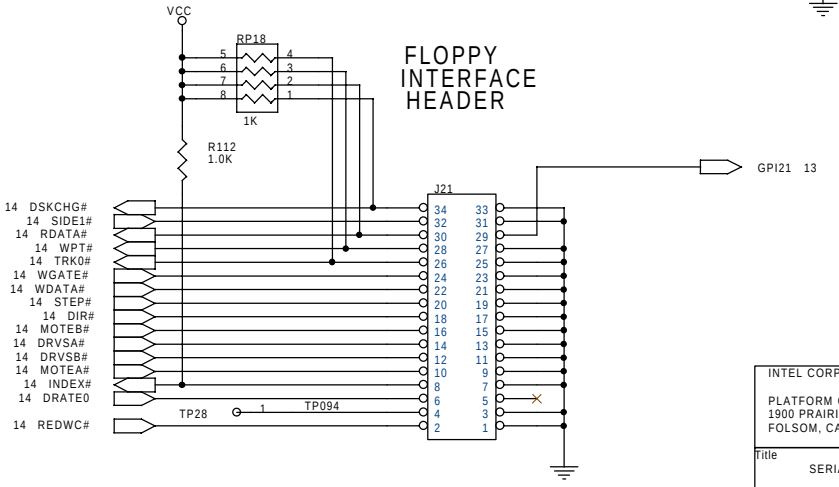




COM 0 HEADER




COM 1 HEADER




FLOPPY INTERFACE HEADER

**** Connected to GPI21 of the PIIX4 for BIOS detection of a floppy drive.**

| | | |
|---|---|---|
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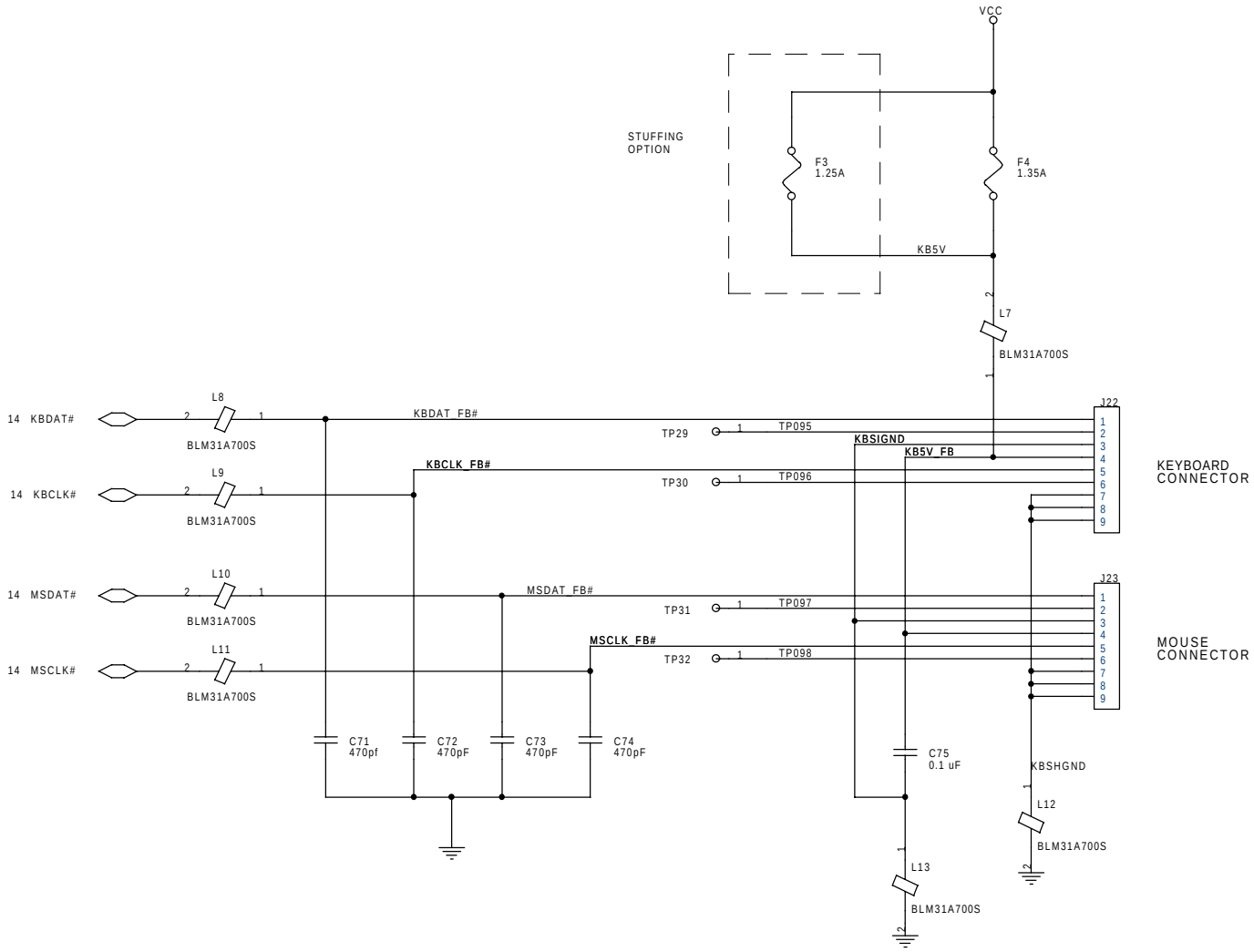
| Title: SERIAL AND FLOPPY | | |
| Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3 |
| Date: 23:44:47 | Sheet 23 of 34 | |




| | | |
|---|---|---|
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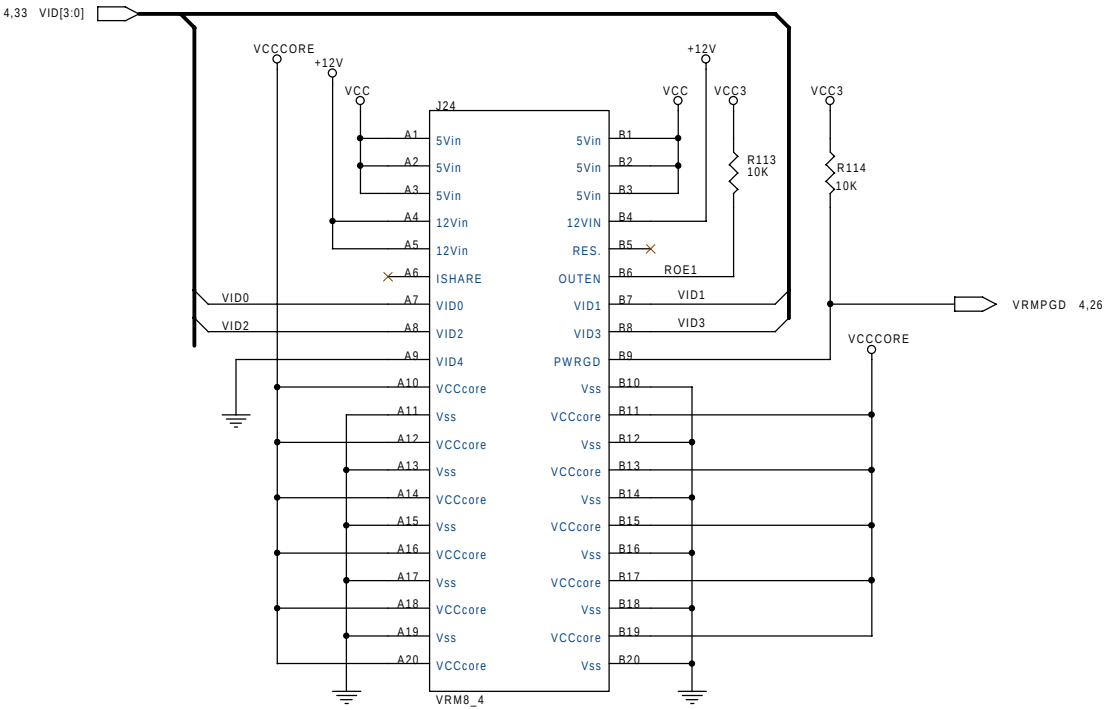
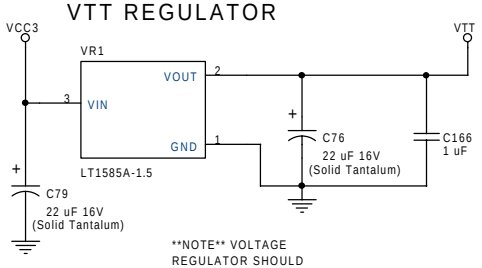
| Title: KEYBOARD/MOUSE INTERFACE | | |
| Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3 |
| Date: 23:44:47 | Sheet 24 of 34 | |

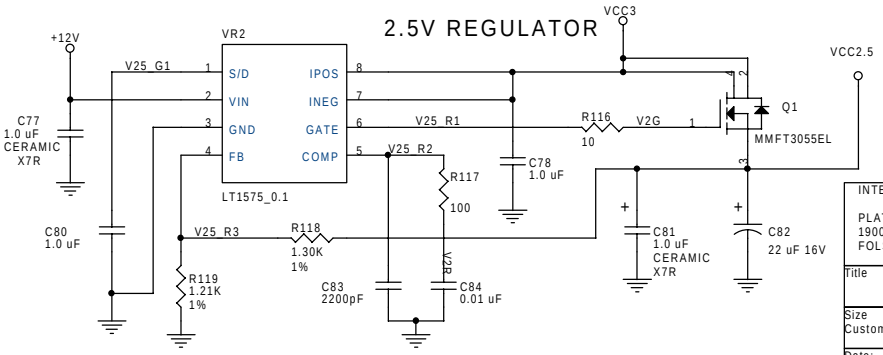



## VTT REGULATOR




**NOTE** VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE 440BX

## 2.5V REGULATOR

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FOLSOM, CA 95630

Title: DC-DC CONVERTER CONNECTORS

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| Custom | Intel(R) 440ZX AGPset | 1.3 |

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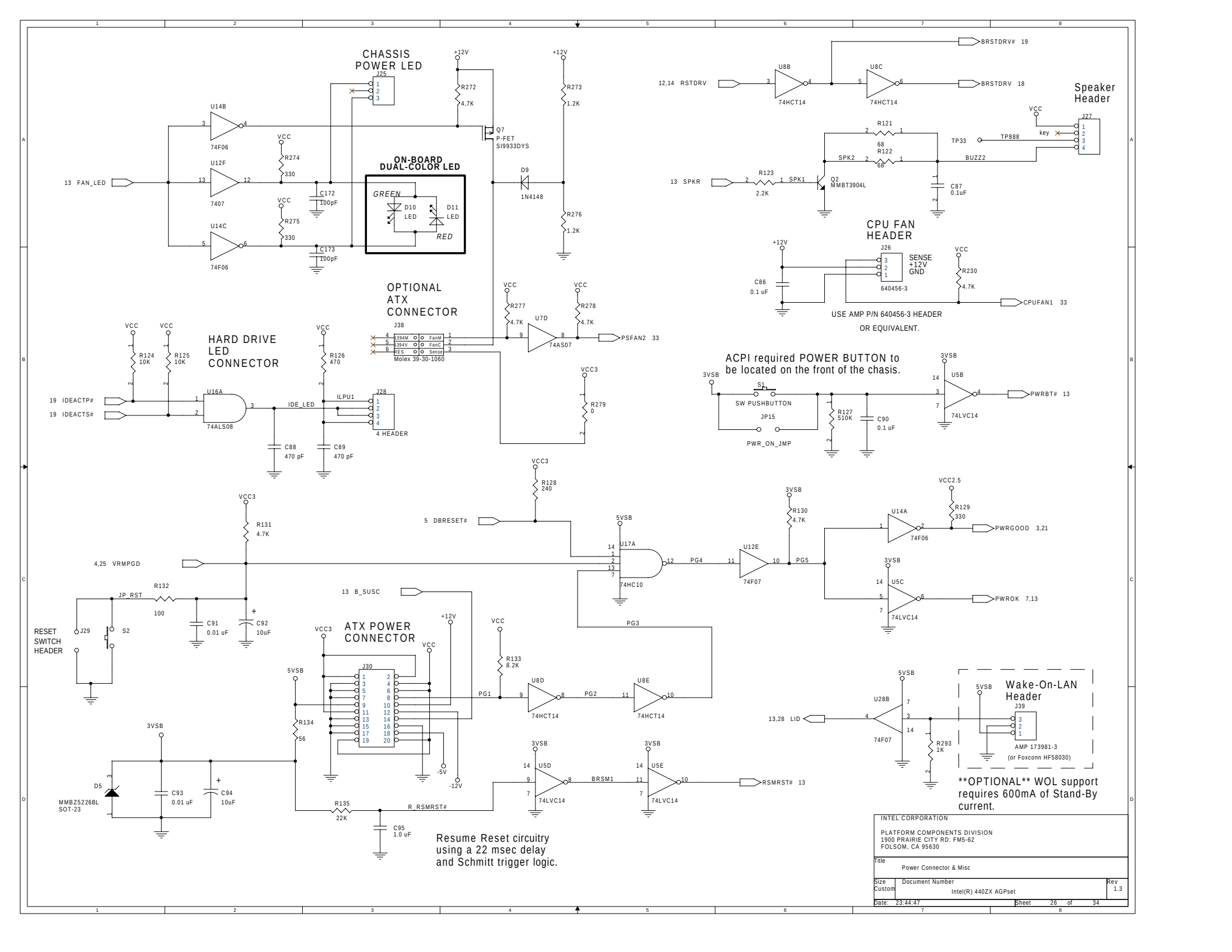
CHASSIS POWER LED
ON-BOARD DUAL-COLOR LED
GREEN
RED
13 FAN_LED
74F06
7407
74F06
1N4148
Q7 P-FET SI9933DYS
Speaker Header
12,14 RSTDRV
74HCT14
74HCT14
BRSTDRV# 19
BRSTDRV 18
13 SPKR
Q2 MMBT3904L
2.2K
68
68
TP33
TP888
key
BUZZ2
C87 0.1uF
CPU FAN HEADER
SENSE
+12V
GND
640456-3
C86 0.1 uF
R230 4.7K
CPUFAN1 33
USE AMP P/N 640456-3 HEADER
OR EQUIVALENT.
OPTIONAL ATX CONNECTOR
Molex 39-30-1060
74AS07
PSFAN2 33
HARD DRIVE LED CONNECTOR
19 IDEACTP#
19 IDEACTS#
74ALS08
IDE_LED
ILPU1
4 HEADER
C88 470 pF
C89 470 pF
ACPI required POWER BUTTON to be located on the front of the chasis.
SW PUSHBUTTON
JP15
PWR_ON_JMP
R127 510K
C90 0.1 uF
74LVC14
PWRBT# 13
5 DBRESET#
74HC10
PG4
PG5
74F07
PWRGOOD 3,21
PWROK 7,13
74F06
74LVC14
4,25 VRMPGD
R131 4.7K
R132 100
JP_RST
RESET SWITCH HEADER
C91 0.01 uF
C92 10uF
13 B_SUSC
PG3
ATX POWER CONNECTOR
R133 8.2K
R134 56
PG1
PG2
74HCT14
74HCT14
MMBZ5226BL SOT-23
C93 0.01 uF
C94 10uF
R135 22K
R_RSMRST#
C95 1.0 uF
BRSM1
74LVC14
74LVC14
RSMRST# 13
Resume Reset circuitry using a 22 msec delay and Schmitt trigger logic.
13,28 LID
74F07
Wake-On-LAN Header
AMP 173981-3
(or Foxconn HF58030)
**OPTIONAL** WOL support requires 600mA of Stand-By current.
INTEL CORPORATION
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FOLSOM, CA 95630
Title
Power Connector & Misc
Size Custom
Document Number
Intel(R) 440ZX AGPset
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Date: 23:44:47
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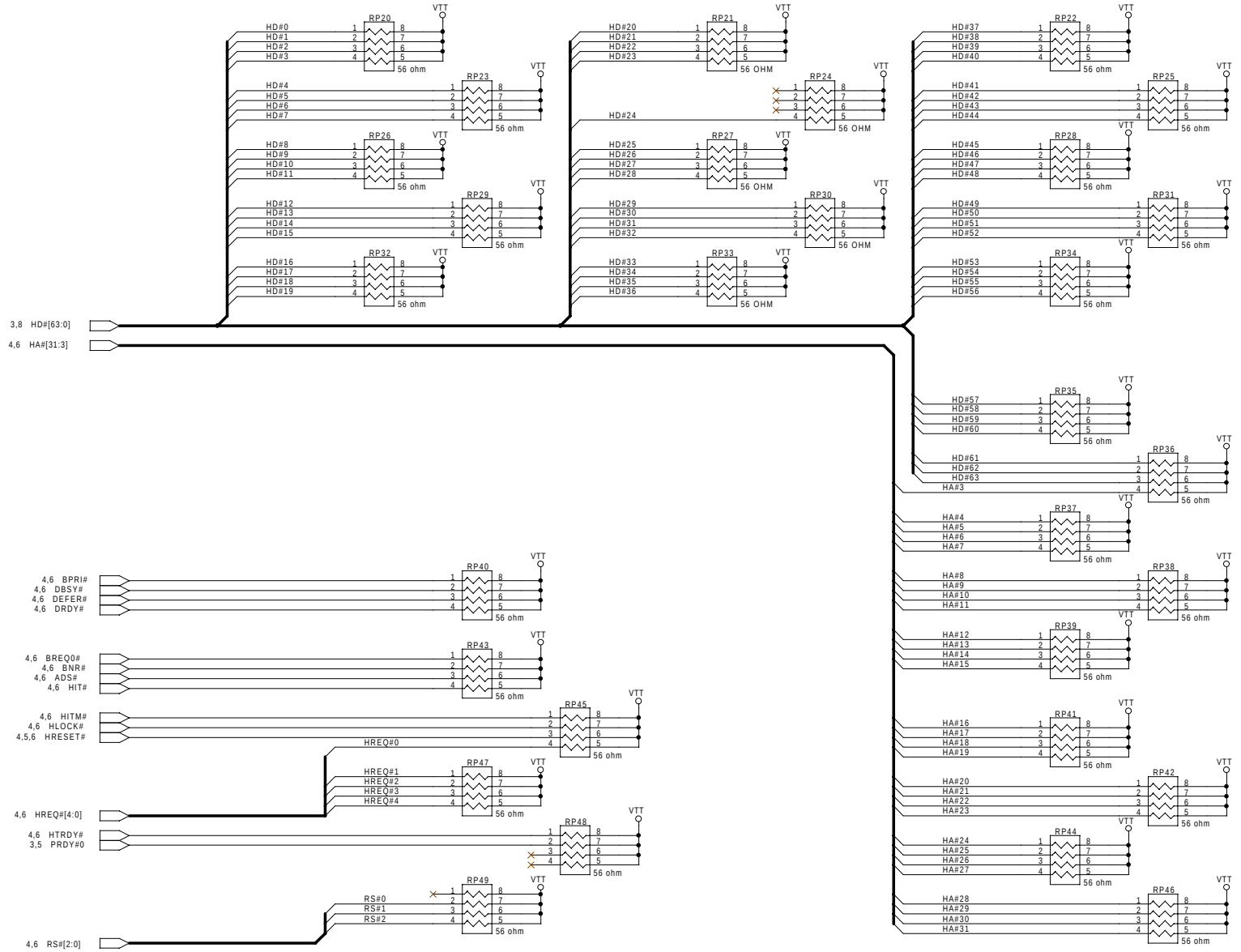
# GTL+ TERMINATION RESISTORS

*NOTE: May be removed if route lengths can be restricted to 1.5" MIN to 4.0" MAX.




NOTE : VTT = TERMINATION VOLTAGE

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Title: GTL TERMINATION

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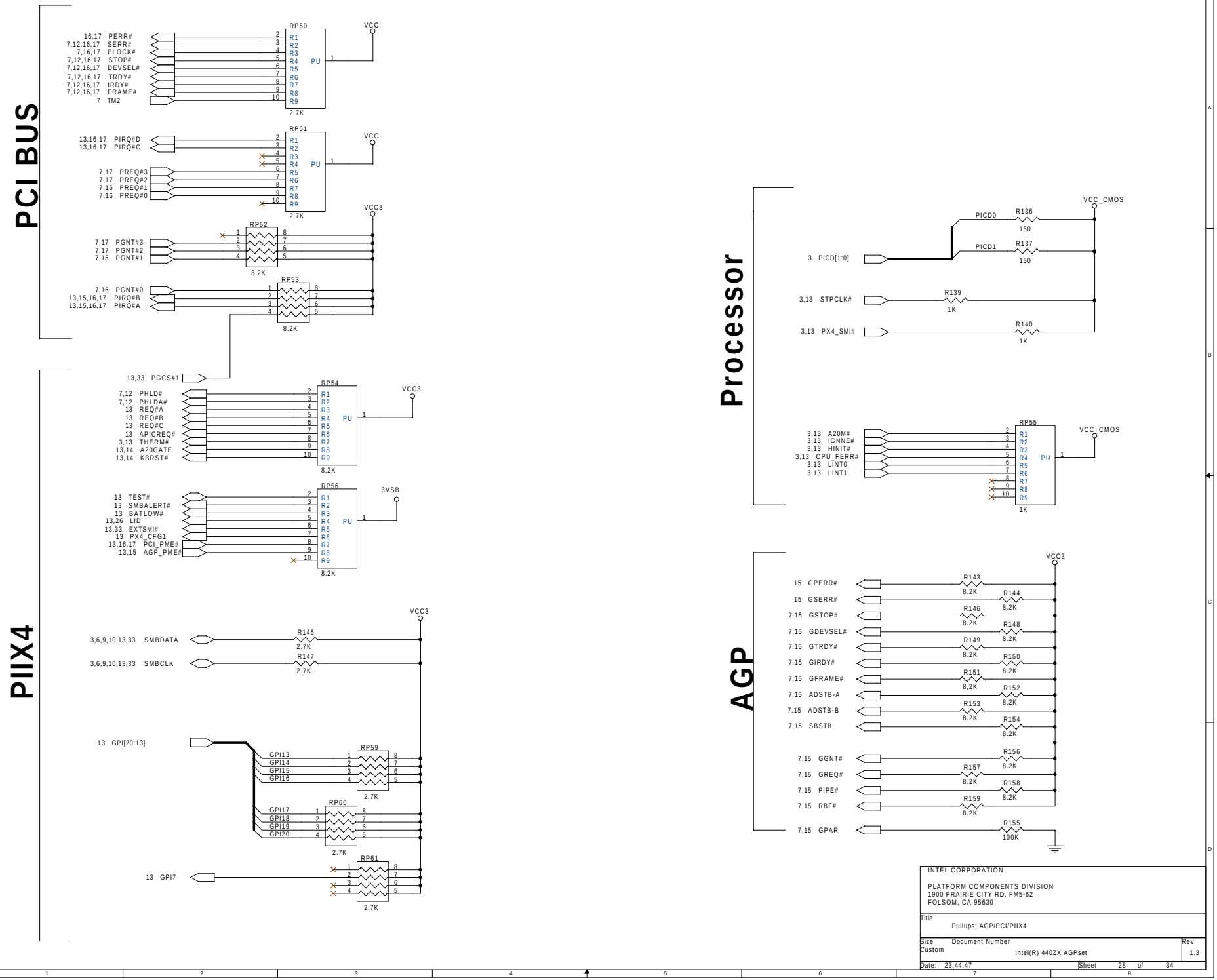


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Title: Pullups; AGP/PCI/PIIX4

Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3

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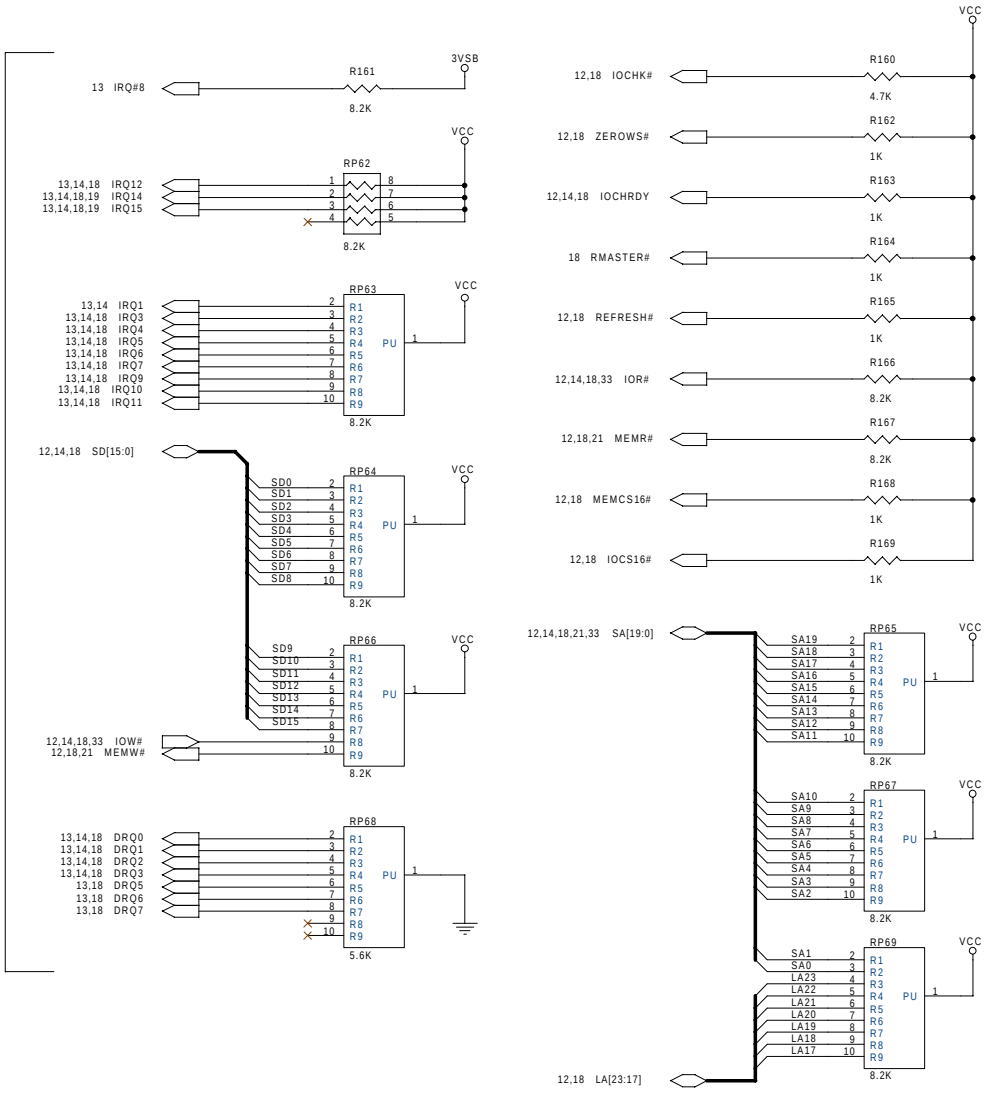
# ISA BUS




| | | |
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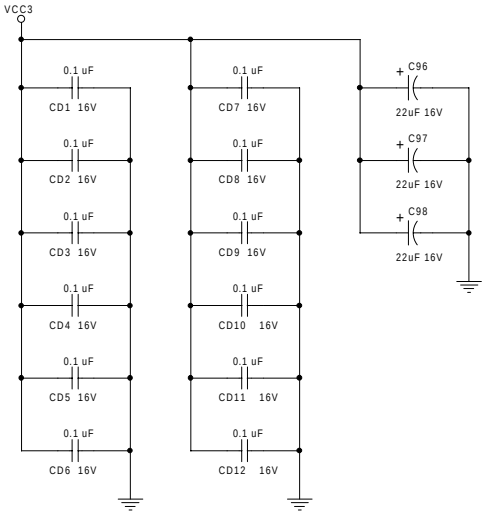
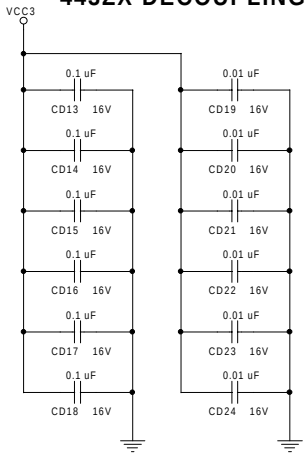
| Title: ISA BUS PULLUPS | | |
| Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3 |
| Date: | Sheet 29 of 34 | |

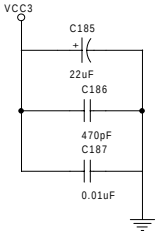
## DIMM DECOUPLING



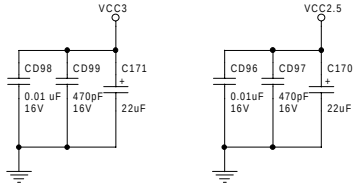

## 443ZX DECOUPLING




## CKBF DECOUPLING




## CK100 DECOUPLING

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FOLSOM, CA 95630

Title: DRAM, CLOCK AND 440ZX DECOUPLING CAPACITORS

| Size | Document Number | Rev |
|---|---|---|
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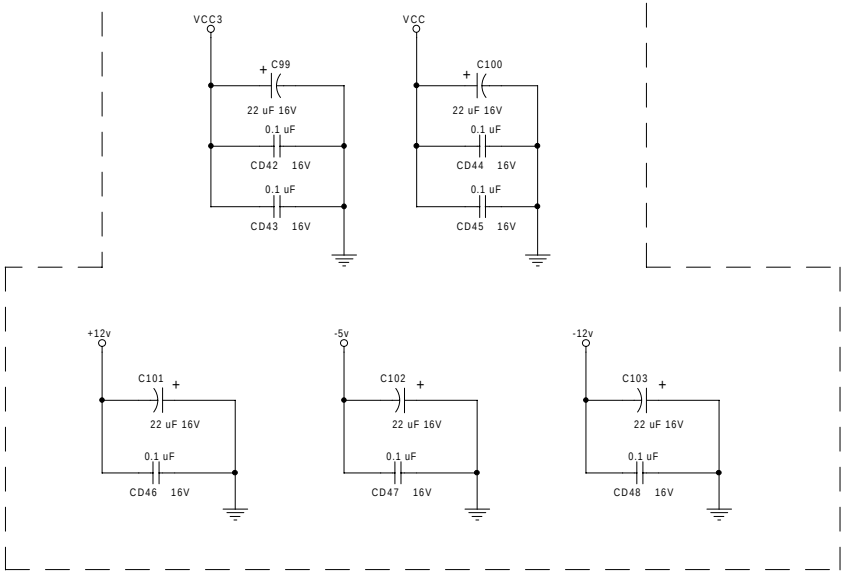
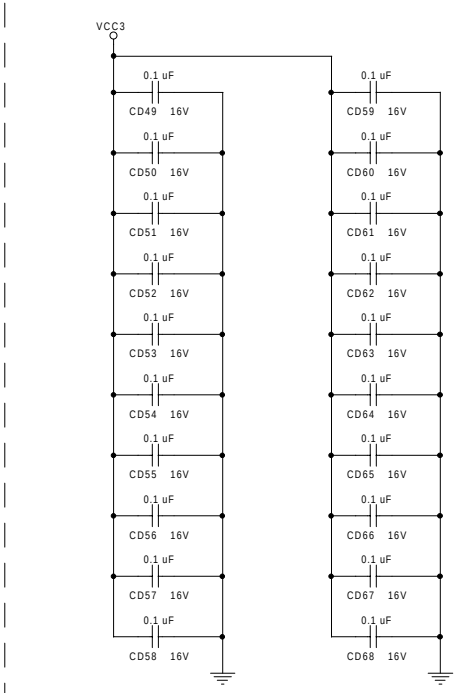
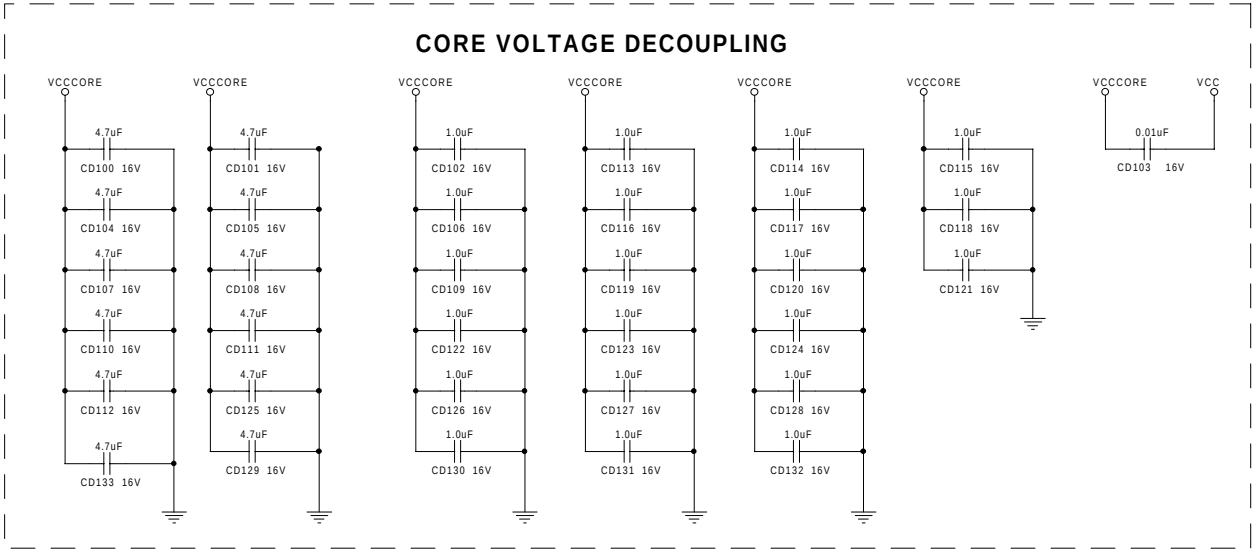
## BULK POWER DECOUPLING




## 3 VOLT DECOUPLING




## CORE VOLTAGE DECOUPLING





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Title: 3.3 VOLT AND BULK POWER DECOUPLING

| Size | Document Number | Rev |
|---|---|---|
| Custom | Intel(R) 440ZX AGPset | 1.3 |

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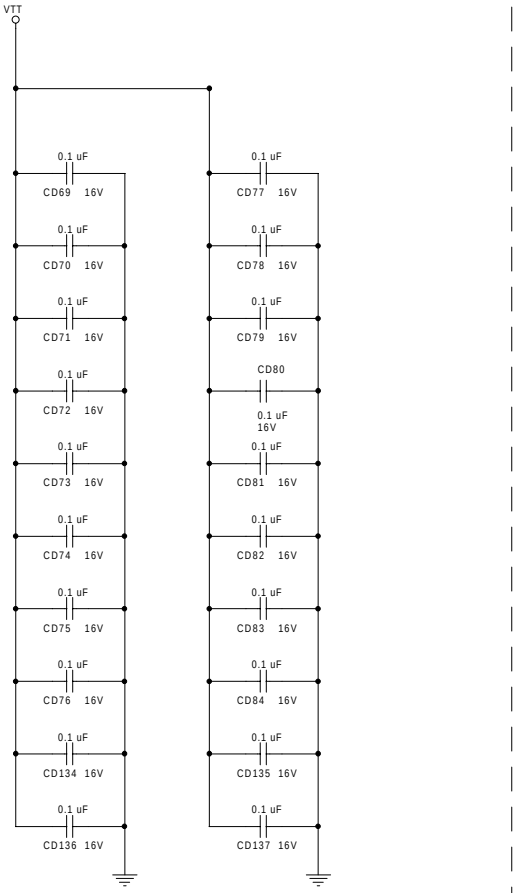
# TERMINATION VOLTAGE DECOUPLING

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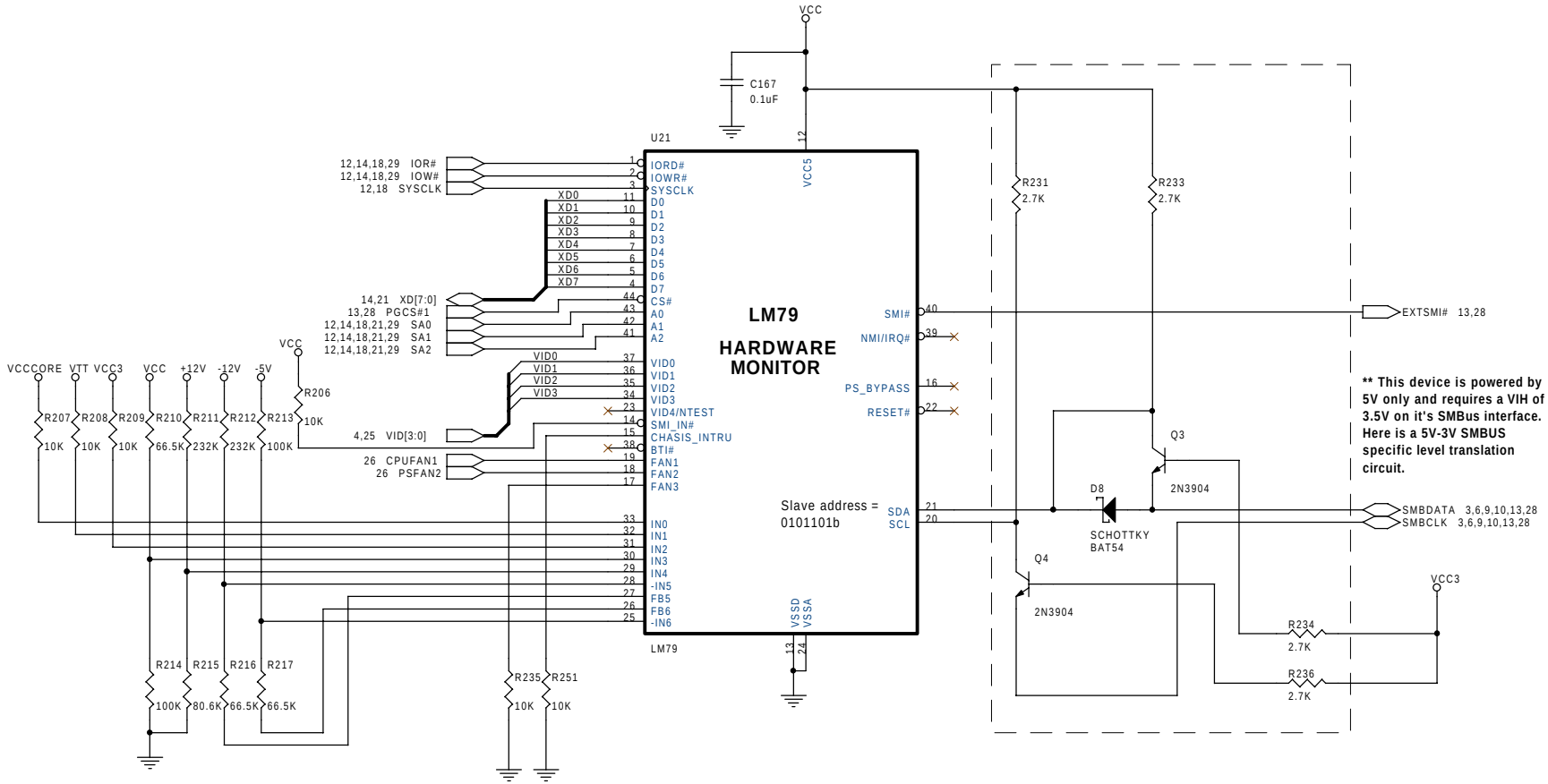
| | | |
|---|---|---|
| Title: TERMINATION DECOUPLING | | |
| Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3 |
| Date: 23:44:47 | Sheet 32 of 34 | |




# **OPTIONAL Manageability Logic

| | | |
|---|---|---|
| INTEL CORPORATION<br>PLATFORM COMPONENTS DIVISION<br>1900 PRAIRIE CITY RD. FM5-62<br>FOLSOM, CA. 95630 | | |
| Title: LM79 MONITOR[*Optional] | | |
| Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3 |
| Date: Tuesday, March 02, 1999 | Sheet 33 of 34 | |

**REVISION 1.0 -** Initial release -- August, 1998

**REVISION 1.1 -** Second release -- December, 1998

REVISION 1.2 - Minor edits for typos. Updated FERR# circuitry, component values, VRMPGD circuit. Feb.99

**REVISION 1.2 -** Added capacitor stuff option and implementation notes on pgs.4 & 6, and changed resistor values for R14&15 on pg5. Mar.99

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: REVISION HISTORY

Size: Custom | Document Number: Intel(R) 440ZX AGPset | Rev: 1.3

Date: 23:44:47 | Sheet 34 of 34

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**2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119**
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**Tel: + 81-29847-8522**

**FRANCE, Intel Corporation S.A.R.L.**
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**Tel: +33 1-45717171**

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**CANADA, Intel Semiconductor of Canada, Ltd.**
**190 Attwell Drive, Suite 500**
**Rexdale, Ontario M9W 6H8**
**Tel: +416 675-2438**