Intel® Celeron™ Processor (PPGA) with the Intel® 440LX AGPset

Design Guide

February 1999

Order Number: 245088-001

Contents

Figures

Tables

Revision History

Date	Revision	Description
1/99	-001	Initial Release.

1

Introduction

Introduction 1

The Intel® Celeron™ processor line includes processors that can be installed in a 370-pin socket. The Intel Celeron processor (PPGA) will also be offered as an Intel Boxed Processor, intended for system integrators who build systems from motherboards and other components. The intent of this document is to organize any special design recommendations and concerns that exist for creating an Intel Celeron processor (PPGA) / Intel® 440LX/EX AGPset based system. Likely design issues have been identified and included here in a checklist format to alleviate problems during the design and debug phases. The information contained in this document should be used in conjunction with the Intel® *Pentium® II Processor* / Intel® *440LX AGPset Design Guide*. Exceptions to the Intel® *Pentium® II Processor* / Intel® *440LX AGPset Design Guide* that are necessary for implementing an Intel Celeron™ processor (PPGA) / Intel® 440LX and Intel® 440EX AGPset based systems are listed in this document. For topics not covered in this document, refer to *Pentium® II Processor/* Intel® *440LX AGPset Design Guide* document.

1.1 Overview

This document contains information necessary for implementing an Intel Celeron processor (PPGA) / Intel 440LX or a Intel 440EX platform design. Throughout the document references to the “processor” refer to the Intel Celeron processor (PPGA) or future processors that are designed to fit in the 370-pin socket. Additionally, design guidelines that are unchanged from the *Pentium® II Processor 440LX AGPset Design Guide* are not covered in this document.

1.2 Reference Documents And Information Sources

Document Name or Information Source	Available From
Intel® Celeron™ Processor Datasheet	Intel Web Site
Intel® 82443LX PCI AGPset Controller	Intel Web Site
Intel® 82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4)	Intel Web Site
Pentium® II Processor 440LX AGPset Design Guide	Intel Web Site
Intel® 82440LX AGPset Design Guide Update	Intel Web Site
82443LX Application Notes	Intel Field Sales Representative
82443LX Specification Update	Intel Web Site
Intel® Celeron™ Processor Specification Update	Intel Web Site

1.3 Design Features

1.3.1 Intel® Celeron™ Processor (PPGA)

The Intel Celeron processor (PPGA) is the next addition to the Intel Celeron processor product line. The Intel Celeron processor (PPGA), like the Intel Celeron processor (S.E.P.P.), implements a Dynamic Execution micro-architecture and executes MMX™ media technology instructions for enhanced media and communication performance. The Intel Celeron processor (PPGA) also uses the same multi-transaction system bus used in the Intel® Pentium II processor. The Intel Celeron processor (PPGA) also supports multiple low-power states such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep to conserve power during idle times.

The Intel Celeron processor (PPGA) is based on the P6 core but is provided in a Plastic Pin Grid Array (PPGA) package for use in low cost systems in the Basic PC market segment. The Intel Celeron processor (PPGA) utilizes the AGTL+ system bus used by the Pentium II processor with support limited to single processor-based systems. Support for multi-processor-based systems is not provided with the Intel Celeron processor (PPGA). Pentium II processors should be used for multi-processor system designs. The Intel Celeron processor (PPGA) includes an integrated 128 KB second level cache with a separate 16 KB instruction and 16 KB data level one caches. The second level cache is capable of caching 4 GB of system memory address space.

To enable cost reduction at both the processor and system level, the Intel Celeron processor (PPGA) utilizes a packaging technology, known as the Plastic Pin Grid Array (PPGA). This packaging technology is similar to the mature Pentium processor package.

1.3.2 Intel® 440LX and Intel® 440EX AGPsets

This information is being provided to Intel customers to begin developing a design with the 82443LX. The 82443LX, 82443EX are Basic PC solutions for an Intel Celeron processor-based platform.

The 82443LX has the following features:

- Maximum of 4 DIMM sockets (512 MB SDRAM memory, 1 GB EDO memory)
- Maximum of 5 PCI slots (5 PREQx#/PGNTx# pairs support 5 PCI masters. PHOLD# and PHLDA# continue to support the PIIX4E as another bus master. There is support for a total of 6 PCI masters including the PIIX4E. Five PCI slots means 5 bus masters using the available 5 PREQx#/PGNTx# pairs. The physical location of these 5 PCI bus masters may be in cards inserted in the 5 PCI slots, or in cards inserted in 4 PCI slots together with one PCI bus master down on the motherboard, or in cards inserted in 3 PCI slots together with two PCI masters down on the motherboard, etc.)
- 66 MHz-only system bus/DRAM bus frequency

The 82443EX has the following features:

- Maximum of 2 DIMM sockets (256 MB memory, SDRAM or EDO)
- Maximum of 3 PCI slots (3 PREQx#/PGNTx# pairs support 3 PCI masters. PHOLD# and PHLDA# continue to support the PIIX4E as another bus master. There is support for a total of 4 PCI masters including the PIIX4E. 3 PCI slots means 3 bus masters using the available 3 PREQx#/PGNTx# pairs. The physical location of these 3 PCI bus masters may be in cards inserted in the 3 PCI slots, or in cards inserted in 2 PCI slots together with one PCI bus master down on the motherboard, or in cards inserted in 1 PCI slots together with two PCI masters down on the motherboard, etc.)
- No system memory ECC
- Single processor support only (no support for IOAPIC)
- 66 MHz-only system bus/DRAM bus frequency

Note: The designation Intel® 440LX AGPset (82443LX) will be used throughout the remainder of this document and will apply to both the Intel® 440LX AGPset and Intel® 440EX AGPset, unless otherwise noted.

1.4 General Design Recommendations

1.4.1 Voltage Definitions

For the purposes of this document the following nominal voltage definitions are used:

Vcc	5.0V
$Vcc_{3.3}$	3.3V
Vcc_{CORE}	Voltage is dependent on the four bit VID setting
$Vcc_{2.5}$	2.5V
Vcc_{CMOS}	2.5V
V_{TT}	1.5V
V_{REF}	1.0V
$AGPV_{REF}$	1.32V

1.4.2 General Design Recommendations

1. Intel recommends using a widely available, programmable Voltage Regulator Module (VRM) installed in a VRM header or an onboard programmable voltage regulator. Please see the *VRM 8.2 DC-DC Converter Design Guidelines*.
2. Motherboard designs targeted for system integrators should design to the boxed processor electrical, mechanical and thermal specifications provided in the boxed processor section of the *Intel® Celeron™ Processor* Datasheet, most notably the required fan power header and fan/heatsink physical clearance on the motherboard.

1.5 Transitioning From an Intel® Pentium® II Processor/ Intel® 440LX AGPset Design

1.5.1 AGTL+ Termination

Termination is no longer provided on the processor and must be implemented on the system board. In addition, high frequency Vtt decoupling is also required on the system board. Intel recommends one 0.1 uF capacitor in the 0603 package for every two resistor packs.

1.5.2 Vref Inputs

Vref (2/3 Vtt) must be supplied to the processor to each of the eight V_{REF} inputs. Intel recommends using one 75 ±1% and 150 ±1% ohm resistor divider of the Vtt supply to generate V_{REF}. Intel also recommends placing four 0.1 uF capacitors, in the 0603 package, within 500 mils of the processor's V_{REF} pins.

1.5.3 System Bus Clock

Due to the change in system bus trace lengths in the PPGA package, chipset and processor clocks must be ganged to minimize pin to pin clock skew. Implementation details are provided in the AGTL+ section of this document.

It is also recommended that a capacitor site be placed near the processor BCLK input to allow the clock skew to be minimized through tuning, by changing the value at the capacitor site, to compensate for the actual motherboard trace lengths.

1.5.4 CMOS Compatibility with Future Processors

All processor CMOS outputs are open drain and require a pullup to drive to external logic. The Intel Celeron processor (PPGA) is 2.5 Volt compatible. **The Intel 440LX AGPset and the Intel 440EX AGPset do not support future processors based on a 1.5V core.**

Intel has defined three new pins for the Intel Celeron processor (PPGA):

- $VCC_{2.5}$: This pin should be connected to the system's 2.5V supply.
- $VCC_{1.5}$: This pin should be left open. (not supported).
- VCC_{CMOS}: This pin should be used as the system CMOS pullup voltage. A 0.1 uF decoupling capacitor is recommended.

For an Intel Celeron processor (PPGA), VCC_{CMOS} will be directly tied to the $VCC_{2.5}$ pin, thereby providing 2.5V to system CMOS pullups. As a design option, the 2.5V supply may be directly used and these three pins may be left as no-connects.

These pins have been defined to permit a current of 500 mA maximum.

1.5.5 Processor Core Voltage Decoupling

High frequency decoupling for the processor core voltage is no longer provided on the processor as in previous generation processors. As a result, the system board must implement these capacitors. Intel recommends ten or more 4.7 uF capacitors in the 1206 package (ceramic X5R or better material) as well as nineteen or more 1.0 uF capacitors in the 0805 package to be placed within the socket cavity. Placement of the capacitors should be such that overall inductance between Vcc/Vss power pins is minimized. Meeting these guidelines will insure system compatibility with future PPGA Intel® Celeron™ processors. Implementation details are provided later in this document.

1.5.6 VID[4]

VID[4] is not provided on the processor. Therefore, according to the *VRM 8.2 DC-DC Converter Guidelines*, VID[4] must be connected to ground on the system board to provide the correct VID[3:0] for 1.3V to 2.05V Voltage ID Encoding.

1.5.7 Phase Lock Loop (PLL) Power

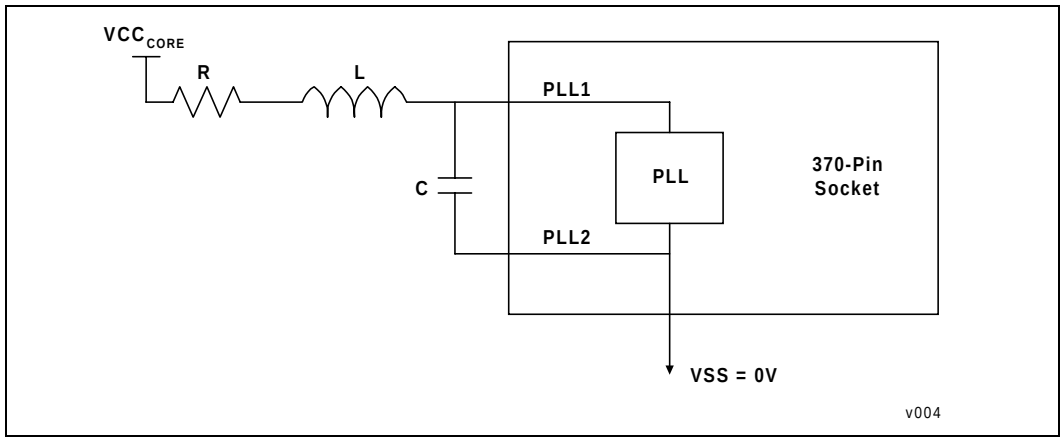
1.5.7.1 Processor PLL Filter Recommendation

All Intel Celeron processors have internal PLL clock generators which are analog and require quiet power supplies for minimum jitter.

1.5.7.2 Topology

The general desired topology is shown in Figure 1-1. Not shown are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

Figure 1-1. Filter Topology



1.5.7.3 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. In general, the low-pass description forms an adequate description for the filter.

The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

< 0.2 dB gain in pass band

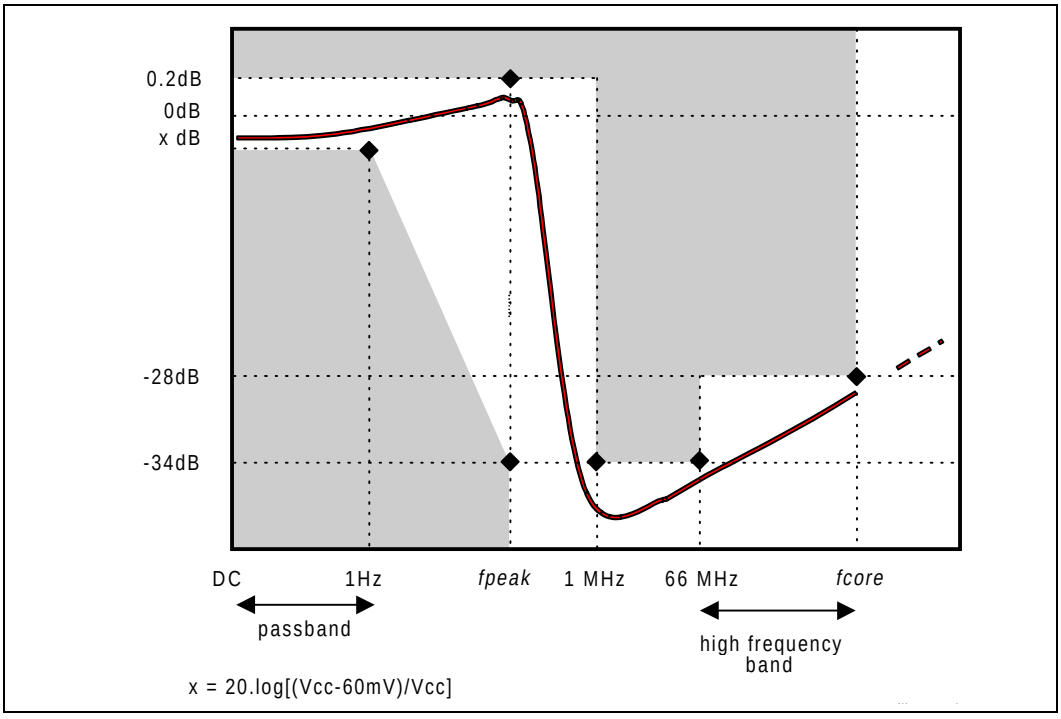
< 0.5 dB attenuation in pass band (see DC drop in next set of requirements)

> 34 dB attenuation from 1 MHz to 66 MHz

> 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 1-2.

Figure 1-2. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak*, if it exists, it should be less than 0.05 MHz.

Other requirements:

- Filter should support DC current > 30 mA.
- Shielded type inductor to minimize magnetic pickup.
- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2W; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

1.5.7.4 Recommendation for Intel Platforms

The following tables are examples of components that meet Intel's recommendations, when configured in the topology presented in Figure 1-1.

Table 1-1. Inductor

Part Number	Value	Tol	SRF	Rated I	DCR
TDK MLF2012A4R7KT	4.7uH	10%	35MHz	30mA	0.56Ω (1W max)
Murata LQG21N4R7K00T1	4.7uH	10%	47MHz	30mA	0.7Ω (±50%)
Murata LQG21C4R7N00	4.7uH	30%	35MHz	30mA	0.3Ω max

Table 1-2. Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33uF	20%	2.5nH	0.225Ω
AVX TPSD336M020S0200	33uF	20%	TBD	0.2Ω

Table 1-3. Resistor

Value	Tolerance	Power	Note
1Ω	10%	1/16W	Resistor may be implemented with trace resistance, in which discrete R is not needed

To satisfy damping requirements, total series resistance in the filter (from VCC_{CORE} to the top plate of the capacitor) must be at least 0.35Ω. This resistor can be in the form of a discrete component, or routing, or both. For example, if the picked inductor has a minimum DCR of 0.25Ω, then a routing resistance of at least 0.10Ω is required. Be careful not to exceed the maximum resistance rule (2Ω). For example, if using discrete R1, the maximum DCR of the L should be less than 2.0 - 1.1 = 0.9Ω, which precludes using some inductors.

Other routing requirements:

- C should be close to PLL1 and PLL2 pins, < 0.1Ω per route. These routes do not count towards the minimum damping R requirement.
- PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- L should be close to C; any routing resistance should be inserted between VCC_{CORE} and L.
- Any discrete R should be inserted between VCC_{CORE} and L.

Figure 1-3. Using Discrete R

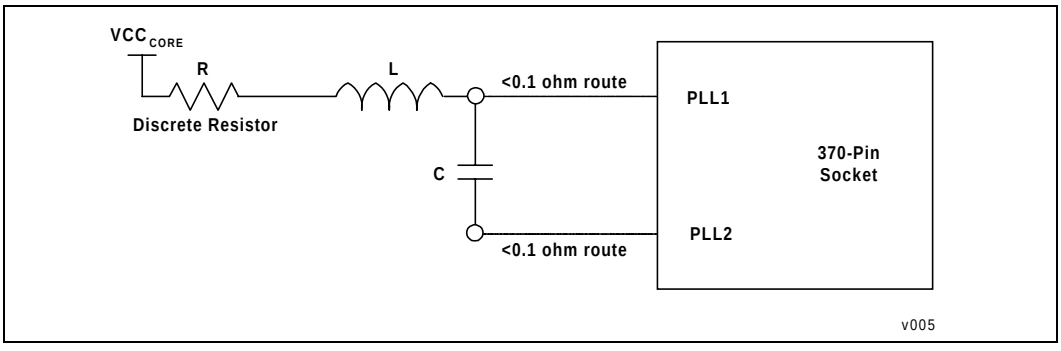
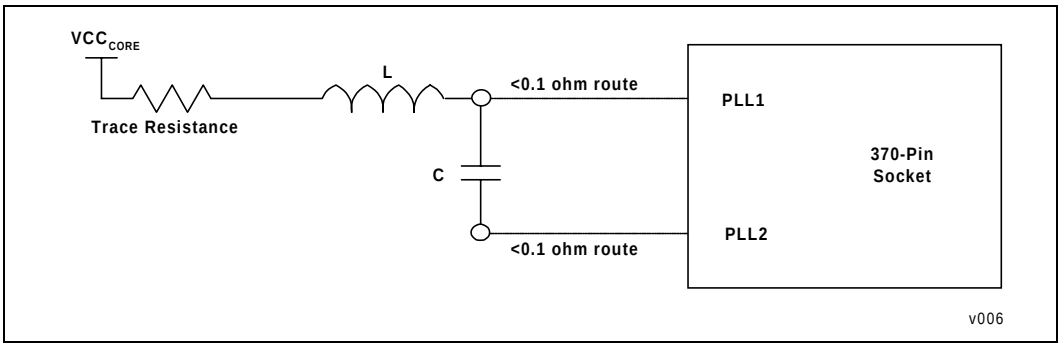


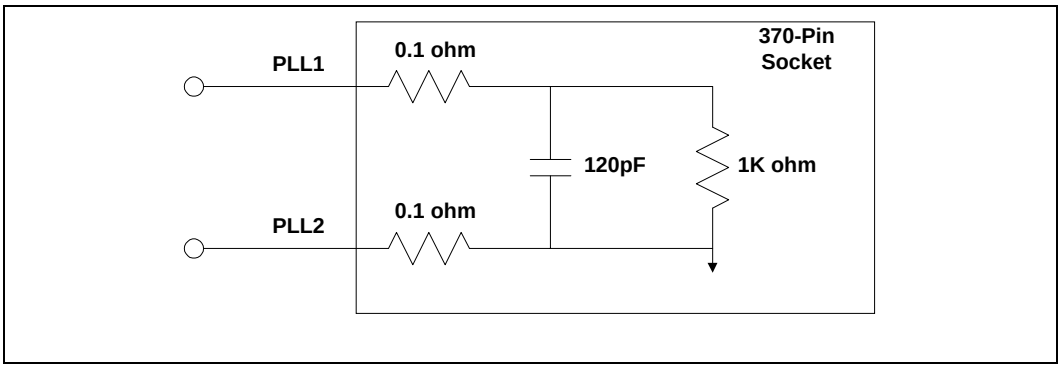
Figure 1-4. No Discrete R



1.5.7.5 Custom Solutions

As long as the filter performance as specified in Figure 1-2 and other requirements outlined in Section 1.5.7.3 are satisfied, other solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown in Figure 1-2.

Figure 1-5. Core Reference Model



NOTES:
1. 0.1Ω resistors represent package routing.
2. 120pF capacitor represents internal decoupling capacitor.
3. 1KΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitics.
5. Please sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30mA and minimum VCC_{CORE} level.

1.5.8 Bus Frequency Selection

The BSEL pin on the Intel Celeron processor (PPGA) is used to select the system bus frequency. BSEL is Low for 66 MHz. BSEL should be pulled to ground on the motherboard.

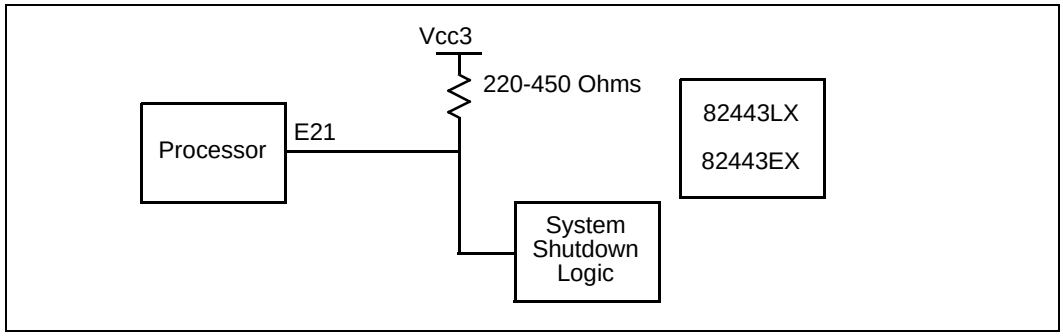
1.5.9 EDGCTRL

A new pin that is required for correct operation of the processor, EDGCTRL, requires 51 ohm 5% pullup to Vcc_{CORE}.

1.5.10 $V_{COREDET}$

The Intel 440LX/EX AGPsets do not support 0.18 micron processors. The $V_{COREDET}$ pin can be used by external motherboard logic to prevent the platform from operating if a 0.18u processor is installed. The $V_{COREDET}$ pin is tied to Vss on the package. Connect this pin to the external motherboard logic. A logic low can gate the platform from powering up. For Intel® Celeron™ processors based on the 0.25 micron process, the $V_{COREDET}$ pin is a no-connect (floating) on the package. Refer to Figure 1-6 as an example.

Figure 1-6. $V_{COREDET}$ Not Supported Using 440LX/EX AGPsets



2

Motherboard Design

Motherboard Layout and Routing Guidelines 2

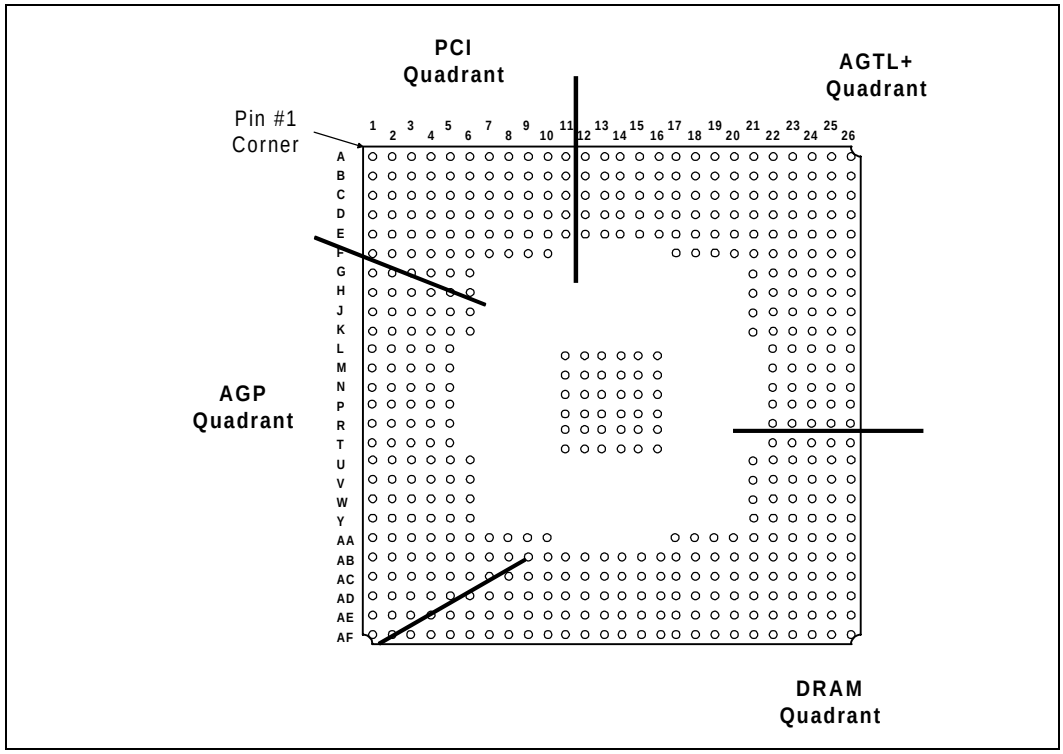
This section describes layout and routing recommendations to insure a robust design. Follow these guidelines as closely as possible. Any deviations from the guidelines listed here should be simulated to insure adequate margin is still maintained in the design.

2.1 BGA Quadrant Assignment

Intel assigned pins on the 82443LX to simplify routing and keep board fab costs down, by permitting a motherboard to be routed in 4-layers. Figure 2-1 shows the 4 signal quadrants of the 82443LX. The component placement on the motherboard should be done with this general flow in mind. This simplifies routing and minimizes the number of signals which must cross. The individual signals within the respective groups have also been optimized in order to be routed using only 2 PCB layers.

The 82443LX datasheet contains a complete list of signals and ball assignments.

Figure 2-1. Major Signal Sections (82443LX Top View)



2.2 Intel® Celeron™ Processor (PPGA) Signal Quadrants

Figure 2-2. Intel® Celeron™ Processor (PPGA) Quadrants

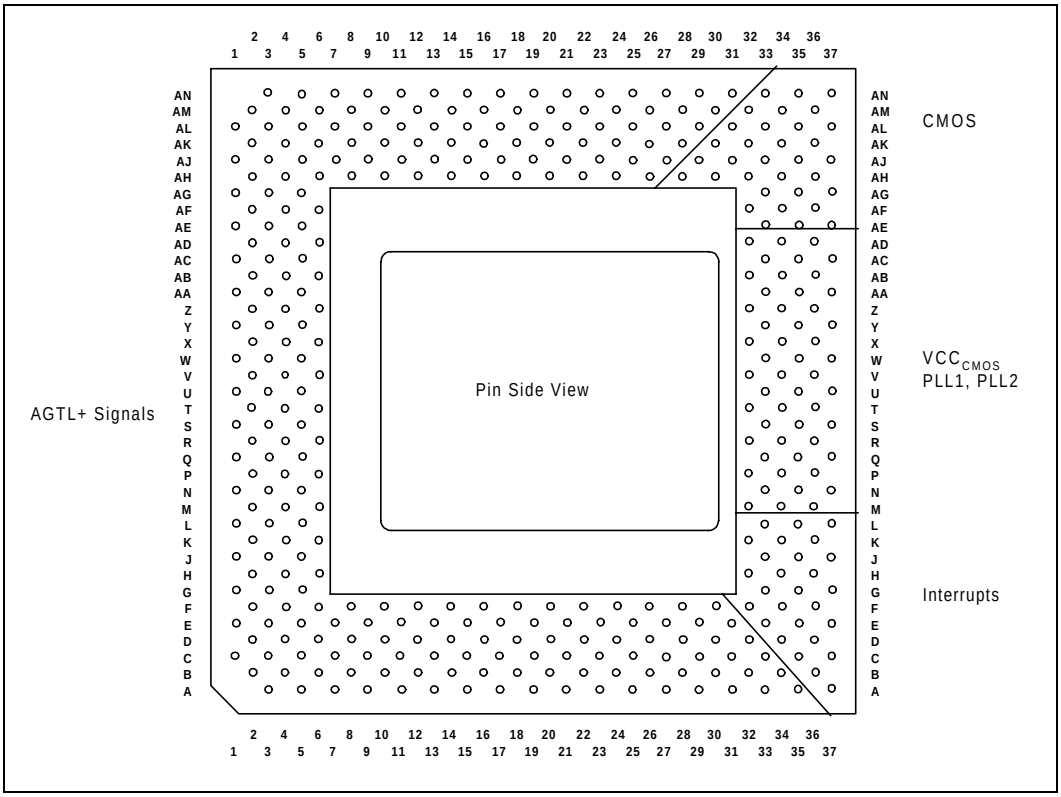
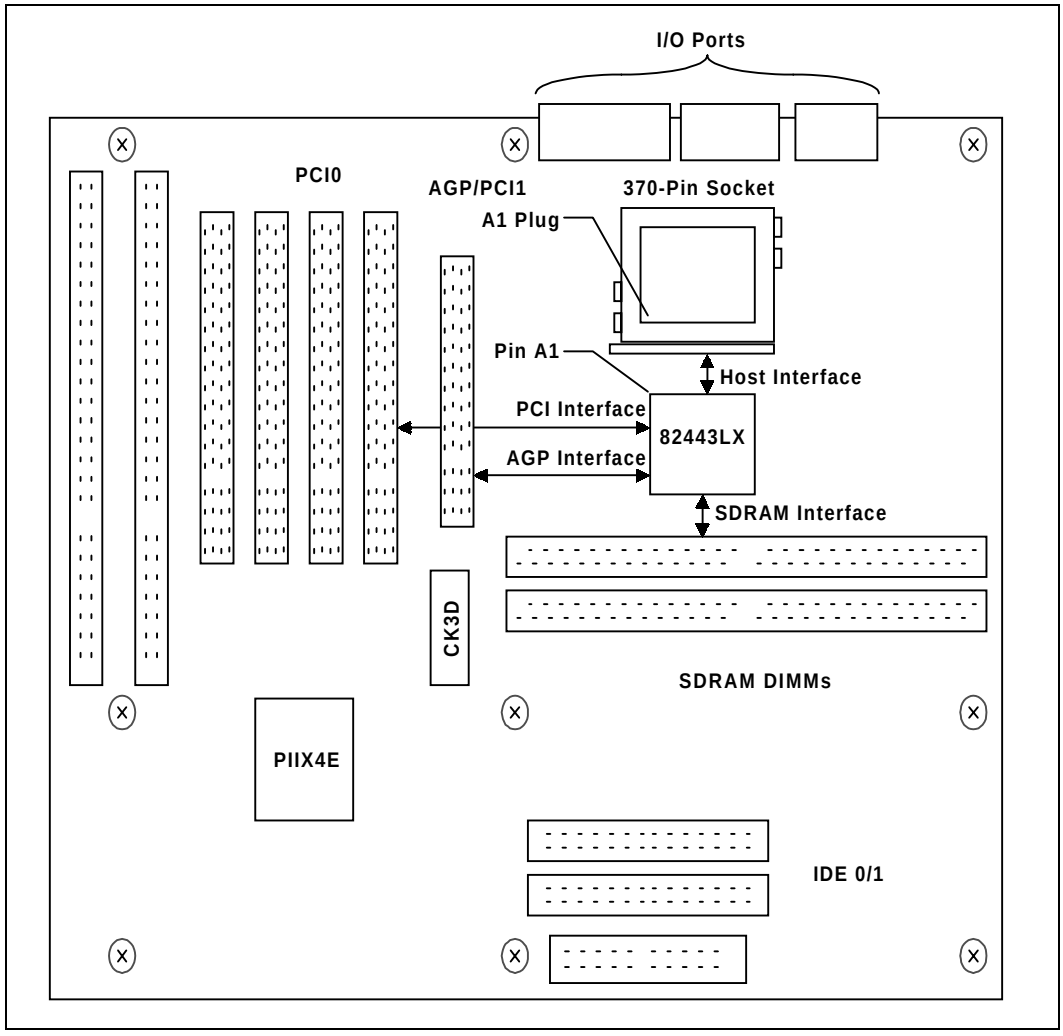


Figure 2-2 indicates the signal quadrants for the Intel Celeron™ processor (PPGA). These quadrants were defined to facilitate layout and placement and show the proposed component placement for an Intel Celeron™ processor (PPGA) for both ATX and NLX form factor designs.

ATX Form Factor:

1. The ATX placement and layout below is recommended for an Intel® Celeron™ processor (PPGA) / Intel® 440LX AGPset system design.
2. The example placement below shows 4 PCI slots, 2 ISA slots, 2 DIMM sockets, and one AGP connector.
3. For an ATX form factor design, the AGP compliant graphics device can be either on the motherboard (device down option), or on an AGP connector (up option).
4. The trace length limitation between critical connections will be addressed later in this document.
5. Figure 2-3 is for ***reference only*** and the trade-off between the number of PCI and ISA slots, number of DIMM sockets, and other motherboard peripherals needs to be evaluated for each design.

Figure 2-3. Example ATX Placement for an Intel® Celeron™ Processor (PPGA) / Intel® 440LX AGPset Design

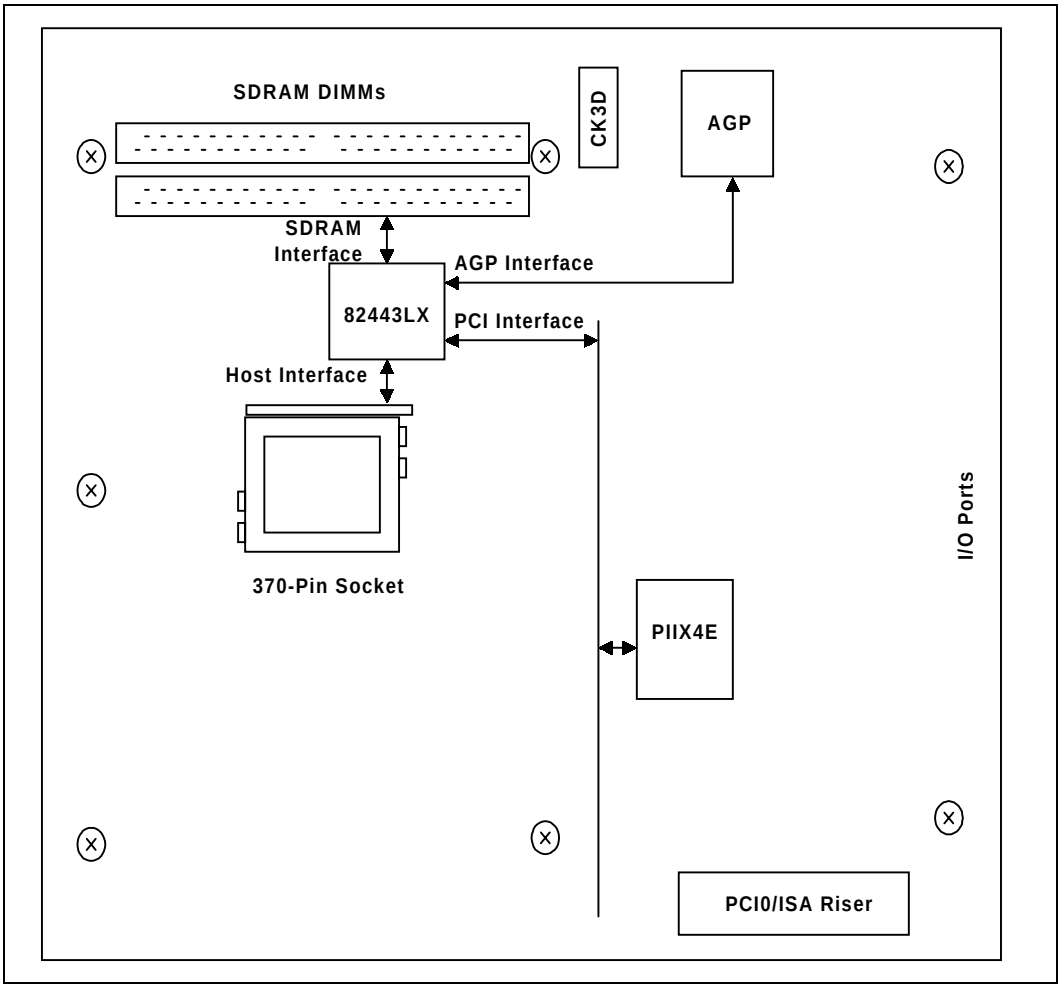


NLX Form Factor:

The NLX placement and layout below is recommended for a Intel® Celeron™ processor (PPGA) / Intel® 440LX AGPset system design.

1. The example placement below shows 2 DIMM sockets, and an AGP compliant device down on the motherboard.
2. For an NLX form factor design, the AGP compliant graphics device may readily be integrated on the motherboard (device down option).
3. The trace length limitation between critical connections will be addressed later in this document.
4. Figure 2-4 is for ***reference only*** and the trade-off between the number of DIMM sockets, and other motherboard peripherals needs to be evaluated for each design.

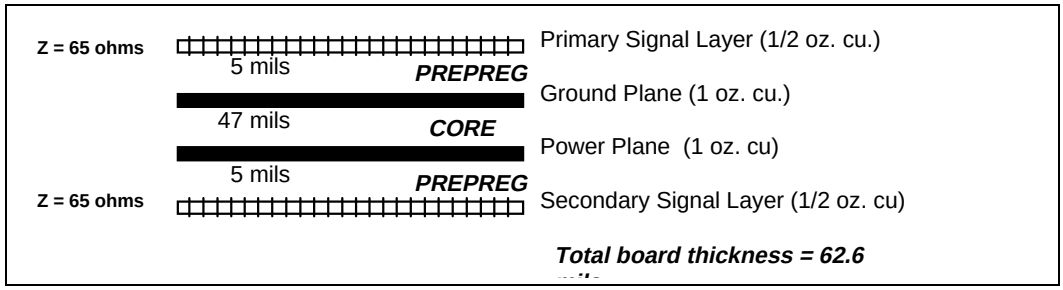
Figure 2-4. Example NLX Placement for an Intel® Celeron™ Processor (PPGA) / Intel® 440LX AGPset Design



2.3 Board Description

A 4 layer stack-up arrangement is recommended for the system board. The stack up of the board is shown in Figure 2-5. The impedance of all the signal layers are to be between 55 and 75 ohms. Lower trace impedance will reduce signal edge rates, over & undershoot, and have less cross-talk than higher trace impedance. Higher trace impedance will increase edge rates and may slightly decrease signal flight times.

Figure 2-5. Four Layer Board Stack-up



Note that the top and bottom routing layers specify 1/2 oz. cu. However, by the time the board is plated, the traces will be about 1 oz. Check with your fab vendor on the exact value and insure that any signal simulation accounts for this.

Note: A thicker core may help reduce board warpage issues.

Additional guidelines on board stackup, placement and layout include:

- Single ended termination is recommended for AGTL+ signals. One termination resistor is present on the system board. The trace lengths should be controlled to 2.0” minimum and 5.5” maximum.
- The termination resistors on the AGTL+ bus should be 56 ohms ±5%.
- The board impedance (Z) should be between 55 and 75 ohms (65 ohms ±15%)
- FR-4 material should be used for the board fabrication.
- The ground plane should not be split on the ground plane layer. If a signal must be routed for a short distance on a power plane, then it should be routed on a VCC plane, not the ground plane.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

2.4 Routing Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order that signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. If the guidelines listed here are not followed, it is important that your design is simulated, especially on the AGTL+ signals. Even when the guidelines are followed, it is still a good idea to simulate as many signals as possible for proper signal integrity, flight time and cross talk.

2.4.1 AGTL+ Description

AGTL+ is the electrical bus technology used for the Intel® Celeron™ processor and Intel® Pentium® II processor host buses. AGTL+ is a low output swing, incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at the end of the bus. The AGTL+ specification is contained in the *Intel® P6 Family Processor Developer's Manual*.

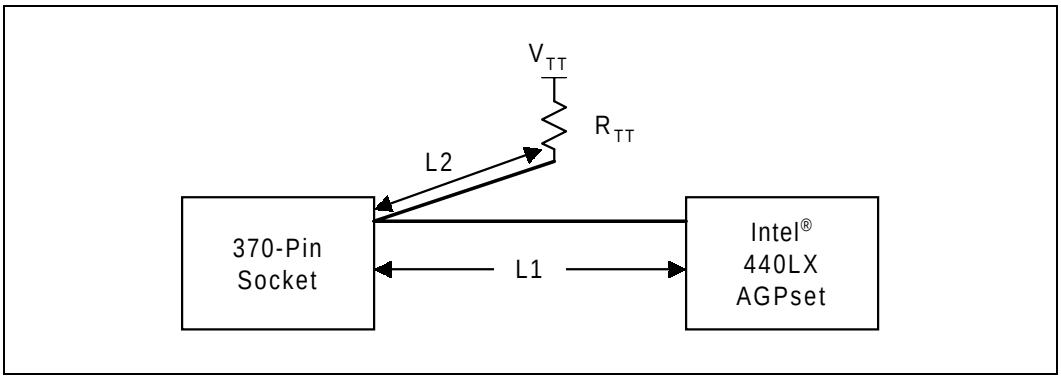
2.5 AGTL+ Layout Recommendations

This section contains the layout recommendations for the AGTL+ signals. The layout recommendations are derived from pre-layout simulations that Intel has performed.

2.5.1 Network Topology and Conditions

The recommended topology for single processor systems is shown in Figure 2-6. A termination resistor is placed on the system board. The recommended value for the termination resistor is 56Ω ± 5%.

Figure 2-6. Recommended Topology



2.5.2 Recommended Trace Lengths

Trace length recommendations are summarized Table 2-1. The recommended lengths are derived from the parametric sweeps and Monte Carlo analysis.

Table 2-1. Recommended Trace Lengths

Trace	Minimum Length	Maximum Length
L1	2.0”	5.5”
L2	0.5”	2.0”

Intel recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design. Simulation will confirm that the design adheres to the guidelines.

2.5.2.1 Single Processor Simulation Results

Parametric Sweeps

The values for interconnect parameter values that were used in all parametric sweeps are summarized in Table 2-2.

Table 2-2. Model M Parameter Values For Interconnect SImulations

Component	Parameter	Fast	Typical	Slow
PPGA	Z_0 [Ω] S_0 [ns/ft]	74.75 1.6 (µstrip) 1.8 (stripline & emb µstrip)	65.00 1.8 (µstrip) 2.0 (stripline & emb µstrip)	55.25 2.0 (µstrip) 2.2 (stripline & emb µstrip)
Mother Board	Z_0 [Ω] S_0 [ns/ft]	74.75 1.8	65.00 2.0	55.25 2.2
Connector	Z_0 [Ω] T_d [ps]	80 30	65 100	50 120
Termination	R_{TT} [Ω]	56 - 5%	56	56 + 5%
	V_{TT} [V]	1.5 + 9%	1.5	1.5 - 9%

Note: For simulation purposes, the socket connector can be modelled as a transmission line. The length of the line and the propagation speed must be selected such that they give a total delay of 120 ps in the slow case and 30 ps in the fast case.

2.5.3 Additional Guidelines

2.5.3.1 For More Information on AGTL+

The general rules for minimizing the impact of crosstalk and other practical considerations in the design of a high speed AGTL+ bus are discussed in the *Pentium® II Processor/440LX AGPset Design Guide* document.

2.5.4 Performance Requirements

Prior to performing interconnect simulations, establish the minimum and maximum flight time requirements. Setup and hold requirements determine the flight time bounds for the system bus. The bus contains two paths which must be considered:

- the processor driving an AGPset component
- the AGPset component driving a processor

Table 2-3 provides recommended flight time specifications. Flight times are measured at the processor pins.

Table 2-3. Recommended 66 MHz System Flight Time Targets

Driver	Receiver	$T_{flight,min}$ [ns]	$T_{flight,max}$ [ns]
Processor	AGPset	0.10	2.10
AGPset	Processor	0.0	4.05

2.5.5 Topology Definition

As described in Section 2.5.1, AGTL+ is sensitive to transmission line stubs, which can result in ringing on the rising edge caused by the high impedance of the output buffer in the high state. AGTL+ signals should be connected in a daisy chain, keeping transmission line stubs to the processor under 2.0 inches.

2.5.6 Pre-Layout Simulation (Sensitivity Analysis)

After an initial timing analysis has been completed, simulations should be performed to determine the bounds on system layout. AGTL+ interconnect simulations using transmission line models are recommended to determine signal quality and flight times for proposed layouts. Recommended parameter values shown in Table 2-2 should be used for simulation. The recommended values in Table 2-2 may be replaced if your supplier's specific capabilities are known. The corner values should comprehend the full range of manufacturing variation. The Intel® Celeron™ processor (PPGA) models include the I/O buffer models, core package parasitics, package trace length, impedance and velocity. Intel® 440LX APGset models are available and include the I/O buffers and package traces. Termination resistors should be controlled to within ± 5%.

2.6 Post-Layout Simulation

Following layout, extract the traces and run simulations to verify that the layout meets timing and noise requirements. A small amount of trace "tuning" may be required, but experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required.

The post layout simulations should take into account the expected variation for all interconnect parameters. For timing simulations, use a V_{REF} of 2/3 V_{TT} ± 2% for both the processor and Intel® 440LX AGPset components. Flight times measured from the processor pins to other system components use the normal flight time method.

2.6.1 Crosstalk and the Multi-Bit Adjustment Factor

Coupled lines should be included in the post-layout simulations. The flight times listed in Table 2-3 apply to single bit simulations only. They do not include an allowance for crosstalk. Crosstalk effects are accounted for separately, as part of the multi-bit timing adjustment factor, T_{adj}, that is defined in Table 2-5. The recommended timing budget includes 300 ps for the adjustment factor.

Use caution in applying T_{adj} to coupled simulations. This adjustment factor encompasses other effects besides board coupling, such as processor and package crosstalk, and ground return inductances. In general, the additional delay introduced by coupled simulations should be less than 300 ps.

2.7 Timing Analysis

To determine the available flight time window, perform an initial timing analysis. Analysis of setup and hold conditions will determine the minimum and maximum flight time bounds for the system bus. Use the following equations to establish the system flight time limits.

Table 2-4. Intel® Celeron™ Processor and Intel® 440LX AGPset System Timing Equations

Driver	Receiver	Equation
processor	AGPset	$T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} + T_{skew,SKT}$
		$T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{skew,SKT} - T_{jit} - T_{adj}$
AGPset	processor	$T_{flight,\min} \geq T_{hold} - T_{co,\min} + T_{skew,CLK} + T_{skew,PCB} + T_{skew,SKT}$
		$T_{flight,\max} \leq T_{cycle} - T_{co,\max} - T_{su} - T_{skew,CLK} - T_{skew,PCB} - T_{skew,SKT} - T_{jit} - T_{adj}$

The terms used in the equations are described below.

Table 2-5. Intel® Celeron™ Processor and Intel® 440LX AGPset System Timing Terms

Term	Description
T_{cycle}	System cycle time, defined as the reciprocal of the frequency
$T_{flight,min}$	Minimum system flight time.
$T_{flight,max}$	Maximum system flight time.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
T_{su}	Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock.
T_{h}	Minimum hold time. Defined as the time for which the input data must remain valid after the input clock.
$T_{skew,CLK}$	Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator.
$T_{skew,PCB}$	PCB skew. Defined as the maximum delay variation between clock signals due to system board variation and Intel® 440LX AGPset loading variation.
$T_{skew,SKT}$	Skew due to delay in the 370-pin socket.
T_{jit}	Clock jitter. Defined as the maximum edge to edge variation in a given clock signal.
T_{adj}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.

Component timings for the Intel® Celeron™ processor are available in the *Intel® Celeron™ Processor* Datasheet.

Recommended values for system timings are contained in Table 2-6. Skew and jitter values for the clock generator device come from the clock driver vendor's datasheet. The PCB skew spec is based on the results of extensive simulations at Intel. The T_{adj} value is based on Intel's experience with systems that use the Intel® Pentium® Pro and Intel® Pentium® II processors.

Table 2-6. Recommended 66 MHz System Timing Parameters

Timing Term	Value
$T_{skew,CLK}$ [ns]	0.00
$T_{skew,SKT}$ [ns]	0.05
$T_{skew,PCB}$ [ns]	0.25
T_{jit} [ns]	0.30
T_{adj} [ns]	0.30

The flight time requirements that result from using the component timing specifications and recommended system timings are summarized in Table 2-3. All component values should be verified against the latest specifications before proceeding with analysis. These include a 2.57ns margin for processor to Intel® 440LX AGPset setup and 0.80ns margin for Intel® 440LX AGPset to processor setup.

2.8 82443LX Layout and Routing Guidelines

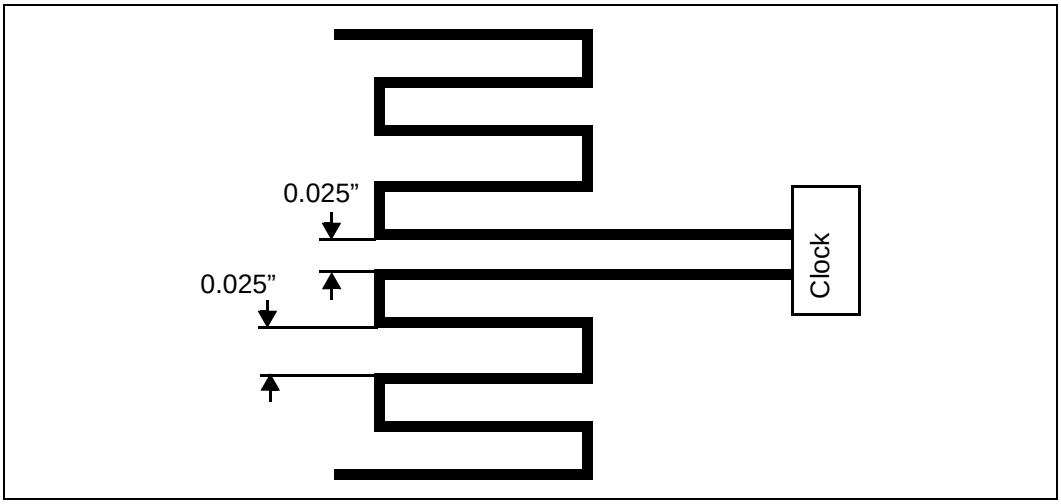
2.8.1 82443LX Clock Layout Recommendations

2.8.1.1 Clock Routing Spacing

The Intel® Celeron™ / Intel® 440LX AGPset platform requires a clock synthesizer for supplying 66 MHz system bus clocks, PCI clocks, APIC clocks, SDRAM clocks and 14 MHz clocks.

To minimize the impact of crosstalk, a minimum of 0.025" spacing should be maintained between the clock traces and other traces. A minimum spacing of 0.025" is also recommended for serpentines.

Figure 2-7. Clock Trace Spacing Guidelines



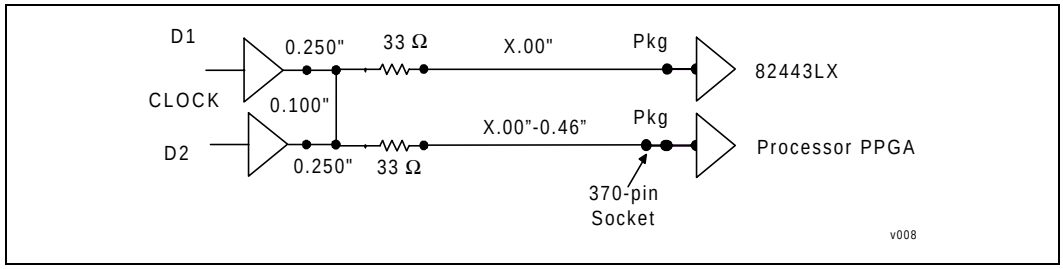
2.8.1.2 System Clock Layout

Series Termination: 33 Ohm series termination should be used for all system clocks. Clock skew between the 82443LX and the CPU can be reduced by tying the clock driver pins together at the clock chip and driving the CPU and LX. The connection should be at a maximum distance of 0.250” from each driver and be 0.100” long. Trace lengths should match the recommendations defined below (See Figure 2-8) Additionally, the max trace length should not exceed 9.0”.

Layout guidelines: Match trace lengths to the longest trace.

Net	Trace length
Clock chip - CPU Socket	X - 0.46”
Clock chip - 82443LX	X

Figure 2-8. Host Clock Topology



2.8.1.3 Other Busses

Busses not mentioned in the previous sections should adhere to the recommendations set forth in the *Pentium® II Processor/ Intel® 440LX AGPset Design Guide* document.

3

Design Checklist

Design Checklist 3

3.1 Overview

The following checklist is intended to be used for schematic reviews of Intel® 440LX AGPset desktop designs. It will be revised as new information is available.

3.2 Pull-up and Pull-down Resistor Values

Pull-up and pull-down values are system dependent. The appropriate value for your system can be determined from an AC/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Engineering judgment should be used to determine the optimal value. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, overshoot/undershoot, and other considerations.

A simplistic DC calculation for a pull-up value is:

$$R_{MAX} = (Vcc_{PU}\ MIN - V_{IH}\ MIN) / I_{Leakage}\ MAX$$

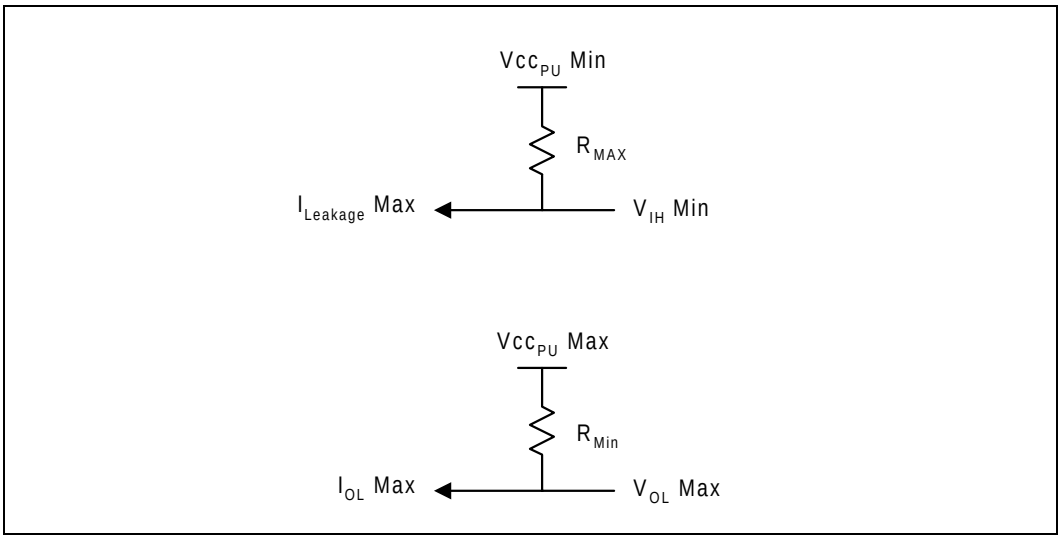
$$R_{MIN} = (Vcc_{PU}\ MAX - V_{OL}\ MAX) / I_{OL}\ MAX$$

Since $I_{Leakage}$ MAX is normally very small, R_{MAX} may not be meaningful. R_{MAX} is also determined by the maximum allowable rise time. The following calculation allows for t, the maximum allowable rise time, and C, the total load capacitance in the circuit, including input capacitance of the devices to be driven, output capacitance of the driver, and line capacitance. This calculation yields the largest pull-up resistor allowable to meet the rise time t.

$$R_{MAX} = -t / (C * \ln(1 - (V_{IH}\ MIN / Vcc_{PU}\ MIN)))$$

It is recommended that a SPICE or equivalent simulation be run to determine the proper values.

Figure 3-1. Pull-up Resistor Example



3.3 Processor Checklist

3.3.1 Intel® Celeron™ Processor

Table 3-1. AGTL+ Connectivity (Sheet 1 of 2)

CPU Pin	Pin Connection
A[31:3]	Terminate to Vtt / Connect to 82443LX PAC
ADS#	Terminate to Vtt / Connect to 82443LX PAC
BNR#	Terminate to Vtt / Connect to 82443LX PAC
BP[3:2]#	Leave as NO CONNECT Optional Debug: If used terminate to Vtt
BPM[1:0]	Leave as NO CONNECT Optional Debug: If used terminate to Vtt
BPRI#	Terminate to Vtt / Connect to 82443LX PAC
BR[0]#	Terminate to Vtt / Connect to 82443LX PAC Pin BREQ# Optional connect to ground with 10-450 ohm resistor
D[63:0]#	Terminate to Vtt / Connect to 82443LX PAC
DBSY#	Terminate to Vtt / Connect to 82443LX PAC
DEFER#	Terminate to Vtt / Connect to 82443LX PAC
DRDY#	Terminate to Vtt / Connect to 82443LX PAC
HIT#	Terminate to Vtt / Connect to 82443LX PAC
HITM#	Terminate to Vtt / Connect to 82443LX PAC
LOCK#	Terminate to Vtt / Connect to 82443LX PAC

Table 3-1. AGTL+ Connectivity (Sheet 2 of 2)

CPU Pin	Pin Connection
PRDY#	Leave as NO CONNECT Optional Debug: Terminate to Vtt / 240 ohm series resistor to ITP connector
REQ[4:0]#	Terminate to Vtt / Connect to 82443LX PAC
RESET#	Terminate to Vtt / Connect to 82443LX PAC, Optional Debug: 240 ohm series resistor to ITP connector
RS[2:0]#	Terminate to Vtt / Connect to 82443LX PAC
TRDY#	Terminate to Vtt / Connect to 82443LX PAC

Table 3-2. CMOS Connectivity

CPU Pin	Pin Connection
A20M#	300 ohm -330 ohm pull-up to $VCC_{CMOS.}$ Connect to PIIX4E.
BSEL	Connect to Ground
FERR#	Pull-up to VCC_{CMOS} with 150-10K ohm and Connect to PIIX4E
FLUSH#	Leave as NO CONNECT
IERR#	Leave as NO CONNECT Optional Pullup to VCC_{CMOS} with calculated Rmin - Rmax and connect to error logic
IGNNE#	Pull-up to VCC_{CMOS} with 330 ohm resistor. Connect to PIIX4E.
INIT#	Pull-up to VCC_{CMOS} with 330 ohm resistor. Connect to PIIX4E.
LINT[1:0]	Pull-up to VCC_{CMOS} with 330 ohm resistor. Connect to PIIX4E.
PICD[1:0]	Pull-up to VCC_{CMOS} with 150 ohm resistor.
PREQ#	Pull up to VCC_{CMOS} with 330 ohm resistor. Optional debug: connect to ITP.
PWRGOOD	Pull-up to VCC_{CMOS} with 330 ohm resistor. Connect to power sense logic.
SLP#	Pull-up to VCC_{CMOS} with 330 ohm resistor. Connect to PIIX4E.
SMI#	Pull-up to VCC_{CMOS} with 430 ohm resistor. Connect to PIIX4E.
STPCLK#	Pull-up to VCC_{CMOS} with 430 ohm resistor. Connect to PIIX4E.
THERMTRIP#	NO CONNECT. Optional: pull-up to VCC_{CMOS} with calculated Rmin - Rmax and connect to error logic.

Table 3-3. TAP Connectivity (optional[1])

CPU Pin	Pin Connection
TCK	1K ohm pull-up to VCC_{CMOS}. 47 ohm series resistor to processor.
TDO	Connected to ITP/processor. 150 ohm pull-up to VCC_{CMOS}.
TDI	Connected to ITP/processor. 150 ohm pull-up to VCC_{CMOS}.
TMS	1K ohm pull-up to VCC_{CMOS}. 47 ohm series resistor to processor.
TRST#	Connect to ITP/processor. 680 ohm pull-down.

NOTES:
1. If not used, connect TCK, TDI, TMS, and TRST# to valid logic level; do not leave floating.

Table 3-4. Miscellaneous Connectivity

CPU Pin	Pin Connection
BCLK	Connect to CK3D. Gang with PAC HCLK, 33 ohm series resistor
CPUPRES#	Tie to GND. Optionally pullup for external system management logic.
EDGCTRL	Pullup to VCC_{CORE} with 51 ohm +/- 5% resistor
PICCLK	Connect to CK3D. 33 ohm series resistor.
PLL1 & PLL2	See Section 4.7.4 for Inductor and capacitor values
THERMDN	NO CONNECT if not used
THERMDP	NO CONNECT if not used
$VCC_{1.5}$	Leave as NO CONNECT
$VCC_{2.5}$	Connect to 2.5 volt supply
VCC_{CMOS}	Use for system CMOS pullup voltage. Provide 0.1uF decoupling
VCC_{CORE}	Connect to VRM output/ Decoupling Guidelines: 10 each (min) 4.7uF in 1206 package / 19 each (min) 1.0 uF in 0805 package
VID[3:0]	10K ohm pull-up to 5V; connect to VRM.
VID[4]	Not on processor. Connect VRM controller pin to ground
V_{REF}[7:0]	Connect to V_{REF} voltage divider made up of 75 and 150 ohm 1% resistors connected to Vtt / Decoupling Guidelines: 4 ea. (min) 0.1uF in 0603 package
Vss	Tie to GND
Vtt	Decoupling Guidelines: 14 each (min) 0.1 uF in 0603 package
Reserved	Leave as NO CONNECT.

3.3.2 GND & Power Pin Definition

Refer to the *Intel® Celeron™ Processor* Datasheet and 440LX datasheet for this information.

3.3.3 Processor Clocks

- PICCLK must be driven by a clock even if an I/O APIC is not being used. This clock can be as high as 33.3 MHz in a UP system.

3.3.4 Processor Signals

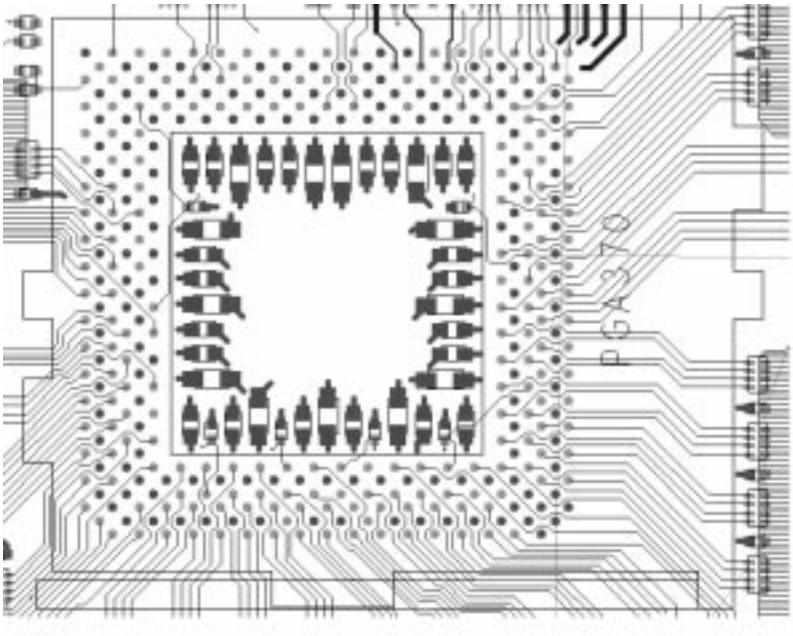
- THERMTRIP# must be pulled-up to VCC_{CMOS} (150 ohm to 10K ohm) if used by system logic. The signal may be wire-OR'ed and does not require an external gate. It may be left as NO CONNECT if it is not used.
- The FERR# output must be pulled up to VCC_{CMOS} (150 ohm to 10K ohm) and connected to the PIIX4E. Please see the reference schematics.
- PICD[1:0]# must have 150 ohm pull-ups to VCC_{CMOS} even if an I/O APIC is not being used.
- All CMOS inputs should be pulled up to VCC_{CMOS} with appropriate resistor value.
- Be sure the processor inputs are not being driven by 3.3V or 5V logic. Logic translation of 3.3V or 5V signals may be accomplished by using open-drain drivers pulled-up to Vcc_{CMOS}.
- The PWRGOOD input should be driven to the appropriate level from the active-high "AND" of the Power-Good signals from the 5V, 3.3V and Vcc_{CORE} supplies. The output of any logic used to drive PWRGOOD should be a $Vcc_{2.5}$ level to the processor.
- V_{REF} should be generated for the processor. Intel recommends using a 75 and 150 1% ohm divider with Vtt for generating V_{REF}. V_{REF} is not locally generated on the processor.
- Vtt must have adequate bulk decoupling based on the reaction time of the regulator used to generate Vtt. It must provide for a current ramp of up to 8A/µS while maintaining the voltage tolerance defined in the *Intel® Celeron™ Processor* Datasheet. In addition, Vtt must have adequate high frequency decoupling on the system board. See decoupling guidelines.
- If an on board voltage regulator is used instead of a VRM, Vcc_{CORE} must have adequate bulk decoupling based on the reaction time of the regulator used to generate Vcc_{CORE}. It must provide for a current ramp of up to 240A/µS while maintaining the VRM 8.2 DC-DC Converter Specification.
- The VID lines should have pull-up resistors on them ONLY if they are required by the Voltage Regulator Module or on board regulator that you have chosen. The pull-up voltage used should be to the regulator input voltage (5V or 12V), however, if 12V is used, a resistor divider should be utilized to lower the VID signal to CMOS/TTL levels. A pull-up is not required unless the VID signals are used by other logic requiring CMOS/TTL logic levels. The VID lines on the processor are 5V tolerant.
- The JTAG port must be properly terminated even if it is not used.
- TRST# must be driven low during reset to all components with TRST# pins. Connecting a pull-down resistor to TRST# will accomplish the reset of the port. See figures in the Integration Tools chapter of the *Pentium® II processor Developer's Manual (order number 243502)*.
- A single V_{TT} regulator may be used. A simplistic, single ended termination, calculation for maximum worst case current is 3.6A. This takes into consideration that some signals are not used by the Intel® 440LX AGPset.
- Motherboards planning to support the boxed processor must provide a matched power header for the boxed processor fan/heatsink power cable connector. Consult the *Intel® Celeron™ Processor* Datasheet for specifications of the fan power cable connector. The power header must be positioned within close proximity to the 370-pin socket.
- The CPUPRES# signal is a ground on the processor. The presence of a CPU core can be determined with this pin if it is pulled up on the system board. If not used, connect to ground to provide additional support to the processor.
- DBRESET (ITP Reset signal) requires a 240 ohm pull-up to VCC3.
- The system board should connect BR0# of the processor to the 82443LX's BREQ0# signal. This will assign an agent ID of 0 to the processor. Optionally, this signal may be grounded at the processor with a 10-450 ohm resistor.

3.3.5 Processor Decoupling Capacitors

3.3.5.1 Core Voltage High Frequency Decoupling

- Intel recommends ten or more 4.7 uF in a 1206 package, nineteen or more 1.0 uF in a 0805 package. All capacitors should be placed within the socket cavity and mounted directly on the primary side of the motherboard. The capacitors should be arranged to minimize the overall inductance between Vcc/Vss power pins (See Figure 3-2). These recommendations are adequate for Future Intel Celeron processors with Vcc_{CORE} of 2.0V, and Icc_{CORE} of 0.8 amps to 15.2 amps.

Figure 3-2. Capacitor Placement Study



- Contact your regulator vendor for bulk decoupling recommendations that will meet the *VRM 8.2 DC-DC Converter Guidelines.*
- Decoupling capacitor traces should be as short and wide as possible.
- The VRM 8.2 regulator 8.2-4 provides the Flexible Motherboard guidelines for processor voltage and current.

3.4 Thermals / Cooling Solutions

- For the Intel® Celeron™ processor, an adequate heat sink and air ventilation must be provided to ensure that the T_{CASE} specification documented in the *Intel® Celeron™ Processor* Datasheet is met. Please see the *Pentium® II Processor Power Distribution Guidelines*, and *Pentium II Processor Thermal Design Guidelines* for thermal design information.
- The Flexible Motherboard guidelines for processor power dissipation is 30 W.
- Verify that all major components, including the 82443LX can be cooled the way they are placed.

3.4.1 Design Considerations:

- Could anything block the air flow to or from the processor (I/O cards, VRM etc.)?
- Is there anything between the processor and the air intake that may preheat the air flowing into the fan/heatsink?
- If a system fan (other than the power supply fan) is used, have all recirculation paths been eliminated?
- What is the air flow through the PSU/system fan?
- What is the maximum ambient operation temperature of the system?

3.5 Mechanicals

- For the processor: The physical space requirements of the processor must be met. See the *Intel® Celeron™ Processor* Datasheet for details. In addition the physical space requirements of your heat sink must be met.
- For the boxed processor: The physical space requirements of the boxed processor fan/heatsink must be met. See the *Intel® Celeron™ Processor* Datasheet for details.

3.6 Electricals

3.6.1 Design Considerations

- It is recommended that simulations be performed on the AGTL+ bus to ensure that proper bus timings and signal integrity are met, especially if the layout guideline recommendations in this document are not followed.
- It is recommended that simulations be performed to ensure proper timings and signal integrity is met, especially if the non AGTL+ (CMOS) layout guideline recommendations in this document are not followed.
- Verify the voltage range and tolerance of your VRM or onboard regulator adequately cover the Vcc_{CORE} requirements of the processor is supported.
- Verify the maximum current value your VRM or on-board regulator can support at $Vcc_{CORE.}$ This should meet the value specified by the *VRM 8.2 DC-DC Converter Guidelines*.
- Verify the voltage tolerance of your VRM or on board regulator at $Vcc_{CORE.}$ This should meet the value specified by the *VRM 8.2 DC-DC Converter Guidelines*.
- Adequate 5V and/or 3.3V decoupling should be provided for all components.
- V_{REF} for the AGPset should be decoupled to V_{TT} with 0.001µF capacitors at each voltage divider. It should be decoupled to ground, to ensure an even better solution.
- It is recommended that AC/DC analysis be performed to determine proper pull-up and pull-down values.

4

Debug Recommendations

Debug Recommendations 4

This section provides tool and model information.

4.1 Debug/Simulation Tools

4.1.1 Logic Analyzer Interface (LAI)

Table 4-1. Third-Party LAIs & Logic Analyzer Software

Vendor	Phone Number/ Web address	Revision	Available	Price
Hewlett Packard Co.	1-800-452-4844 www.tmo.hp.com/tmo	Contact Vendor	Contact Vendor	Contact Vendor
American Arium	714-731-1661 www.arium.com	Contact Vendor	Contact Vendor	Contact Vendor
Tektronix Inc.	503-627-1922 www.tek.com/Measurement	Contact Vendor	Contact Vendor	Contact Vendor

Note: Contact the respective tool vendor for details. Certain products are available only under RS-NDA and license agreement. Contact your Intel Field Sales representative.

4.1.2 In-Target Probe (ITP)

The ITP32A provides a software debug capability allowing the setting/clearing of hardware/ software breakpoints, assembly/disassembly of code, display/modification of the processor register set, display/modification of system memory, display/modification of I/O space and includes a macro language for custom debug procedure creation, etc. Contact your local Field Sales representative for availability of this tool from Intel.

Table 4-2. Intel In-Target Probe (ITP) Debuggers

Part Number	Supported Processors	Revision	Available	Price
ITP32A	P6 family processors	1.5	Yes	Note 2
ITP32AUP	P6 family processors	1.5	Yes	Note 2
ITP565UPGFR560	P6 family processors	1.5	Yes	Note 2

NOTES:
1. For ITP technical support: Call 1-800-628-8686 and ask for help with an “XTG tool”.
2. Contact your local Intel Field Sales representative.

Table 4-3. Third-Party ITP-like Debuggers and Run Control Solutions

Tool Vendor	Phone Number/ Web address	Revision	Available	Price
American Arium	714-731-1661 www.arium.com	Contact Vendor	Contact Vendor	Contact Vendor
Hewlett-Packard Co.	1-800-452-4844 www.tmo.hp.com/tmo	Contact Vendor	Contact Vendor	Contact Vendor

NOTES:
1. Contact the respective tool vendor for details. Certain products are available only under RS-NDA and license agreement.

Contact your local Intel Field Sales representative to complete the proper software license agreement and non-disclosure agreement required to receive the ITP.

4.1.3 I/O Buffer Models

IBIS Models are available from Intel for:

1. Intel® Celeron™ Processor (PPGA) (QUAD only)
2. 82443LX IBIS Models
3. PIIX4E PCI ISA IDE Xcelerator IBIS Models

Contact your local Intel Field Sales representative for a copy of these models and to complete the appropriate non-disclosure agreements.

5

Third Party Vendors

Third-Party Vendor Information 5

This design guide has been compiled to give an overview of important design considerations while providing sources for additional information. This section refers to listings of various third-party vendors who provide products to support the Intel® Celeron™ Processor and Intel® 440LX AGPset. The lists of vendors can be used as a starting point for the designer. Intel does not endorse any one vendor, nor guarantee the availability or functionality of outside components. Contact the manufacturer for specific information regarding performance, availability, pricing, and compatibility.

5.1 Voltage Regulator Control Silicon

Intel's *Developer* web site lists vendors who offer DC-DC converter silicon and reference designs for Celeron processor voltage and current requirements per the *VRM 8.2 DC-DC Converter Design Guidelines*.

http://developer.intel.com/design/celeron/components/#POWER.

5.2 Clock Drivers

Intel's *Developer* web site lists vendors who offer clock drivers for the Celeron processor and Intel® 440LX AGPset.

http://developer.intel.com/design/celeron/components/#CLOCK.

5.3 370-Pin Socket

The *370-pin Socket Guidelines* document can be obtained from:

http://developer.intel.com/design/celeron/applnots/244410.htm

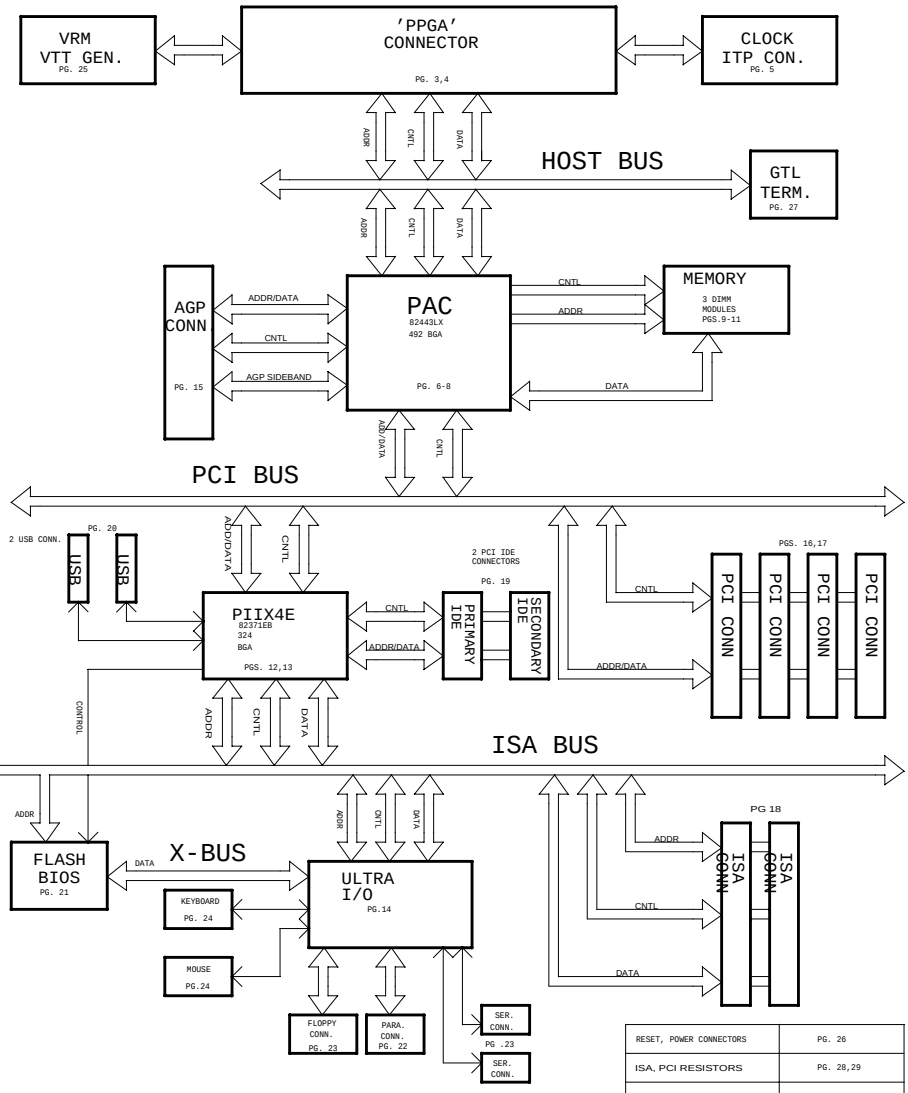
A

Reference Design Schematics

Intel(R) 440LX APGset PPGA REFERENCE DESIGN

INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: Cover Sheet		
Size: A	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 1 of 33	



RESET, POWER CONNECTORS	PG. 26
ISA, PCI RESISTORS	PG. 28,29
DECOUPLING CAPACITORS	PGS. 30-32

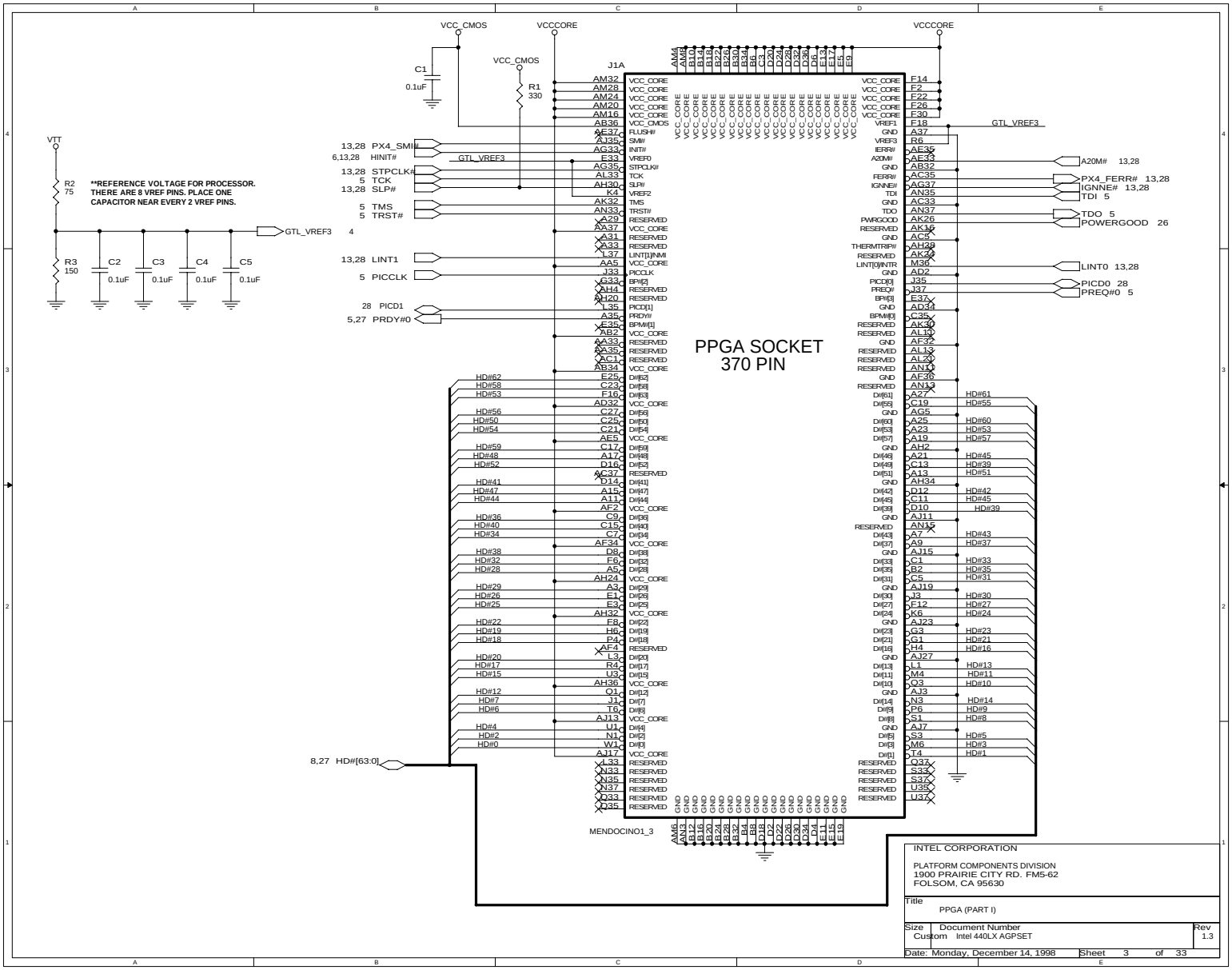
INTEL CORPORATION

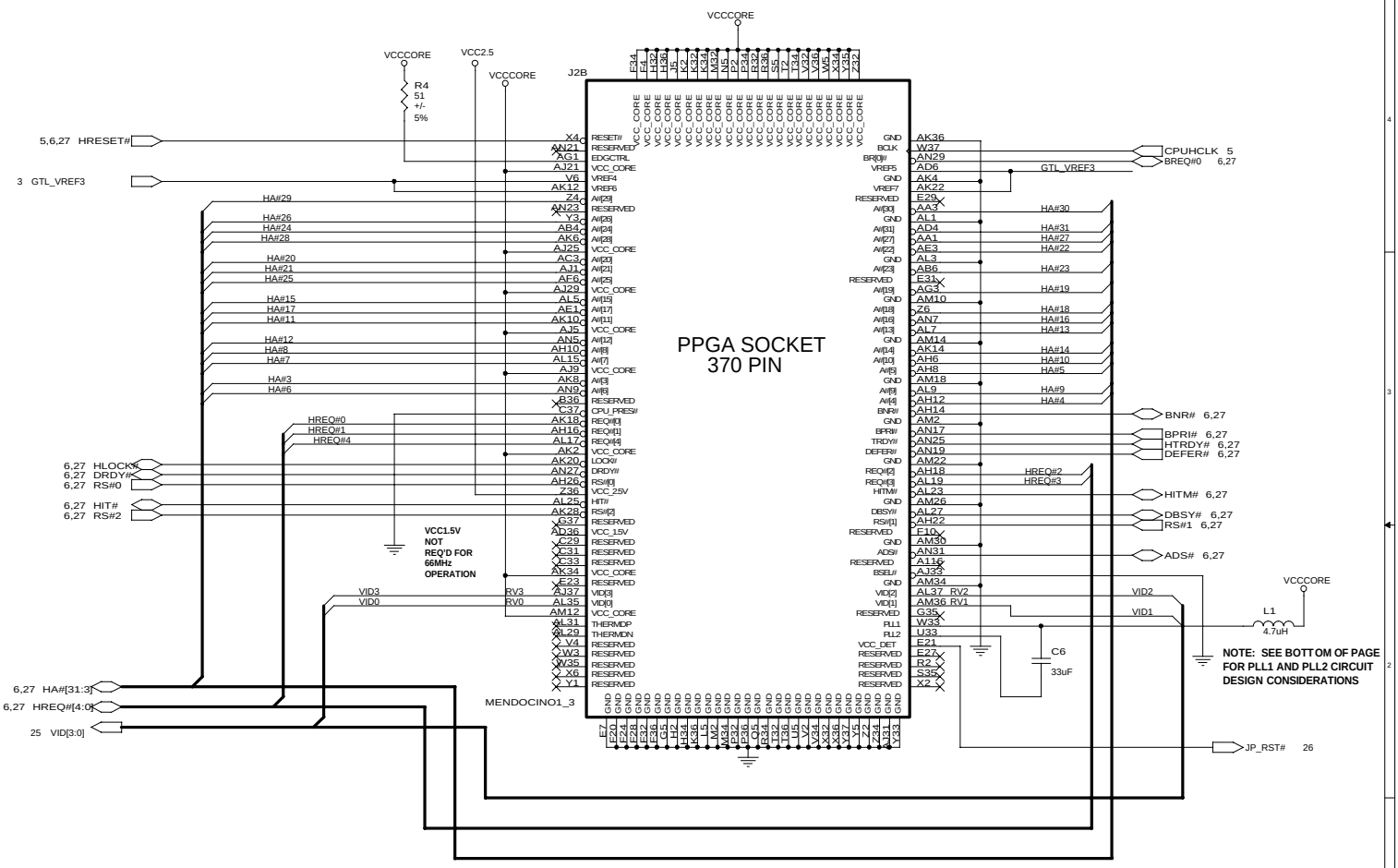
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title
Intel 440LX AGPset Block Diagram

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 Sheet 2 of 33


PPGA SOCKET
370 PIN
J1A
VCC_CMOS
VCCCORE
C1
0.1uF
R1
330
VTT
R2
75
R3
150
C2
C3
C4
C5
0.1uF
**REFERENCE VOLTAGE FOR PROCESSOR.
THERE ARE 8 VREF PINS. PLACE ONE
CAPACITOR NEAR EVERY 2 VREF PINS.
GTL_VREF3
13,28 PX4_SMI#
6,13,28 HINIT#
13,28 STPCLK#
5 TCK
13,28 SLP#
5 TMS
5 TRST#
13,28 LINT1
5 PICCLK
28 PICD1
5,27 PRDY#0
8,27 HD#[63:0]
MENDOCINO1_3
A20M# 13,28
PX4_FERR# 13,28
IGNNE# 13,28
TDI 5
TDO 5
POWERGOOD 26
LINT0 13,28
PICD0 28
PREQ#0 5
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
PPGA (PART I)
Size Custom
Document Number Intel 440LX AGPSET
Rev 1.3
Date: Monday, December 14, 1998
Sheet 3 of 33



NOTE:

PLL FILTER DESIGN CONSIDERATIONS:

TO SATISFY DAMPING REQUIREMENTS, TOTAL SERIES RESISTANCE IN THE FILTER MUST BE AT LEAST 0.6 OHM. THIS RESISTOR CAN BE IN THE FORM OF A DISCRETE COMPONENT, OR ROUTING, OR BOTH. MAXIMUM RESISTANCE OF 2 OHMS TOTAL MUST NOT BE EXCEEDED.

COMPONENT RECOMMENDATION FOR PLL FILTER - PLL1 / PLL2:

INDUCTOR:	CAPACITOR:
TDK MLF2012A4R7KT	KEMET
MURATA LQG21N4R7K00T1	T495D336M016AS
MURATA LQG21C4R7N00	AVX
	TPSD336M020S0200

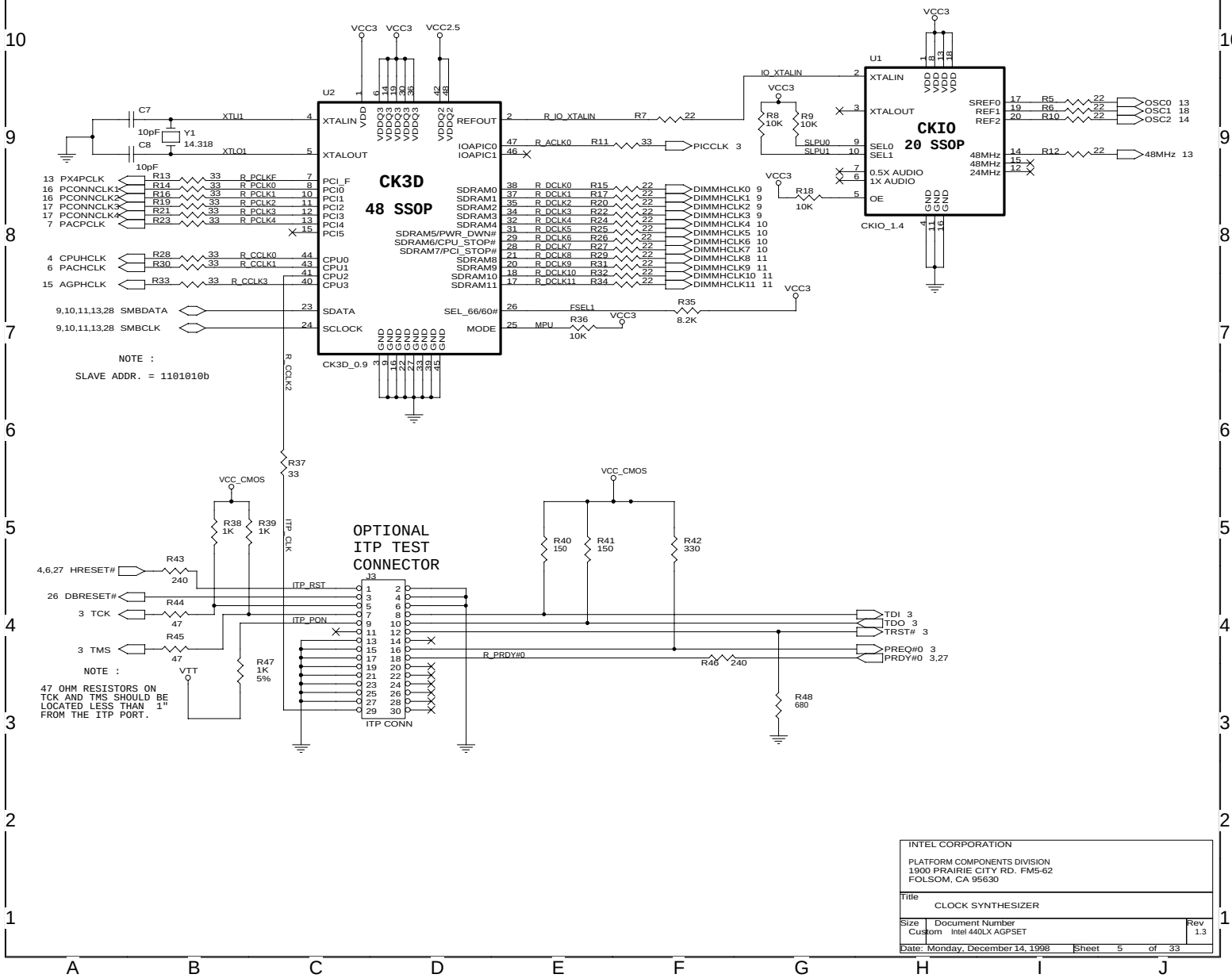
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

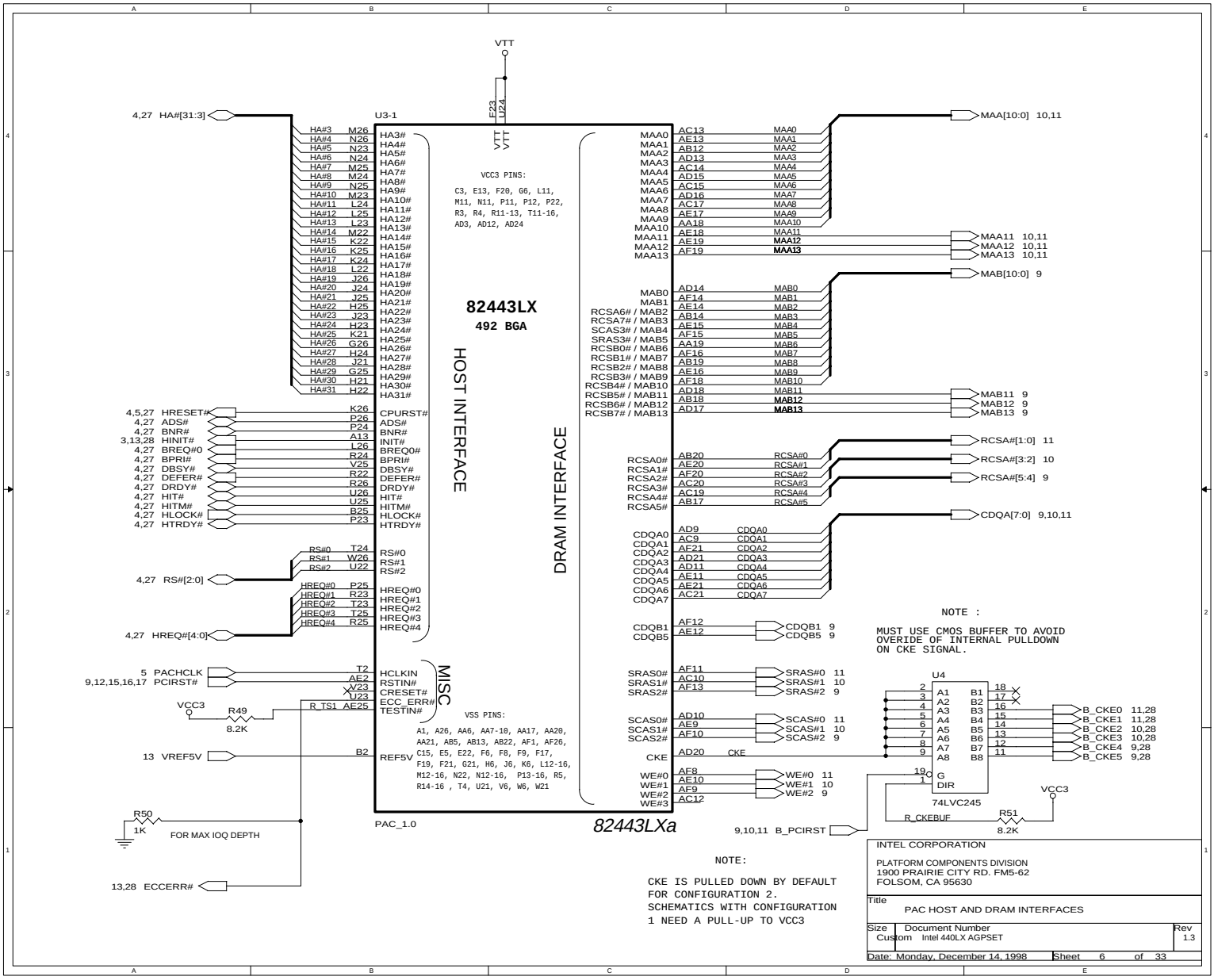
Title: PPGA (PART II)

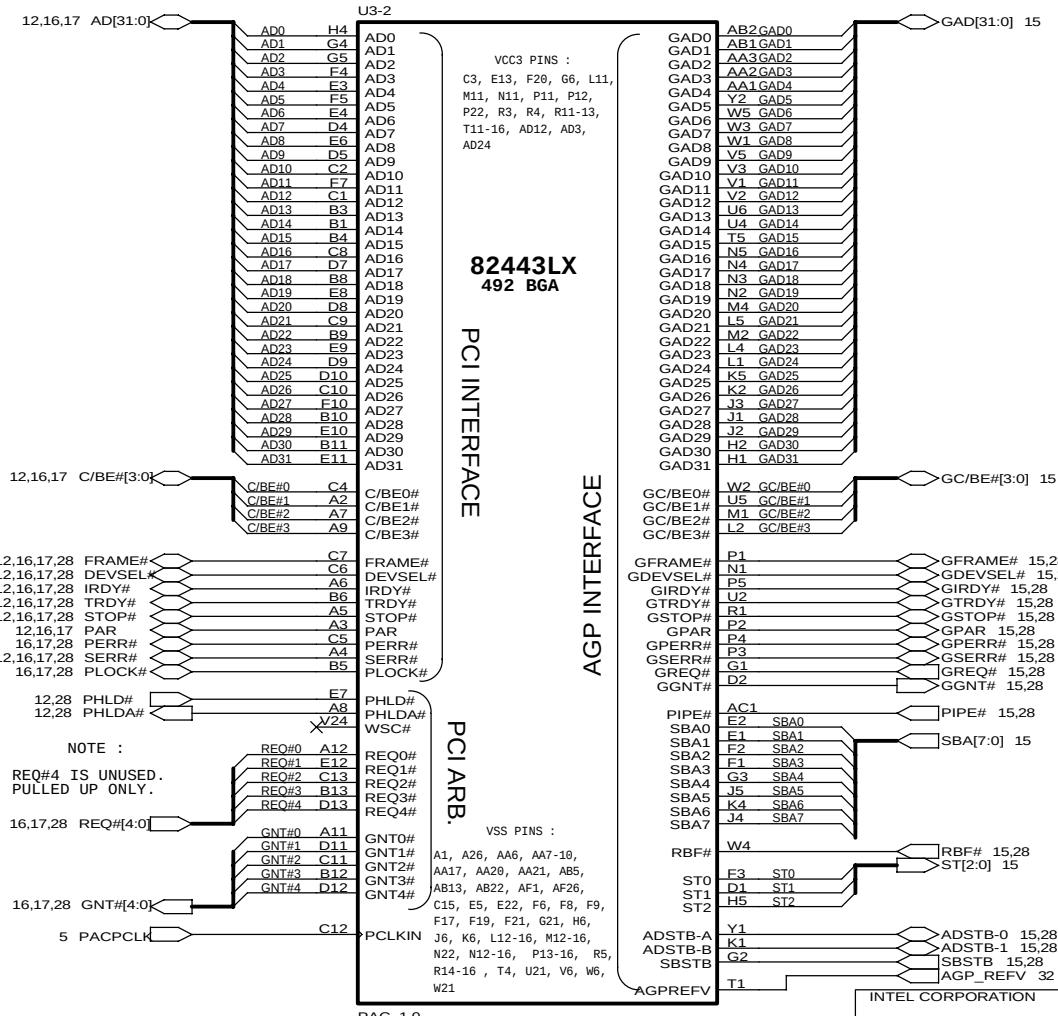
Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 Sheet 4 of 33



INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title	CLOCK SYNTHESIZER
Size: Custom	Document Number: Intel 440LX AGPSET
Rev	1.3
Date: Monday, December 14, 1998	Sheet 5 of 33


VTT
F23
U24
4,27 HA#[31:3]
U3-1
HA#3 M26
HA#4 N26
HA#5 N23
HA#6 N24
HA#7 M25
HA#8 M24
HA#9 N25
HA#10 M23
HA#11 L24
HA#12 L25
HA#13 L23
HA#14 M22
HA#15 K22
HA#16 K25
HA#17 K24
HA#18 L22
HA#19 J26
HA#20 J24
HA#21 J25
HA#22 H25
HA#23 J23
HA#24 H23
HA#25 K21
HA#26 G26
HA#27 H24
HA#28 J21
HA#29 G25
HA#30 H21
HA#31 H22
HA3# HA4# HA5# HA6# HA7# HA8# HA9# HA10# HA11# HA12# HA13# HA14# HA15# HA16# HA17# HA18# HA19# HA20# HA21# HA22# HA23# HA24# HA25# HA26# HA27# HA28# HA29# HA30# HA31#
VTT VTT
VCC3 PINS:
C3, E13, F20, G6, L11, M11, N11, P11, P12, P22, R3, R4, R11-13, T11-16, AD3, AD12, AD24
82443LX
492 BGA
HOST INTERFACE
DRAM INTERFACE
MISC
4,5,27 HRESET# K26 CPURST#
4,27 ADS# P26 ADS#
4,27 BNR# P24 BNR#
3,13,28 HINIT# A13 INIT#
4,27 BREQ#0 L26 BREQ0#
4,27 BPRI# R24 BPRI#
4,27 DBSY# V25 DBSY#
4,27 DEFER# R22 DEFER#
4,27 DRDY# R26 DRDY#
4,27 HIT# U26 HIT#
4,27 HITM# U25 HITM#
4,27 HLOCK# B25 HLOCK#
4,27 HTRDY# P23 HTRDY#
RS#0 T24 RS#0
RS#1 W26 RS#1
RS#2 U22 RS#2
4,27 RS#[2:0]
HREQ#0 P25 HREQ#0
HREQ#1 R23 HREQ#1
HREQ#2 T23 HREQ#2
HREQ#3 T25 HREQ#3
HREQ#4 R25 HREQ#4
4,27 HREQ#[4:0]
5 PACHCLK T2 HCLKIN
9,12,15,16,17 PCIRST# AE2 RSTIN#
V23 CRESET#
U23 ECC_ERR#
R_TS1 AE25 TESTIN#
VCC3
R49
8.2K
13 VREF5V B2 REF5V
R50
1K
FOR MAX IOQ DEPTH
13,28 ECCERR#
VSS PINS:
A1, A26, AA6, AA7-10, AA17, AA20, AA21, AB5, AB13, AB22, AF1, AF26, C15, E5, E22, F6, F8, F9, F17, F19, F21, G21, H6, J6, K6, L12-16, M12-16, N22, N12-16, P13-16, R5, R14-16 , T4, U21, V6, W6, W21
PAC_1.0
MAA0 AC13 MAA0
MAA1 AE13 MAA1
MAA2 AB12 MAA2
MAA3 AD13 MAA3
MAA4 AC14 MAA4
MAA5 AD15 MAA5
MAA6 AC15 MAA6
MAA7 AD16 MAA7
MAA8 AC17 MAA8
MAA9 AE17 MAA9
MAA10 AA18 MAA10
MAA11 AE18 MAA11
MAA12 AE19 MAA12
MAA13 AF19 MAA13
MAA[10:0] 10,11
MAA11 10,11
MAA12 10,11
MAA13 10,11
MAB0 AD14 MAB0
MAB1 AF14 MAB1
RCSA6# / MAB2 AE14 MAB2
RCSA7# / MAB3 AB14 MAB3
SCAS3# / MAB4 AE15 MAB4
SRAS3# / MAB5 AF15 MAB5
RCSB0# / MAB6 AA19 MAB6
RCSB1# / MAB7 AF16 MAB7
RCSB2# / MAB8 AB19 MAB8
RCSB3# / MAB9 AE16 MAB9
RCSB4# / MAB10 AF18 MAB10
RCSB5# / MAB11 AD18 MAB11
RCSB6# / MAB12 AB18 MAB12
RCSB7# / MAB13 AD17 MAB13
MAB[10:0] 9
MAB11 9
MAB12 9
MAB13 9
RCSA0# AB20 RCSA#0
RCSA1# AE20 RCSA#1
RCSA2# AF20 RCSA#2
RCSA3# AC20 RCSA#3
RCSA4# AB19 RCSA#4
RCSA5# AB17 RCSA#5
RCSA#[1:0] 11
RCSA#[3:2] 10
RCSA#[5:4] 9
CDQA0 AD9 CDQA0
CDQA1 AC9 CDQA1
CDQA2 AF21 CDQA2
CDQA3 AD21 CDQA3
CDQA4 AD11 CDQA4
CDQA5 AE11 CDQA5
CDQA6 AE21 CDQA6
CDQA7 AC21 CDQA7
CDQA[7:0] 9,10,11
CDQB1 AF12 CDQB1 9
CDQB5 AE12 CDQB5 9
NOTE :
MUST USE CMOS BUFFER TO AVOID OVERIDE OF INTERNAL PULLDOWN ON CKE SIGNAL.
SRAS0# AF11 SRAS#0 11
SRAS1# AC10 SRAS#1 10
SRAS2# AF13 SRAS#2 9
SCAS0# AD10 SCAS#0 11
SCAS1# AE9 SCAS#1 10
SCAS2# AF10 SCAS#2 9
CKE AD20 CKE
WE#0 AF8 WE#0 11
WE#1 AE10 WE#1 10
WE#2 AF9 WE#2 9
WE#3 AC12
U4
2 3 4 5 6 7 8 9
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
18 17 16 15 14 13 12 11
B_CKE0 11,28
B_CKE1 11,28
B_CKE2 10,28
B_CKE3 10,28
B_CKE4 9,28
B_CKE5 9,28
19 1
G DIR
74LVC245
VCC3
R_CKEBUF
R51
8.2K
9,10,11 B_PCIRST
NOTE:
CKE IS PULLED DOWN BY DEFAULT FOR CONFIGURATION 2. SCHEMATICS WITH CONFIGURATION 1 NEED A PULL-UP TO VCC3
82443LXa
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
PAC HOST AND DRAM INTERFACES
Size Custom
Document Number Intel 440LX AGPSET
Rev 1.3
Date: Monday, December 14, 1998
Sheet 6 of 33



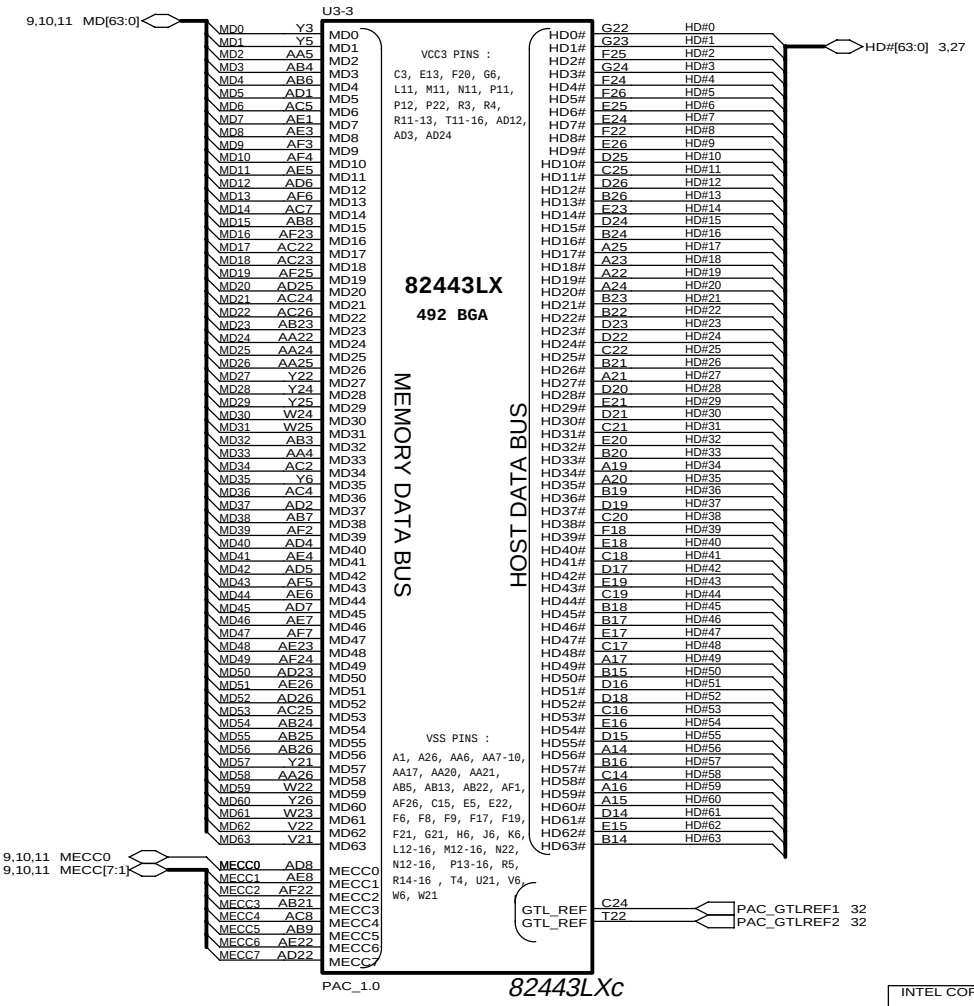
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title
PAC PCI AND AGP INTERFACES

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 7 of 33



INTEL CORPORATION

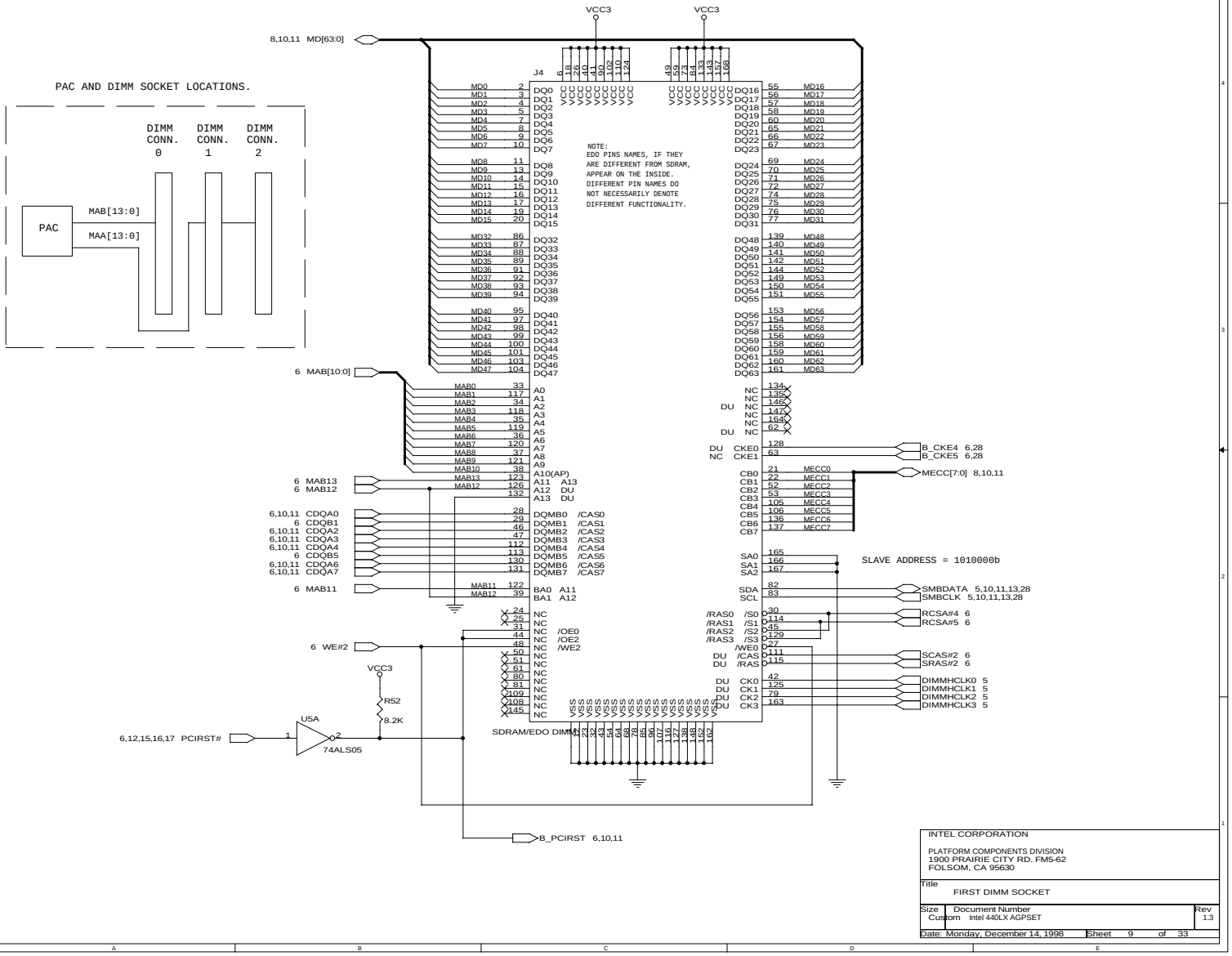
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: PAC DATA BUSES

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

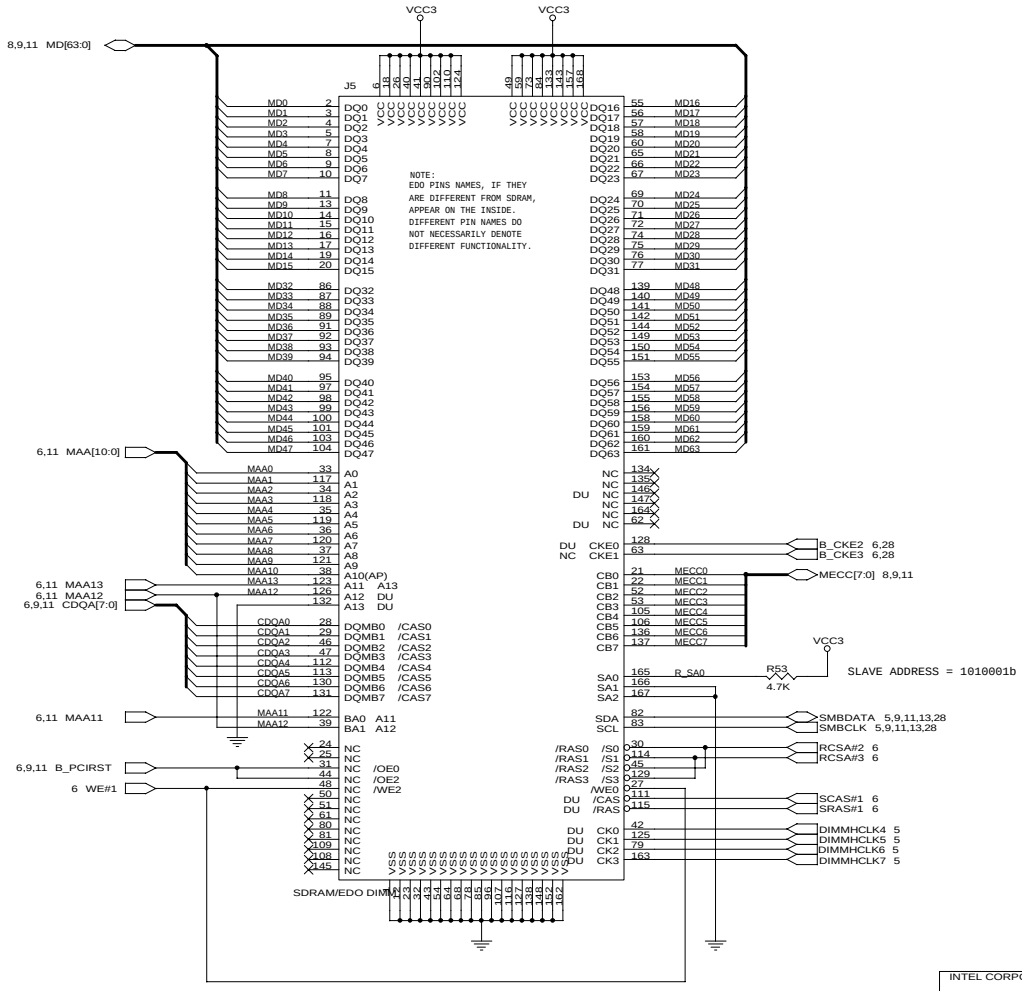
Date: Monday, December 14, 1998 Sheet 8 of 33

DIMM CONNECTOR 0



INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title: FIRST DIMM SOCKET	
Size: Custom — Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 9 of 33

DIMM CONNECTOR 1



INTEL CORPORATION

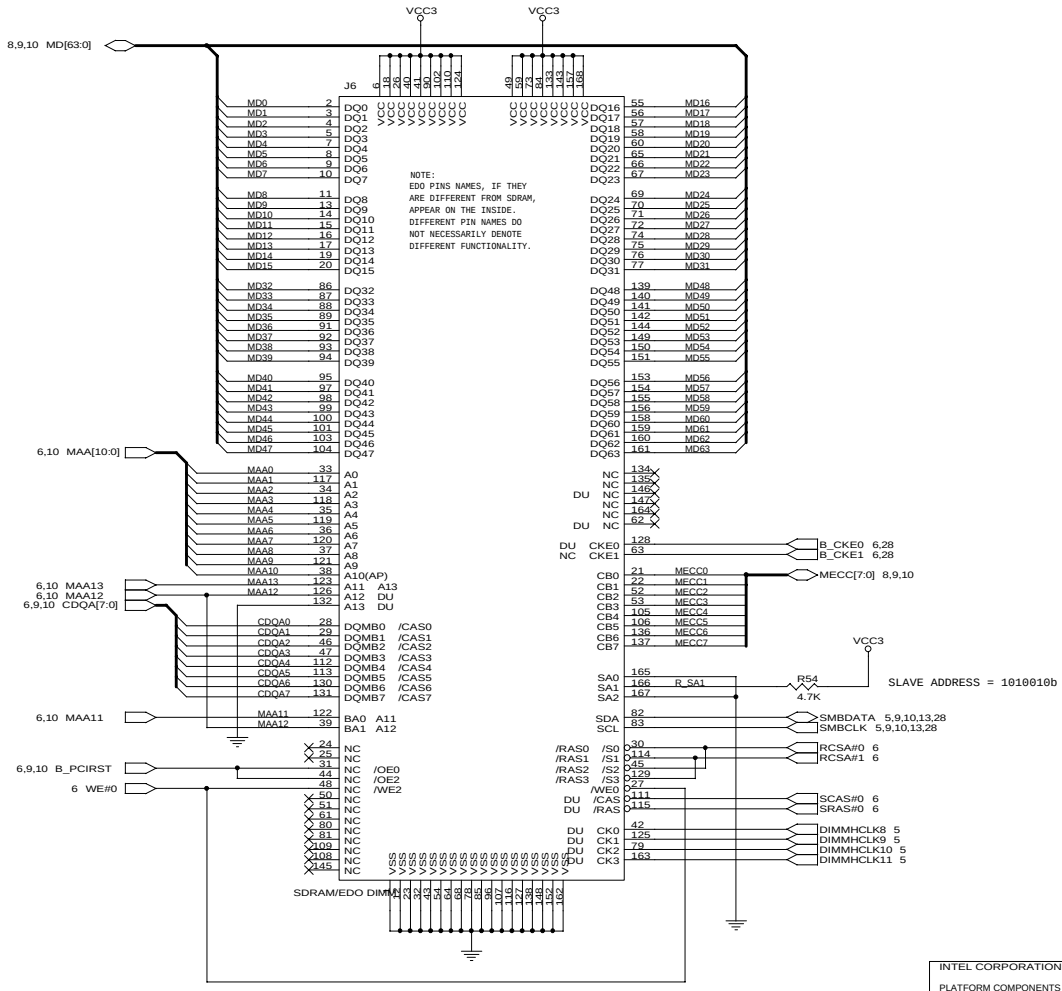
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: SECOND DIMM SOCKET

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 10 of 33

DIMM CONNECTOR 2



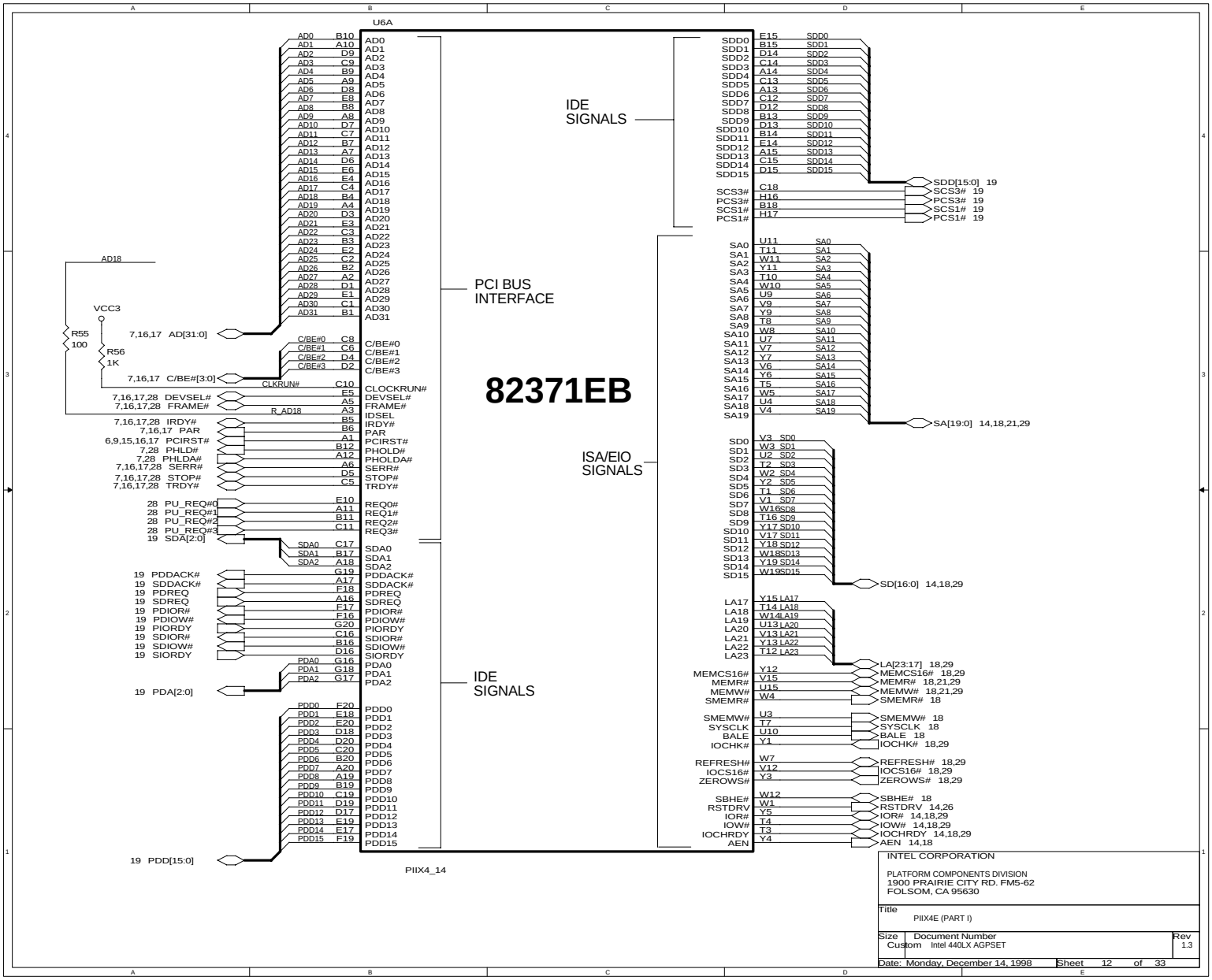
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FMS-62
FOLSOM, CA 95630

Title: THIRD DIMM SOCKET

Size: Custom | Document Number: Intel 440LX AGPSET | Rev: 1.3

Date: Monday, December 14, 1998 | Sheet 11 of 33



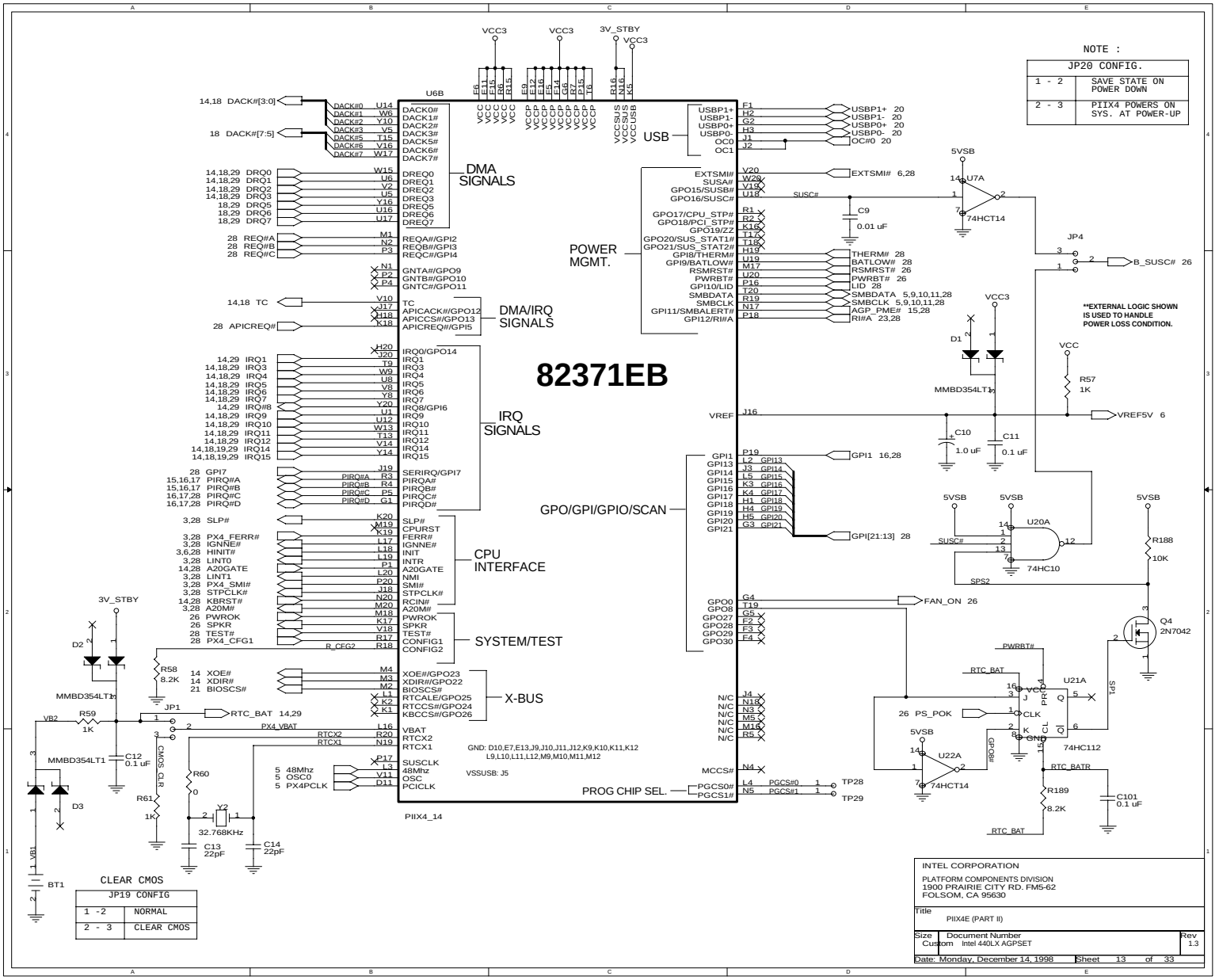
INTEL CORPORATION

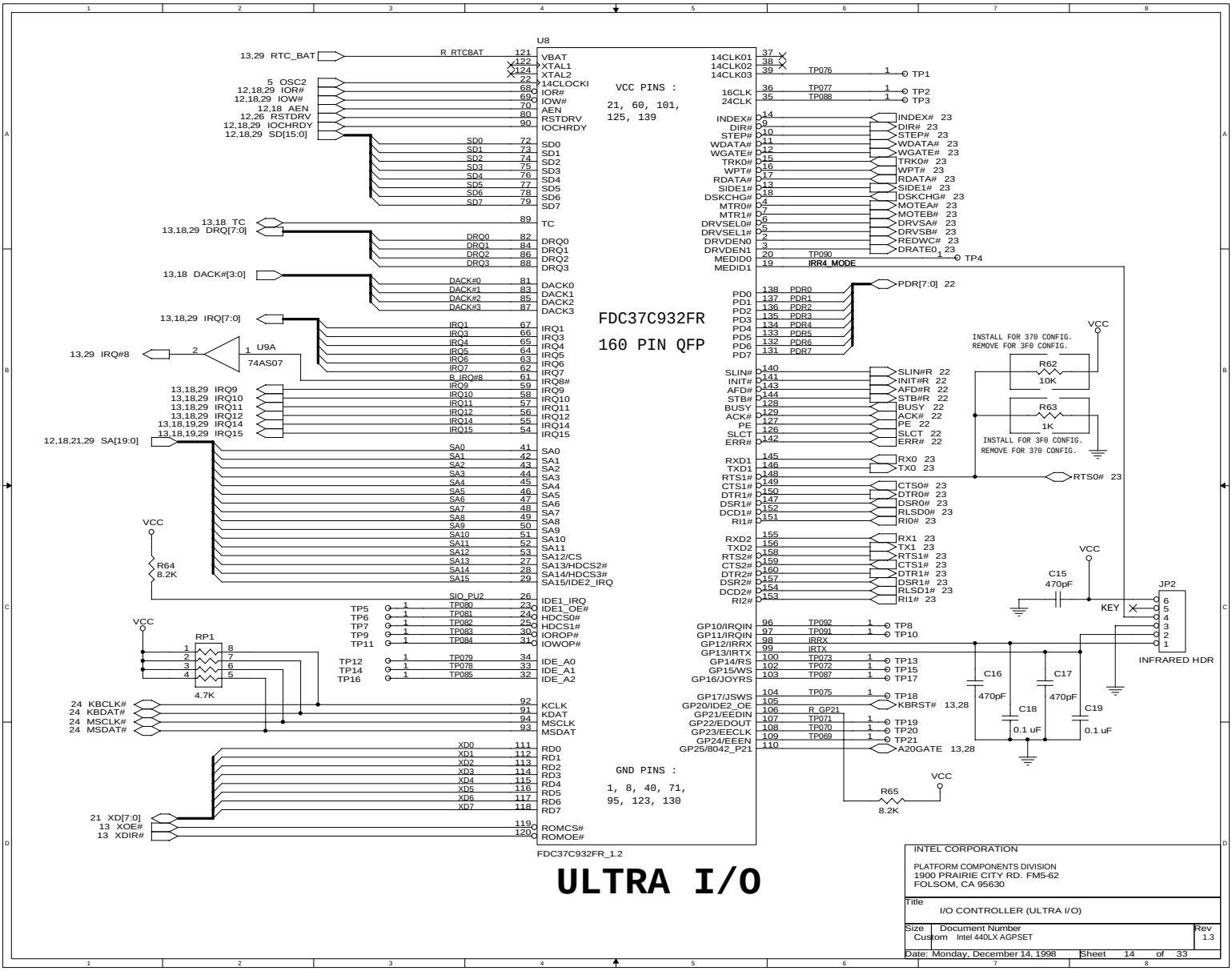
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: PIIX4E (PART I)

Size: Custom | Document Number: Intel 440LX AGPSET | Rev: 1.3

Date: Monday, December 14, 1998 | Sheet 12 of 33


82371EB
U6B
DMA SIGNALS
DMA/IRQ SIGNALS
IRQ SIGNALS
CPU INTERFACE
SYSTEM/TEST
X-BUS
USB
POWER MGMT.
GPO/GPI/GPIO/SCAN
PROG CHIP SEL.
NOTE :
JP20 CONFIG.
1 - 2 SAVE STATE ON POWER DOWN
2 - 3 PIIX4 POWERS ON SYS. AT POWER-UP
**EXTERNAL LOGIC SHOWN IS USED TO HANDLE POWER LOSS CONDITION.
CLEAR CMOS
JP19 CONFIG
1 -2 NORMAL
2 - 3 CLEAR CMOS
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
PIIX4E (PART II)
Size Custom
Document Number Intel 440LX AGPSET
Rev 1.3
Date: Monday, December 14, 1998
Sheet 13 of 33

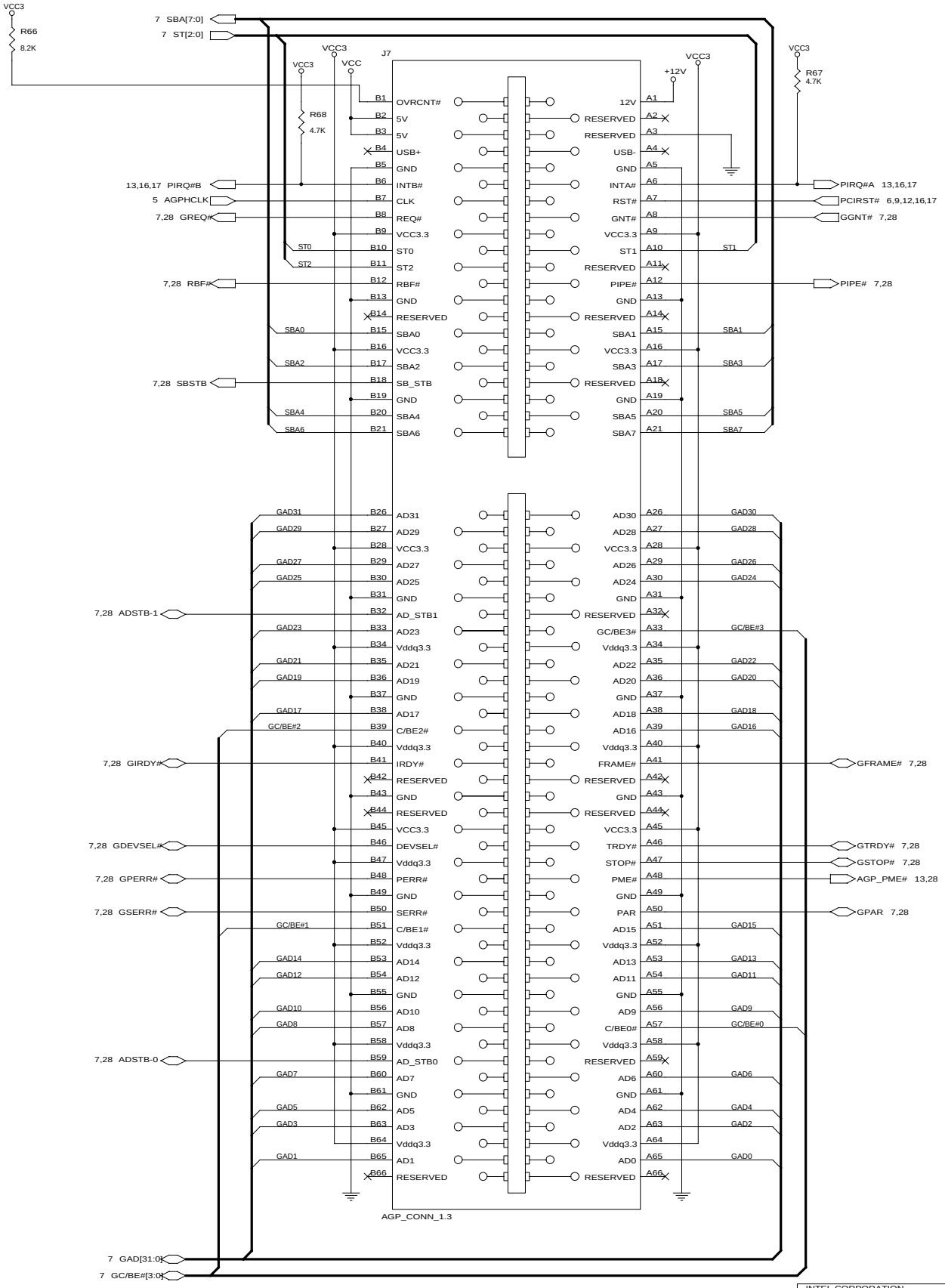


ULTRA I/O

INTEL CORPORATION

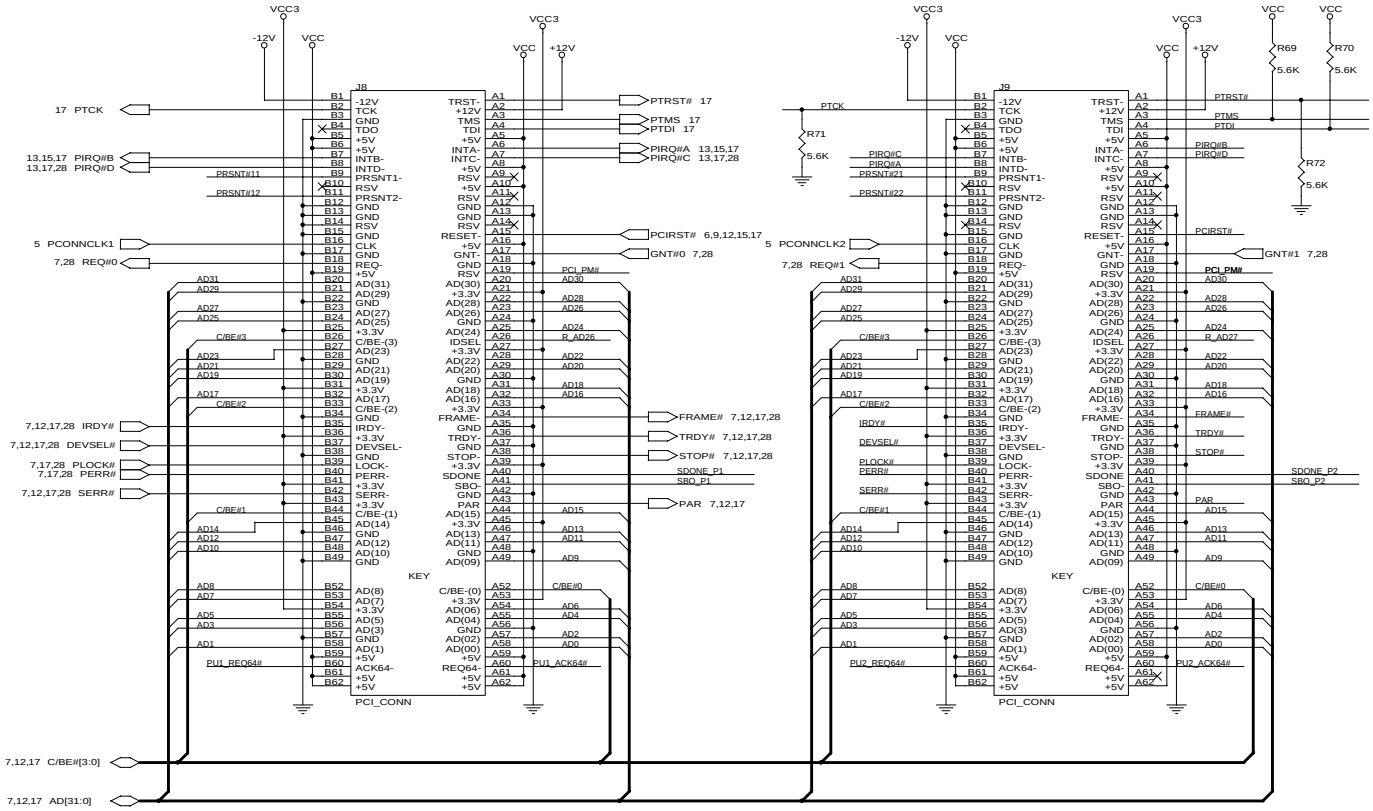
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

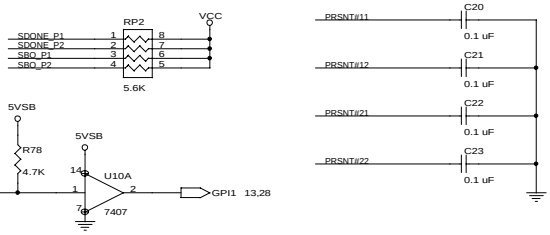
Title: I/O CONTROLLER (ULTRA I/O)		
Size: Custom	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 14 of 33	



INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title	ACCELERATED GRAPHICS PORT (AGP) CONNECTOR
Size: Custom	Document Number: Intel 440LX AGPSET
Rev	1.3
Date: Monday, December 14, 1998	Sheet 15 of 33

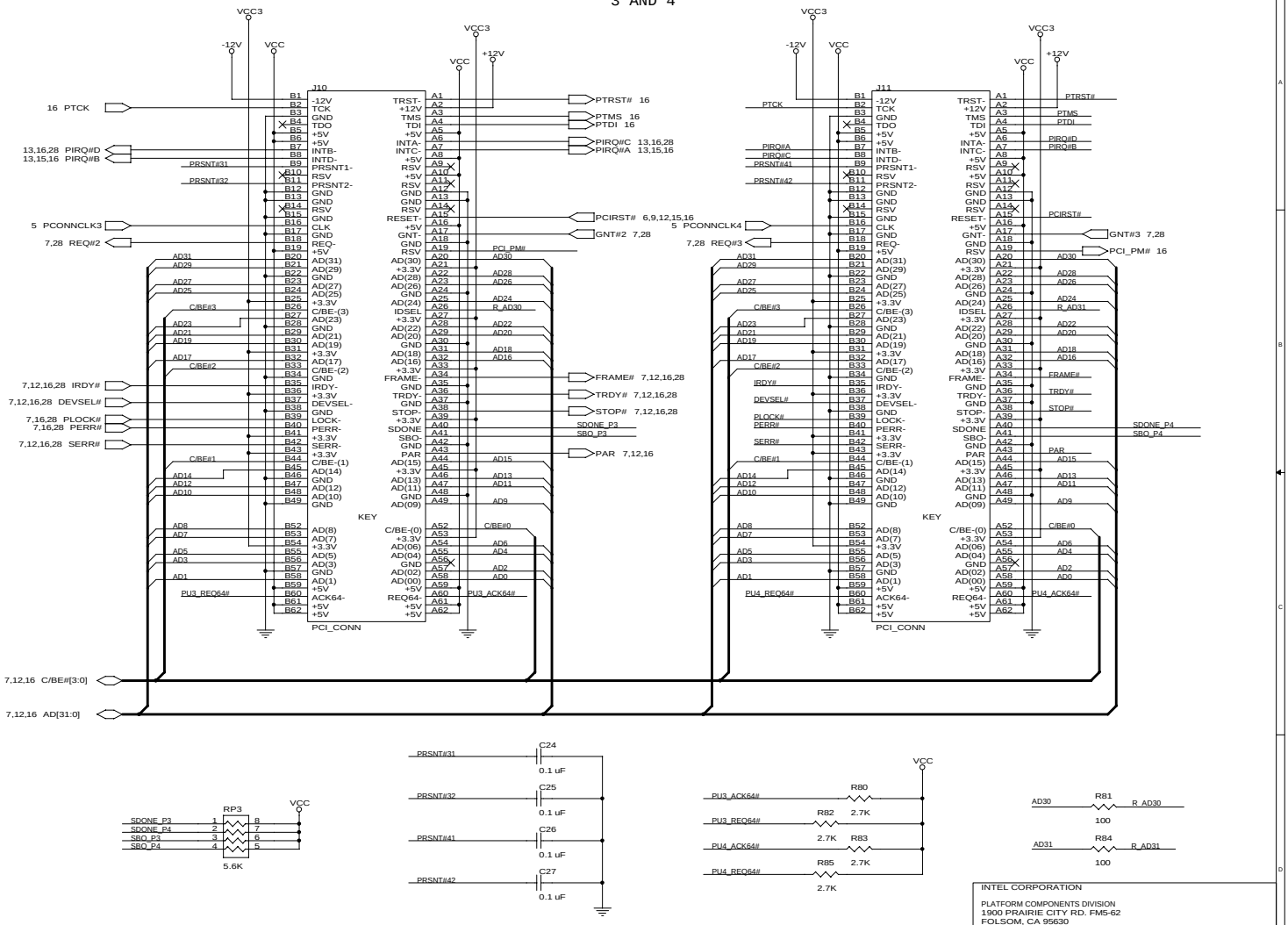
PCI CONNECTORS
1 AND 2





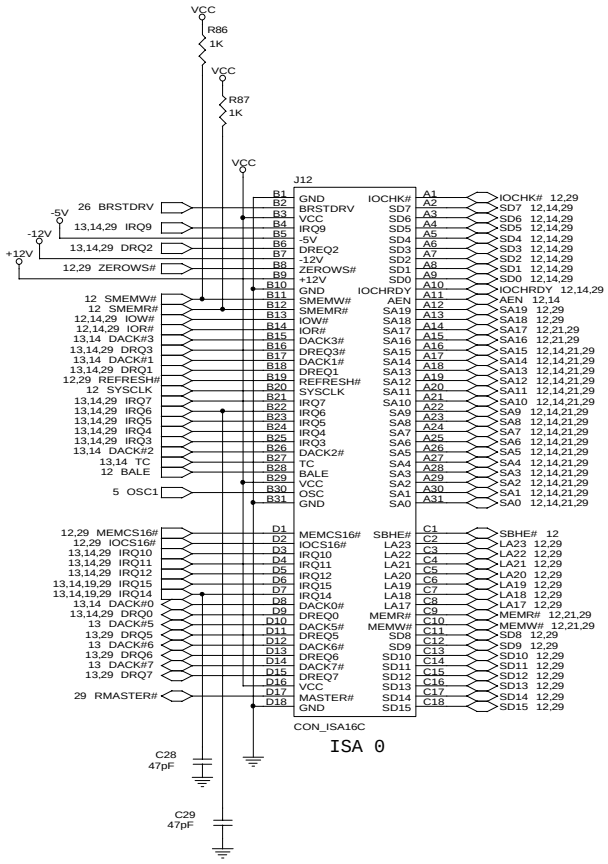
INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: PCI CONNECTORS 1 & 2		
Size: Custom	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 16 of 33	

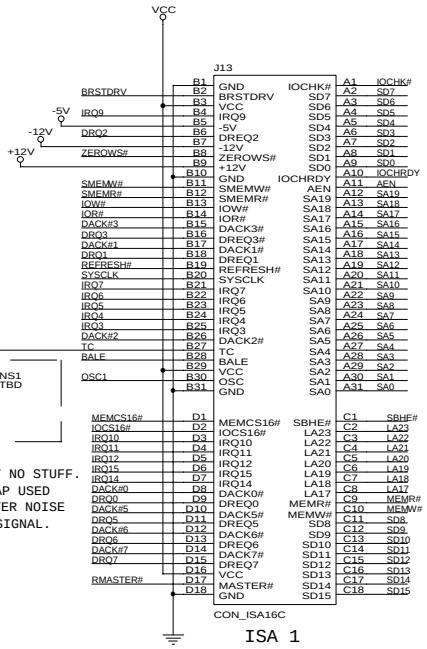
PCI CONNECTORS
3 AND 4



INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title: PCI CONNECTORS 3 & 4	
Size: Custom — Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 17 of 33

ISA SLOTS





NOTE : DEFAULT NO STUFF. THIS CAP USED TO FILTER NOISE ON TC SIGNAL.

INTEL CORPORATION

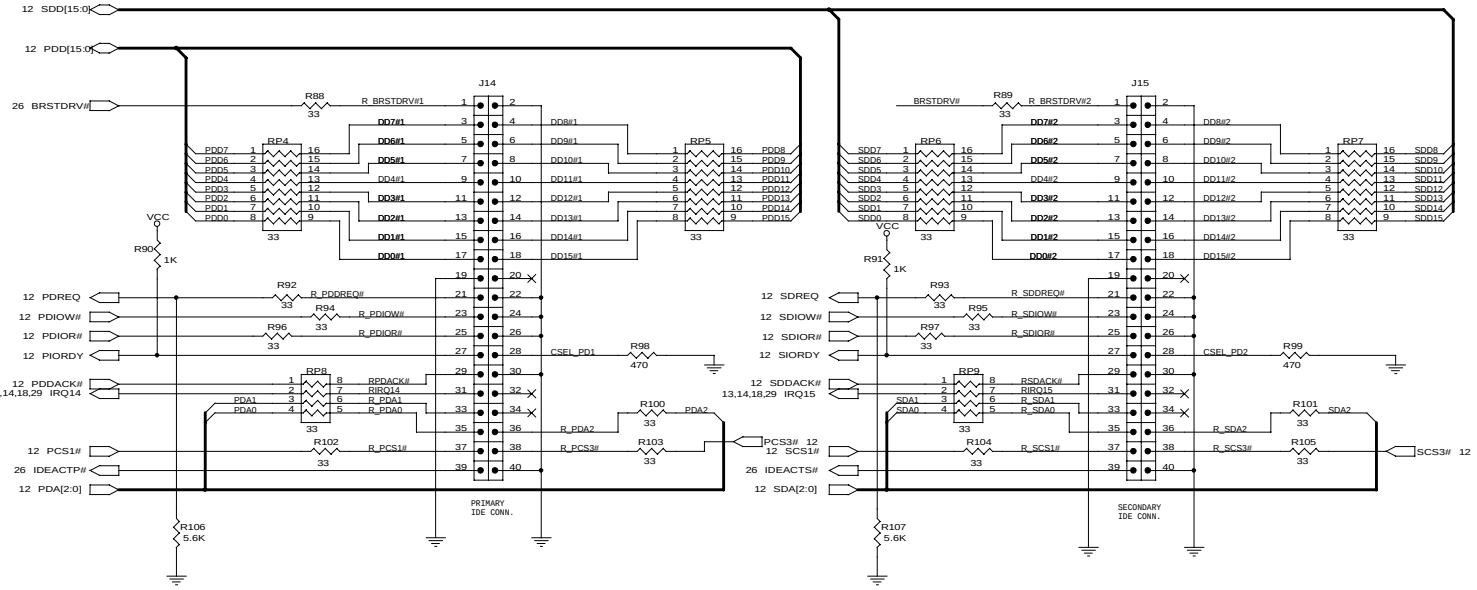
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FMS-62
FOLSOM, CA 95630

Title: ISA SLOTS

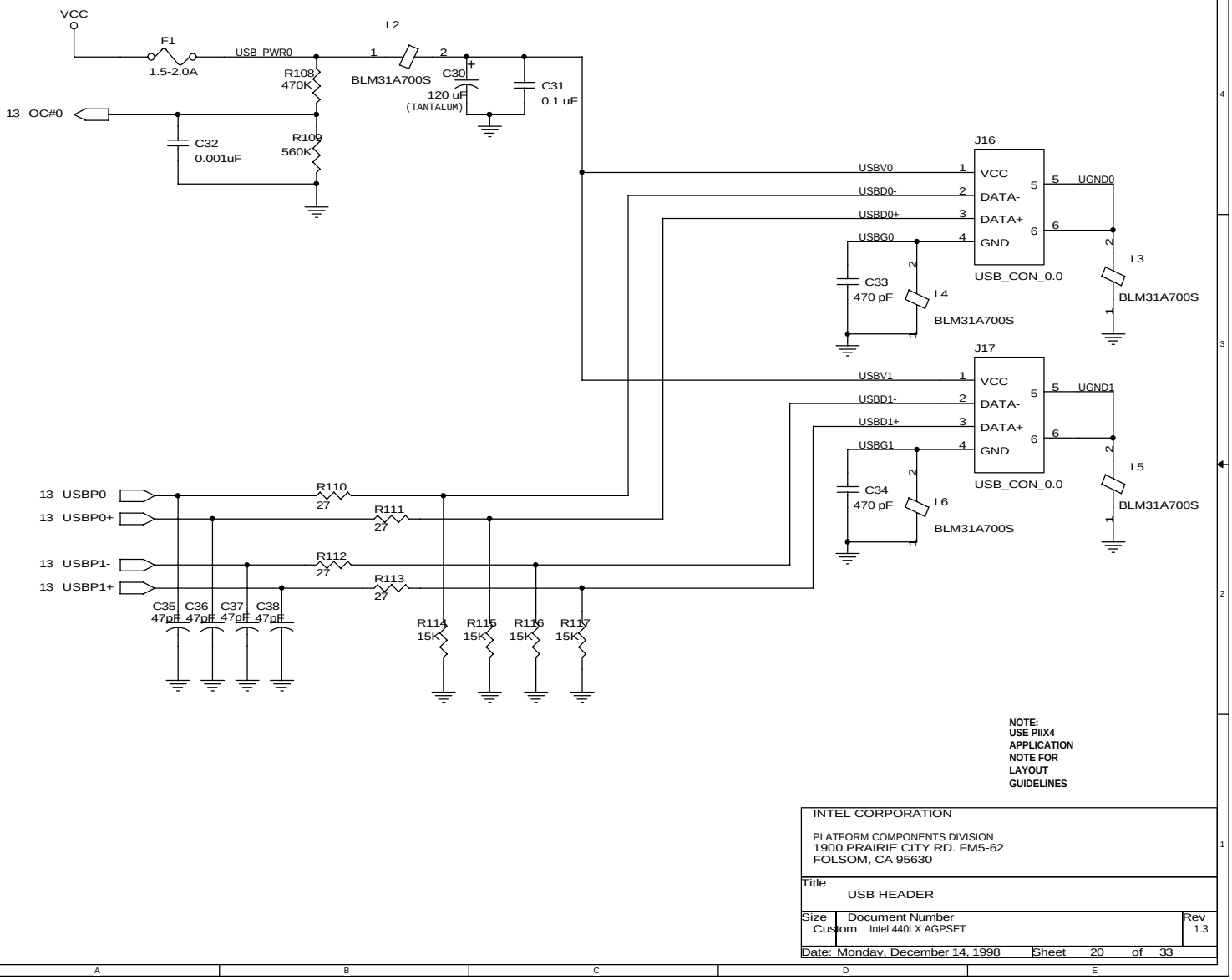
Size: Custom | Document Number: Intel 440LX AGPSET | Rev: 1.3

Date: Monday, December 14, 1998 | Sheet 18 of 33

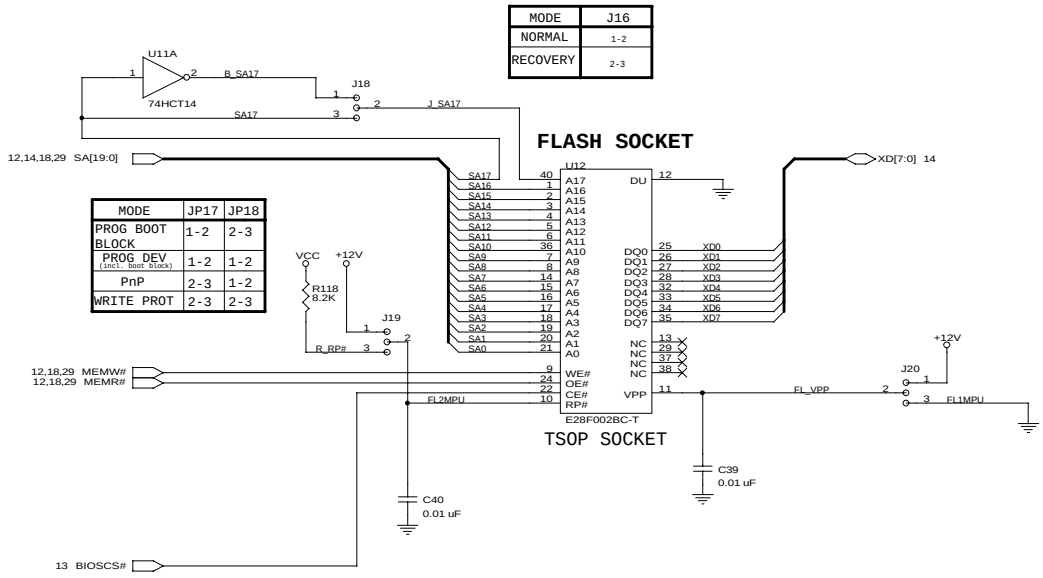
IDE CONNECTORS



INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: PCI IDE CONNECTORS		
Size: Custom	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 19 of 33	


VCC
F1
1.5-2.0A
USB_PWR0
L2
BLM31A700S
R108
470K
C30
120 uF
(TANTALUM)
C31
0.1 uF
13 OC#0
C32
0.001uF
R109
560K
J16
USBV0
USBD0-
USBD0+
USBG0
VCC
DATA-
DATA+
GND
UGND0
USB_CON_0.0
C33
470 pF
L4
BLM31A700S
L3
BLM31A700S
J17
USBV1
USBD1-
USBD1+
USBG1
UGND1
C34
470 pF
L6
L5
13 USBP0-
13 USBP0+
13 USBP1-
13 USBP1+
R110
27
R111
27
R112
27
R113
27
C35 47pF
C36 47pF
C37 47pF
C38 47pF
R114 15K
R115 15K
R116 15K
R117 15K
NOTE:
USE PIIX4
APPLICATION
NOTE FOR
LAYOUT
GUIDELINES
INTEL CORPORATION
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630
Title
USB HEADER
Size
Custom
Document Number
Intel 440LX AGPSET
Rev
1.3
Date: Monday, December 14, 1998
Sheet 20 of 33

SYSTEM ROM



MODE	J16
NORMAL	1-2
RECOVERY	2-3

MODE	JP17	JP18
PROG BOOT BLOCK	1-2	2-3
PROG DEV (incl. boot block)	1-2	1-2
PnP	2-3	1-2
WRITE PROT	2-3	2-3

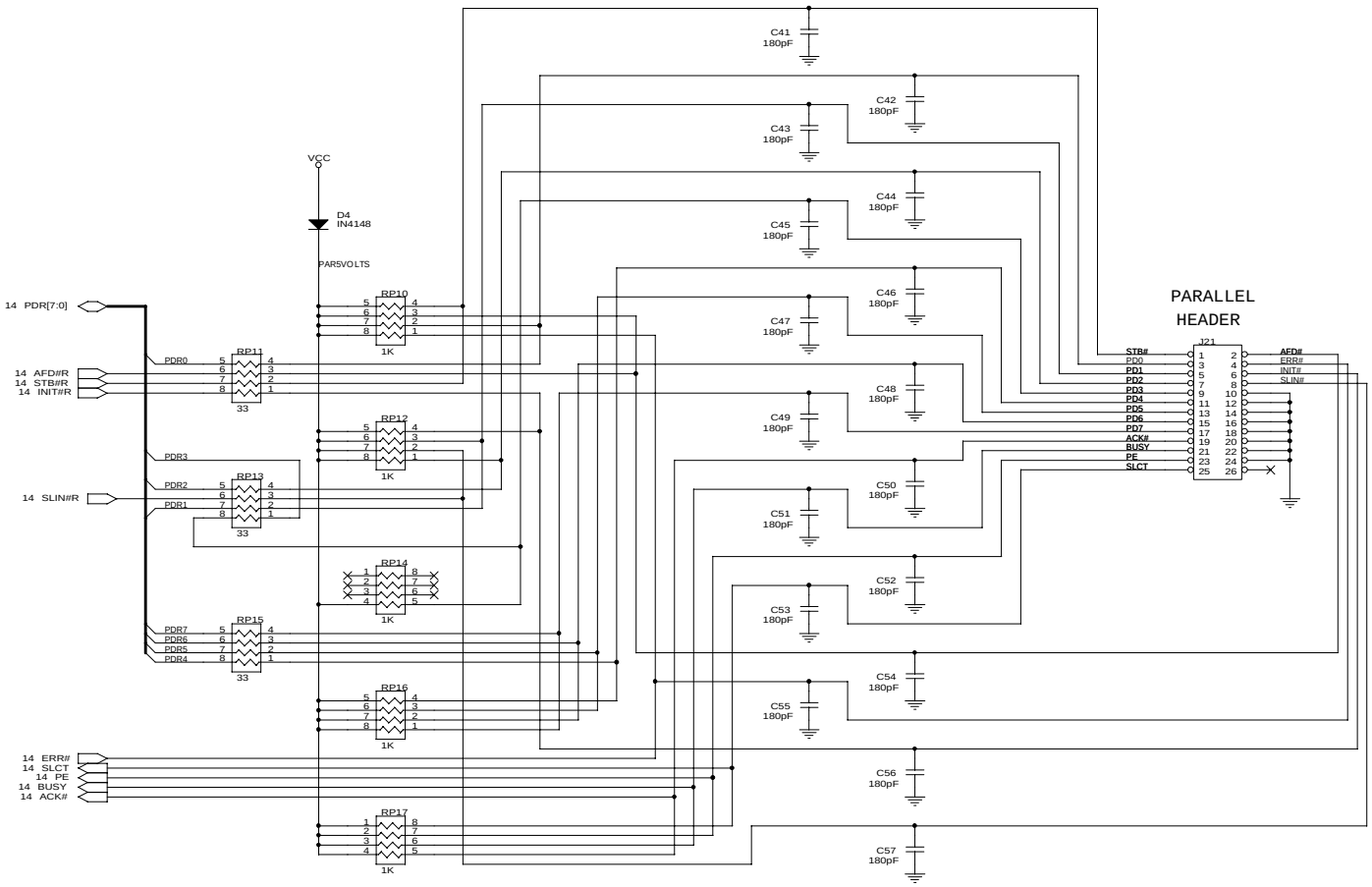
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FMS-62
FOLSOM, CA 95630

Title: SYSTEM ROM

Size: Custom | Document Number: Intel 440LX AGPSET | Rev: 1.3

Date: Monday, December 14, 1998 | Sheet 21 of 33



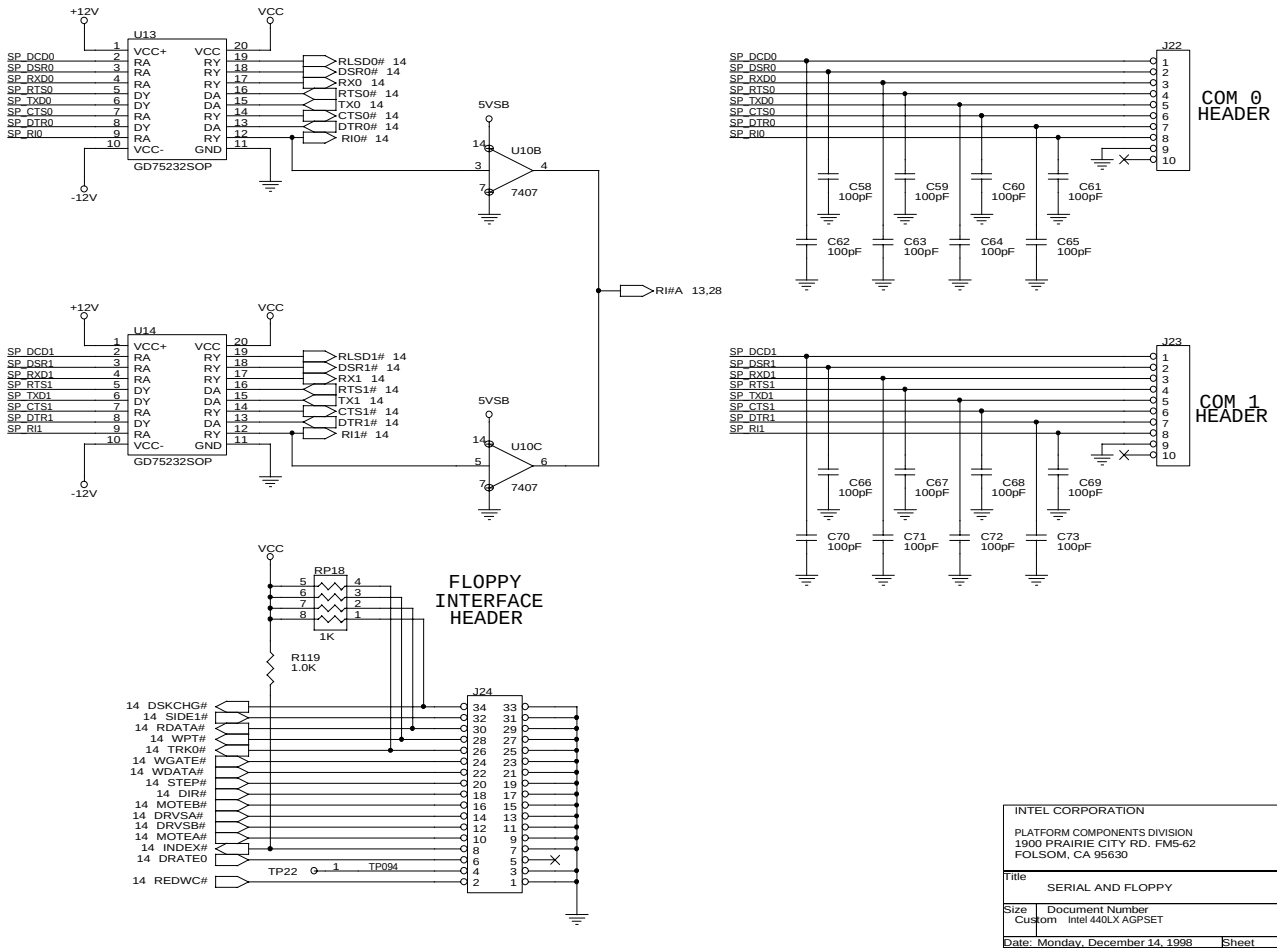
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

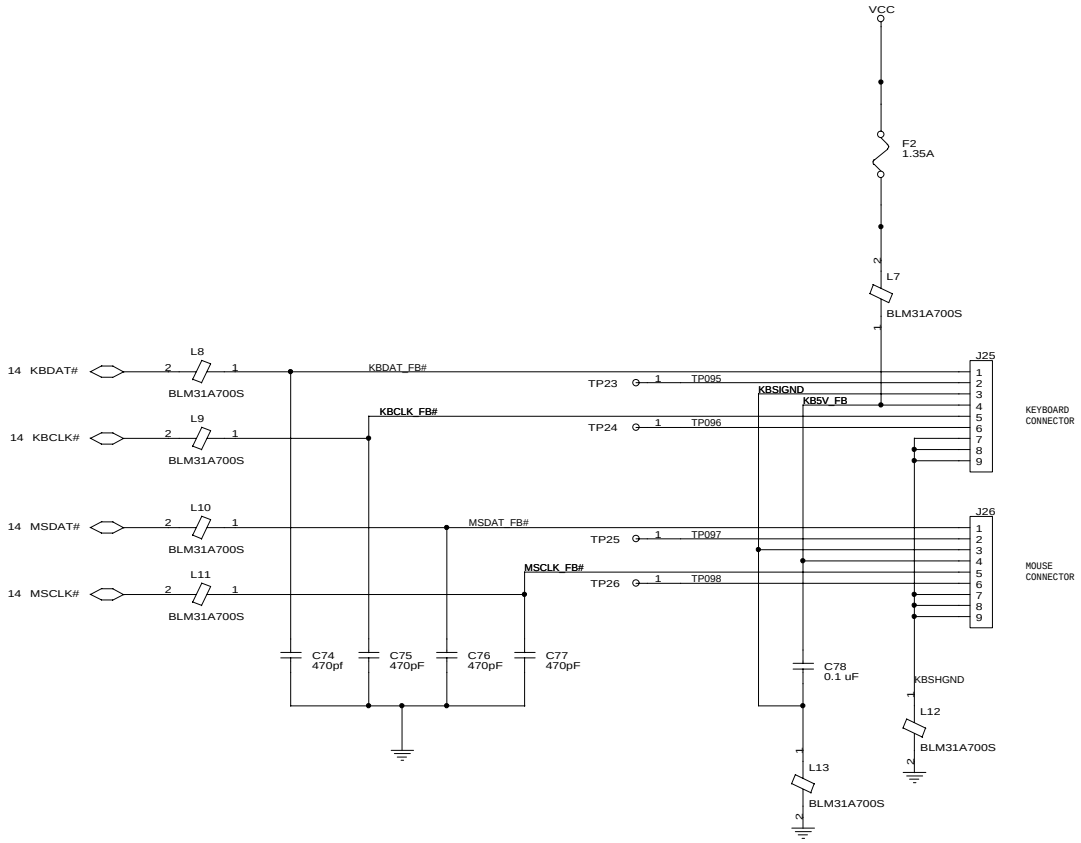
Title: PARALLEL PORT

Size: Custom | Document Number: Intel 440LX A GPSET | Rev: 1.3

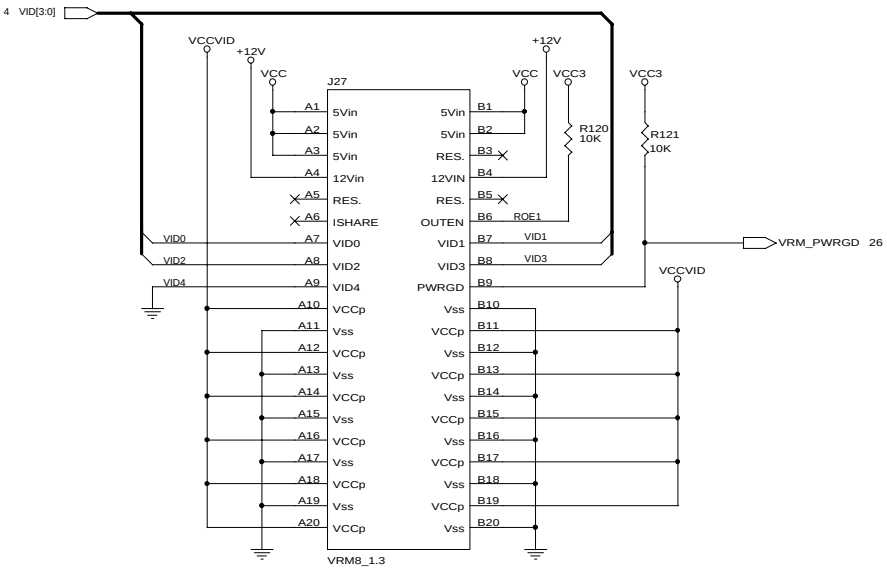
Date: Monday, December 14, 1998 | Sheet 22 of 33

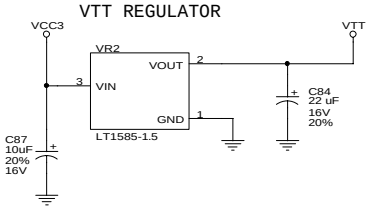


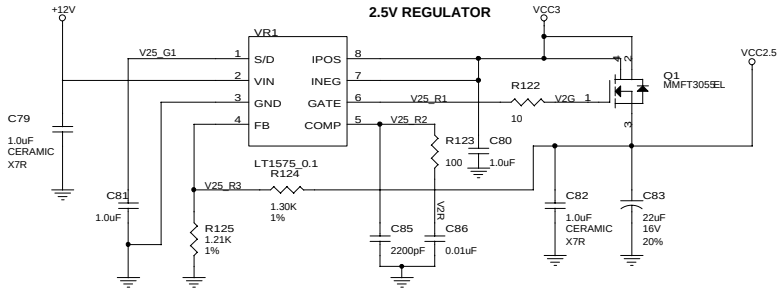
INTEL CORPORATION	
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630	
Title: SERIAL AND FLOPPY	
Size: Custom	Document Number: Intel 440LX AGPSET — Rev: 1.3
Date: Monday, December 14, 1998	Sheet 23 of 33



INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: KEYBOARD/MOUSE INTERFACE		
Size: Custom	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 24 of 33	







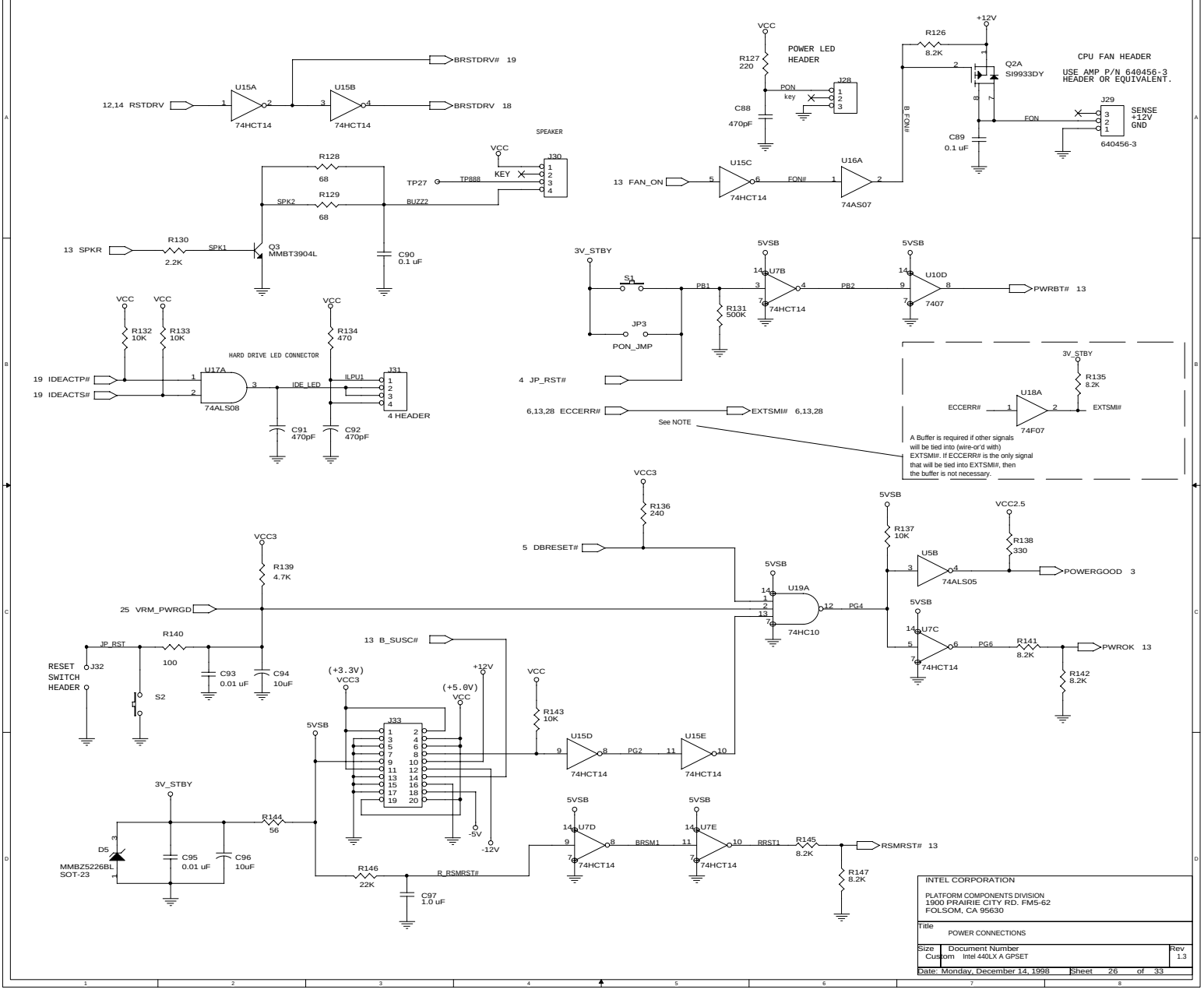
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: DC-DC CONVERTER CONNECTORS

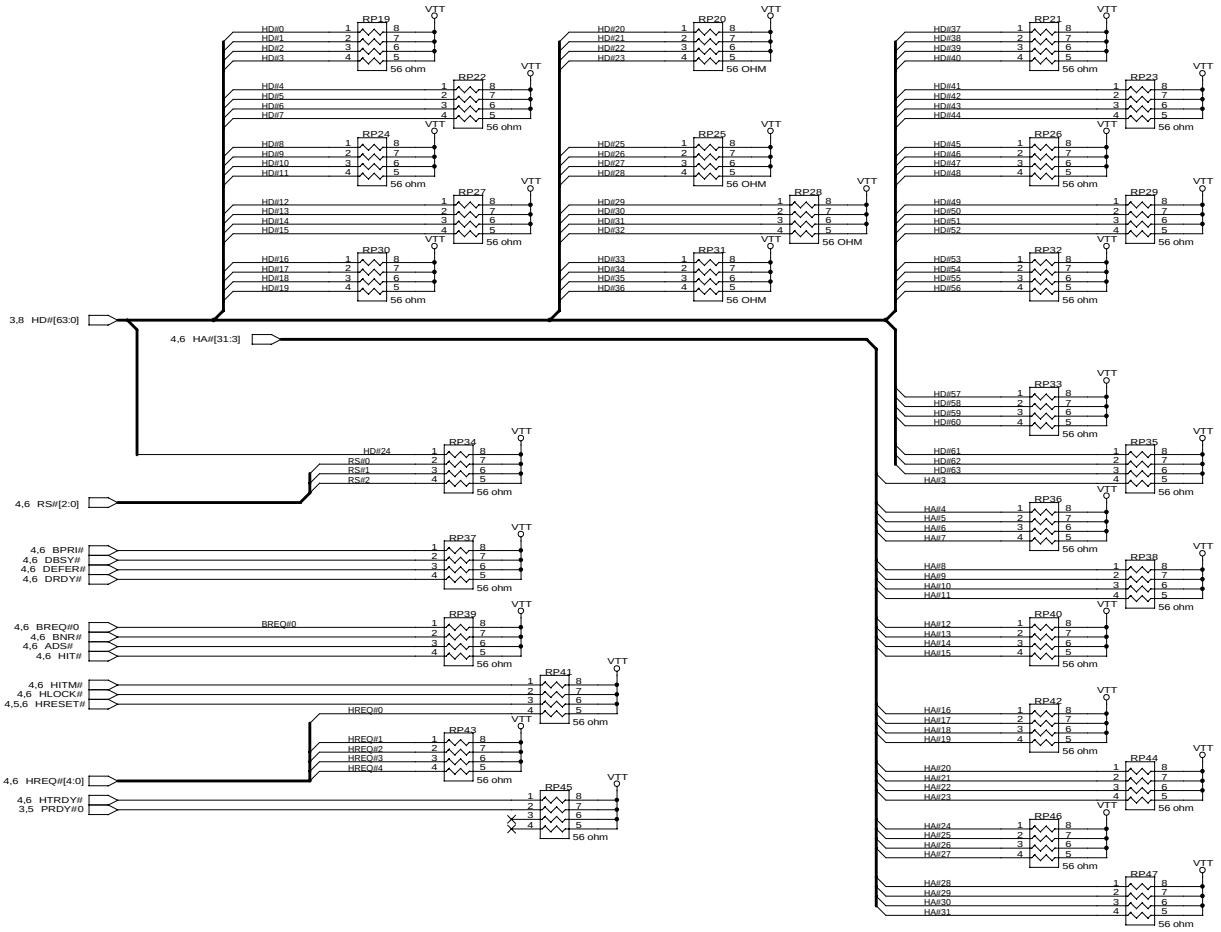
Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 Sheet 25 of 33



INTEL CORPORATION		
PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: POWER CONNECTIONS		
Size: Custom	Document Number: Intel 440LX A GPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 26 of 33	

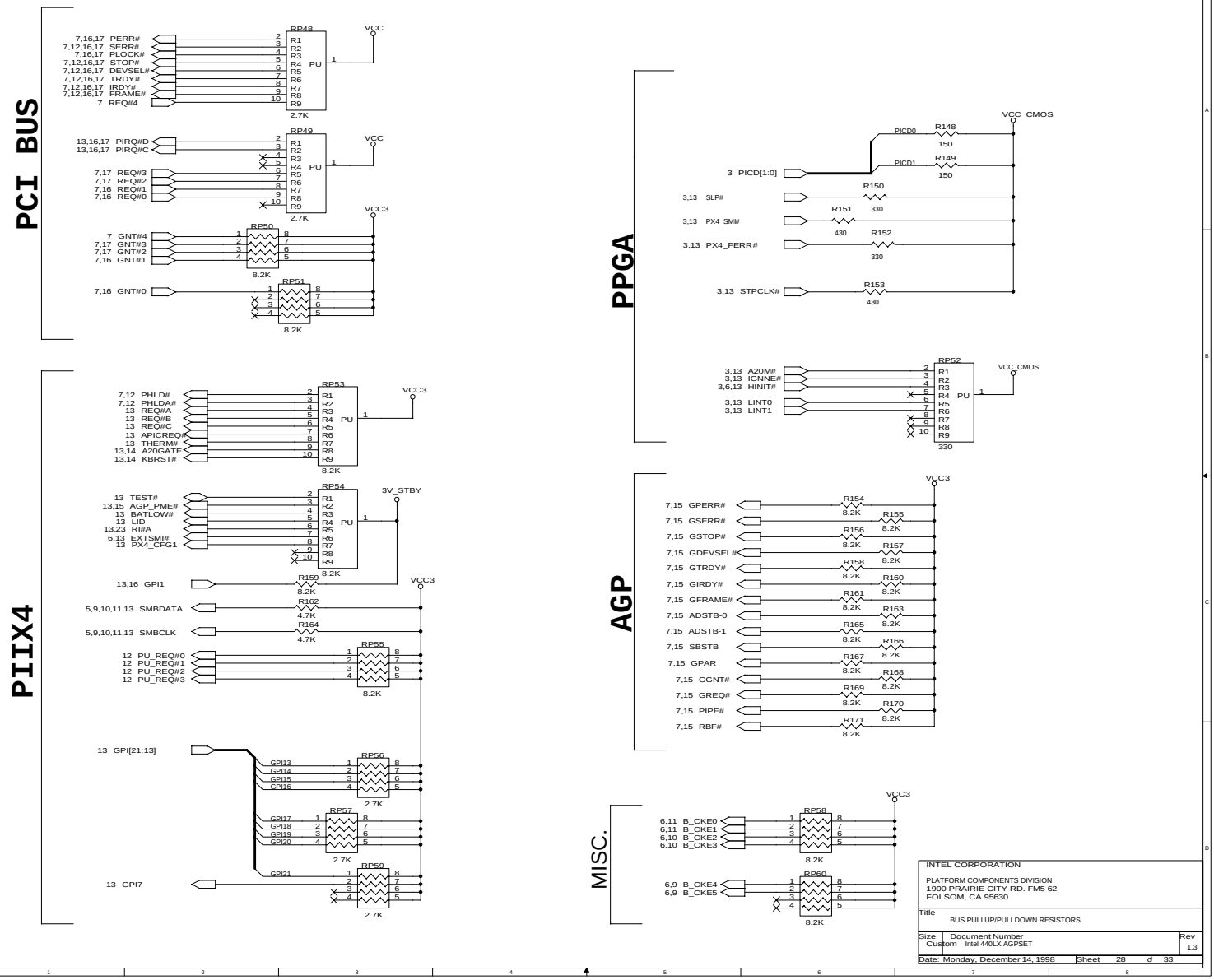
GTL+ TERMINATION RESISTORS



NOTE:

VTT=TERMINATION VOLTAGE

INTEL CORPORATION PLATFORM COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: GTL TERMINATION		
Size: Custom	Document Number: Intel 440LX AGPSET	Rev: 1.3
Date: Monday, December 14, 1998	Sheet 27 of 33	



INTEL CORPORATION

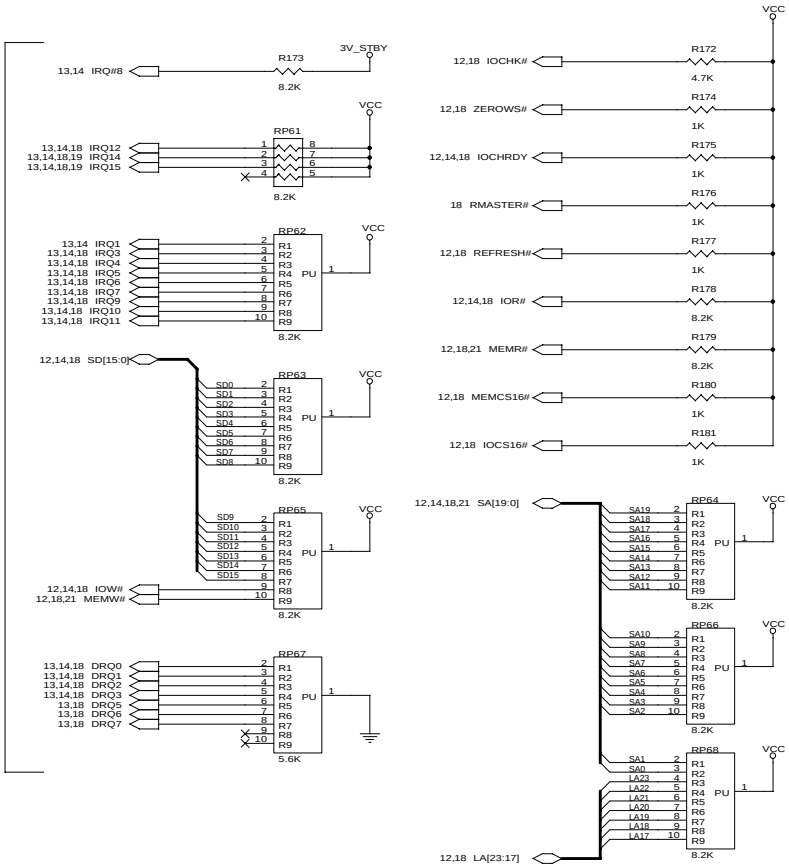
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: BUS PULLUP/PULLDOWN RESISTORS

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 28 of 33

ISA BUS



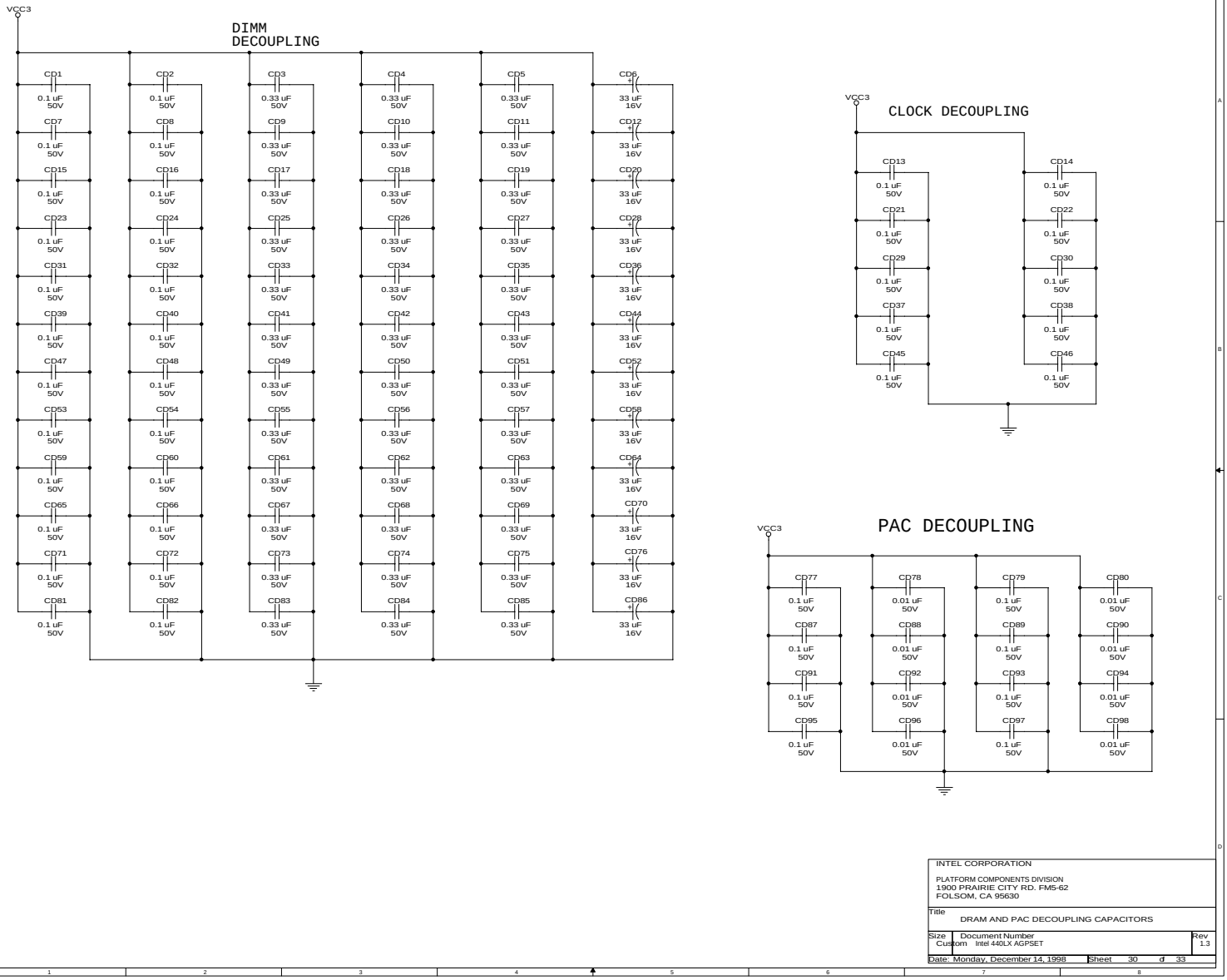
INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: ISA BUS PULLUPS

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 Sheet 29 of 33



INTEL CORPORATION

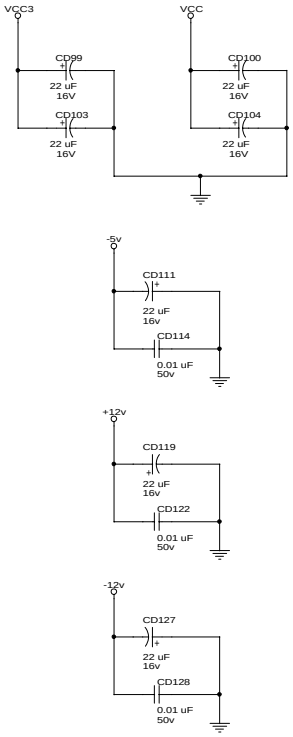
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: DRAM AND PAC DECOUPLING CAPACITORS

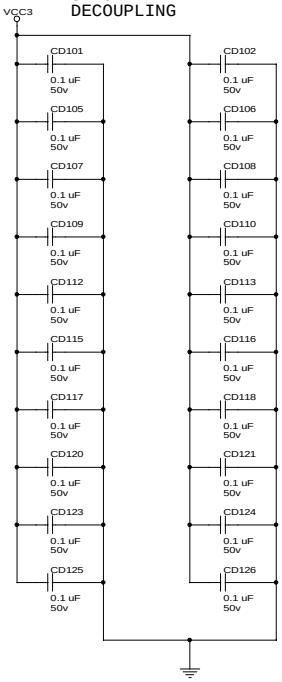
Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 30 of 33

BULK DECOUPLING



3 VOLT DECOUPLING



INTEL CORPORATION

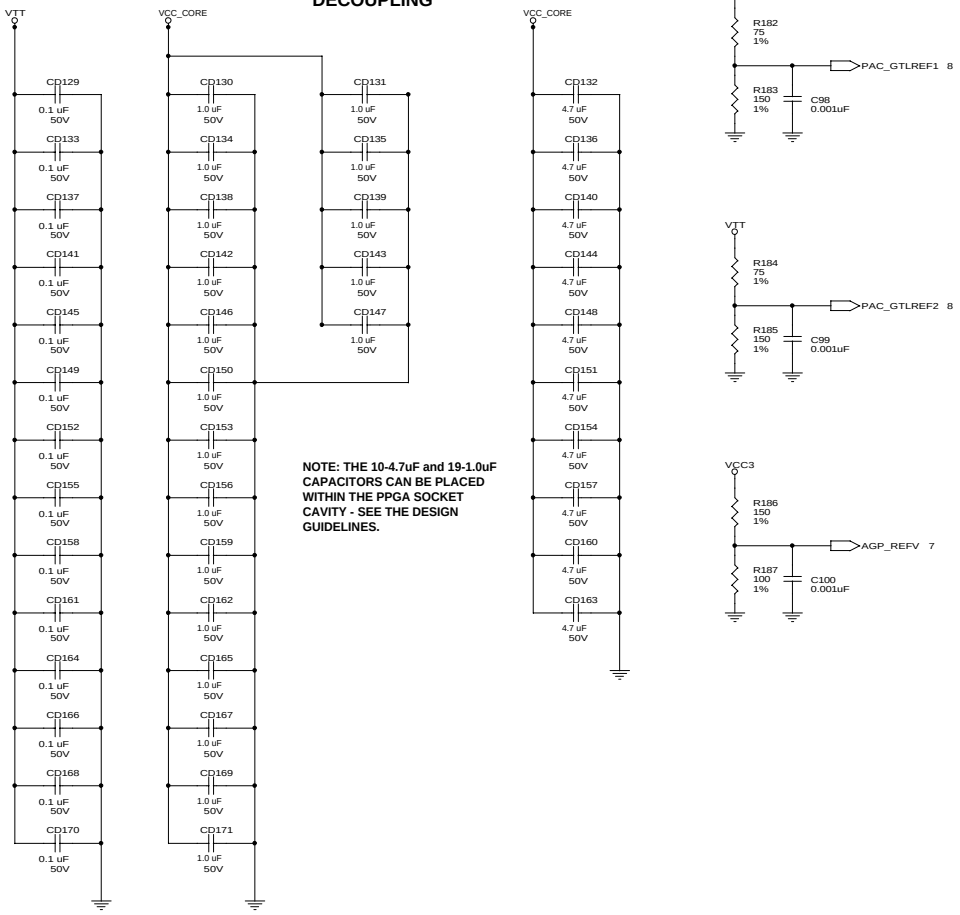
PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: 3.3 VOLT AND BULK POWER DECOUPLING

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 31 of 33

TERMINATION VOLTAGE DECOUPLING



NOTE: THE 10-4.7uF and 19-1.0uF CAPACITORS CAN BE PLACED WITHIN THE PPGA SOCKET CAVITY - SEE THE DESIGN GUIDELINES.

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title: GTL VREF CIRCUIT AND TERMINATION DECOUPLING

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 | Sheet 32 of 33

REVISION 1.0 - First release of PPGA 440LX
PCISet schematics.

REVISION 1.1 - Corrected PIIX4E Pullups.

REVISION 1.2 - Added Power Loss Circuit
to PIIX4E
Sheet 13.
Made VCC1.5V on PPGA Sheet 4 a No
Connect - not
req'd for 66MHz operation.

REVISION 1.3 - Public Version of Rev
1.2 schematics

INTEL CORPORATION

PLATFORM COMPONENTS DIVISION
1900 PRAIRIE CITY RD. FM5-62
FOLSOM, CA 95630

Title
REVISION HISTORY

Size	Document Number	Rev
Custom	Intel 440LX AGPSET	1.3

Date: Monday, December 14, 1998 Sheet 33 of 33