Clarifying the Reset Operation for the 80C186XL/80C188XL

An active RES# causes the processor to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the clock. The processor begins fetching instructions approximately 2.5 clock cycles after RES# is returned HIGH. For proper initialization, VCC must be within specifications and the clock signal must be stable for more than 4 clocks with RES# held LOW. RES# is internally synchronized.

Reset may be either cold (power-up) or warm. A cold reset is performed when the RES# input is asserted during power supply and oscillator startup. The processor's pins assume their reset pin states a maximum of 28 X1 periods after X1 and Vcc stabilize. RES# needs to be asserted an additional 4 X1 periods after the device pins assume their reset states. An RC time constant of 100ms is usually sufficient.

Applying RES# when the device is running constitutes a warm reset. In this case, assert RES# for at least 4 CLKOUT periods. The device pins will assume their reset states on the second falling edge of X1 following the assertion of RES#.

There are some precautions that need to be taken when using just a simple RC circuit to drive the RESET signal. Because of the large RC time constant associated with the reset circuit, it is highly susceptible to noise or glitches in the RESET signal. Since there is a singular switching point that separates what is defined as a logic high signal and what is defined as a logic low signal, it is possible that a slight glitch would cause a rising signal to toggle from low to high, then low again in immediate succession. This low-to-high and back to low transition can place the system in an unknown state. As was stated previously, once the RESET changes from low to high, it must be held high for a minimum amount of time before it can be driven low again.

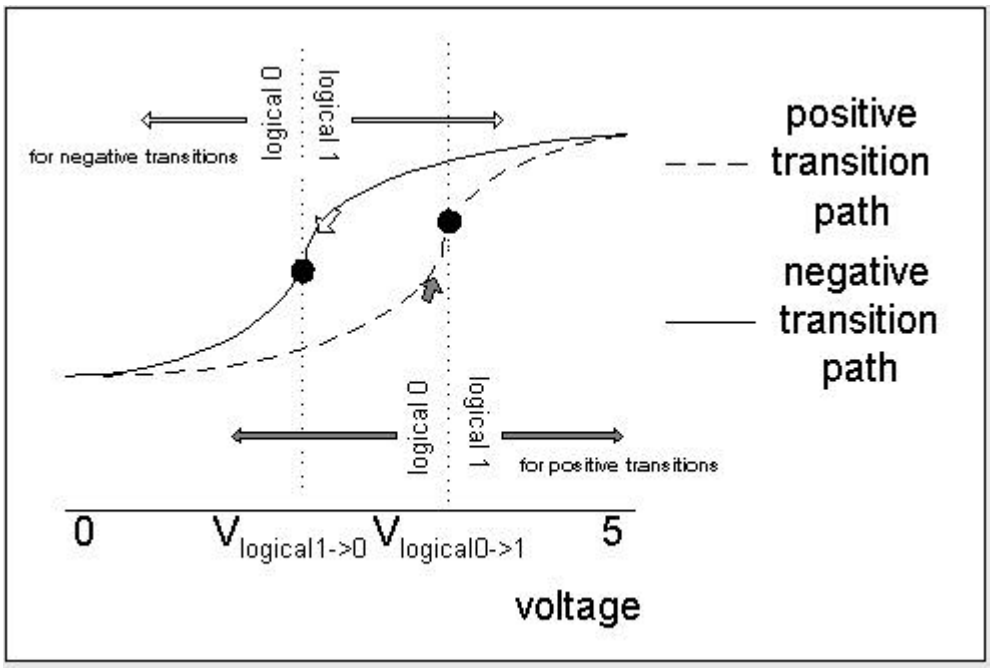

Figure 1. Hysteresis Graph of the RESET Signal

Hysteresis has been added to the RES# input so that the switching point for a low-to-high transition differs from the switching point for a high-to-low transition (see Figure 1). This is done to ensure that any noise in the reset circuit will not be able to cause a rising RESET signal to go back from high-to-low once the signal has gone from low-to-high. The value of the hysteresis on the RES# input of the 80C186XL/80C188XL is significantly less than that of other proliferations. Below is a table that compares some observed hysteresis values for the 80C186XL and the 80C186. A limited number of parts were tested representing typical production material. All values given are at room temperature, as the value varies little over temperature.

	Hysteresis@Max VCC	**Hysteresis@Min VCC**	**Range**
80C186XL	0.5589 V (avg.)	0.5844 V (avg.)	0.5119 V to 0.6950 V
80C186	0.6755 V (avg.)	0.6558 V (avg.)	0.6369 V to 0.6950 V

Note:
If upgrading from the 8018x or the 80C18x to the 80C18xXL, this small hysteresis needs to be put into consideration. In addition to this document, please see FaxBack Document 2132.

There are two options if the hysteresis of the RES# input is not sufficient for your current design. The RC time constant on the input can be reduced to produce a faster rise time or hysteresis can be added externally.

If the RC time constant is altered, certain considerations must be made. The constant must be long enough to keep the RES# input low until the clock input has stabilized and VCC has reached 4.5 Volts. The clock signal is important for designs using a crystal oscillator, a canned oscillator will already have a stable output. VCC must be allowed to reach 4.5 Volts because if the device exits the reset state with VCC less than 4.5 Volts, indeterminate operation will occur. Reducing the RC constant will yield a faster rise time, making the design less susceptible to noise.

If adjusting the RC time constant doesn't help, hysteresis should be added externally. To add hysteresis, an external Schmitt trigger needs to be incorporated into the reset circuit. This can be implemented as either one non-inverting Schmitt trigger (see Figure 2) or more commonly (and with greater cost efficiency), two inverting Schmitt triggers in series.

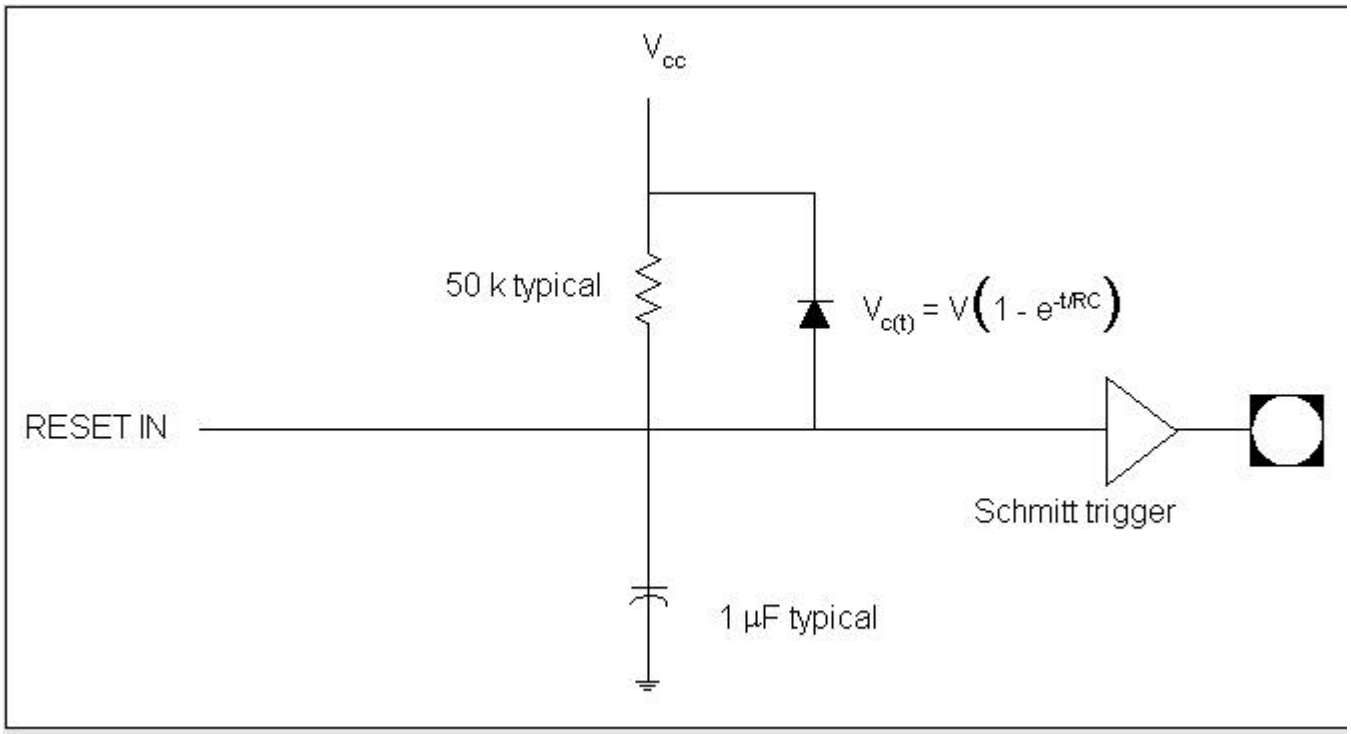

Figure 2. Simple RC Circuit for Powerup Reset

For more information regarding the reset operation of the 80C18xXL, please consult the 80C18xXL Microprocessor User's Manual (Order Number: 272164).