80C186XL/C188XL C-Step Compatibility with the 80186/188

80186/188

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ABSTRACT

This document details changes in AC and DC specifications, design considerations, and errata between the Intel Industry Standard 80186/188 and the C-Step 80C186XL/C188XL. The changes occur for two reasons: the XL parts have a CMOS fully static and modular core and are produced on a faster 1 micron

process. The XL core and process provide 0 to 25 MHz operation and lower power consumption. The faster process also reduces minimum timings on some signals. In general, these changes will have no effect on system timings provided the system does not contain synchronous control logic. Additionally, 80186/188 errata have all been corrected on the 80C186XL/C188XL. Essentially, the 80C186XL/C188XL parts are higher performance, lower power, pin for pin replacements for the 80186/188 parts.

DC SPECIFICATION DIFFERENCES

Symbol	80186		80C186XL		Units	Notes
	Min	Max	Min	Max		
VIL	-0.5	+ 0.8	-0.5 -0.5	+ 0.8 (except X1) 0.6 (X1)	V	
VIH	2.0 3.0 (RES#)	Vcc + 0.5 Vcc + 0.5	0.2VCC+ 0.9 3.0 (RES#) 3.9 (X1)	Vcc + 0.5 Vcc + 0.5 Vcc + 0.5	V	
Icc		550		N/A	mA	8 MHz, 0°C, Vcc = 5.25V(1)
		550		50	mA	10 MHz, 0°C, Vcc = 5.5V(1)
		N/A		65	mA	12.5 MHz, 0°C, Vcc = 5.5V(1)
		N/A		100	uA	0 MHz, 0°C, Vcc = 5.5V

NOTES:
1. Current is measured with the device in RESET with X1, X2, inputs, and bi-directional outputs driven .

Icc Specifications

The specifications for Icc at all operating frequencies have been reduced significantly on the 80C186XL. This reduction is a direct result of the 1 micron process and the fully static core on the 80C186XL. The fully static core allows the processor clock to be stopped during operation without loss of the processor's current state. The 80C186XL part consumes less than a 100 uA at 0 MHz.

AC SPECIFICATION DIFFERENCES

The 80C186XL is on a new 1 micron process. This process is inherently faster than the 1.5 micron process used to produce the 80186. Due to the higher speed of this process, a number of timings have changed. The minimum delay timings have been reduced. This will have no effect on systems requiring 3 ns or less of hold time in synchronous control logic. Possible effects on system timings are discussed below.

Symbol	80186		80C186XL		Units	Frequency	Parameter
	Min	Max	Min	Max		(MHz)	
TCHSV	10	45	3	45	ns	10	Status Active Delay
			3	35	ns	12.5	
			3	25	ns	20	
TCLSH	10	50	3	46	ns	10	Status Inactive Delay
			3	35	ns	12.5	
			3	25	ns	20	
TCLAV	5	44	3	44	ns	10	Address Valid Delay
			3	36	ns	12.5	
			3	27	ns	20	
TCLDV	10	40	3	40	ns	10	Data Valid Delay
			3	36	ns	12.5	
			3	27	ns	20	
TCHCSX	5	35	3	35	ns	10	Chip-Select Inactive Delay
			3	30	ns	12.5	
			3	20	ns	20	
TcvDEX	10	56	3	44	ns	10	DEN# Inactive Delay
			3	37	ns	12.5	
			3	22	ns	20	
TCHCTV	10	44	3	44	ns	10	Control Active Delay 2
			3	37	ns	12.5	
TCVCTV	5	44	3	44	ns	10	Control Active Delay 1
			3	37	ns	12.5	
			3	22	ns	20	
TCLRL	10	56	3	44	ns	10	RD# Active Delay
			3	37	ns	12.5	
			3	27	ns	20	
TCLRH	10	44	3	44	ns	10	RD# Inactive Delay

			3	37	ns	12.5	
			3	27	ns	20	
TCLLV	5	60	3	40	ns	10	LOCK# Valid/Invalid Delay
			3	37	ns	12.5	
			3	22	ns	20	

Symbol	80186		80C186XL		Units	Frequency	Parameter
	Min	Max	Min	Max		(MHz)	
TCKIN	50	250	50	oo	ns	10	CLKIN Period
			40	oo	ns	12.5	
			31.25	oo	ns	16	
			25	oo	ns	20	
TCLCK	20		20	oo	ns	10	CLKIN Low Time
			16	oo	ns	12.5	
			13	oo	ns	16	
			10	oo	ns	20	
TCHCK	20		20	oo	ns	10	CLKIN High Time
			16	oo	ns	12.5	
			13	oo	ns	16	
			10	oo	ns	20	
TCLCH	0.5 TCLCL - 6		0.5 TCLCL - 6		ns	10	CLKOUT Low Time
(Min)			0.5 TCLCL - 5		ns	12.5	CL = 100 pF
			0.5 TCLCL - 5		ns	16	
			0.5 TCLCL - 5		ns	20	
TCHCL	0.5 TCLCL - 6		0.5 TCLCL - 6		ns	10	CLKOUT High Time
(Min)			0.5 TCLCL - 5		ns	12.5	CL = 100 pF
			0.5 TCLCL - 5		ns	16	
			0.5 TCLCL - 5		ns	20	

Control Logic Considerations

The reduced minimum timings will affect hold time requirements relative to synchronous control logic. If the required hold time is 3 ns or less, no problems will occur. Designs with tight timing margins for hold times should be evaluated to ensure the hold time requirements are still met. The timing specifications affected in this situation are: TCHSV(min), TCLSH(min), TCLAV(min) (BHE# only), and TCHCSX(min). The specifications for TCLRL(min) and TCLRH(min) could also be an issue if RD# is used in the synchronous control logic, but this is uncommon.

Address and Data Valid Considerations

TCLAV(min) (Address) should not cause a problem. Most designs are not affected by having the address valid too early. The same situation exists for TCLDV(min), data being valid earlier in the bus cycle. This should not cause difficulties in most designs.

Buffered Design Considerations

TCVDEX(min) and TCHCTV(min) changes will not affect system designs. This is due to the fact TCLDX(min) and TCVDEX(min) are both 3 ns. Therefore, you are guaranteed to meet the data hold time requirement. TCHCTV(min) should not affect system designs either. DT/R# is used to control buffer data flow direction. If this signal goes valid/invalid earlier, it will not matter because the buffers are not enabled unless DEN# is active. DT/R# remains active long after DEN# goes inactive.

CLKIN Considerations

Because the 80C186XL/C188XL are fully static devices, they can operate down to 0 MHz without losing their present state. The maximum timings for TCKIN, TCLCK, and TCHCK have been set to infinity, reflecting the XL processor's ability to retain its current state, even with the clock stopped (infinite clock period).

CLKOUT High / Low Time Considerations

TCLCH(min) and TCHCL(min) are both improved for the 80C186XL/C188XL. The specifications for 50 pF loading were eliminated because the new 100 pF loading numbers are identical to the old 50 pF specifications. The same performance is achieved with heavier loading.

DESIGN CONSIDERATIONS

Compatible vs Enhanced mode

The 80C186XL has two major modes of operation, Compatible and Enhanced. In Compatible Mode, the 80C186XL is pin-to-pin compatible with the NMOS 80186/80188, with the exception of 8087 support. The ET (ESC Trap) bit in the Relocation register has no effect in Compatible Mode. If an ESCape opcode is executed, the 80C186XL/80C188XL will always trap to an interrupt vector Type 7.

The Enhanced Mode, the 80C186XL added three new features to the system design. These are Power-Save control, Dynamic RAM Refresh, and an Asynchronous Numerics Coprocessor Interface (80C186XL only). These new features can not be accidentally invoked in Compatible Mode because the control registers are not accessible.

Enhanced mode is selected during RESET. The 80C186XL/188XL samples the TEST# pin before and just after RES# input is removed to determine if the device will enter Enhanced mode. Tying the RESET output pin back to the TEST# input pin will automatically force the processor into Enhanced mode.

When the 80C186XL/188XL is in enhanced mode, three of the MCS# chip select lines change functionality to support the 80C187 Numerics Coprocessor Extension.

UCS#, LCS#, and LOCK# at Reset

LOCK# on the 80C186XL/C188XL is driven HIGH during reset, while it was driven high for one CLKOUT and then floated on the 80186/188. LOCK# must not be pulled low during reset or a factory test mode will be invoked. Similarly, UCS# and LCS# must either both be pulled LOW or both be left HIGH at reset (they are weakly pulled up during reset). Pulling both pins low during reset will enter ONCE mode. Pulling only one of these pins low will invoke a factory test mode. On the 80186/188, pulling only one of these pins low during reset did not inhibit normal operation.

Chip Selects and the Peripheral Control Block

Chip select regions on the 80186/188 which overlapped the Peripheral Control Block (PCB) would cause incorrect operation of the chip select signal. If the PCB were accessed, the chip select signal would go active, initially, but would go inactive prematurely. Additionally, if one or more wait states were programmed, the Chip Select Unit would only insert one. Because of the location of the Relocation Register on the 80186/188, the Chip Select Unit did not immediately realize that no chip select activity was to occur (for a PCB access), so it would activate the chip select signal. When it was determined that a PCB access was occurring, the chip select was deactivated, prematurely. The Relocation Register was moved inside the Chip Select Unit on the 80C186XL/C188XL and no chip select activity occurs during accesses to the PCB.

Overlapping Chip Selects

Although overlapping chip selects is not recommended, it is occasionally done. On the 80186/188, the requirement for overlapping selects was that they have identical wait state/ready programming. If they did not, indeterminate operation occurred. On the 80C186XL/C188XL, if two overlapping chip selects do not have identical wait state/ready programming, the following priority scheme is used: Mid-Memory, Upper/Lower Memory, and then Peripherals.

Writes to the DHLT Bit in Slave Mode

Bit 15 in the Interrupt Status Register is the DHLT bit. In Slave Mode on the 80186/188, regardless of the value of bit 15 in the word written to the Interrupt Status Register, DHLT is cleared. This means that DMA activity could resume if the Interrupt Status Register is accessed during an NMI service routine. On the 80C186XL/C188XL, the DHLT bit cannot be altered during Slave Mode operation.

Accesses to Undefined Peripheral Control Block Registers

When an undefined Peripheral Control Block Register was accessed on the 80186/188, the value returned was 0FFFFH. On the 80C186XL/C188XL, the returned value will be undefined. The only exceptions to this are the PDCON register and the DRAM Refresh Registers in Compatible Mode. The CPU will force 0FFFFH onto the bus. This was done because some software will check these registers to determine if the part is operating in Enhanced Mode or Compatible Mode. If the PDCON and the DRAM Refresh registers return 0FFFFH when read, the part is operating in Compatible Mode

Device Reset Input

The hysteresis of the reset input on the 80C186XL/C188XL is slightly less than that of the 80186/188. For environments with little noise, there should be no problem due to decreased hysteresis. Designs with a long RC time constant on the reset input or measurable noise may need to change the RC constant to a smaller value or add hysteresis externally. The RC constant must be long enough to allow the crystal oscillator to stabilize and allow Vcc to reach 4.5 Volts at power-up. To add hysteresis externally, two Schmitt triggers (74AC14) in series can be added between the RC network and the reset input.

External Ready During Interrupt Acknowledge

If the Peripheral Control Block (PCB) is located in I/O space from 0000H to 00FFH, and at least one interrupt is configured in cascade mode, external ready will be ignored during an interrupt acknowledge bus cycle. The data on the internal bus is monitored to determine if a location within the PCB is being accessed. Normally, a PCB access will ignore external ready. During an interrupt acknowledge cycle, the internal bus is driven to 0000H. The internal logic recognizes an interrupt acknowledge cycle as an I/O cycle and looks at the internal bus for an address. Because it is driven to 0000H and the PCB overlaps that address, the bus cycle is assumed to be a PCB access and external ready is ignored.

The PCB must be located so it does not include location 0000H. Locating it anywhere else in I/O space or moving it to memory space will correct the problem. Systems not using cascade mode or operating external interrupt controllers at zero wait states are not affected.

More Design Considerations:

The 80C186XL/188XL is a high performance device. Some careful considerations must be taken for high speed designs including careful board layout and oscillator design.

- Careful board layout is needed :
- Use short traces if possible
- Terminate clock lines
- Buffer large loads
- Use bypass capacitors (be generous)

- More careful oscillator design is needed:

  The external requirements for 80C186XL oscillator operation are somewhat different than for the NMOS counterpart because of CMOS design and higher frequencies. Designers of 80C186XL/188XL circuits above 10mhz will need to consider 3rd overtone crystal circuits. The use of a 3rd overtone crystal requires that an inductor and an additional capacitor be connected to the x2 pin to suppress the fundamental mode oscillations.

  The usual method to supply an external frequency input to the 80C186XL/188XL is to drive x1 while minimizing the capacitance on x2. In situations where x2 has a significant stray capacitance connected, for example during customer incoming tests, it is preferable to drive x2 with an inverted x1 signal.

  Under no circumstances should x2 be driven with x1 grounded, even though this was possible with the NMOS 80186. x2 is the output of CMOS inverter.

Software considerations:

With the 8087, it was necessary for ASM86 to insert an FWAIT instruction before every 8087 instruction synchronization. With the new numerics coprocessor, a check of the BUSY pin is done automatically for each numerics instruction and the explicit WAITs are no longer necessary.

The new instructions available with the new numerics coprocessor include: FCOS, FSIN, FSINCOS, improved, FPTAN, and improved FPATAN.

ERRATA COMPARISON

The current C stepping of the 80C186XL/C188XL has no known errata. Please consult FAXBACK at 1-800-628-2283 for the latest errata updates. A disposition of all known errata on the current 80186/188 is included below. The effect of putting an 80C186XL/C188XL into an existing 80186/188 design containing errata workarounds is also considered.

LOCK# / INTA Cycles

- Description: If an interrupt arrives during a LOCK'ed bus cycle, a loss of synchronization can occur and LOCK# may not be asserted between the first and second INTA# pulses. Without LOCK# being active, the DMA controller or an auxiliary bus master can steal the bus, separating the INTA pulses. Some peripherals cannot tolerate separated INTA pulses, but the 82C59A will not be affected.
- Disposition: Fixed within the Bus Interface Unit on the 80C186XL/C188XL.

Interrupt Status Register

- Description: A timer interrupt request occurring during a write operation to the register may be ignored or redirected to the wrong interrupt vector. All instructions capable of affecting the register are implicated.
- Disposition: Declassified as an errata. Continue to disable interrupts during accesses to the DHLT bit.

DHLT Bit Under Slave Mode

- Description: The DHLT bit in the interrupt status register works incorrectly in Slave Mode. The bit cannot be set by either the occurrence of NMI or by direct programming. Any read of the DHLT bit from Slave Mode yields a zero. Furthermore, if the DHLT function is set from master mode, any subsequent write to the interrupt status register from slave mode will clear the bit (as seen from master mode), enabling DMA activity. The IRET instruction correctly resets DHLT from either mode.
- Disposition: Declassified as an errata. On the 80C186XL/C188XL, the DHLT bit cannot be altered during Slave Mode operation.

10mhz BHE# During DMA

- Description: When a read from either of the DMA control registers is followed by a DMA byte transfer from an odd to an even address, BHE# on the 80186/188 may not go active on the odd byte read part of the DMA cycle. This problem is speed dependent, and has only been observed between 9 and 10mhz.

- Disposition: This errata does not exist on the 80C186XL/188XL.

Interrupt Fault Condition

- Description: A race condition in the CPU microcode latch may cause the 80186/80188 to latch an incorrect address. The most likely result is that the CPU locks up. However, the bus controller continues to run until the prefetch queue is full, then the bus goes idle. The problem is sporadic and related to instruction execution, interrupt execution, voltage, temperature, and device processing.
- Disposition: This errata does not exist on the 80C186XL/188XL.

Sequential Locked Instructions

- Description: When the 80186/80188 executes back-to-back LOCK'ed instructions, the LOCK# signal remains active between the read/write execution cycles of the two instructions. Once the bus is LOCK'ed, any remaining cycles of the second instruction cannot be fetched. This condition causes the processor to hang.
- Disposition: This errata does not exist on the 80C186XL/188XL.

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