80C186/188EB and 80C186/188EC SIO Mode 0 Max Baud Rate

Abstract:
This techbit explains that the maximum baud rate for Mode 0 (synchronous) operation of the serial I/O port (SIO) is incorrectly explained in the manuals.

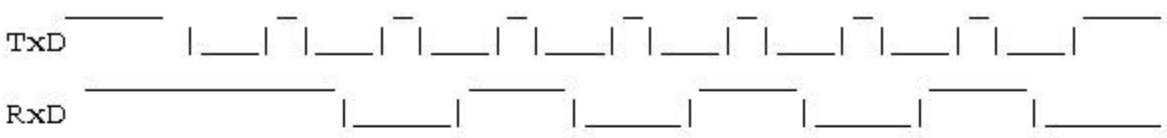
Devices Covered:
This techbit covers all steppings of the 80C186/188EB and 80C186/188EC.

Description:
When using the Serial I/O Port's Mode 0 synchronous function of the 80C186/188EB/EC device, the User's Manual and the Data Sheets do not state the correct maximum baud rate. The actual maximum baud rate depends on the frequency and is inversely proportional to the value loaded into the baud rate compare register. However, the baud rate compare register (BxCMP) must have a value of x002h or greater (where x determines if the internal clock (CLKIN/2), x=1, or BCLK, x=0, is the clock source for the baudrate generator). The smaller the value in the baud rate register the higher the baud rate at which the device operates.

If the device is run at a faster baud rate than when BxCMP ò x002h (i.e. BxCMP=x001h), the serial port buffer register (SxBUF) will not **receive** the correct data. The receive shift register is clocked from an internal signal, not from the signal on TxD. Although the two signals are normally synched, when BxCMP = x001h the receive shift register clock puts out **one** clock ahead of, and out of synch with, the first pulse transmitted by TxD. This causes whatever data is on the RxD pin before the reception is actually supposed to begin (i.e., before the first rising edge of the first pulse transmitted by of TxD) to be clocked in as the LSB. Then the reception continues in the normal synchronous fashion except that the data being received is now shifted left once by the false start of the receive shift register and the seventh real data bit is received as the MSB and the eighth data bit or true MSB is never shifted into the receive shift register.

The following timing diagram and explanation show the missed MSB.

Serial Port Mode 0 Reception of a 055h value



BxCMP > x001h
DATA BITS 1 0 1 0 1 0 1 0 = 055h
True LSB MSB
BxCMP < x002h
DATA BITS 1 1 0 1 0 1 0 1
= 0ABh

False LSB = Extra bit clocked in internally causing the false MSB to = 7th data bit, not the 8th.

If BxCMP = x001h, then the SxBUF register will contain the incorrect data of 0ABh at the end of reception. If BxCMP register greater than or equal to x002h, then the SxBUF register will contain the correct data of 055h at the end of reception. Therefore, x002h is the minimum value for the baud rate compare register.

Customer Impact:
The serial port in synchronous mode (Mode 0) cannot be operated with the BxCMP register holding a value of less than x002h.