MILITARY Intel486™ PROCESSOR FAMILY

- **Write-Back Enhanced IntelDX4™ Processor**
  - **— Up to 100-MHz Operation**
  - **— Speed-Multiplying Technology**
  - **— 32-Bit Architecture**
  - **— 16K-Byte On-Chip Write-Back Cache**
  - **— Integrated Floating-Point Unit**
  - **— 3.3V Core Operation with 5V Tolerant I/O Buffers**
  - **— SL Technology**
  - **— Static Design**
  - **— IEEE 1149.1 Boundary Scan Compatibility**
  - **— Binary Compatible with Large Software Base**
- **IntelDX2™ Processor**
  - **— Speed-Multiplying Technology**
  - **— 32-Bit Architecture**
  - **— 8K-Byte On-Chip Cache**
  - **— Integrated Floating-Point Unit**
  - **— SL Technology**
  - **— Static Design**
  - **— IEEE 1149.1 Boundary Scan Compatibility**
  - **— Binary Compatible with Large Software Base**
- **Military Intel486™ DX Processor**
  - **— 32-Bit Architecture**
  - **— 8K-Byte On-Chip Cache**
  - **— Integrated Floating-Point Unit**
  - **— SL Technology**
  - **— Static Design**
  - **— IEEE 1149.1 Boundary Scan Compatibility**
  - **— Binary Compatible with Large Software Base**
- **All Devices Available in 168-Lead PGA Package and 196-Lead Ceramic Quad Flatpack**
- **Supported in Multiple Product Grades**

NOTE:
References to devices within this document refer to Military versions.

Military Intel486™ Processor	Product Grade		
	SE1	SE2	SE3
Military Intel486™ DX Processor	Q		✓
IntelDX2™ Processor	Q		✓
IntelDX4™ Processor	Q	Q	Q

Definitions:
SE1 = Special Environment Temperature, −55°C to +125°C
SE2 = Special Environment Temperature, −40°C to +125°C
SE3 = Special Environment Temperature, −40°C to +110°C
Q = QML qualified to MIL-STD-38535

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Data Sheet Marking	Description
Product Preview	Contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product becomes available.
Advance Information	Contains information on products being sampled or in the initial production phase of development.†
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1.0 INTRODUCTION

The Military Intel486 processor family enables a range of low-cost, high-performance system designs for Military embedded ground, missile and Avionics applications. This family includes the IntelDX4 processor, the fastest Military Intel486 processor (up to 50% faster than an IntelDX2 processor). The IntelDX4 processor integrates a 16K unified cache and floating point hardware on-chip for improved performance. The IntelDX2 processor integrates an 8K unified cache and floating point hardware on chip. The IntelDX4 and IntelDX2 processors use Intel's speed-multiplying technology, allowing the processor to operate at frequencies higher than the external memory bus. The Military Intel486 DX processor offers the features of the IntelDX2 processors without speed-multiplying. The entire Military Intel486 processor family incorporates energy efficient ''SL Technology'' for low power computing.

SL Technology enables system designs that exceed the Environment Protection Agency's (EPA) Energy Star program guidelines, without compromising performance. It also increases system design flexibility and improves battery life in mobile applications. SLTechnology allows system designers to differentiate their power management schemes with a variety of energy-efficient or battery-life preserving features. Military Intel486 processors provide power management features that are transparent to application and operating system software. Stop Clock, Auto HALT Power Down, and Auto Idle power down allow software transparent control over processor power management. Equally important is the capability of the processor to manage system power consumption. Military Intel486 processor System Management Mode (SMM) incorporates a non-maskable System Management Interrupt (SMI#), a corresponding Resume (RSM) instruction and a new memory space for system management code. Intel's SMM ensures seamless power control of the processor core, system logic, main memory, and one or more peripheral devices, that is transparent to any application or operating system.

Military Intel486 processors are available in a full range of speeds (25 MHz to 100 MHz), packages (PGA, CQFP), and voltages (5V, 3.3V) to meet any system design requirements.

1.1 Processor Features

All of the Military Intel486 processors consist of a 32-bit integer processing unit, an on-chip cache, and a memory management unit. This ensures full binary compatibility with the 8086, 8088, 80186, 80286, Intel386™ SX, Intel386 DX, and all versions of Military Intel486 processors. All of the Military Intel486 processors offer the following features:

- *32-bit RISC integer core*—The Military Intel486 processor performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general purpose registers.
- *Single Cycle Execution*—Many instructions execute in a single clock cycle.
- *Instruction Pipelining*—The fetching, decoding, address translation and execution of instructions are overlapped within the Military Intel486 processor.
- *On-Chip Floating Point Unit*—Military Intel486 processors support the 32-, 64-, and 80-bit formats specified in IEEE standard 754. The unit is binary compatible with the 8087, Intel287™, Intel387™ coprocessors.
- *On-Chip Cache with Cache Consistency Support*—An 8-Kbyte (16 Kbyte on the IntelDX4 processor) internal cache is used for both data and instructions. Cache hits provide zero wait-state access times for data within the cache. Bus activity is tracked to detect alterations in the memory represented by the internal cache. The internal cache can be invalidated or flushed so that an external cache controller can maintain cache consistency.
- *External Cache Control*—Write-back and flush controls for an external cache are provided so the processor can maintain cache consistency.
- *On-Chip Memory Management Unit*—Address management and memory space protection mechanisms maintain the integrity of memory in a multitasking and virtual memory environment. Both segmentation and paging are supported.
- *Burst Cycles*—Burst transfers allow a new double word to be read from memory on each bus clock cycle. This capability is especially useful for instruction prefetch and for filling the internal cache.

- *Write Buffers*—The processor contains four write buffers to enhance the performance of consecutive writes to memory. The processor can continue internal operations after a write to these buffers, without waiting for the write to be completed on the external bus.
- *Bus Backoff*—If another bus master needs control of the bus during a processor initiated bus cycle, the Military Intel486 processor will float its bus signals, then restart the cycle when the bus becomes available again.
- *Instruction Restart*—Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.
- *Dynamic Bus Sizing*—External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16, or 32 bits can be used.
- *Boundary Scan (JTAG)*—Boundary Scan provides in-circuit testing of components on printed circuit boards. The Intel Boundary Scan implementation conforms with the IEEE Standard Test Access Port and Boundary Scan Architecture.

SL Technology provides the following features:

- *Intel System Management Mode*—A unique Intel architecture operating mode provides a dedicated special purpose interrupt and address space that can be used to implement intelligent power management and other enhanced functions in a manner that is completely transparent to the operating system and applications software.
- *I/O Restart*—An I/O instruction interrupted by a System Management Interrupt (SMI#) can automatically be restarted following the execution of the RSM instruction.
- *Stop Clock*—The Military Intel486 processor has a stop clock control mechanism that provides two low-power states: a ''fast wake-up'' Stop Grant state (~20 mA–100 mA) and a ''slow wake-up'' Stop Clock state with CLK frequency at 0 MHz (100 μA–1000 μA).
- *Auto HALT Power Down*—After the execution of a HALT instruction, the Military Intel486 processor issues a normal Halt bus cycle and the clock input to the Military Intel486 processor core is automatically stopped, causing the processor to enter the Auto HALT Power Down state (~20 mA–100 mA).
- *Auto Idle Power Down* —This function allows the processor to reduce the core frequency to the bus frequency when both the core and bus are idle. Auto Idle Power Down is software transparent and does not affect processor performance. Auto Idle Power Down provides an average power savings of 10% and is only applicable to clock multiplied processors.

Enhanced Bus Mode Features (for the Write-Back Enhanced IntelDX4 Processor only):

- *Write Back Internal Cache*—The Write-Back Enhanced IntelDX4 processor adds write-back support to the unified cache. The on-chip cache is configurable to be write-back or write-through on a line by line basis. The internal cache implements a modified MESI protocol, which is most applicable to uniprocessor systems.
- *Enhanced Bus Mode*—The definitions of some signals have been changed to support the new Enhanced Bus mode (write-back mode).
- *Write Bursting*—Data written from the processor to memory can be bursted (zero wait state transfer).

1.2 Military Intel486™ Processor Product Family

Table 1-1 shows the Military Intel486 processors available by Maximum Frequency and Package.

Table 1-1. Product Options

Military Intel486™ Processor	Processor Frequency (MHz)						Package Type	
	25	33	50	66	75	100	168-Pin PGA	196-Lead CQFP
Military Intel486™ DX Processor	✓	✓					✓	✓
IntelDX2™ Processor			✓	✓			✓	✓
IntelDX4™ Processor					✓	✓	✓	✓

2.0 HOW TO USE THIS DOCUMENT

2.1 Introduction

This data sheet is a compilation of previously published individual data sheets for the Military Intel486 DX, IntelDX2 and IntelDX4 processors. This data sheet encompasses the entire current Military Intel486 processor family.

This data sheet describes the Military Intel486 processor architecture, features and technical details. Unless otherwise stated, any description for the Military Intel486 processor listed in this data sheet applies to all Military Intel486 processors. Where architectural or other differences do occur (for example, the IntelDX4 processor has a 16-Kbyte on-chip cache, all other Military Intel486 processors have an 8-Kbyte on-chip cache), these differences are described in separate sections. Section 2.2 provides a brief section description, highlighting the specific sections that contain processor-unique information.

It is important to note that all Military Intel486 DX, IntelDX2, and IntelDX4 processors have an on-chip floating point unit.

Boundary Scan (JTAG) testability features, capability and associated test signals (TCK, TMS, TDI, and TDO) are standard on all Military Intel486 processors.

2.2 Section Contents and Processor Specific Information

The following is a brief description of the contents of each section:

Section 1: ''Introduction.'' This section is an overview of the current Military Intel486 processor family, product features and highlights. This section also lists product frequency, voltage and package offerings.

Section 2: ''How to Use This Document.'' This section presents information to aid in the use of this data sheet.

Section 3: ''Pin Description.'' This section contains all of the pin configurations for the various package options (168-Pin PGA and 196-Lead CQFP), package diagrams, pin assignment tables and pin assignment differences for the various processors within a package class.

This section also provides a quick pin reference table that lists pin signals for the Military Intel486 processor family. The table, whenever necessary, has sections applicable to each current Military Intel486 processor family member.

Section 4: ''Architectural Overview.'' This section describes the Military Intel486 processor architecture, including the register and instruction sets, memory organization, data types and formats, and interrupts for all Military Intel486 processors.

The architectural overview describes the 32-bit RISC integer core of the Military Intel486 processor. The on-chip floating point unit for the Military Intel486 DX IntelDX2 and IntelDX4 processors is included in this section.

Section 5: ''Real Mode Architecture.'' This section describes the Military Intel486 processor real-mode architecture, including memory addressing, reserved locations, interrupts, and Shutdown and HALT. This section applies to all Military Intel486 processors.

Section 6: ''Protected Mode Architecture.'' This section describes the Military Intel486 protected-mode architecture, including addressing mechanism, segmentation, protection, paging and virtual 8086 environment. This section applies to all Military Intel486 processors.

Section 7: ''On-Chip Cache.'' This section describes the on-chip cache of the Military Intel486 processors. Specific information on size, features, modes, and configurations is described. The differences between the IntelDX4 processor on-chip cache (16-KByte) and other members of the Military Intel486 processor family on chip cache (8-KByte) are detailed.

This section also documents features, modes and operational issues specific to the Write-Back Enhanced IntelDX4 processor. The specifics for the Write-Back Enhanced IntelDX4 processor are interleaved with sections on the Standard mode (Write-Through cache) of other Intel486 processors as appropriate.

Section 8: ''System Management Mode (SMM) Architectures.'' This section describes the System Management Mode architecture of the Military Intel486 processors, including system management mode interrupt processing and programming mode.

Section 9: ''Hardware Interface.'' This section describes the hardware interface of the current Military Intel486 processor family, including signal descriptions, interrupt interfaces, write buffers, reset and initialization, and clock control.

The IntelDX4 processor speed multiplying options are detailed in this section. Reset and initialization, as it applies to all of the Military Intel486 processor family, is also documented here.

Use and operation of the Stop Clock, Auto HALT Power Down and other power-saving SL Technology features are described.

Section 10: ''Bus Operation.'' This section describes the Military Intel486 processor bus operation, including the data transfer mechanism and bus functional description.

Section 11: ''Testability.'' This section describes the testability of the Military Intel486 processors, including the built-in self test (BIST), on-chip cache testing, translation lookaside buffer (TLB) testing, tri-state output test mode, and boundary scan (JTAG).

Section 12: ''Debugging Support.'' This section describes the Military Intel486 processor debugging support, including the breakpoint instruction, single-step trap and debug registers. This section applies to all Military Intel486 processors.

Section 13: ''Instruction Set Summary.'' This section provides clock count and instruction encoding summaries for all the Military Intel486 processors.

Section 14: ''Differences between Military Intel486 Processors and Intel386™ Processors.'' This section lists the differences between the Military Intel486 processor family and the Intel386 processor family. Also described and documented are differences between the Intel386 with an Intel387™ math coprocessors and the Military Intel486 processors with on-chip floating point units. This section applies to all Military Intel486 processors.

Section 15: ''Electrical Data.'' This section lists the AC and DC specifications for all Military Intel486 processors. Processor specific information is listed in both common and separate tables and sections as appropriate.

Section 16: ''Mechanical Data.'' This section lists the mechanical and thermal data, including the package specifications (PGA and CQFP) for all Military Intel486 processors. Processor specific information is listed in both common and separate tables and sections as appropriate.

Appendix A: ''Features Determination.'' This section documents the CPUID function to determine the Military Intel486 processor family identification and processor specific information. This section applies to all Military Intel486 processors.

Appendix B: ''IBIS Models.'' This section provides a detailed sample listing of the types of I/O buffer modeling information available for the Military Intel486 processor family. This section applies to all Military Intel486 processors.

Appendix C: ''BSDL Listing.'' This section provides a sample listing of a BSDL file for the Military Intel486 processor family. This section applies to all Military Intel486 processors.

Appendix D: ''System Design Notes.'' This section provides design notes applicable to the use of System Management Mode and SMM routines with the Military Intel486 processor.

2.3 Documents Replaced by This Data Sheet

This Data Sheet contains all of the latest information for the Military Intel486 processor family and replaces the following documentation:

Military i486 ™ *DX Microprocessor Datasheet*, Order Number 271136

Military Intel486 ™ *DX2 Microprocessor Datasheet*, Order Number 271280

Military Intel486 ™ *Processor Family Datasheet*, Order Number 271329

3.0 PIN DESCRIPTION

3.1 Pin Assignments

The following figures show the pin assignments of each package type for the Military Intel486 processor product family. Tables are provided showing the pin differences between the existing Military Intel486 processor products and the Military Intel486 processor products.

168-Pin PGA—Pin Grid Array

- Package Diagram
- Pin Assignment Difference Table
- Pin Cross Reference by Pin Name

196-Lead CQFP—Quad Flat Pack

- Package Diagram
- Pin Assignment Difference Table
- Pin Assignment Table in numerical order

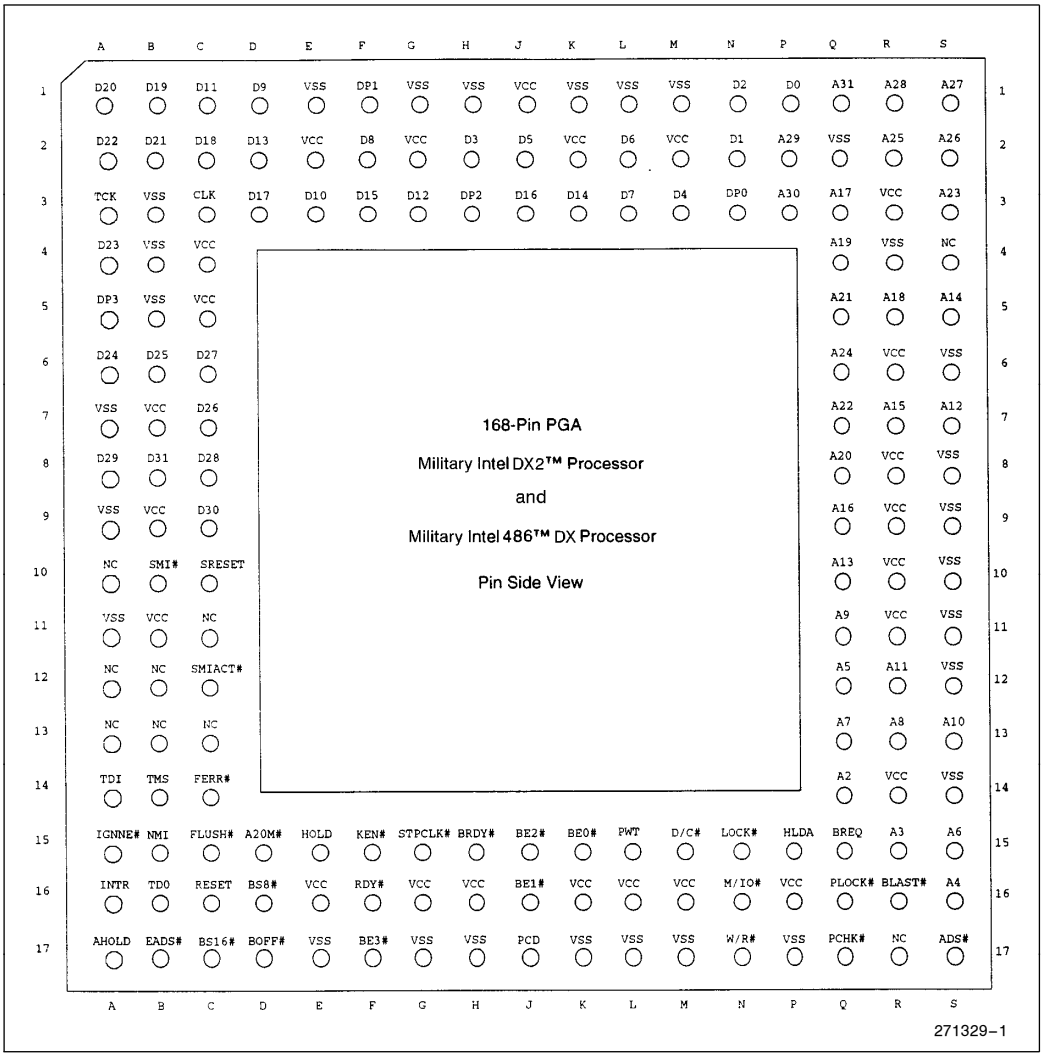


Figure 3-1. Package Diagram for 168-Pin PGA Package of the Military IntelDX2™ Processor and the Military Intel486™ DX Processor

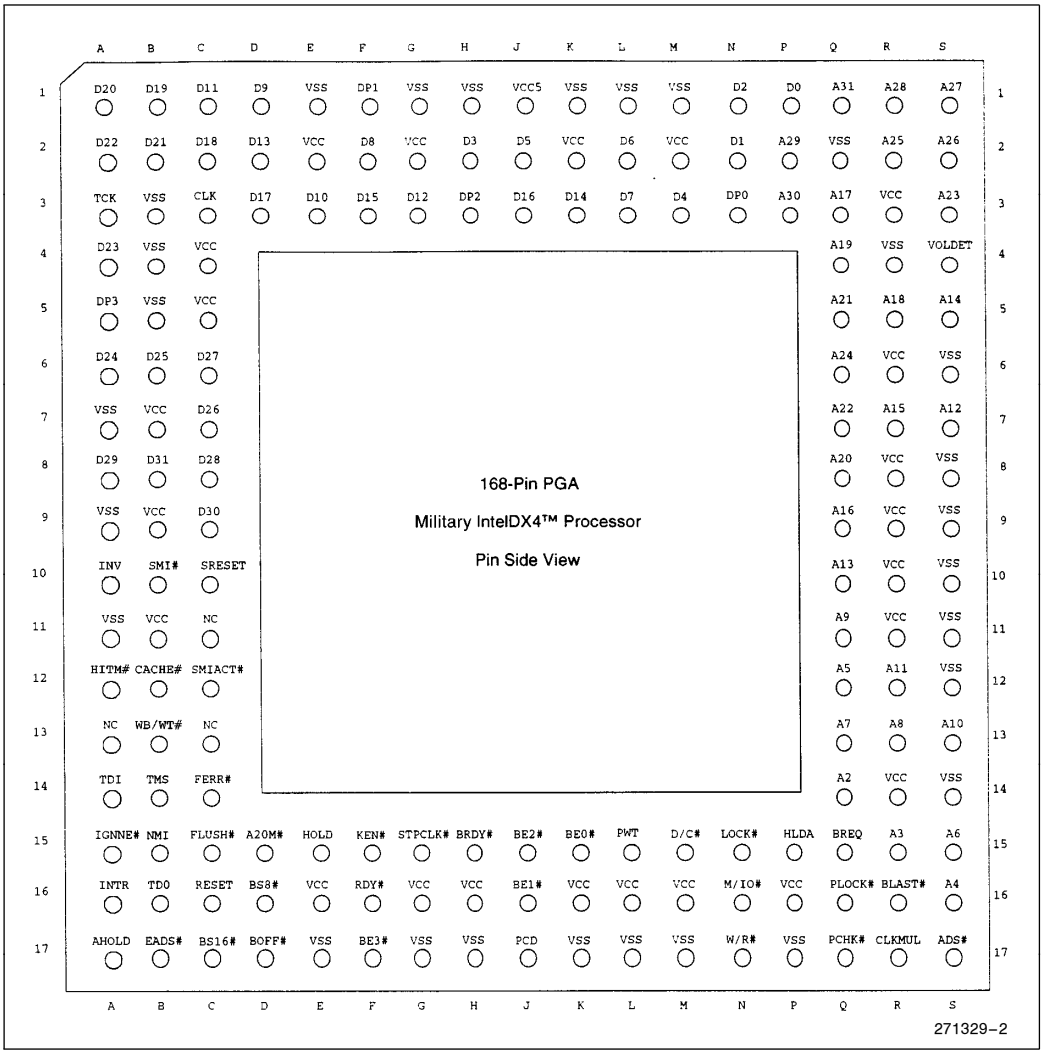


Figure 3-2. 168-Pin PGA Pinout Diagram (Pin Side) for the Military IntelDX4™ Processor

Table 3-1. Pinout Differences for 168-Pin PGA Package

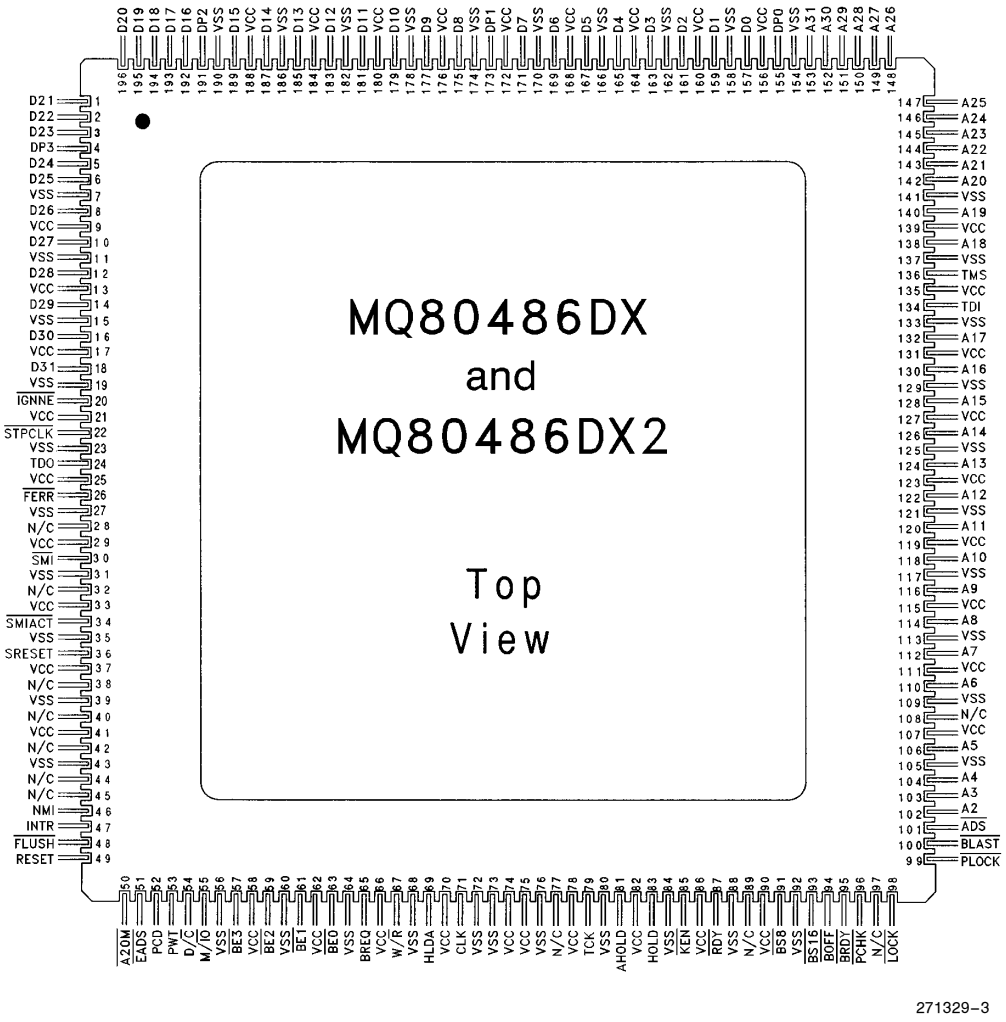
Pin	Previous Military Intel486 DX Processor(4)	Military Intel486 DX Processor	Previous IntelDX2™ Processor(4)	IntelDX2 Processor	IntelDX4™ Processor
A3(3)	NC	TCK	TCK	TCK	TCK
A14(3)	NC	TDI	TDI	TDI	TDI
B10(3)	NC	SMI#	NC	SMI#	SMI#
B14(3)	NC	TMS	TMS	TMS	TMS
B16(3)	NC	TDO	TDO	TDO	TDO
C10(3)	NC	SRESET	NC	SRESET	SRESET
C12	NC	SMIACT#	NC	SMIACT#	SMIACT#
G15(3)	NC	STPCLK#	NC	STPCLK#	STPCLK#
J1	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC5}(2)
R17	NC	NC	NC	NC	CLKMUL
S4	NC	NC	NC	NC	VOLDET
A10	NC	NC	NC	NC	INV
A12	NC	NC	NC	NC	HITM#
B12	NC	NC	NC	NC	CACHE#
B13	NC	NC	NC	NC	WB/WT#

NOTES:
1. NC. Do Not Connect. These pins should always remain unconnected. Connection of NC pins to V_{CC} or V_{SS} or to any other signal can result in component malfunction or incompatibility with future steppings of the Military Intel486 processors.
2. This pin location is for the V_{CC5} pin on the IntelDX4 processor. For compatibility with 3.3V processors that have 5V safe input buffers (i.e., IntelDX4 processors), this pin should be connected to a V_{CC} trace, not to the V_{CC} plane. See section 3.2, ''Quick Pin Reference,'' for a description of the V_{CC5} pin on the IntelDX4 processor.
3. These pins were No Connects on previous Military Intel486 DX and IntelDX2 processors. For compatibility with old designs, they can still be left unconnected.
4. Previous versions of the Military Intel486 processor family do not implement SL Technology and are not described in this data sheet.

Table 3-2. Pin Cross Reference for 168-Pin PGA Package of the IntelDX2™ Processor, Intel486™ DX Processor and IntelDX4™ Processor

Address	Data	Control	NC (2)	V_{CC}	V_{SS}
A2 .....Q14	D0.....P1	A20M# D15	A10	B7	A7
A3 .....R15	D1 .....N2	ADS# S17	A12	B9	A9
A4.....S16	D2 .....N1	AHOLD A17	A13	B11	A11
A5 .....Q12	D3 .....H2	BE0# K15	B12	C4	B3
A6.....S15	D4 .....M3	BE1# J16	B13	C5	B4
A7 .....Q13	D5 .....J2	BE2# J15	C11	E2	B5
A8 .....R13	D6 .....L2	BE3# F17	C13	E16	E1
A9 .....Q11	D7 .....L3	BLAST# R16	R17	G2	E17
A10 ....S13	D8 .....F2	BOFF# D17	S4	G16	G1
A11 ....R12	D9 .....D1	BRDY# H15		H16	G17
A12.....S7	D10 .....E3	BREQ Q15		J1	H17
A13 ....Q10	D11 .....C1	BS8# D16		K2	H1
A14.....S5	D12 .....G3	BS16# C17		K16	K1
A15 .....R7	D13 .....D2	CLK C3		L16	K17
A16 .....Q9	D14 .....K3	D/C# M15		M2	L1
A17 .....Q3	D15.....F3	DP0 .....N3		M16	L17
A18 .....R5	D16.....J3	DP1 .....F1		P16	M1
A19 .....Q4	D17 .....D3	DP2 .....H3		R3	M17
A20 .....Q8	D18 .....C2	DP3 .....A5		R6	P17
A21 .....Q5	D19 .....B1	EADS# B17		R8	Q2
A22 .....Q7	D20 .....A1	FERR# C14		R9	R4
A23.....S3	D21 .....B2	FLUSH# C15		R10	S6
A24 .....Q6	D22 .....A2	HLDA P15		R11	S8
A25 .....R2	D23 .....A4	HOLD E15		R14	S9
A26.....S2	D24 .....A6	IGNNE# A15		V_{CC5}(1)	S10
A27.....S1	D25 .....B6	INTR A16			S11
A28 .....R1	D26 .....C7	KEN# F15		J1	S12
A29.....P2	D27 .....C6	LOCK# N15			S14
A30.....P3	D28 .....C8	M/IO# N16			
A31 .....Q1	D29 .....A8	NMI B15			
	D30 .....C9	PCD J17			
	D31 .....B8	PCHK# Q17			
		PWT L15			
		PLOCK Q16			
		RDY# F16			
		RESET C16			
		SMI# B10			
		SMIACT# ...C12			
		W/R# N17			
		STPCLK# ..G15			
		SRESET C10			
		TCK A3			
		TDI A14			
		TDO B16			
		TMS B14			
		VOLDET(3) ...S4			
		CLKMUL(3) ..R17			
		CACHE#(3) .B12			
		HITM#(3) ...A12			
		INV(3).....A10			
		WB/WT#(3) .B13			

NOTES:
1. V_{CC5} is for the IntelDX4 processor only.
2. NC. Do Not Connect. These pins should always remain unconnected. Connection of NC pins to V_{CC} or V_{SS} or to any other signal can result in component malfunction or incompatibility with future steppings of the Military Intel486 processors.
3. Present only on the IntelDX4 processor.



NOTE:
SL Enhanced features not available on MQ80486DX. Pins 22, 30, 34, and 36 are "No Connects" on MQ80486DX.

Figure 3-3. 196-Pin Ceramic Quad Flatpack (CQFP) Pin Configuration—View from Lid Side

Military Intel486™ DX and Intel DX2™ CQFP Pin Cross Reference

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	D21	35	V_{SS}	69	HLDA	103	A3	137	V_{SS}	171	D7
2	D22	36	SRESET	70	V_{CC}	104	A4	138	A18	172	V_{CC}
3	D23	37	V_{CC}	71	CLK	105	V_{SS}	139	V_{CC}	173	DP1
4	DP3	38	N/C	72	V_{SS}	106	A5	140	A19	174	V_{SS}
5	D24	39	V_{SS}	73	V_{SS}	107	V_{CC}	141	V_{SS}	175	D8
6	D25	40	N/C	74	V_{CC}	108	N/C	142	A20	176	V_{CC}
7	V_{SS}	41	V_{CC}	75	V_{CC}	109	V_{SS}	143	A21	177	D9
8	D26	42	N/C	76	V_{SS}	110	A6	144	A22	178	V_{SS}
9	V_{CC}	43	V_{SS}	77	N/C	111	V_{CC}	145	A23	179	D10
10	D27	44	N/C	78	V_{CC}	112	A7	146	A24	180	V_{CC}
11	V_{SS}	45	N/C	79	TCK	113	V_{SS}	147	A25	181	D11
12	D28	46	NMI	80	V_{SS}	114	A8	148	A26	182	V_{SS}
13	V_{CC}	47	INTR	81	AHOLD	115	V_{CC}	149	A27	183	D12
14	D29	48	$\overline{FLUSH}$	82	V_{CC}	116	A9	150	A28	184	V_{CC}
15	V_{SS}	49	RESET	83	HOLD	117	V_{SS}	151	A29	185	D13
16	D30	50	$\overline{A20M}$	84	V_{SS}	118	A10	152	A30	186	V_{SS}
17	V_{CC}	51	$\overline{EADS}$	85	$\overline{KEN}$	119	V_{CC}	153	A31	187	D14
18	D31	52	PCD	86	V_{CC}	120	A11	154	V_{SS}	188	V_{CC}
19	V_{SS}	53	PWT	87	$\overline{RDY}$	121	V_{SS}	155	DP0	189	D15
20	$\overline{IGNNE}$	54	D/$\overline{C}$	88	V_{SS}	122	A12	156	V_{CC}	190	V_{SS}
21	V_{CC}	55	M/$\overline{IO}$	89	N/C	123	V_{CC}	157	D0	191	DP2
22	$\overline{STPCLK}$	56	V_{SS}	90	V_{CC}	124	A13	158	V_{SS}	192	D16
23	V_{SS}	57	$\overline{BE3}$	91	$\overline{BS8}$	125	V_{SS}	159	D1	193	D17
24	TDO	58	V_{CC}	92	V_{SS}	126	A14	160	V_{CC}	194	D18
25	V_{CC}	59	$\overline{BE2}$	93	$\overline{BS16}$	127	V_{CC}	161	D2	195	D19
26	$\overline{FERR}$	60	V_{SS}	94	$\overline{BOFF}$	128	A15	162	V_{SS}	196	D20
27	V_{SS}	61	$\overline{BE1}$	95	$\overline{BRDY}$	129	V_{SS}	163	D3		
28	N/C	62	V_{CC}	96	$\overline{PCHK}$	130	A16	164	V_{CC}		
29	V_{CC}	63	$\overline{BE0}$	97	N/C	131	V_{CC}	165	D4		
30	$\overline{SMI}$	64	V_{SS}	98	$\overline{LOCK}$	132	A17	166	V_{SS}		
31	V_{SS}	65	BREQ	99	$\overline{PLOCK}$	133	V_{SS}	167	D5		
32	N/C	66	V_{CC}	100	$\overline{BLAST}$	134	TDI	168	V_{CC}		
33	V_{CC}	67	W/$\overline{R}$	101	$\overline{ADS}$	135	V_{CC}	169	D6		
34	$\overline{SMIACT}$	68	V_{SS}	102	A2	136	TMS	170	V_{SS}		

NOTES:
No Connect (N/C) pins must not be connected.
SL Enhanced features not available on MQ80486DX. Pins 22, 30, 34, and 36 are ''No Connects'' on MQ80486DX.

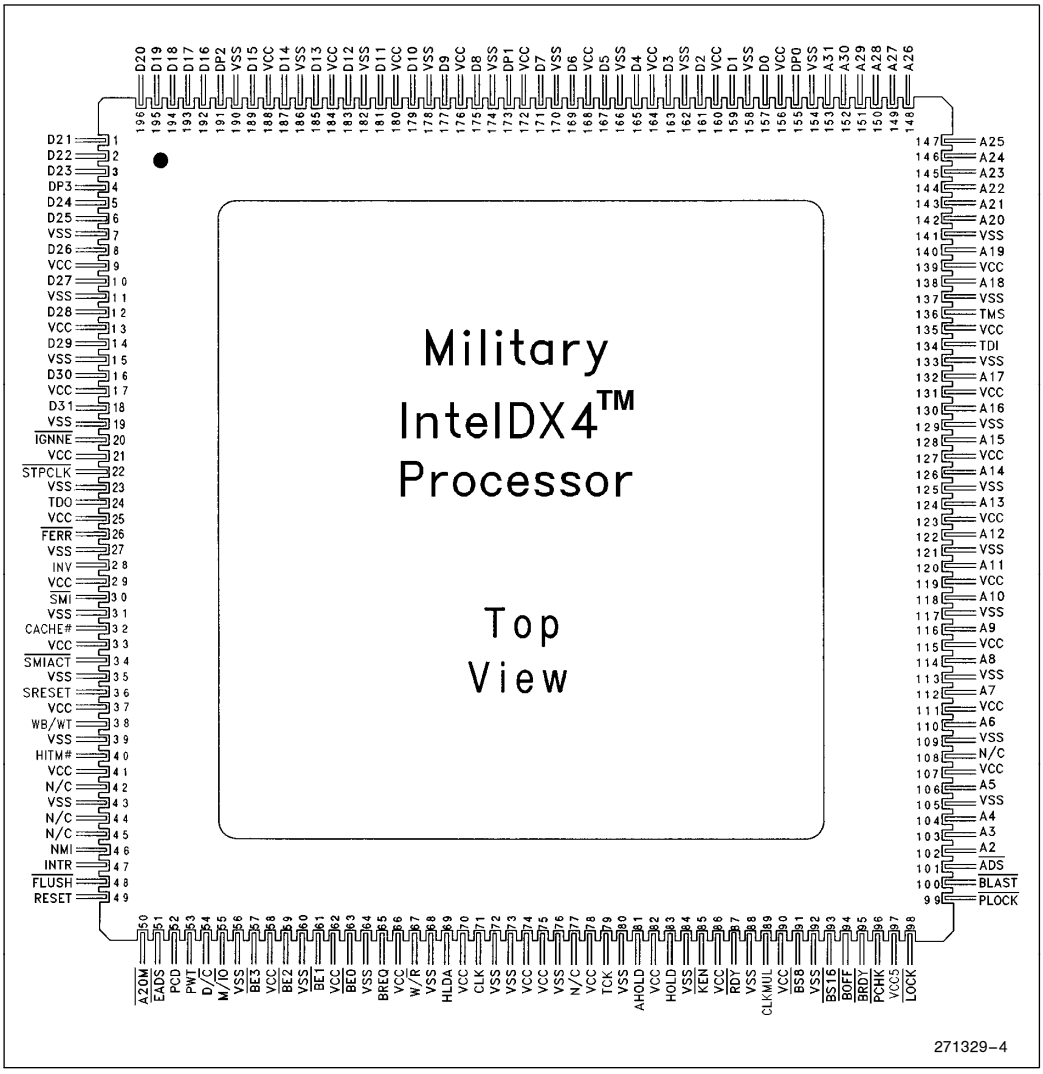


Figure 3-4. 196-Pin Ceramic Quad Flatpack (CQFP) Pin Configuration—View from Lid Side

Military IntelDX4™ CQFP Pin Cross Reference

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	D21	35	V_{SS}	69	HLDA	103	A3	137	V_{SS}	171	D7
2	D22	36	SRESET	70	V_{CC}	104	A4	138	A18	172	V_{CC}
3	D23	37	V_{CC}	71	CLK	105	V_{SS}	139	V_{CC}	173	DP1
4	DP3	38	WB/WT#	72	V_{SS}	106	A5	140	A19	174	V_{SS}
5	D24	39	V_{SS}	73	V_{SS}	107	V_{CC}	141	V_{SS}	175	D8
6	D25	40	HITM#	74	V_{CC}	108	N/C	142	A20	176	V_{CC}
7	V_{SS}	41	V_{CC}	75	V_{CC}	109	V_{SS}	143	A21	177	D9
8	D26	42	N/C	76	V_{SS}	110	A6	144	A22	178	V_{SS}
9	V_{CC}	43	V_{SS}	77	N/C	111	V_{CC}	145	A23	179	D10
10	D27	44	N/C	78	V_{CC}	112	A7	146	A24	180	V_{CC}
11	V_{SS}	45	N/C	79	TCK	113	V_{SS}	147	A25	181	D11
12	D28	46	NMI	80	V_{SS}	114	A8	148	A26	182	V_{SS}
13	V_{CC}	47	INTR	81	AHOLD	115	V_{CC}	149	A27	183	D12
14	D29	48	$\overline{FLUSH}$	82	V_{CC}	116	A9	150	A28	184	V_{CC}
15	V_{SS}	49	RESET	83	HOLD	117	V_{SS}	151	A29	185	D13
16	D30	50	$\overline{A20M}$	84	V_{SS}	118	A10	152	A30	186	V_{SS}
17	V_{CC}	51	$\overline{EADS}$	85	$\overline{KEN}$	119	V_{CC}	153	A31	187	D14
18	D31	52	PCD	86	V_{CC}	120	A11	154	V_{SS}	188	V_{CC}
19	V_{SS}	53	PWT	87	$\overline{RDY}$	121	V_{SS}	155	DP0	189	D15
20	$\overline{IGNNE}$	54	D/$\overline{C}$	88	V_{SS}	122	A12	156	V_{CC}	190	V_{SS}
21	V_{CC}	55	M/$\overline{IO}$	89	CLKMUL	123	V_{CC}	157	D0	191	DP2
22	$\overline{STPCLK}$	56	V_{SS}	90	V_{CC}	124	A13	158	V_{SS}	192	D16
23	V_{SS}	57	$\overline{BE3}$	91	$\overline{BS8}$	125	V_{SS}	159	D1	193	D17
24	TDO	58	V_{CC}	92	V_{SS}	126	A14	160	V_{CC}	194	D18
25	V_{CC}	59	$\overline{BE2}$	93	$\overline{BS16}$	127	V_{CC}	161	D2	195	D19
26	$\overline{FERR}$	60	V_{SS}	94	$\overline{BOFF}$	128	A15	162	V_{SS}	196	D20
27	V_{SS}	61	$\overline{BE1}$	95	$\overline{BRDY}$	129	V_{SS}	163	D3		
28	INV	62	V_{CC}	96	$\overline{PCHK}$	130	A16	164	V_{CC}		
29	V_{CC}	63	$\overline{BE0}$	97	V_{CC5}	131	V_{CC}	165	D4		
30	$\overline{SMI}$	64	V_{SS}	98	$\overline{LOCK}$	132	A17	166	V_{SS}		
31	V_{SS}	65	BREQ	99	$\overline{PLOCK}$	133	V_{SS}	167	D5		
32	CACHE#	66	V_{CC}	100	$\overline{BLAST}$	134	TDI	168	V_{CC}		
33	V_{CC}	67	W/$\overline{R}$	101	$\overline{ADS}$	135	V_{CC}	169	D6		
34	$\overline{SMIACT}$	68	V_{SS}	102	A2	136	TMS	170	V_{SS}		

NOTE:
No Connect (N/C) pins must not be connected.

3.2 Quick Pin Reference

The following is a brief pin description. For detailed signal descriptions refer to section 9.2, ''Signal Description.''

Table 3-3. Military Intel486™ Processor Pin Descriptions

Symbol	Type	Name and Function
CLK	I	**CLocK** provides the fundamental timing and the internal operating frequency for the Military Intel486 processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31–A4 **A2–A3**	I/O O	The **Address Lines.** A31–A2, together with the byte enables signals. BE0#–BE3#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the processor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE0–3#	O	The **Byte Enable** signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24–D31, BE2# applies to D16–D23, BE1# applies to D8–D15 and BE0# applies to D0–D7. BE0#–BE3# are active LOW and are not driven during bus hold.
DATA BUS		
D31–D0	I/O	The **Data Lines,** D0–D7, define the least significant byte of the data bus while lines D24–D31 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP0–DP3	I/O	There is one **Data Parity** pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the Military Intel486 processor. Even parity information must be driven back into the processor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the Military Intel486 processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP0–DP3 should be connected to V_{CC} through a pull-up resistor in systems that do not use parity. DP0–DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	**Parity Status** is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the processor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
BUS CYCLE DEFINITION		
M/IO# **D/C#** **W/R#**	O O O	The **memory/input-output, data/control** and **write/read** lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted. **M/IO# D/C# W/R# — Bus Cycle Initiated** 0 0 0 Interrupt Acknowledge 0 0 1 Halt/Special Cycle 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write The bus definition signals are not driven during bus hold and follow the timing of the address bus. Refer to section 10.2.11, ''Special Bus Cycles,'' for a description of the special bus cycles.
LOCK#	O	The **Bus Lock** pin indicates that the current bus cycle is locked. The Military Intel486 processor will not allow a bus hold when LOCK# is asserted (but address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. LOCK# is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active.
PLOCK#	O	The **Pseudo-Lock** pin indicates that the current bus transaction requires more than one bus cycle to complete. For the Military Intel486 processor, examples of such operations are segment table descriptor reads (64 bits), in addition to cache line fills (128 bits). The Military Intel486 processor will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. However during the first bus cycle of a 64-bit floating point write (for Military Intel486 processors with on-chip FPU), both PLOCK# and BLAST# will be asserted. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock RDY# is returned. PLOCK# is active LOW and is not driven during bus hold.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
BUS CONTROL		
ADS#	O	The **Address Status** output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock as the addresses are driven. ADS# is active LOW and is not driven during bus hold.
RDY#	I	The **Non-burst Ready** input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the Military Intel486 processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the processor while AHOLD is active. RDY# is active LOW, and is not provided with an internal pull-up resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.
BURST CONTROL		
BRDY#	I	The **Burst Ready** input performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the processor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. BRDY# is active LOW and is provided with a small pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	The **Burst Last** signal indicates that the next time BRDY# is returned the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	The **Reset** input forces the Military Intel486 processor to begin execution at a known state. The processor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to insure proper processor operation. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
INTERRUPTS (Continued)		
INTR	I	The **Maskable Interrupt** indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The Military Intel486 processor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	The **Non-Maskable Interrupt** request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SRESET	I	The **Soft Reset pin** duplicates all the functionality of the RESET pin with the following exception: 1. The SMBASE register will retain its previous value. For soft resets, SRESET should remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SMI#	I	The **System Management Interrupt** input is used to invoke the System Management Mode (SMM). SMI# is a falling edge triggered signal which forces the processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The processor will latch the falling edge of one pending SMI# signal while the processor is executing an existing SMI#. The nested SMI# will not be recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	The **System Management Interrupt ACTive** is an active low output, indicating that the processor is operating in SMM. It is asserted when the processor begins to execute the SMI# state save sequence and will remain active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	The **SToP CLocK request** input signal indicates a request has been made to turn off the CLK input. When the processor recognizes a STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, empty all internal pipelines and the write buffers and generate a Stop Grant acknowledge bus cycle. STPCLK# is active LOW and is provided with an internal pull-up resistor. **STPCLK# is an asynchronous signal, but must remain active until the processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle.**

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
BUS ARBITRATION		
BREQ	O	The **Bus Request** signal indicates that the Military Intel486 processor has internally generated a bus request. BREQ is generated whether or not the Military Intel486 processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	The **Bus Hold** *request* allows another bus master complete control of the processor bus. In response to HOLD going active the Military Intel486 processor will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The Military Intel486 processor will remain in this state until HOLD is de-asserted. HOLD is active high and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.
HLDA	O	**Hold Acknowledge** goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Military Intel486 processor has given the bus to another local bus master. HLDA is driven active in the same clock that the Military Intel486 processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	The **Backoff** input forces the Military Intel486 processor to float its bus in the next clock. The processor will float all pins normally floated during bus hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The processor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	The **Address Hold** request allows another bus master access to the processor's address bus for a cache invalidation cycle. The Military Intel486 processor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pull-down resistor. For proper operation AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	This signal indicates that a *valid* **External Address** has been driven onto the Military Intel486 processor address pins. This address will be used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	The **Cache Enable** pin is used to determine whether the current cycle is cacheable. When the Military Intel486 processor generates a cycle that can be cached and KEN# is active one clock before RDY# or BRDY# during the first transfer of the cycle, the cycle will become a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pull-up resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	The **Cache Flush** input forces the Military Intel486 processor to flush its entire internal cache. FLUSH# is active low and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
PAGE CACHEABILITY		
PWT **PCD**	O O	The **Page Write-Through** and **Page Cache Disable** pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry, page directory entry or control register 3 (CR3) when paging is enabled. If paging is disabled, the processor ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT pins. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C#, and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.
BUS SIZE CONTROL		
BS16# **BS8#**	I I	The **Bus Size 16** and **Bus Size 8** pins (bus sizing pins) cause the Military Intel486 processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Military Intel486 processor to determine the bus size. These signals are active LOW and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	When the **Address Bit 20 Mask** pin is asserted, the Military Intel486 processor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte, which occurs on the 8086 processor. A20M# is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled high at the falling edge of RESET.
TEST ACCESS PORT		
TCK	I	**Test ClocK** is an input to the Military Intel486 processor and provides the clocking function required by the JTAG Boundary scan feature. TCK is used to clock state information and data into component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the part on the falling edge of TCK and TDO. TCK is provided with an internal pull-up resistor.
TDI	I	**Test Data Input** is the serial input used to shift JTAG instructions and data into component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR TAP controller states. During all other tap controller states, TDI is a ‘‘don’t care.’’ TDI is provided with an internal pull-up resistor.
TDO	O	**Test Data Output** is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state.
TMS	I	**Test Mode Select** is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller TMS is provided with an internal pull-up resistor.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
NUMERIC ERROR REPORTING FOR MILITARY INTEL486 DX, INTELDX2™, AND INTELDX4™ PROCESSORS		
FERR#	O	The **Floating point ERRor** pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ Math CoProcessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# will not go active if FP errors are masked in FPU register. FERR# is active LOW, and is not floated during bus hold.
IGNNE#	I	When the **IGNore Numeric Error** pin is asserted the processor will ignore a numeric error and continue executing non-control floating point instructions, but FERR# will still be activated by the processor. When IGNNE# is de-asserted the processor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pull-up resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
INTELDX4 PROCESSOR CLKMUL, VCC5, AND VOLDET		
CLKMUL	I	The **CLocK MULtiplier** input, defined during device RESET, defines the ratio of internal core frequency to external bus frequency. If sampled low, the core frequency operates at twice the external bus frequency (speed doubled mode). If driven high or left floating, speed triple mode is selected. CLKMUL has an internal pull-up speed to V_{CC} and may be left floating in designs that select speed tripled clock mode.
V_{CC5}	I	The **5V reference voltage** input is the reference voltage for the 5V-tolerant I/O buffers. This signal should be connected to $+5V \pm 5\%$ for use with 5V logic. If all inputs are from 3V logic, this pin should be connected to 3.3V.
VOLDET	O	A **VOLtage DETect** signal allows external system logic to distinguish between a 5V Military Intel486 processor and the 3.3V IntelDX4 processor. This signal is active low for a 3.3V IntelDX4 processor.
WRITE-BACK ENHANCED IntelDX4 PROCESSOR SIGNAL PINS		
CACHE#	O	The **CACHE#** output indicates internal cacheability on read cycles and burst write-back on write cycles. CACHE# is asserted for cacheable reads, cacheable code fetches and write-backs. It is driven inactive for non-cacheable reads, I/O cycles, special cycles, and write-through cycles.

Table 3-3. Military Intel486™ Processor Pin Descriptions (Continued)

Symbol	Type	Name and Function
WRITE-BACK ENHANCED IntelDX4 PROCESSOR SIGNAL PINS (Continued)		
FLUSH#	I	**Cache FLUSH#** is an existing pin that operates differently if the processor is configured as Enhanced Bus mode (write-back). FLUSH# will cause the processor to write back all modified lines and flush (invalidate) the cache. FLUSH# is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
HITM#	O	The **Hit/Miss to a Modified Line** pin is a cache coherency protocol pin that is driven only in Enhanced Bus mode. When a snoop cycle is run, HITM# indicates that the processor contains the snooped line and that the line has been modified. Assertion of HITM# implies that the line will be written back in its entirety, unless the processor is already in the process of doing a replacement write-back of the same line.
INV	I	The **Invalidation Request** pin is a cache coherency protocol pin that is used only in the Enhanced Bus mode. It is sampled by the processor on EADS#-driven snoop cycles. It is necessary to assert this pin to get the effect of the processor invalidate cycle on write-through-only lines. INV also invalidates the write-back lines. However, if the snooped line is modified, the line will be written back and then invalidated. INV must satisfy setup and hold times t_{12} and t_{13} for proper operation.
PLOCK#	O	In the Enhanced bus mode, **Pseudo-Lock Output** is always driven inactive. In this mode, a 64-bit data read (caused by an FP operand access or a segment descriptor read) is treated as a multiple cycle read request, which may be a burst or a non-burst access based on whether BRDY# or RDY# is returned by the system. Because only write-back cycles (caused by Snoop write-back or replacement write-back) are write burstable, a 64-bit write will be driven out as two non-burst bus cycles. BLAST# is asserted during both writes. Refer to the Bus Functional Description section 10.3 for details on Pseudo-Locked bus cycles.
SRESET	I	For the Write-Back Enhanced Intel486 processors, **Soft RESET** operates similar to other Intel486 processors. On SRESET, the internal SMRAM base register retains its previous value, does not flush, write-back or disable the internal cache. Because SRESET is treated as an interrupt, it is possible to have a bus cycle while SRESET is asserted. SRESET is serviced only on an instruction boundary. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
WB/WT#	I	The **Write-Back/Write-Through** pin enables Enhanced Bus mode (write-back cache). It also defines a cached line as write-through or write-back. For cache configuration, WB/WT# must be valid during RESET and be active for at least two clocks before and two clocks after RESET is de-asserted. To define write-back or write-through configuration of a line, WB/WT# is sampled in the same clock as the first RDY# or BRDY# is returned during a line fill (allocation) cycle.

Table 3-4. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE3#–BE0#	LOW	Bus Hold
PWT, PCD	HIGH/LOW	Bus Hold
W/R#, M/IO#, D/C#	HIGH/LOW	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR#	LOW	
A3–A2	N/A	Bus, Address Hold
SMIACT#	LOW	
VOLDET(1)	LOW	
CACHE#(1)	LOW	Bus, Address Hold
HITM#(1)	LOW	Bus, Address Hold

NOTE:
1. Present on the IntelDX4 processor only.

Table 3-5. Input/Output Pins

Name	Active Level	When Floated
D31–D0	HIGH/LOW	Bus Hold
DP3–DP0	HIGH	Bus Hold
A31–A4	HIGH/LOW	Bus, Address Hold

Table 3-6. Test Pins

Name	Input or Output	Sampled/Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

Table 3-7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Pull-Up/ Pull-Down
CLK			
RESET	HIGH	Asynchronous	
SRESET	HIGH	Asynchronous	Pull-Down
HOLD	HIGH	Synchronous	
AHOLD	HIGH	Synchronous	Pull-Down
EADS#	LOW	Synchronous	Pull-Up
BOFF#	LOW	Synchronous	Pull-Up
FLUSH#	LOW	Asynchronous	Pull-Up
A20M#	LOW	Asynchronous	Pull-Up
BS16#, BS8#	LOW	Synchronous	Pull-Up
KEN#	LOW	Synchronous	Pull-Up
RDY#	LOW	Synchronous	
BRDY#	LOW	Synchronous	Pull-Up
INTR	HIGH	Asynchronous	
NMI	HIGH	Asynchronous	
IGNNE#	LOW	Asynchronous	Pull-Up
SMI#	LOW	Asynchronous	Pull-Up
STPCLK#	LOW	Asynchronous	Pull-Up
TCK	HIGH		Pull-Up
TDI	HIGH		Pull-Up
TMS	HIGH		Pull-Up
CLKMUL# (1)	N/A		Pull-Up
WB/WT#(1)	HIGH/ LOW	Synchronous	Pull-Down
INV(1)	HIGH	Synchronous	Pull-Up

NOTE:
1. Present on the IntelDX4 processor only.

4.0 ARCHITECTURAL OVERVIEW

4.1 Introduction

The Military Intel486 processor family is a 32-bit architecture with on-chip memory management, floating point, and cache memory units. Figure 4-1 is a block diagram of the Military Intel486 processor family. The Military Intel486 processor contains all the features of the Intel386™ processor with enhancements to increase performance.

The Military Intel486 processor instruction set includes the complete Intel386 processor instruction set along with extensions to serve new applications and increase performance. The on-chip memory management unit (MMU) is completely compatible with the Intel386 processor MMU. Software written for previous members of the Intel architecture family will run on the Military Intel486 processor without any modifications.

On-chip cache memory allows frequently used data and code to be stored on-chip reducing accesses to the external bus. RISC design techniques reduce instruction cycle times. A burst bus feature enables fast cache fills.

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4-Kbyte segments. To implement a virtual memory system, full restartability for all page and segment faults is supported.

Memory is organized into one or more variable length segments, each up to four Gbytes (232 bytes) in size. A segment can have attributes associated with it which include its location, size, type (i.e., stack, code or data), and protection characteristics. Each task on a Military Intel486 processor can have a maximum of 16,381 segments and each are up to four Gbytes in size. Thus, each task has a maximum of 64 terabytes (trillion bytes) of virtual memory.

The segmentation unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows the design of systems with a high degree of software integrity.

The Military Intel486 processor has two modes of operation: Real Address Mode (Real Mode) and Protected Mode Virtual Address Mode (Protected Mode). In Real Mode the Military Intel486 processor operates as a very fast 8086. Real Mode is required primarily to set up the Military Intel486 processor for Protected Mode operation. Protected Mode provides access to the sophisticated memory management paging and privilege capabilities of the processor.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each Virtual 8086 task behaves with 8086 semantics, allowing 8086 processor software (an application program or an entire operating system) to execute.

System Management Mode (SMM) provides the system designer with a means of adding new software controlled features to their computer products that always operate transparently to the Operating System (OS) and software applications. SMM is intended for use only by system firmware, not by applications software or general purpose systems software.

The on-chip cache is 16 Kbytes in size for the IntelDX4 processor and 8 Kbytes in size for all other members of the Military Intel486 processor family. It is 4-way set associative and follows a write-through policy. The on-chip cache includes features to provide flexibility in external memory system design. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware. The Write-Back Enhanced IntelDX4 Processor can be set to use an on-chip write-back cache policy.

The Military Intel486 processor also has features that facilitate high-performance hardware designs. The 1X bus clock input eases high-frequency board-level designs. The clock multiplier on IntelDX2 and IntelDX4 processors improves execution performance without increasing board design complexity. The clock multiplier enhances all operations operating out of the cache and/or not blocked by external bus accesses. The burst bus feature enables fast cache fills.

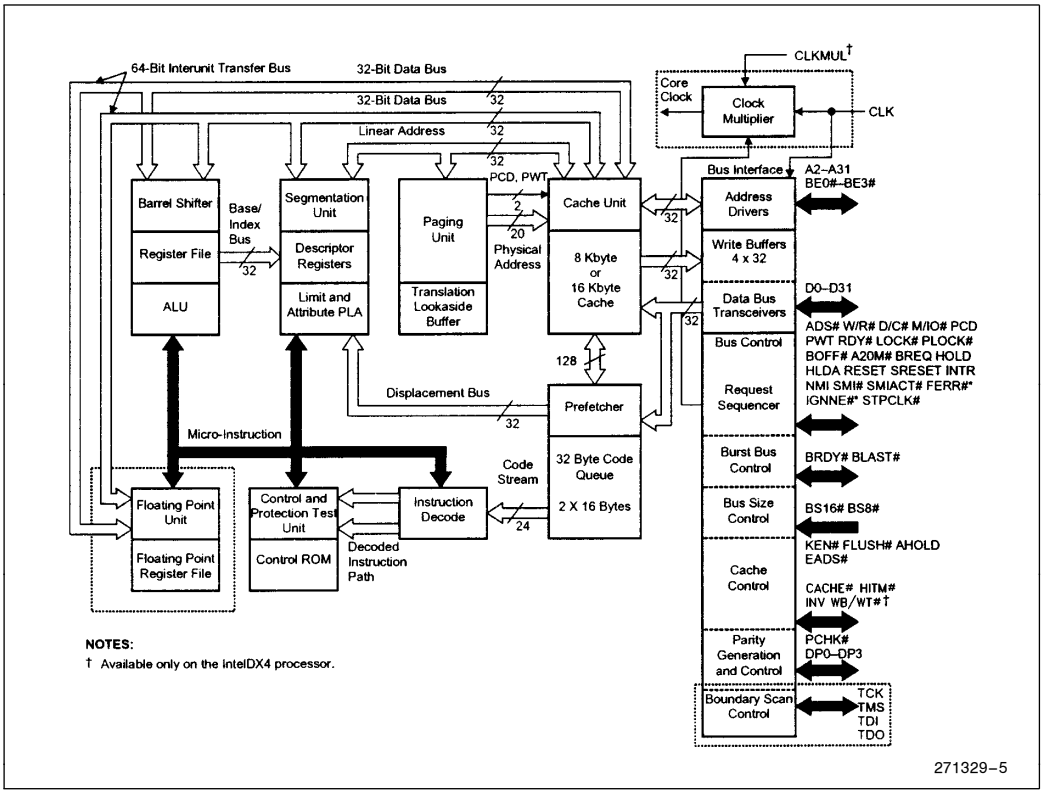


Figure 4-1. Military Intel486™ Processor Block Diagram

4.1.1 MILITARY INTEL486 DX, INTELDX2™, AND INTELDX4™ PROCESSOR ON-CHIP FLOATING POINT UNIT

The Military Intel486 DX, IntelDX2, and IntelDX4 processors incorporate the basic Military Intel486 processor 32-bit architecture with on-chip memory management and cache memory units. They also have an on-chip floating point unit (FPU) that operates in parallel with the arithmetic and logic unit. The FPU provides arithmetic instructions for a variety of numeric data types and executes numerous built-in transcendental functions (e.g., tangent, sine, cosine, and log functions). The floating point unit fully conforms to the ANSI/IEEE standard 754-1985 for floating point arithmetic.

All software written for the Intel386 processor, Intel387 math coprocessor and previous members of the 86/87 architectural family will run on these processors without any modifications.

4.2 Register Set

The Military Intel486 processor register set can be split into the following categories:

- Base Architecture Registers
  - — General Purpose Registers
  - — Instruction Pointer
  - — Flags Register
  - — Segment Registers

- Systems Level Registers
  - — Control Registers
  - — System Address Registers
- Debug and Test Registers

The base architecture and floating point registers (see below) are accessible by the applications program. The system level registers can only be accessed at privilege level 0 and used by system level programs. The debug and test registers also can only be accessed at privilege level 0.

4.2.1 FLOATING POINT REGISTERS

In addition to the registers listed above, the Military Intel486 DX, IntelDX2, and IntelDX4 processors also have the following:

- Floating Point Registers
  - — Data Registers
  - — Tag Word
  - — Status Word
  - — Instruction and Data Pointers
  - — Control Word

4.2.2 BASE ARCHITECTURE REGISTERS

Figure 4-2 shows the Military Intel486 processor base architecture registers. The contents of these registers are task-specific and are automatically loaded with a new context upon a task switch operation.

The base architecture includes six directly accessible descriptors, each specifying a segment up to 4 Gbytes in size. The descriptors are indicated by the selector values placed in the Military Intel486 processor segment registers. Various selector values can be loaded as a program executes.

The selectors are also task-specific, so the segment registers are automatically loaded with new context upon a task switch operation.

NOTE:
In register descriptions, ''set'' means ''set to 1,'' and ''reset'' means ''reset to 0.''

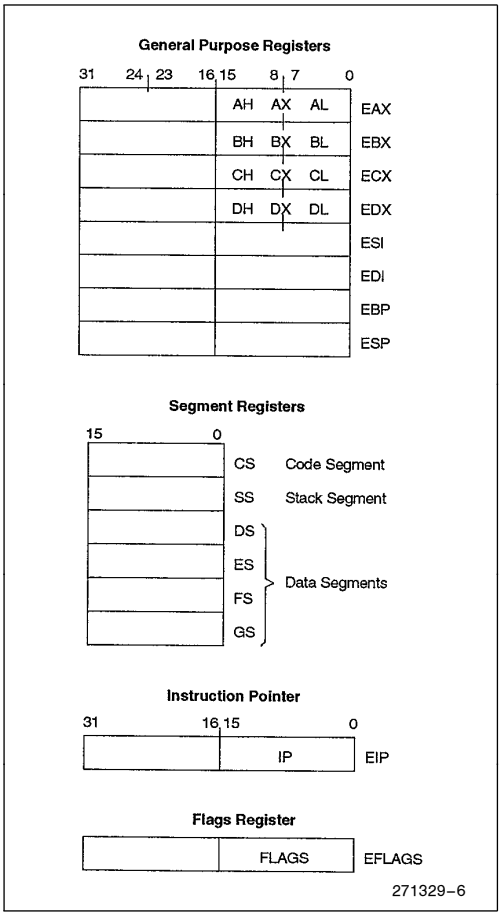


Figure 4-2. Base Architecture Registers

4.2.2.1 General Purpose Registers

The eight 32-bit general purpose registers are shown in Figure 4-2. These registers hold data or address quantities. The general purpose registers can support data operands of 1, 8, 16 and 32 bits, and bit fields of 1 to 32 bits. Address operands of 16 and 32 bits are supported. The 32-bit registers are named EAX, EBX, ECX, EDX, ESI, EDI, EBP and ESP.

The least significant 16 bits of the general purpose registers can be accessed separately by using the 16-bit names of the registers AX, BX, CX, DX, SI, DI, BP and SP. The upper 16 bits of the register are not changed when the lower 16 bits are accessed separately.

Finally, 8-bit operations can individually access the lower byte (bits 0–7) and the highest byte (bits 8–15) of the general purpose registers AX, BX, CX and DX. The lowest bytes are named AL, BL, CL and DL respectively. The higher bytes are named AH, BH, CH and DH respectively. The individual byte accessibility offers additional flexibility for data operations, but is not used for effective address calculation.

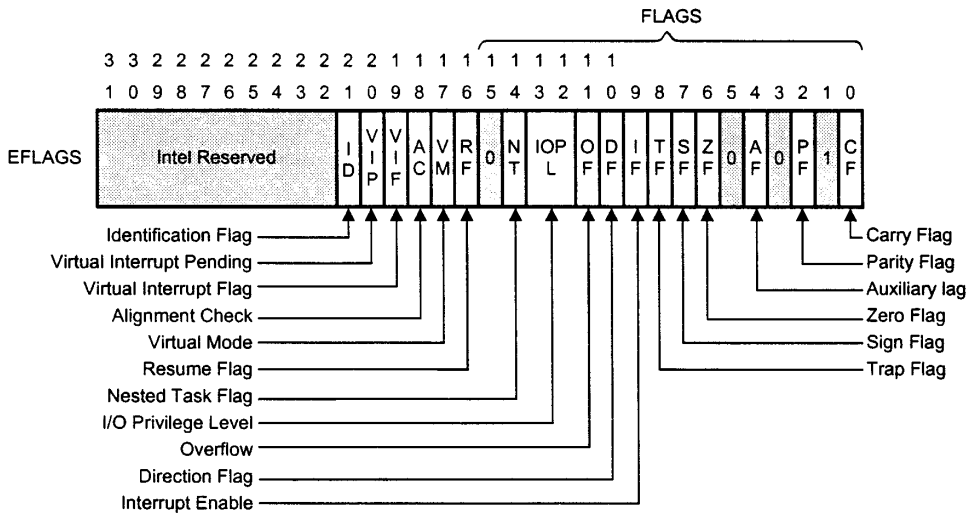
4.2.2.2 Instruction Pointer

The instruction pointer shown in Figure 4-2 is a 32-bit register named EIP. EIP holds the offset of the next instruction to be executed. The offset is always relative to the base of the code segment (CS). The lower 16 bits (bits 0–15) of the EIP contain the 16-bit instruction pointer named IP, which is used for 16-bit addressing.

4.2.2.3 Flags Register

The flags register is a 32-bit register named EFLAGS. The defined bits and bit fields within EFLAGS control certain operations and indicate status of the Military Intel486 processor. The lower 16 bits (bit 0–15) of EFLAGS contain the 16-bit register named FLAGS, which is most useful when executing 8086 and 80286 processor code. EFLAGS is shown in Figure 4-3.

EFLAGS bits 1, 3, 5, 15 and 22–31 are defined as "Intel Reserved." When these bits are stored during interrupt processing or with a PUSHF instruction (push flags onto stack), a one is stored in bit 1 and zeros in bits 3, 5, 15 and 22–31.



NOTE:
See section 4.2.7 "Compatibility."

Figure 4-3. Flag Registers

ID (Identification Flag, bit 21)

The ability of a program to set and clear the ID flag indicates that the processor supports the CPUID instruction. (Refer to section 13, ''Instruction Set Summary,'' and Appendix A, ''Feature Determination: CPUID Instruction.'')

VIP (Virtual Interrupt Pending Flag, bit 20)

The VIP flag together with the VIF enable each applications program in a multitasking environment to have virtualized versions of the system's IF flag.

VIF (Virtual Interrupt Flag, bit 19)

The VIF is a virtual image of IF (the interrupt flag) used with VIP.

AC (Alignment Check, bit 18)

The AC bit is defined in the upper 16 bits of the register. It enables the generation of faults if a memory reference is to a misaligned address. Alignment faults are enabled when AC is set to 1. A misaligned address is a word access an odd address, a dword access to an address that is not on a dword boundary, or an 8-byte reference to an address that is not on a 64-bit word boundary. (See section 10.1.5, ''Operand Alignment.'')

Alignment faults are only generated by programs running at privilege level 3. The AC bit setting is ignored at privilege levels 0, 1 and 2. Note that references to the descriptor tables (for selector loads), or the task state segment (TSS), are implicitly level 0 references even if the instructions causing the references are executed at level 3. Alignment faults are reported through interrupt 17, with an error code of 0. Table 4-1 gives the alignment required for the Military Intel486 processor data types.

Table 4-1. Data Type Alignment Requirements

Memory Access	Alignment (Byte Boundary)
Word	2
Dword	4
Single Precision Real	4
Double Precision Real	8
Extended Precision Real	8
Selector	2
48-Bit Segmented Pointer	4
32-Bit Flat Pointer	4
32-Bit Segmented Pointer	2
48-Bit ''Pseudo-Descriptor''	4
FSTENV/FLDENV Save Area	4/2 (On Operand Size)
FSAVE/FRSTOR Save Area	4/2 (On Operand Size)
Bit String	4

IMPLEMENTATION NOTE:

Several instructions on the Military Intel486 processor generate misaligned references, even if their memory address is aligned. For example, on the Military Intel486 processor, the SGDT/SIDT (store global/interrupt descriptor table) instruction reads/writes two bytes, and then reads/writes four bytes from a ''pseudo-descriptor'' at the given address. The Military Intel486 processor will generate misaligned references unless the address is on a 2 mod 4 boundary. The FSAVE and FRSTOR instructions (floating point save and restore state) will generate misaligned references for one-half of the register save/restore cycles. The Military Intel486 processor will not cause any AC faults if the effective address given in the instruction has the proper alignment.

VM (Virtual 8086 Mode, bit 17)

The VM bit provides Virtual 8086 Mode within Protected Mode. If set while the Military Intel486 processor is in Protected Mode, the Military Intel486 processor will switch to Virtual 8086 operation, handling segment loads as the 8086 processor does, but generating exception 13 faults on privileged opcodes. The VM bit can be set only in Protected Mode, by the IRET instruction (if current privilege level = 0) and by task switches at any privilege level. The VM bit is unaffected by POPF. PUSHF always pushes a 0 in this bit, even if executing in Virtual 8086 Mode. The EFLAGS image pushed during interrupt processing or saved during task switches will contain a 1 in this bit if the interrupted code was executing as a Virtual 8086 Task.

RF (Resume Flag, bit 16)

The RF flag is used in conjunction with the debug register breakpoints. It is checked at instruction boundaries before breakpoint processing. When RF is set, it causes any debug fault to be ignored on the next instruction. RF is then automatically reset at the successful completion of every instruction (no faults are signaled) except the IRET instruction, the POPF instruction, (and JMP, CALL, and INT instructions causing a task switch). These instructions set RF to the value specified by the memory image. For example, at the end of the breakpoint service routine, the IRET instruction can pop an EFLAG image having the RF bit set and resume the program's execution at the breakpoint address without generating another breakpoint fault on the same location.

NT (Nested Task, bit 14)

The flag applies to Protected Mode. NT is set to indicate that the execution of this task is within another task. If set, it indicates that the current nested task's Task State Segment (TSS) has a valid back link to the previous task's TSS. This bit is set or reset by control transfers to other tasks. The value of NT in EFLAGS is tested by the IRET instruction to determine whether to do an inter-task return or an intra-task return. A POPF or an IRET instruction will affect the setting of this bit according to the image popped, at any privilege level.

IOPL (Input/Output Privilege Level, bits 12–13)

This two-bit field applies to Protected Mode. IOPL indicates the numerically maximum CPL (current privilege level) value permitted to execute I/O instructions without generating an exception 13 fault or consulting the I/O Permission Bitmap. It also indicates the maximum CPL value allowing alteration of the IF (INTR Enable Flag) bit when new values are popped into the EFLAG register. POPF and IRET instruction can alter the IOPL field when executed at CPL = 0. Task switches can always alter the IOPL field, when the new flag image is loaded from the incoming task's TSS.

OF (Overflow Flag, bit 11)

is set if the operation resulted in a signed overflow. Signed overflow occurs when the operation resulted in carry/borrow **into** the sign bit (high-order bit) of the result but did not result in a carry/borrow **out of** the high-order bit, or vice-versa. For 8-, 16-, 32-bit operations, OF is set according to overflow at bit 7, 15, 31, respectively.

DF (Direction Flag, bit 10)

DF defines whether ESI and/or EDI registers post decrement or post increment during the string instructions. Post increment occurs if DF is reset. Post decrement occurs if DF is set.

IF (INTR Enable Flag, bit 9)

IF flag, when set, allows recognition of external interrupts signaled on the INTR pin. When IF is reset, external interrupts signaled on the INTR are not recognized. IOPL indicates the maximum CPL value allowing alteration of the IF bit when new values are popped into EFLAGS or FLAGS.

TF (Trap Enable Flag, bit 8)

TF controls the generation of exception 1 trap when single-stepping through code. When TF is set, the Military Intel486 processor generates an exception 1 trap after the next instruction is executed. When TF is reset, exception 1 traps occur only as a function of the breakpoint addresses loaded into debug registers DR0–DR3.

SF (Sign Flag, bit 7)

SF is set if the high-order bit of the result is set, it is reset otherwise. For 8-, 16-, 32-bit operations, SF reflects the state of bit 7, 15, 31 respectively.

ZF (Zero Flag, bit 6)

ZF is set if all bits of the result are 0. Otherwise, it is reset.

AF (Auxiliary Carry Flag, bit 4)

The Auxiliary Flag is used to simplify the addition and subtraction of packed BCD quantities. AF is set if the operation resulted in a carry out of bit 3 (addition) or a borrow into bit 3 (subtraction). Otherwise, AF is reset. AF is affected by carry out of, or borrow into bit 3 only, regardless of overall operand length: 8, 16 or 32 bits.

PF (Parity Flags, bit 2)

PF is set if the low-order eight bits of the operation contains an even number of "1's" (even parity). PF is reset if the low-order eight bits have odd parity. PF is a function of only the low-order eight bits, regardless of operand size.

CF (Carry Flag, bit 0)

CF is set if the operation resulted in a carry out of (addition), or a borrow into (subtraction) the high-order bit. Otherwise, CF is reset. For 8-, 16- or 32-bit operations, CF is set according to carry/borrow at bit 7, 15 or 31, respectively.

4.2.2.4 Segment Registers

Six 16-bit segment registers hold segment selector values identifying the currently addressable memory segments. In protected mode, each segment may range in size from one byte up to the entire linear and physical address space of the machine, 4 Gbytes (2^{32} bytes). In real address mode, the maximum segment size is fixed at 64 Kbytes (2^{16} bytes).

The six addressable segments are defined by the segment registers CS, SS, DS, ES, FS and GS. The selector in CS indicates the current code segment; the selector in SS indicates the current stack segment; the selectors in DS, ES, FS and GS indicate the current data segments.

4.2.2.5 Segment Descriptor Cache Registers

The segment descriptor cache registers are not programmer visible, yet it is very useful to understand their content. A programmer invisible descriptor cache register is associated with each programmer-visible segment register, as shown by Figure 4-4. Each descriptor cache register holds a 32-bit base address, a 32-bit segment limit, and the other necessary segment attributes.

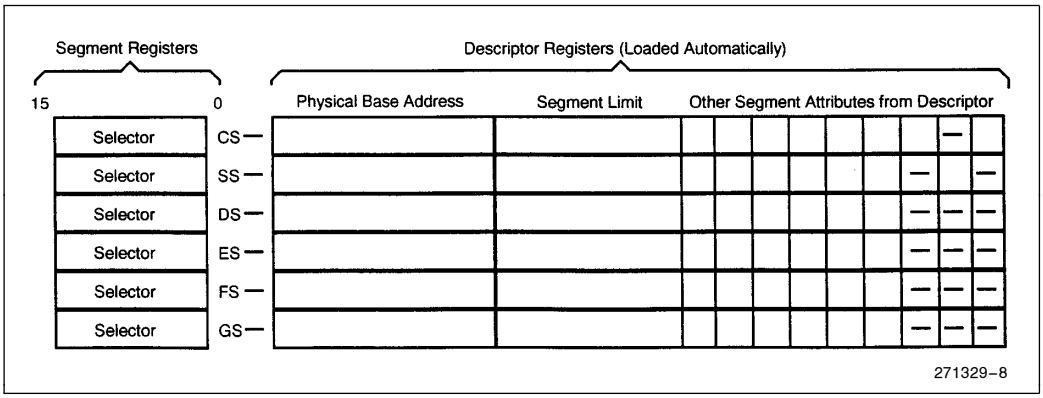


Figure 4-4. Military Intel486™ Processor Segment Registers and Associated Descriptor Cache Registers

When a selector value is loaded into a segment register, the associated descriptor cache register is automatically updated with the correct information. In Real Mode, only the base address is updated directly (by shifting the selector value four bits to the left), because the segment maximum limit and attributes are fixed in Real Mode. In Protected Mode, the base address, the limit, and the attributes are all updated per the contents of the segment descriptor indexed by the selector.

Whenever a memory reference occurs, the segment descriptor cache register associated with the segment being used is automatically involved with the memory reference. The 32-bit segment base address becomes a component of the linear address calculation, the 32-bit limit is used for the limit-check operation, and the attributes are checked against the type of memory reference requested.

4.2.3 SYSTEM LEVEL REGISTERS

Figure 4-5 illustrates the system level registers, which are the control operation of the on-chip cache, the on-chip floating point unit (on the Military Intel486 DX, IntelDX2, and IntelDX4 processors) and the segmentation and paging mechanisms. These registers are only accessible to programs running at privilege level 0, the highest privilege level.

The system level registers include three control registers and four segmentation base registers. The three control registers are CR0, CR2 and CR3. CR1 is reserved for future Intel processors. The four segmentation base registers are the Global Descriptor Table Register (GDTR), the Interrupt Descriptor Table Register (IDTR), the Local Descriptor Table Register (LDTR) and the Task State Segment Register (TR).

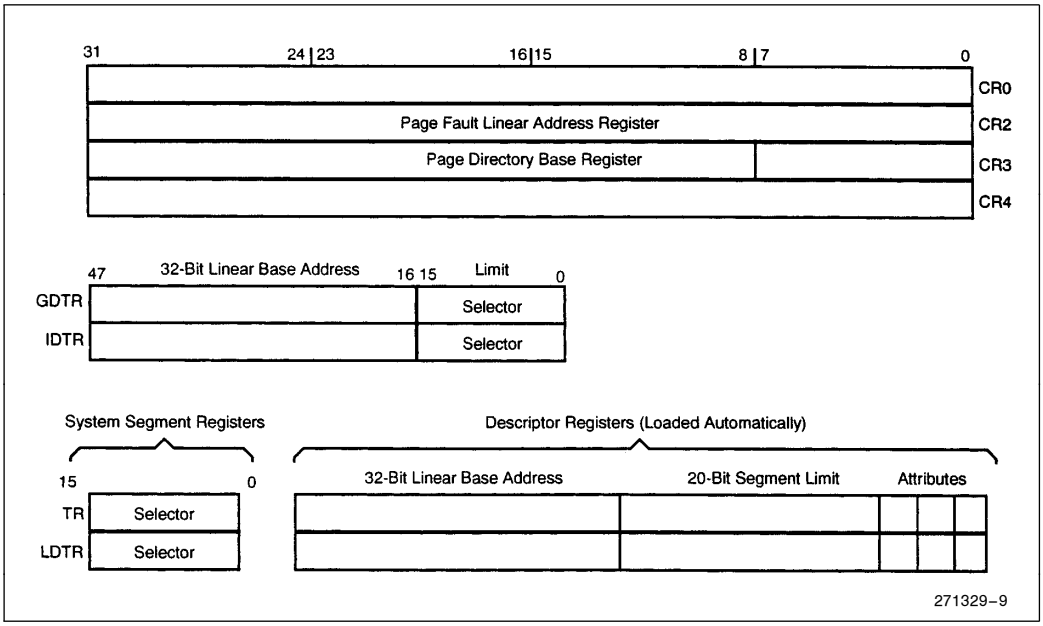
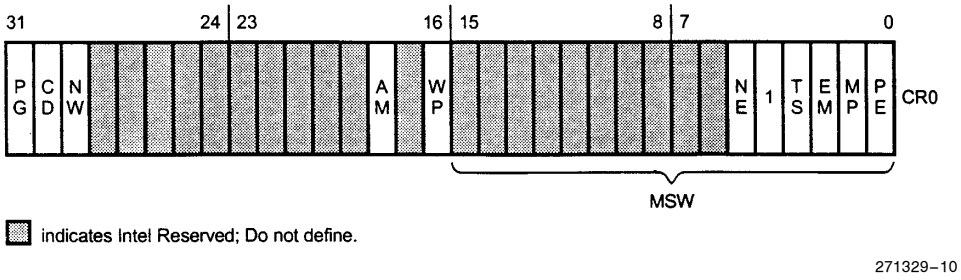


Figure 4-5. System Level Registers



NOTE:
See Section 4.2.7 ''Compatibility''.

Figure 4-6. Control Register 0

4.2.3.1 Control Registers

Control Register 0 (CR0)

CR0, shown in Figure 4-6, contains 10 bits for control and status purposes. The function of the bits in CR0 can be categorized as follows:

- Military Intel486 Processor Operating Modes: PG, PE (Table 4-2)
- On-Chip Cache Control Modes: CD, NW (Table 4-3)
- On-Chip Floating Point Unit: NE, TS, EM, TS (Tables 4-4 and 4-5).
- Alignment Check Control: AM
- Supervisor Write Protect: WP

Table 4-2. Military Intel486™ Processor Operating Modes

PG	PE	Mode
0	0	REAL Mode. Exact 8086 processor semantics, with 32-bit extensions available with prefixes.
0	1	Protected Mode. Exact 80286 processor semantics, plus 32-bit extensions through both prefixes and ''default'' prefix setting associated with code segment descriptors. Also, a sub-mode is defined to support a virtual 8086 processor within the context of the extended 80286 processor protection model.
1	0	UNDEFINED. Loading CR0 with this combination of PG and PE bits will raise a GP fault with error code 0.
1	1	Paged Protected Mode. All the facilities of Protected mode, with paging enabled underneath segmentation.

Table 4-3. On-Chip Cache Control Modes

CD	NW	Operating Mode
1	1	Cache fills disabled, write-through and invalidates disabled.
1	0	Cache fills disabled, write-through and invalidates enabled.
0	1	INVALID. If CR0 is loaded with this configuration of bits, a GP fault with error code is raised.
0	0	Cache fills enabled, write-through and invalidates enabled.

The low-order 16 bits of CR0 are also known as the Machine Status Word (MSW), for compatibility with the 80286 processor protected mode. LMSW and SMSW (load and store MSW) instructions are taken as special aliases of the load and store CR0 operations, where only the low-order 16 bits of CR0 are involved. The LMSW and SMSW instructions in the Military Intel486 processor work in an identical fashion to the LMSW and SMSW instructions in the 80286 processor (i.e., they only operate on the low-order 16 bits of CR0 and ignores the new bits). New Military Intel486 processor operating systems should use the MOV CR0, Reg instruction.

NOTE:

All Intel386 and Military Intel486 processor CR0 bits, except for ET and NE, are upwardly compatible with the 80286 processor, because they are in register bits not defined in the 80286 processor. For strict compatibility with the 80286 processor, the load machine status word (LMSW) instruction is defined to not change the ET or NE bits.

The defined CR0 bits are described below.

PG (Paging Enable, bit 31)

PG bit is used to indicate whether paging is enabled (PG = 1) or disabled (PG = 0). (See Table 4-2.)

CD (Cache Disable, bit 30)

The CD bit is used to enable the on-chip cache. When CD = 1, the cache will not be filled on cache misses. When CD = 0, cache fills may be performed on misses. (See Table 4-3.)

The state of the CD bit, the cache enable input pin (KEN#), and the relevant page cache disable (PCD) bit determine if a line read in response to a cache miss will be installed in the cache. A line is installed in the cache only if CD = 0 and KEN# and PCD are both zero. The relevant PCD bit comes from either the page table entry, page directory entry or control register 3. (Refer to section 7.6, ''Page Cacheability.'')

CD is set to one after RESET.

NW (Not Write-Through, bit 29)

The NW bit enables on-chip cache write-throughs and write-invalidate cycles (NW = 0).

When NW = 0, all writes, including cache hits, are sent out to the pins. Invalidate cycles are enabled when NW = 0. During an invalidate cycle a line will be removed from the cache if the invalidate address hits in the cache. (See Table 4-3.)

When NW = 1, write-throughs and write-invalidate cycles are disabled. A write will not be sent to the pins if the write hits in the cache. With NW = 1 the only write cycles that reach the external bus are cache misses. Write hits with NW = 1 will never update main memory. Invalidate cycles are ignored when NW = 1.

AM (Alignment Mask, bit 18)

The AM bit controls whether the alignment check (AC) bit in the flag register (EFLAGS) can allow an alignment fault. AM = 0 disables the AC bit. AM = 1 enables the AC bit. AM = 0 is the Intel386 processor compatible mode.

Intel386 processor software may load incorrect data into the AC bit in the EFLAGS register. Setting AM = 0 will prevent AC faults from occurring before the Military Intel486 processor has created the AC interrupt service routine.

WP (Write Protect, bit 16)

WP protects read-only pages from supervisor write access. The Intel386 processor allows a read-only page to be written from privilege levels 0–2. The Military Intel486 processor are compatible with the Intel386 processor when WP = 0. WP = 1 forces a fault on a write to a read-only page from any privilege level. Operating systems with Copy-on-Write features can be supported with the WP bit. (Refer to section 6.4.3 ''Page Level Protection (R/W, U/S Bits).'')

NOTE:

Refer to Tables 4-4 and 4-5 for values and interpolation of NE, EM, TS, and MP bits, in addition to the sections below.

NE (Numerics Exception, bit 5)

Military Intel486 DX, IntelDX2 and IntelDX4 Processor NE Bit

For Military Intel486 DX, IntelDX2, and IntelDX4 processors, the NE bit controls whether unmasked floating point exceptions (UFPE) are handled through interrupt vector 16 (NE = 1) or through an external interrupt (NE = 0). NE = 0 (default at reset) supports the DOS operating system error reporting scheme from the 8087, Intel287 and Intel387 math coprocessors. In DOS systems, math coprocessor errors are reported via external interrupt vector 13. DOS uses interrupt vector 16 for an operating system call. (Refer to sections 9.2.14, ''Numeric Error Reporting (FERR#, IGNNE#),'' and 10.2.14 ''Floating Point Error Handling.'')

For any UFPE, the floating point error output pin (FERR#) will be driven active.

For NE = 0, the Military Intel486 DX, IntelDX2 and IntelDX4 processors work in conjunction with the ignore numeric error input (IGNNE#) and the FERR# output pins. When a UFPE occurs and the IGNNE# input is inactive, the Military Intel486 DX, IntelDX2, and IntelDX4 processors freeze immediately before executing the next floating point instruction. An external interrupt controller will supply an interrupt vector when FERR# is driven active. The UFPE is ignored if IGNNE# is active and floating point execution continues.

NOTE:

The freeze does not take place if the next instruction is one of the control instructions FNCLEX, FNINIT, FNSAVE, FNSTENV, FNSTCW, FNSTSW, FNSTSW AX, FNENI, FNDISI and FNSETPM. The freeze does occur if the next instruction is WAIT.

For NE = 1, any UFPE will result in a software interrupt 16, immediately before executing the next non-control floating point or WAIT instruction. The ignore numeric error input (IGNNE#) signal will be ignored.

TS (Task Switch, bit 3)

Military Intel486 DX, IntelDX2, and IntelDX4 Processor TS Bit

For Military Intel486 DX, IntelDX2, and IntelDX4 processors, the TS bit is set whenever a task switch operation is performed. Execution of floating point instructions with TS = 1 will cause a Device Not Available (DNA) fault (trap vector 7). If TS = 1 and MP = 1 (monitor coprocessor in CR0), a WAIT instruction will cause a DNA fault.

EM (Emulate Coprocessor, bit 2)

Military Intel486 DX, IntelDX2, and IntelDX4 Processor EM Bit

For the Military Intel486 DX, IntelDX2, and IntelDX4 processors, the EM bit determines whether floating point instructions are trapped (EM = 1) or executed. If EM = 1, all floating point instructions will cause fault 7.

If EM = 0, the on-chip floating point will be used.

NOTE:

WAIT instructions are not affected by the state of EM. (See Table 4-5.)

MP (Monitor Coprocessor, bit 1)

Military Intel486 DX, IntelDX2, and IntelDX4 Processor MP Bit

For the Military Intel486 DX, IntelDX2, and IntelDX4 processors, the MP is used in conjunction with the TS bit to determine if WAIT instructions cause fault 7. (See Table 4-5.) The TS bit is set to 1 on task switches by the Military Intel486 DX, IntelDX2, and IntelDX4 processors. Floating point instructions are not affected by the state of the MP bit. It is recommended that the MP bit be set to one for normal processor operation.

PE (Protection Enable, bit 0)

The PE bit enables the segment based protection mechanism if PE = 1 protection is enabled. When PE = 0 the Military Intel486 processor operates in REAL mode, with segment based protection disabled, and addresses formed as in an 8086 processor. (Refer to Table 4-2.)

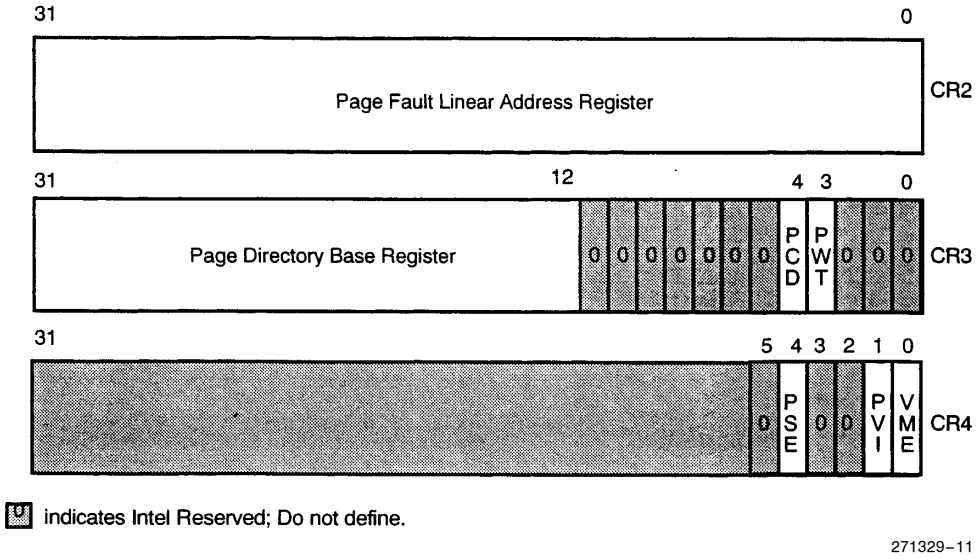
Table 4-4. Recommended Values of the Floating Point Related Bits for All Military Intel486™ Processors

CR0 Bit	Military Intel486 DX, IntelDX2™, and IntelDX4™ Processors
EM	0
MP	1
NE	0, for DOS Systems 1, for User-Defined Exception Handler

Table 4-5. Interpretation of Different Combinations of the EM, TS and MP Bits for All Military Intel486™ Processors

CR0 Bit			Instruction Type	
EM	TS	MP	Floating Point	Wait
0	0	0	Execute	Execute
0	0	1	Execute	Execute
0	1	0	Exception 7	Execute
0	1	1	Exception 7	Exception 7
1	0	0	Exception 7	Execute
1	0	1	Exception 7	Execute
1	1	0	Exception 7	Execute
1	1	1	Exception 7	Exception 7

NOTE:
For Military Intel486 DX, IntelDX2™ and IntelDX4™ processors, if MP = 1 and TS = 1, the processor will generate a trap 7 so that the system software can save the floating point status of the old task.



NOTE:
See section 4.2.7, "Compatibility."

Figure 4-7. Control Registers 2, 3 and 4

Control Register 1 (CR1)

CR1 is reserved for use in future Intel processors.

Control Register 2 (CR2)

CR2, shown in Figure 4-7, holds the 32-bit linear address that caused the last page fault detected. The error code pushed onto the page fault handler's stack when it is invoked provides additional status information on this page fault.

Control Register 3 (CR3)

CR3, shown in Figure 4-7, contains the physical base address of the page directory table. The page directory is always page aligned (4 Kbyte-aligned). This alignment is enforced by only storing bits 12–31 in CR3.

In the Military Intel486 processor, CR3 contains two bits, page write-through (PWT) (bit 3) and page cache disable (PCD) (bit 4). The page table entry (PTE) and page directory entry (PDE) also contain PWT and PCD bits. PWT and PCD control page cacheability. When a page is accessed in external memory, the state of PWT and PCD are driven out on the PWT and PCD pins. The source of PWT and PCD can be CR3, the PTE or the PDE. PWT and PCD are sourced from CR3 when the PDE is being updated. When paging is disabled (PG = 0 in CR0), PCD and PWT are assumed to be 0, regardless of their state in CR3.

A task switch through a task state segment (TSS) which changes the values in CR3, or an explicit load into CR3 with any value, will invalidate all cached page table entries in the translation lookaside buffer (TLB).

The page directory base address in CR3 is a physical address. The page directory can be paged out while its associated task is suspended, but the operating system must ensure that the page directory is resident in physical memory before the task is dispatched. The entry in the TSS for CR3 has a physical address, with no provision for a present bit. This means that the page directory for a task must be resident in physical memory. The CR3 image in a TSS must point to this area, before the task can be dispatched through its TSS.

Control Register 4 (CR4)

CR4, shown in Figure 4-7, contains bits that enable virtual mode extensions and protected mode virtual interrupts.

VME (Virtual-8086 Mode Extensions, bit 0 of CR4)

Setting this bit to 1 enables support for a virtual interrupt flag in virtual-8086 mode. This feature can improve the performance of virtual-8086 applications by eliminating the overhead of faulting to a virtual-8086 monitor for emulation of certain operations.

PVI (Protected-Mode Virtual Interrupts, bit 1 of CR4)

Setting this bit to 1 enables support for a virtual interrupt flag in protected mode. This feature can enable some programs designed for execution at privilege level 0 to execute at privilege level 3.

4.2.3.2 System Address Registers

Four special registers are defined to reference the tables or segments supported by the 80286, Intel386, and Military Intel486 processors' protection model. These tables or segments are: GDT (Global Descriptor Table), IDT (Interrupt Descriptor Table), LDT (Local Descriptor Table), TSS (Task State Segment).

The addresses of these tables and segments are stored in special registers, the System Address and System Segment Registers, illustrated in Figure 4-5. These registers are named GDTR, IDTR, LDTR and TR respectively. Section 6, ''Protected Mode Architecture,'' describes how to use these registers.

System Address Registers: GDTR and IDTR

The GDTR and IDTR hold the 32-bit linear-base address and 16-bit limit of the GDT and IDT, respectively.

Because the GDT and IDT segments are global to all tasks in the system, the GDT and IDT are defined by 32-bit linear addresses (subject to page translation if paging is enabled) and 16-bit limit values.

System Segment Registers: LDTR and TR

The LDTR and TR hold the 16-bit selector for the LDT descriptor and the TSS descriptor, respectively.

Because the LDT and TSS segments are task specific segments, the LDT and TSS are defined by selector values stored in the system segment registers.

NOTE:
A programmer-invisible segment descriptor register is associated with each system segment register.

4.2.4 FLOATING POINT REGISTERS

Figure 4-8 shows the floating point register set. The on-chip FPU contains eight data registers, a tag word, a control register, a status register, an instruction pointer and a data pointer.

The operation of the Military Intel486 DX, IntelDX2, and IntelDX4 processor on-chip floating point unit is exactly the same as the Intel387 math coprocessor. Software written for the Intel387 math coprocessor will run on the on-chip floating point unit (FPU) without any modifications.

4.2.4.1 Floating Point Data Registers

Floating point computations use the Military Intel486 DX, IntelDX2, and IntelDX4 processor FPU data registers. These eight 80-bit registers provide the equivalent capacity of twenty 32-bit registers. Each of the eight data registers is divided into ''fields'' corresponding to the FPU's extended-precision data type.

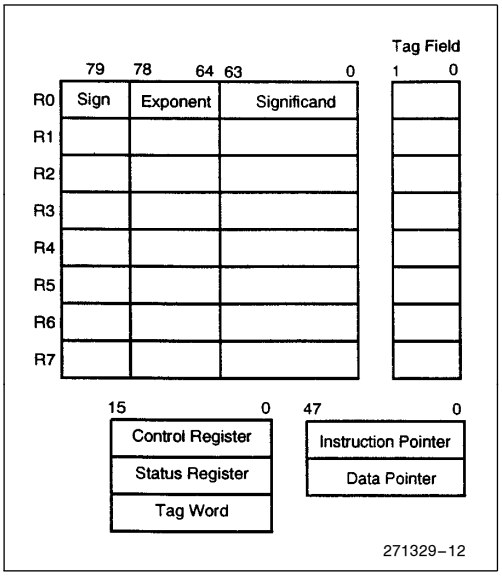


Figure 4-8. Floating Point Registers

The FPU's register set can be accessed either as a stack, with instructions operating on the top one or two stack elements, or as a fixed register set, with instructions operating on explicitly designated registers. The TOP field in the status word identifies the current top-of-stack register. A ''push'' operation decrements TOP by one and loads a value into the new top register. A ''pop'' operation stores the value from the current top register and then increments TOP by one. Like other Military Intel486 DX, IntelDX2, and IntelDX4 processor stacks in memory, the FPU register stack grows ''down'' toward lower-addressed registers.

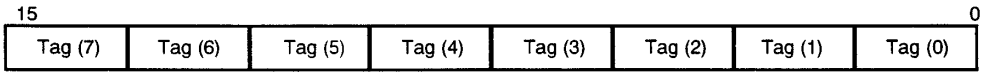
Instructions may address the data registers either implicitly or explicitly. Many instructions operate on the register at the TOP of the stack. These instructions implicitly address the register at which TOP points. Other instructions allow the programmer to explicitly specify which register to use. This explicit register addressing is also relative to TOP.

4.2.4.2 Floating Point Tag Word

The tag word marks the content of each numeric data register, as shown in Figure 4-9. Each two-bit tag represents one of the eight data registers. The principal function of the tag word is to optimize the FPU's performance and stack handling by making it possible to distinguish between empty and non-empty register locations. It also enables exception handlers to check the contents of a stack location without the need to perform complex decoding of the actual data.

4.2.4.3 Floating Point Status Word

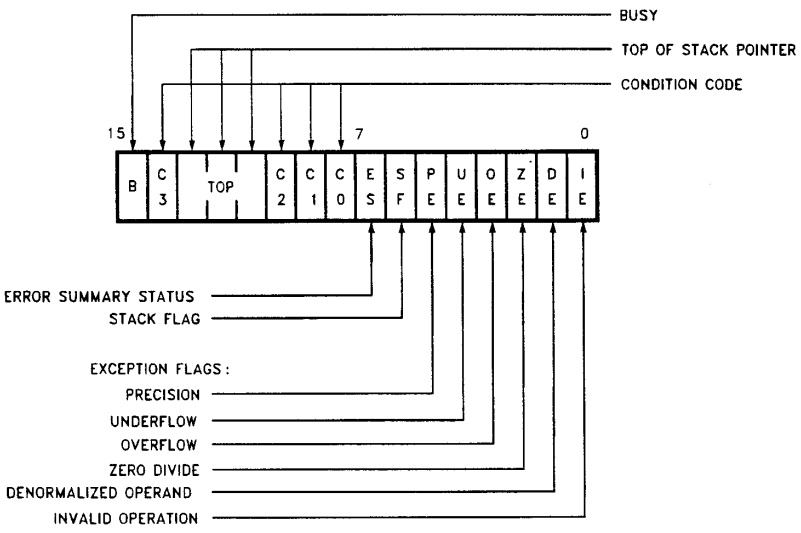
The 16-bit status word reflects the overall state of the FPU. The status word is shown in Figure 4-10 and is located in the status register.



NOTE:
The index i of tag(i) is not top-relative. A program typically uses the ''top'' field of Status Word to determine which tag(i) field refers to logical top of stack.

TAG VALUES:
00 = Valid
01 = Zero
10 = QNaN, SNaN, Infinity, Denormal and Unsupported Formats
11 = Empty

Figure 4-9. Floating Point Tag Word



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ES is set if any unmasked exception bit is set; cleared otherwise.
See Table 4-7 for interpretation of condition code.
TOP values:

000 = Register 0 is Top of Stack
001 = Register 1 is Top of Stack
•
•
•
111 = Register 7 is Top of Stack

For definitions of exceptions, refer to the section entitled ''Exception Handling''.

NOTES:
The B bit (Busy, bit 15) is included for 8087 compatibility. The B bit reflects the contents of the ES bit (bit 7 of the status word).
Bits 13–11 (TOP) point to the FPU register that is the current top-of-stack.
The four numeric condition code bits, C0–C3, are similar to the flags in EFLAGS. Instructions that perform arithmetic operations update C0–C3 to reflect the outcome. The effects of these instructions on the condition codes are summarized in Table 4-6 through Table 4-9.

Figure 4-10. Floating Point Status Word

Table 4-6. Floating Point Condition Code Interpretation

Instruction	C0 (S)	C3 (Z)	C1 (A)	C2 (C)
FPREM, FPREM1	Three least significant bits of quotient (See Table 4-8.)			Reduction 0 = complete 1 = incomplete
	Q2	Q0	Q1 or O/U#	
FCOM, FCOMP, FCOMPP, FTST, FUCOM, FUCOMP, FUCOMPP, FICOM, FICOMP	Result of comparison (see Table 4-9)		Zero or O/U#	Operand is not comparable
FXAM	Operand class (see Table 4-10)		Sign or O/U#	Operand class
FCHS, FABS, FXCH, FINCTOP, FDECTOP, Constant loads, FXTRACT, FLD, FILD, FBLD, FSTP (ext real)	UNDEFINED		Zero or O/U#	UNDEFINED
FIST, FBSTP, FRNDINT, FST, FSTP, FADD, FMUL, FDIV, FDIVR, FSUB, FSUBR, FSCALE, FSQRT, FPATAN, F2XM1, FYL2X, FYL2XP1	UNDEFINED		Roundup or O/U#	UNDEFINED
FPTAN, FSIN, FCOS, FSINCOS	UNDEFINED		Roundup or O/U#, if C2 = 1	Reduction 0 = complete 1 = incomplete
FLDENV, FRSTOR	Each bit loaded from memory			
FINIT	Clears these bits			
FLDCW, FSTENV, FSTCW, FSTSW, FCLEX, FSAVE	UNDEFINED			

NOTES:

O/U# When both IE and SF bits of status word are set, indicating a stack exception, this bit distinguishes between stack overflow (C1 = 1) and underflow (C1 = 0).

Reduction If FPREM or FPREM1 produces a remainder that is less than the modulus, reduction is complete. When reduction is incomplete the value at the top of the stack is a partial remainder, which can be used as input to further reduction. For FPTAN, FSIN, FCOS, and FSINCOS, the reduction bit is set if the operand at the top of the stack is too large. In this case the original operand remains at the top of the stack.

Roundup When the PE bit of the status word is set, this bit indicates whether the last rounding in the instruction was upward.

UNDEFINED Do not rely on finding any specific value in these bits. (See Section 4.2.7, ''Compatibility.'')

Table 4-7. Condition Code Interpretation after FPREM and FPREM1 Instructions

Condition Code				Interpretation after FPREM and FPREM1	
C2	C3	C1	C0		
1	X	X	X	Incomplete Reduction: further interaction required for complete reduction	
	Q1	Q0	Q2	Q MOD8	
0	0	0	0	0	Complete Reduction: C0, C3, and C1 contain the three least-significant bits of the quotient
	0	1	0	1	
	1	0	0	2	
	1	1	0	3	
	0	0	1	4	
	0	1	1	5	
	1	0	1	6	
	1	1	1	7	

Table 4-8. Condition Code Resulting from Comparison

Order	C3	C2	C0
TOP > Operand	0	0	0
TOP < Operand	0	0	1
TOP = Operand	1	0	0
Unordered	1	1	1

Table 4-9. Condition Code Defining Operand Class

C3	C2	C1	C0	Value at TOP
0	0	0	0	+ Unsupported
0	0	0	1	+ NaN
0	0	1	0	− Unsupported
0	0	1	1	− NaN
0	1	0	0	+ Normal
0	1	0	1	+ Infinity
0	1	1	0	− Normal
0	1	1	1	− Infinity
1	0	0	0	+ 0
1	0	0	1	+ Empty
1	0	1	0	− 0
1	0	1	1	− Empty
1	1	0	0	+ Denormal
1	1	1	0	− Denormal

Bit 7 is the error summary (ES) status bit. The ES bit is set if any unmasked exception bit (bits 0–5 in the status word) is set; ES is clear otherwise. The FERR# (floating point error) signal is asserted when ES is set.

Bit 6 is the stack flag (SF). This bit is used to distinguish invalid operations due to stack overflow or underflow. When SF is set, bit 9 (C1) distinguishes between stack overflow (C1 = 1) and underflow (C1 = 0).

Table 4-10 shows the six exception flags in bits 0–5 of the status word. Bits 0–5 are set to indicate that the FPU has detected an exception while executing an instruction.

The six exception flags in the status word can be individually masked by mask bits in the FPU control word. Table 4-10 lists the exception conditions, and their causes in order of precedence. Table 4-10 also shows the action taken by the FPU if the corresponding exception flag is masked.

An exception that is not masked by the control word will cause three things to happen: the corresponding exception flag in the status word will be set, the ES bit in the status word will be set and the FERR# output signal will be asserted. When the Military Intel486 DX, IntelDX2, or IntelDX4 processor attempts to execute another floating point or WAIT instruction, exception 16 occurs or an external interrupt happens if the NE = 1 in control register 0. The exception condition must be resolved via an interrupt service routine. The FPU saves the address of the floating point instruction that caused the exception and the address of any memory operand required by that instruction in the instruction and data pointers. (See section 4.2.4.4, ''Instruction and Data Pointers.'')

Note that when a new value is loaded into the status word by the FLDENV (load environment) or FRSTOR (restore state) instruction, the value of ES (bit 7) and its reflection in the B bit (bit 15) are not derived from the values loaded from memory. The values of ES and B are dependent upon the values of the exception flags in the status word and their corresponding masks in the control word. If ES is set in such a case, the FERR# output of the Military Intel486 DX, IntelDX2, or IntelDX4 processor is activated immediately.

Table 4-10. FPU Exceptions

Exception	Cause	Default Action (if exception is masked)
Invalid Operation	Operation on a signaling NaN, unsupported format, indeterminate form (0 * ∞, 0/0, (+ ∞) + (− ∞), etc.), or stack overflow/underflow (SF is also set).	Result is a quiet NaN, integer indefinite, or BCD indefinite
Denormalized Operand	At least one of the operands is denormalized, i.e., it has the smallest exponent but a non-zero significand.	Normal processing continues
Zero Divisor	The divisor is zero while the dividend is a non-infinite, non-zero number.	Result is ∞
Overflow	The result is too large in magnitude to fit in the specified format.	Result is largest finite value or ∞
Underflow	The true result is non-zero but too small to be represented in the specified format, and, if underflow exception is masked, denormalization causes loss of accuracy.	Result is denormalized or zero
Inexact Result (Precision)	The true result is not exactly representable in the specified format (e.g., 1/3); the result is rounded according to the rounding mode.	Normal processing continues

4.2.4.4 Instruction and Data Pointers

Because the FPU operates in parallel with the ALU (in the Military Intel486 DX, IntelDX2 and IntelDX4 processors the arithmetic and logic unit (ALU) consists of the base architecture registers), any errors detected by the FPU may be reported after the ALU has executed the floating point instruction that caused it. To allow identification of the failing numeric instruction, the Military Intel486 DX, IntelDX2, and IntelDX4 processors contain two pointer registers that supply the address of the failing numeric instruction and the address of its numeric memory operand (if appropriate).

The instruction and data pointers are provided for user-written error handlers. These registers are accessed by the FLDENV (load environment), FSTENV (store environment), FSAVE (save state) and FRSTOR (restore state) instructions. Whenever the Military Intel486 DX, IntelDX2, and IntelDX4 processors decode a new floating point instruction, it saves the instruction (including any prefixes that may be present), the address of the operand (if present) and the opcode.

The instruction and data pointers appear in one of four formats depending on the operating mode of the Military Intel486 DX, IntelDX2, and IntelDX4 processors (protected mode or real-address mode) and depending on the operand-size attribute in effect (32-bit operand or 16-bit operand). When the Military Intel486 DX, IntelDX2, or IntelDX4 processor is in the virtual-86 mode, the real address mode formats are used. The four formats are shown in Figure 4-11 through Figure 4-14. The floating point instructions FLDENV, FSTENV, FSAVE and FRSTOR are used to transfer these values to and from memory. Note that the value of the data pointer is undefined if the prior floating point instruction did not have a memory operand.

NOTE:
The operand size attribute is the D bit in a segment descriptor.

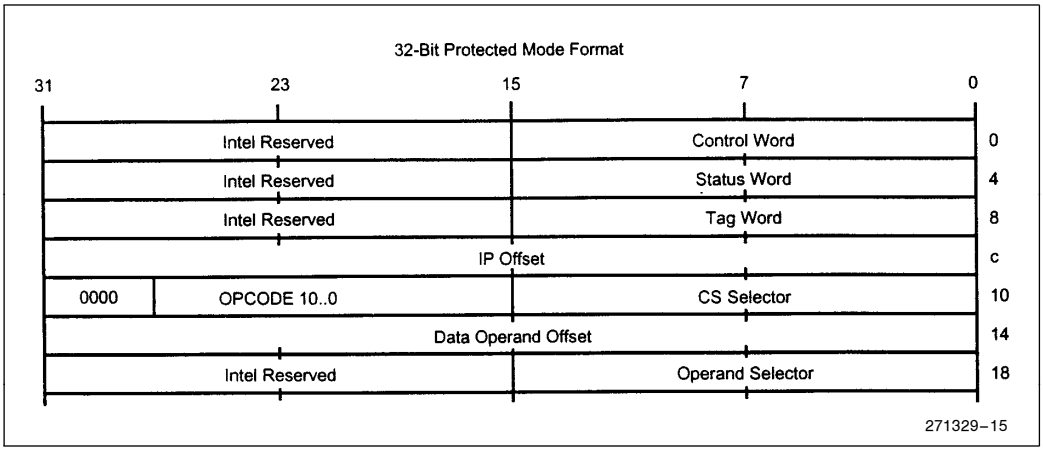


Figure 4-11. Protected Mode FPU Instructions and Data Pointer Image in Memory, 32-Bit Format

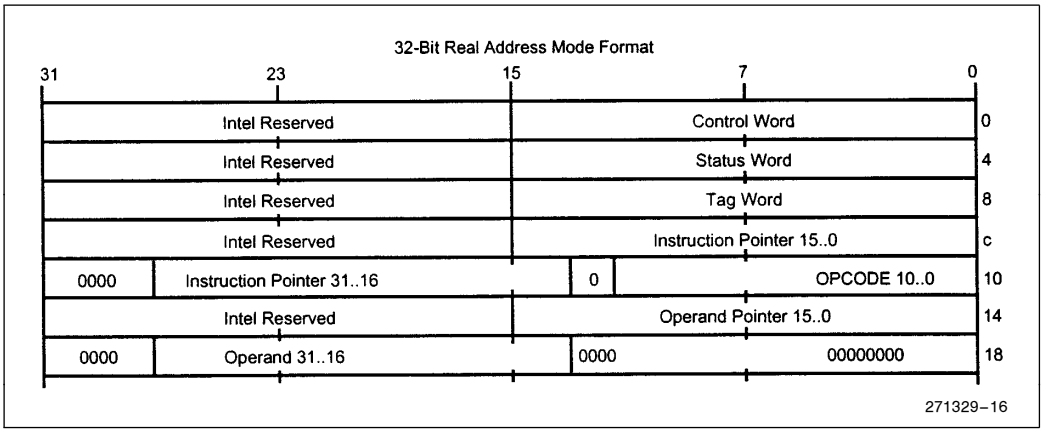


Figure 4-12. Real Mode FPU Instruction and Data Pointer Image in Memory, 32-Bit Format

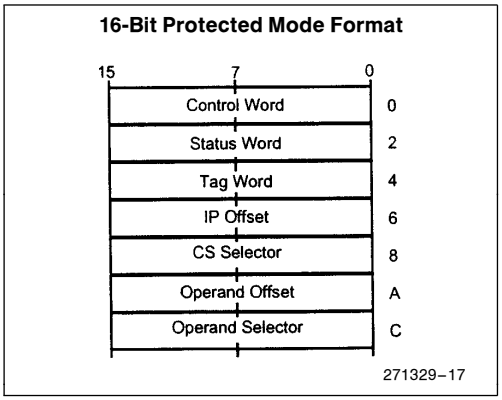


Figure 4-13. Protected Mode FPU Instruction and Data Pointer Image in Memory, 16-Bit Format

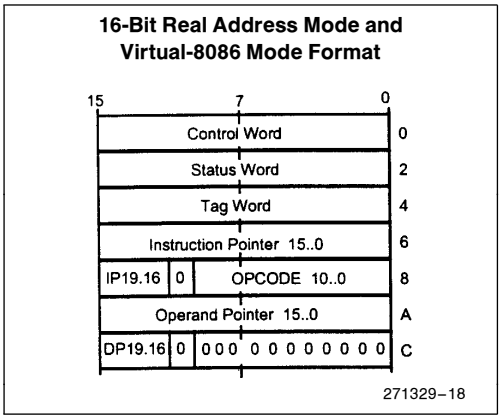
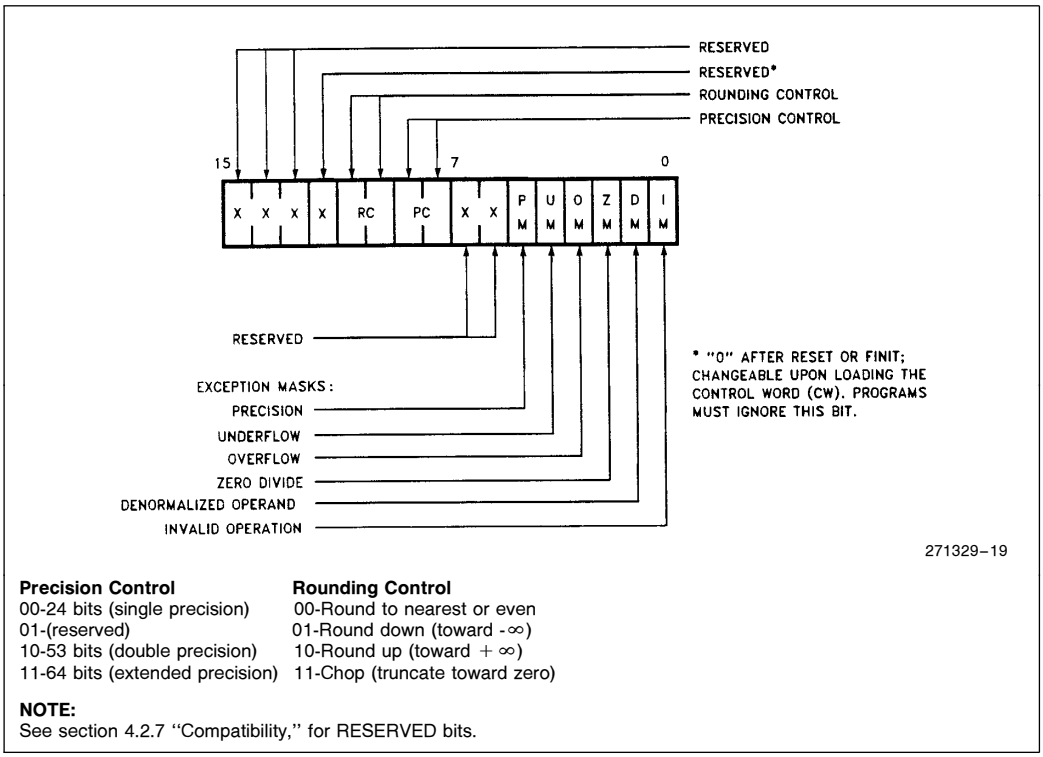


Figure 4-14. Real Mode FPU Instruction and Data Pointer Image in Memory, 16-Bit Format



Precision Control	**Rounding Control**
00-24 bits (single precision)	00-Round to nearest or even
01-(reserved)	01-Round down (toward -∞)
10-53 bits (double precision)	10-Round up (toward + ∞)
11-64 bits (extended precision)	11-Chop (truncate toward zero)

NOTE:
See section 4.2.7 "Compatibility," for RESERVED bits.

Figure 4-15. FPU Control Word

4.2.4.5 FPU Control Word

The FPU provides several processing options that are selected by loading a control word from memory into the control register. Figure 4-15 shows the format and encoding of fields in the control word.

The low-order byte of the FPU control word configures the FPU error and exception masking. Bits 0–5 of the control word contain individual masks for each of the six exceptions that the FPU recognizes.

The high-order byte of the control word configures the FPU operating mode, including precision and rounding.

RC (Rounding Control, bits 10–11)

RC bits provide for directed rounding and true chop, as well as the unbiased round to nearest even mode specified in the IEEE standard. Rounding control affects only those instructions that perform rounding at the end of the operation (and thus can generate a precision exception); namely, FST, FSTP, FIST, all arithmetic instructions (except FPREM, FPREM1, FXTRACT, FABS and FCHS), and all transcendental instructions.

PC (Precision Control, bits 8–9)

PC bits can be used to set the FPU internal operating precision of the significand at less than the default of 64 bits (extended precision). This can be useful in providing compatibility with early generation arithmetic processors of smaller precision. PC affects only the instructions ADD, SUB, DIV, MUL, and SQRT. For all other instructions, either the precision is determined by the opcode or extended precision is used.

4.2.5 DEBUG AND TEST REGISTERS

4.2.5.1 Debug Registers

The six programmer accessible debug registers (Figure 4-16) provide on-chip support for debugging. Debug registers DR0–3 specify the four linear breakpoints. The Debug control register DR7, is used to set the breakpoints and the Debug Status Register, DR6, displays the current state of the breakpoints. The use of the Debug registers is described in section 12, ''Debugging Support.''

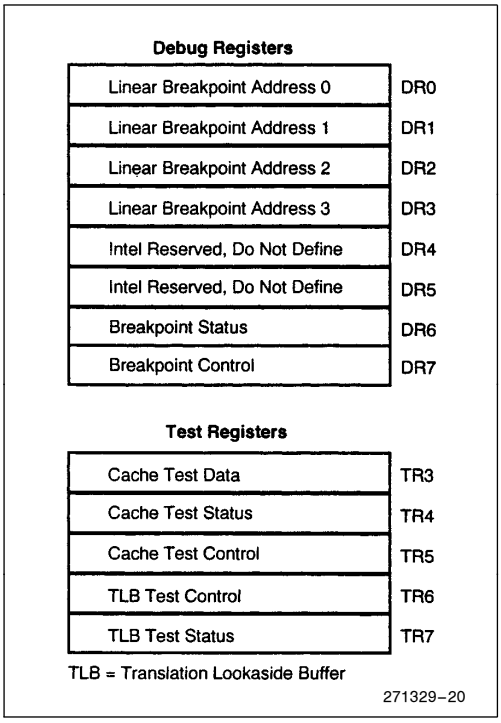


Figure 4-16. Debug and Test Registers

4.2.5.2 Test Registers

The Military Intel486 processor contains five test registers. The test registers are shown in Figure 4-16. TR6 and TR7 are used to control the testing of the translation look- aside buffer. TR3, TR4 and TR5 are used for testing the on-chip cache. The use of the test registers is discussed in section 11, ''Testability.''

4.2.6 REGISTER ACCESSIBILITY

There are a few differences regarding the accessibility of the registers in Real and Protected Mode. Table 4-11 summarizes these differences. (See section 6, ''Protected Mode Architecture.'')

4.2.6.1 FPU Register Usage

In addition to the differences listed in Table 4-11, Table 4-12 summarizes the differences for the on-chip FPU.

Table 4-11. Register Usage

Register	Use in Real Mode		Use in Protected Mode		Use in Virtual 8086 Mode	
	Load	Store	Load	Store	Load	Store
General Registers	Yes	Yes	Yes	Yes	Yes	Yes
Segment Register	Yes	Yes	Yes	Yes	Yes	Yes
Flag Register	Yes	Yes	Yes	Yes	IOPL(1)	IOPL
Control Registers	Yes	Yes	PL = 0(2)	PL = 0	No	Yes
GDTR	Yes	Yes	PL = 0	Yes	No	Yes
IDTR	Yes	Yes	PL = 0	Yes	No	Yes
LDTR	No	No	PL = 0	Yes	No	No
TR	No	No	PL = 0	Yes	No	No
Debug Registers	Yes	Yes	PL = 0	PL = 0	No	No
Test Registers	Yes	Yes	PL = 0	PL = 0	No	No

NOTES:
1. IOPL: The PUSHF and POPF instructions are made I/O Privilege Level sensitive in Virtual 8086 Mode.
2. PL = 0: The registers can be accessed only when the current privilege level is zero.

Table 4-12. FPU Register Usage Differences

Register	Use in Real Mode		Use in Protected Mode		Use in Virtual 8086 Mode	
	Load	Store	Load	Store	Load	Store
FPU Data Registers	Yes	Yes	Yes	Yes	Yes	Yes
FPU Control Registers	Yes	Yes	Yes	Yes	Yes	Yes
FPU Status Registers	Yes	Yes	Yes	Yes	Yes	Yes
FPU Instruction Pointer	Yes	Yes	Yes	Yes	Yes	Yes
FPU Data Pointer	Yes	Yes	Yes	Yes	Yes	Yes

4.2.7 COMPATIBILITY

VERY IMPORTANT NOTE:
COMPATIBILITY WITH FUTURE PROCESSORS

In the preceding register descriptions, note certain Military Intel486 processor register bits are Intel reserved. When reserved bits are called out, treat them as fully undefined. This is essential for your software compatibility with future processors! Follow the guidelines below:

1. **Do not depend on the states of any undefined bits when testing the values of defined register bits. Mask them out when testing.**
2. **Do not depend on the states of any undefined bits when storing them to memory or another register.**
3. **Do not depend on the ability to retain information written into any undefined bits.**
4. **When loading registers, always load the undefined bits as zeros.**
5. **However, registers that have been previously stored may be reloaded without masking.**

Depending upon the values of undefined register bits will make your software dependent upon the unspecified Military Intel486 processor handling of these bits. Depending on undefined values risks making your software incompatible with future processors that define usages for the Military Intel486 processor-undefined bits. AVOID ANY SOFTWARE DEPENDENCE UPON THE STATE OF UNDEFINED MILITARY INTEL486 PROCESSOR REGISTER BITS.

4.3 Instruction Set

The Military Intel486 processor instruction set can be divided into the following categories of operations:

- Data Transfer
- Arithmetic
- Shift/Rotate
- String Manipulation
- Bit Manipulation
- Control Transfer
- High Level Language Support
- Operating System Support
- Processor Control

The Military Intel486 processor instructions are listed in section 13, ''Instruction Set Summary.''

All Military Intel486 processor instructions operate on either 0, 1, 2 or 3 operands; where an operand resides in a register, in the instruction itself or in memory. Most zero operand instructions (e.g., CLI, STI) take only one byte. One operand instructions generally are two bytes long. The average instruction is 3.2-bytes long. Because the Military Intel486 processor has a 32-byte instruction queue, an average of 10 instructions will be prefetched. The use of two operands permits the following types of common instructions:

- Register to Register
- Memory to Register
- Memory to Memory
- Immediate to Register
- Register to Memory
- Immediate to Memory

The operands can be either 8-, 16-, or 32-bits long. As a general rule, when executing 32-bit code, operands are 8 or 32 bits; when executing existing 80286 or 8086 processor code (16-bit code), operands are 8 or 16 bits. Prefixes can be added to all instructions that override the default length of the operands (i.e., use 32-bit operands for 16-bit code, or 16-bit operands for 32-bit code).

4.3.1 FLOATING POINT INSTRUCTIONS

In addition to the instructions listed above, the Military Intel486, IntelDX2, and IntelDX4 processors have the following floating point instructions. Note that all floating point unit instruction mnemonics begin with an F.

- Floating Point
- Floating Point Control

4.4 Memory Organization

Memory on the Military Intel486 processor is divided up into 8-bit quantities (bytes), 16-bit quantities (words), and 32-bit quantities (dwords). Words are stored in two consecutive bytes in memory with the low-order byte at the lowest address, the high order byte at the high address. Dwords are stored in four consecutive bytes in memory with the low-order byte at the lowest address, the high-order byte at the highest address. The address of a word or dword is the byte address of the low-order byte.

In addition to these basic data types, the Military Intel486 processor supports two larger units of memory: pages and segments. Memory can be divided up into one or more variable-length segments, which can be swapped to disk or shared between programs. Memory can also be organized into one or more 4-Kbyte pages. Both segmentation and paging can be combined, gaining the advantages of both systems. The Military Intel486 processor supports both pages and segments in order to provide maximum flexibility to the system designer. Segmentation and paging are complementary. Segmentation is useful for organizing memory in logical modules, and as such is a tool for the application programmer, while pages are useful for the system programmer for managing the physical memory of a system.

4.4.1 ADDRESS SPACES

The Military Intel486 processor has three distinct address spaces: **logical, linear,** and **physical**. A **logical** address (also known as a **virtual** address) consists of a selector and an offset. A selector is the contents of a segment register. An offset is formed by summing all of the addressing components (BASE, INDEX, DISPLACEMENT) discussed in section 4.6.3 "32-Bit Memory Addressing Modes," into an effective address. Because each task on the Military Intel486 processor has a maximum of 16K ($2^{14}-1$) selectors, and offsets can be 4 Gbytes (2^{32} bits), this gives a total of 2^{46} bits or 64 terabytes of **logical** address space per task. The programmer sees this virtual address space.

The segmentation unit translates the **logical** address space into a 32-bit **linear** address space. If the paging unit is not enabled then the 32-bit **linear** address corresponds to the **physical** address. The paging unit translates the **linear** address space into the **physical** address space. The **physical address** is what appears on the address pins.

The primary difference between Real Mode and Protected Mode is how the segmentation unit performs the translation of the **logical** address into the **linear** address. In Real Mode, the segmentation unit shifts the selector left four bits and adds the result to the offset to form the **linear** address. While in Protected Mode every selector has a **linear** base address associated with it. The **linear base** address is stored in one of two operating system tables (i.e., the Local Descriptor Table or Global Descriptor Table). The selector's **linear base** address is added to the offset to form the final **linear** address.

Figure 4-17 shows the relationship between the various address spaces.

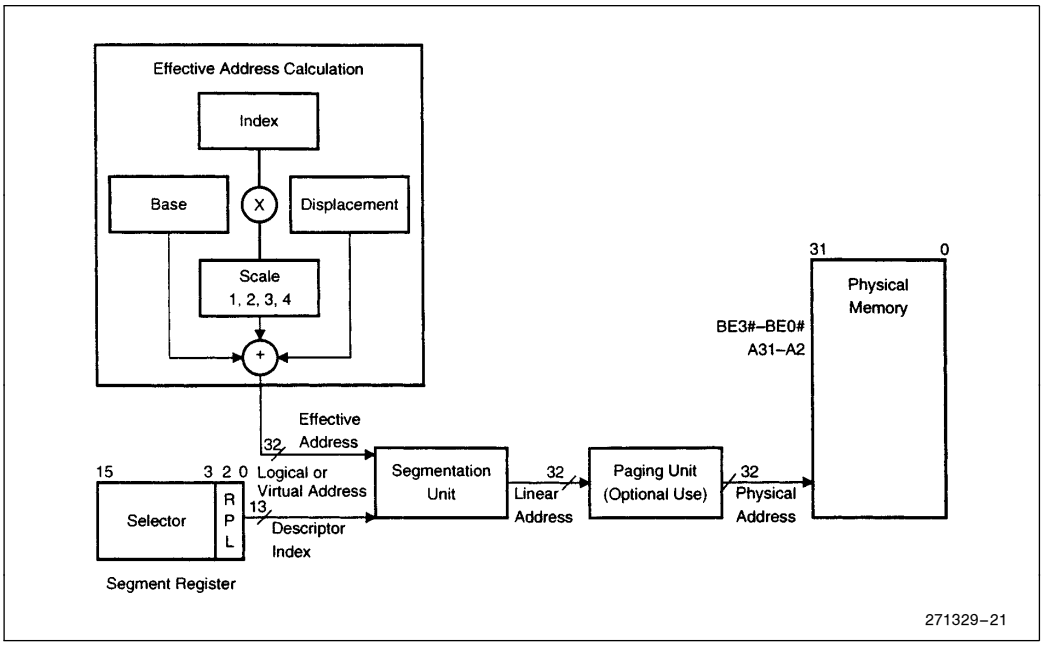


Figure 4-17. Address Translation

4.4.2 SEGMENT REGISTER USAGE

The main data structure used to organize memory is the segment. On the Military Intel486 processor, segments are variable sized blocks of linear addresses which have certain attributes associated with them. There are two main types of segments: code and data. The segments are of variable size and can be as small as 1 byte or as large as 4 Gbytes (2^{32} bytes).

In order to provide compact instruction encoding, and increase Military Intel486 processor performance, instructions do not need to explicitly specify which segment register is used. A default segment register is automatically chosen according to the rules of Table 4-13. In general, data references use the selector contained in the DS register; Stack references use the SS register and Instruction fetches use the CS register. The contents of the Instruction Pointer provide the offset. Special segment override prefixes allow the explicit use of a given segment register, and override the implicit rules listed in Table 4-13. The override prefixes also allow the use of the ES, FS and GS segment registers.

There are no restrictions regarding the overlapping of the base addresses of any segments. Thus, all 6 segments could have the base address set to zero and create a system with a 4-Gbyte linear address space. This creates a system where the virtual address space is the same as the linear address space. Further details of segmentation are discussed in section 6.0, ''Protected Mode Architecture.''

4.5 I/O Space

The Military Intel486 processor has two distinct physical address spaces: Memory and I/O. Generally, peripherals are placed in I/O space although the Military Intel486 processor also supports memory-mapped peripherals. The I/O space consists of 64 Kbytes, it can be divided into 64K 8-bit ports, 32K 16-bit ports, or 16K 32-bit ports, or any combination of ports which add up to less than 64 Kbytes. The 64K I/O address space refers to physical memory rather than linear address, because I/O instructions do not go through the segmentation or paging hardware. The M/IO# pin acts as an additional address line thus allowing the system designer to easily determine which address space the processor is accessing.

Table 4-13. Segment Register Selection Rules

Type of Memory Reference	Implied (Default) Segment Use	Segment Override Prefixes Possible
Code Fetch	CS	None
Destination of PUSH, PUSHF, INT, CALL, PUSHA Instructions	SS	None
Source of POP, POPA, POPF, IRET, RET instructions	SS	None
Destination of STOS, MOVS, REP STOS, REP MOVS Instructions (DI is Base Register)	ES	None
Other Data References, with Effective Address using Base Register of:		
[EAX]	DS	All
[EBX]	DS	
[ECX]	DS	
[EDX]	DS	
[ESI]	DS	
[EDI]	DS	
[EBP]	SS	
[ESP]	SS	

The I/O ports are accessed via the IN and OUT I/O instructions, with the port address supplied as an immediate 8-bit constant in the instruction or in the DX register. All 8- and 16-bit port addresses are zero extended on the upper address lines. The I/O instructions cause the M/IO# pin to be driven low.

I/O port addresses 00F8H through 00FFH are reserved for use by Intel.

I/O instruction code is cacheable.

I/O data is not cacheable.

I/O transfers (data or code) can be bursted.

4.6 Addressing Modes

4.6.1 ADDRESSING MODES OVERVIEW

The Military Intel486 processor provides a total of 11 addressing modes for instructions to specify operands. The addressing modes are optimized to allow the efficient execution of high-level languages such as C and FORTRAN, and they cover the vast majority of data references needed by high-level languages.

4.6.2 REGISTER AND IMMEDIATE MODES

The following two addressing modes provide for instructions that operate on register or immediate operands:

- **Register Operand Mode:** The operand is located in one of the 8-, 16- or 32-bit general registers.
- **Immediate Operand Mode:** The operand is included in the instruction as part of the opcode.

4.6.3 32-BIT MEMORY ADDRESSING MODES

The remaining modes provide a mechanism for specifying the effective address of an operand. The linear address consists of two components: the segment base address and an effective address. The effective address is calculated by using combinations of the following four address elements:

- **DISPLACEMENT:** An 8-, or 32-bit immediate value, following the instruction.
- **BASE:** The contents of any general purpose register. The base registers are generally used by compilers to point to the start of the local variable area.
- **INDEX:** The contents of any general purpose register except for ESP. The index registers are used to access the elements of an array, or a string of characters.
- **SCALE:** The index register's value can be multiplied by a scale factor, either 1, 2, 4 or 8. Scaled index mode is especially useful for accessing arrays or structures.

Combinations of these 4 components make up the 9 additional addressing modes. There is no performance penalty for using any of these addressing combinations, because the effective address calculation is pipelined with the execution of other instructions. The one exception is the simultaneous use of Base and Index components, which requires one additional clock.

As shown in Figure 4-18, the effective address (EA) of an operand is calculated according to the following formula:

EA = Base Reg + (Index Reg * Scaling) + Displacement

Direct Mode: The operand's offset is contained as part of the instruction as an 8-, 16- or 32-bit displacement.

Example: INC Word PTR [500]

Register Indirect Mode: A BASE register contains the address of the operand.

Example: MOV [ECX], EDX

Based Mode: A BASE register's contents is added to a DISPLACEMENT to form the operand's offset.

Example: MOV ECX, [EAX+24]

Index Mode: An INDEX register's contents is added to a DISPLACEMENT to form the operand's offset.

Example: ADD EAX, TABLE[ESI]

Scaled Index Mode: An INDEX register's contents is multiplied by a scaling factor which is added to a DISPLACEMENT to form the operand's offset.

Example: IMUL EBX, TABLE[ESI*4],7

Based Index Mode: The contents of a BASE register is added to the contents of an INDEX register to form the effective address of an operand.

Example: MOV EAX, [ESI] [EBX]

Based Scaled Index Mode: The contents of an INDEX register is multiplied by a SCALING factor and the result is added to the contents of a BASE register to obtain the operand's offset.

Example: MOV ECX, [EDX*8] [EAX]

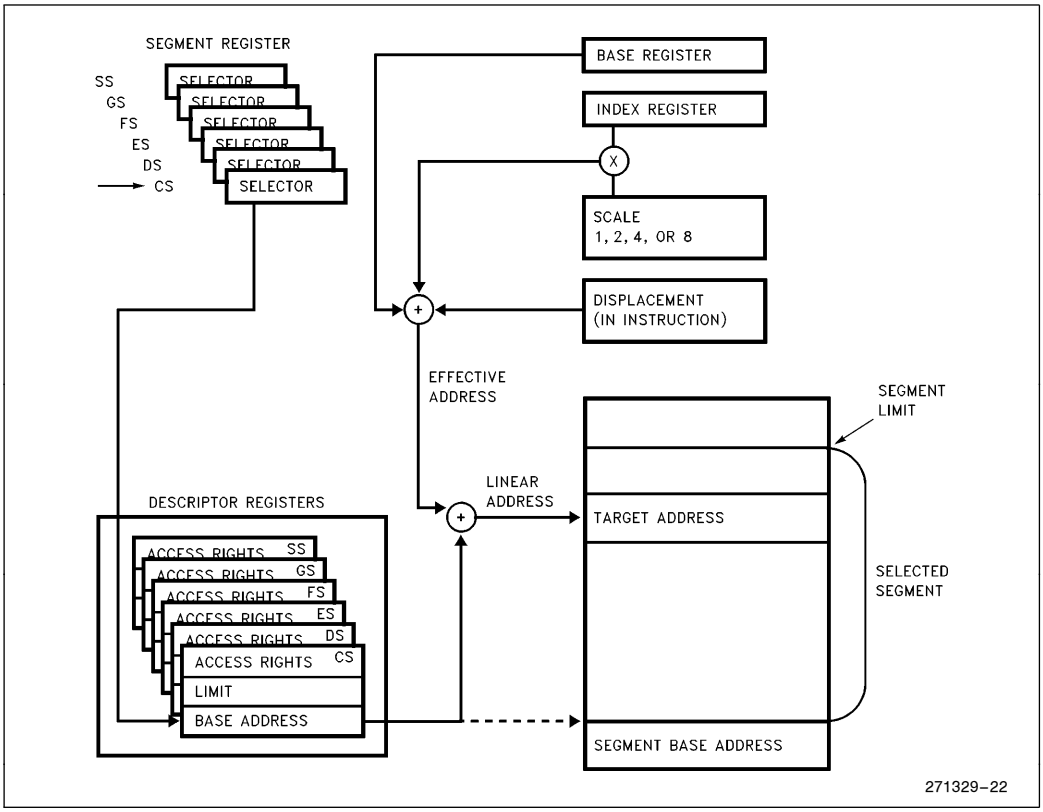


Figure 4-18. Addressing Mode Calculations

Based Index Mode with Displacement: The contents of an INDEX Register and a BASE register's contents and a DISPLACEMENT are all summed together to form the operand offset.

Example: ADD EDX, [ESI] [EBP + 00FFFFF0H]

Based Scaled Index Mode with Displacement: The contents of an INDEX register are multiplied by a SCALING factor, the result is added to the contents of a BASE register and a DISPLACEMENT to form the operand's offset.

Example: MOV EAX, LOCALTABLE[EDI*4] [EBP + 80]

4.6.4 DIFFERENCES BETWEEN 16- AND 32-BIT ADDRESSES

In order to provide software compatibility with 80286 and 8086 processors, the Military Intel486 processor can execute 16-bit instructions in Real and Protected Modes. The processor determines the size of the instructions it is executing by examining the D bit in the CS segment Descriptor. If the D bit is 0 then all operand lengths and effective addresses are assumed to be 16 bits long. If the D bit is 1 then the default length for operands and addresses is 32 bits. In Real Mode the default size for operands and addresses is 16-bits.

Regardless of the default precision of the operands or addresses, the Military Intel486 processor is able to execute either 16- or 32-bit instructions. This is

specified via the use of override prefixes. Two prefixes, the **Operand Size Prefix** and the **Address Length Prefix**, override the value of the D bit on an individual instruction basis. These prefixes are automatically added by Intel assemblers.

Example: The Military Intel486 processor is executing in Real Mode and the programmer needs to access the EAX registers. The assembler code for this might be MOV EAX, 32-bit MEMORYOP, ASM486 Macro Assembler automatically determines that an Operand Size Prefix is needed and generates it.

Example: The D bit is 0, and the programmer wishes to use Scaled Index addressing mode to access an array. The Address Length Prefix allows the use of MOV DX, TABLE[ESI*2]. The assembler uses an Address Length Prefix because, with D = 0, the default addressing mode is 16-bits.

Example: The D bit is 1, and the program wants to store a 16-bit quantity. The Operand Length Prefix is used to specify only a 16-bit value; MOV MEM16, DX.

The OPERAND LENGTH and Address Length Prefixes can be applied separately or in combination to any instruction. The Address Length Prefix does not allow addresses over 64 Kbytes to be accessed in Real Mode. A memory address which exceeds FFFFH will result in a General Protection Fault. An Address Length Prefix only allows the use of the additional Military Intel486 processor addressing modes.

When executing 32-bit code, the Military Intel486 processor uses either 8-, or 32-bit displacements, and any register can be used as base or index registers. When executing 16-bit code, the displacements are either 8, or 16 bits, and the base and index register conform to the 80286 processor model. Table 4-14 illustrates the differences.

Table 4-14. BASE and INDEX Registers for 16- and 32-Bit Addresses

	16-Bit Addressing	32-Bit Addressing
BASE REGISTER	BX,BP	Any 32-bit GP Register
INDEX REGISTER	SI,DI	Any 32-bit GP Register Except ESP
SCALE FACTOR	none	1, 2, 4, 8
DISPLACEMENT	0, 8, 16 bits	0, 8, 32 bits

4.7 Data Formats

4.7.1 DATA TYPES

The Military Intel486 processor can support a wide-variety of data types. In the following descriptions, the processor consists of the base architecture registers.

4.7.1.1 Unsigned Data Types

Byte: Unsigned 8-bit quantity

Word: Unsigned 16-bit quantity

Dword: Unsigned 32-bit quantity

The least significant bit (LSB) in a byte is bit 0, and the most significant bit is 7.

4.7.1.2 Signed Data Types

All signed data types assume 2's complement notation. The signed data types contain two fields, a sign bit and a magnitude. The sign bit is the most significant bit (MSB). The number is negative if the sign bit is 1. If the sign bit is 0, the number is positive. The magnitude field consists of the remaining bits in the number. (Refer to Figure 4-19.)

8-bit Integer: Signed 8-bit quantity

16-bit Integer: Signed 16-bit quantity

32-bit Integer: Signed 32-bit quantity

64-bit Integer: Signed 64-bit quantity

The integer core of the Military Intel486 processors only support 8-, 16- and 32-bit integers. (See section 4.7.1.4, ''Floating Point Data Types.'')

4.7.1.3 BCD Data Types

The Military Intel486 processor supports packed and unpacked binary coded decimal (BCD) data types. A packed BCD data type contains two digits per byte, the lower digit is in bits 0–3 and the upper digit in bits 4–7. An unpacked BCD data type contains 1 digit per byte stored in bits 0–3.

The Military Intel486 processor supports 8-bit packed and unpacked BCD data types. (Refer to Figure 4-19.)

4.7.1.4 Floating Point Data Types

In addition to the base registers, the Military Intel486 DX, IntelDX2, and IntelDX4 processors' on-chip floating point unit consists of the floating point registers. The floating point unit data type contain three fields: sign, significand and exponent. The sign field is one bit and is the MSB of the floating point number. The number is negative if the sign bit is 1. If the sign bit is 0, the number is positive. The significand gives the significant bits of the number. The exponent field contains the power of 2 needed to scale the significand. (Refer to Figure 4-19.)

Only the FPU supports floating point data types.

Single Precision Real:	23-bit significand and 8-bit exponent. 32 bits total.
Double Precision Real:	52-bit significand and 11-bit exponent. 64 bits total.
Extended Precision Real:	64-bit significand and 15-bit exponent. 80 bits total.

Floating Point Unsigned Data Types

The on-chip FPU does not support unsigned data types. (Refer to Figure 4-19.)

Floating Point Signed Data Types

The on-chip FPU only supports 16-, 32- and 64-bit integers.

Floating Point BCD Data Types

The on-chip FPU only supports 80-bit packed BCD data types.

4.7.1.5 String Data Types

A string data type is a contiguous sequence of bits, bytes, words or dwords. A string may contain between 1 byte and 4 Gbytes. (Refer to Figure 4-20.)

String data types are only supported by the CPU section of the Military Intel486 processor.

Byte String:	Contiguous sequence of bytes.
Word String:	Contiguous sequence of words.
Dword String:	Contiguous sequence of dwords.
Bit String:	A set of contiguous bits. In the Military Intel486 processor bit strings can be up to 4-gigabits long.

4.7.1.6 ASCII Data Types

The Military Intel486 processor supports ASCII (American Standard Code for Information Interchange) strings and can perform arithmetic operations (such as addition and division) on ASCII data. The Military Intel486 processor can only operate on ASCII data. (Refer to Figure 4-20.)

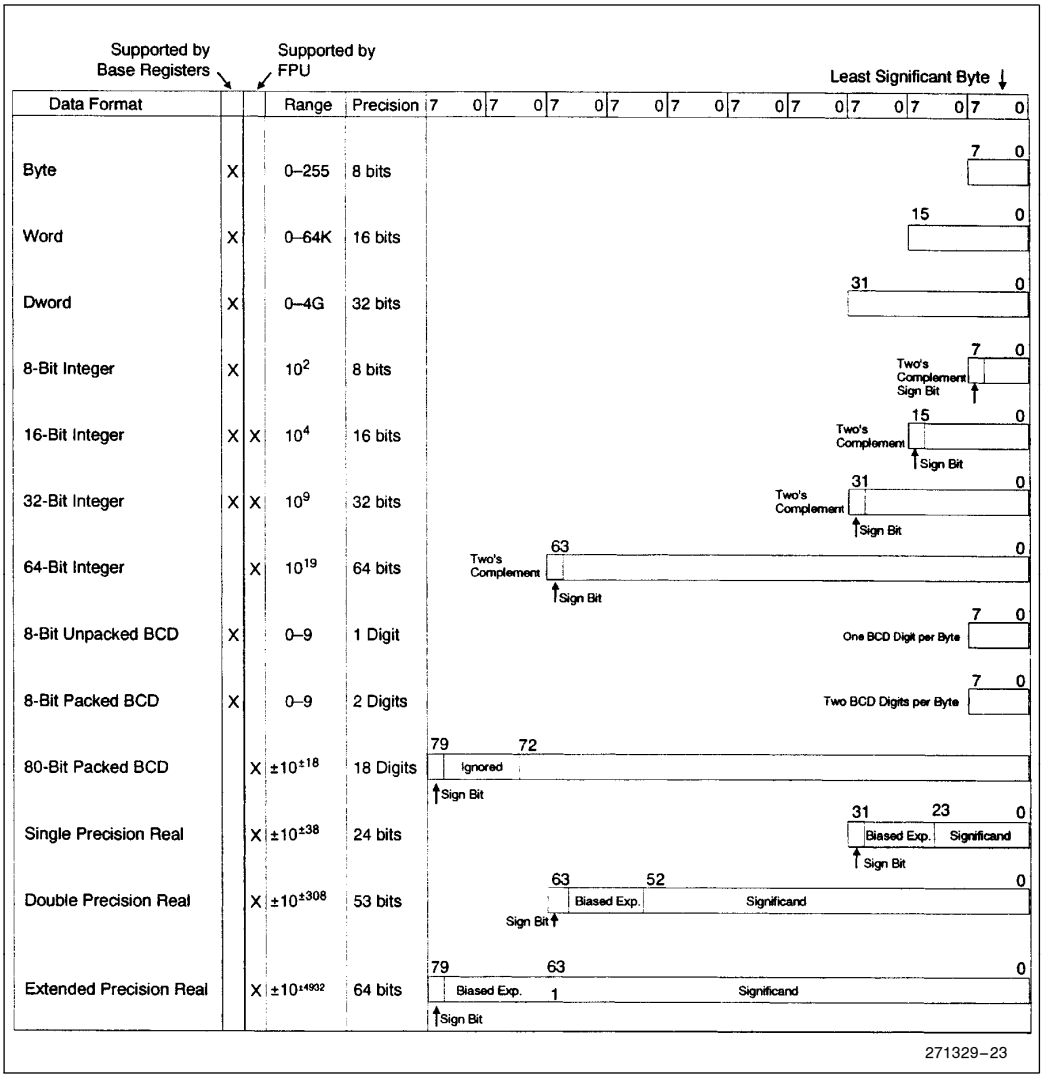


Figure 4-19. Military Intel486™ Processor Data Types

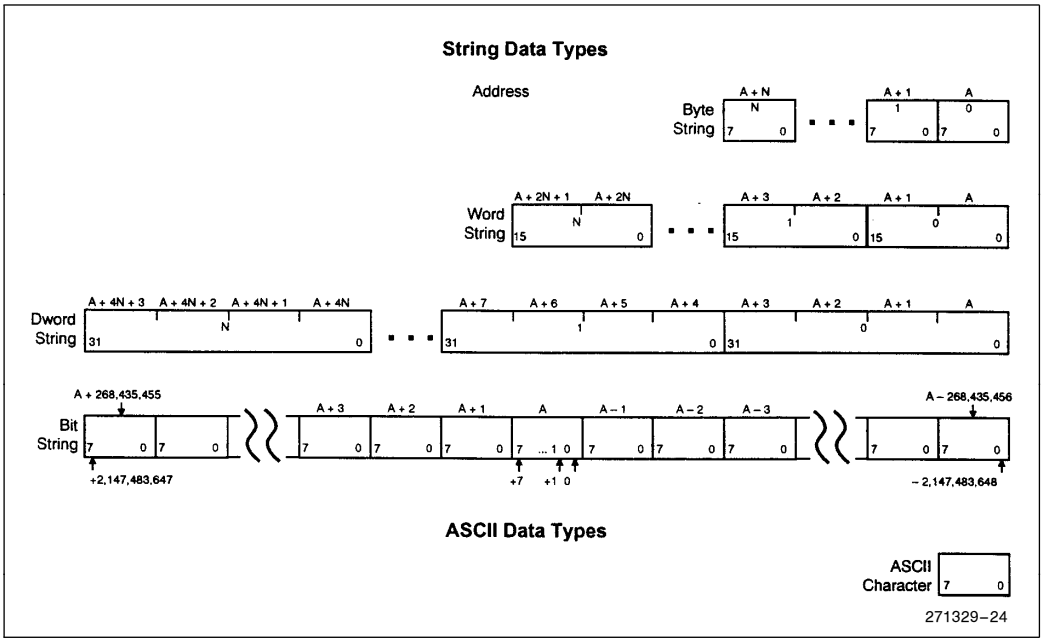


Figure 4-20. String and ASCII Data Types

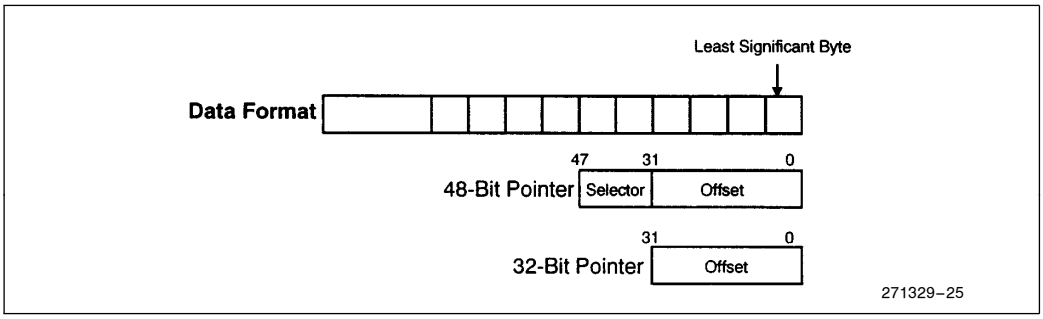


Figure 4-21. Pointer Data Types

4.7.1.7 Pointer Data Types

A pointer data type contains a value that gives the address of a piece of data. Military Intel486 processors support the following two types of pointers (see Figure 4-21):

- 48-bit Pointer: 16-bit selector and 32-bit offset
- 32-bit Pointer: 32-bit offset

4.7.2 LITTLE ENDIAN vs. BIG ENDIAN DATA FORMATS

The Military Intel486 processors, as well as all other members of the Intel architecture, use the ''little-endian'' method for storing data types that are larger than one byte. Words are stored in two consecutive bytes in memory with the low-order byte at the lowest address and the high order byte at the high address. Dwords are stored in four consecutive bytes in memory with the low-order byte at the lowest address and the high order byte at the highest address. The address of a word or dword data item is the byte address of the low-order byte.

Figure 4-22 illustrates the differences between the big-endian and little-endian formats for dwords. The 32 bits of data are shown with the low order bit numbered bit 0 and the high order bit numbered 32. Big-endian data is stored with the high-order bits at the lowest addressed byte. Little-endian data is stored with the high-order bits in the highest addressed byte.

The Military Intel486 processor has the following two instructions that can convert 16- or 32-bit data between the two byte orderings:

- BSWAP (byte swap) handles 4-byte values
- XCHG (exchange) handles 2-byte values

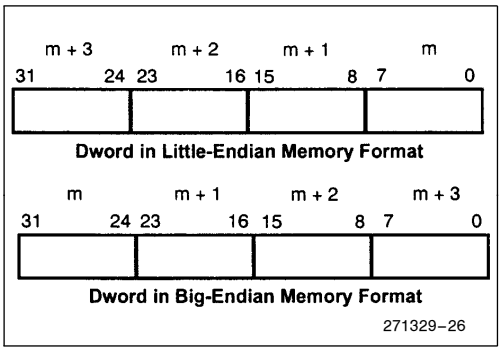


Figure 4-22. Big vs. Little Endian Memory Format

4.8 Interrupts

4.8.1 INTERRUPTS AND EXCEPTIONS

Interrupts and exceptions alter the normal program flow, in order to handle external events, to report errors or exceptional conditions. The difference between interrupts and exceptions is that interrupts are used to handle asynchronous external events while exceptions handle instruction faults. Although a program can generate a software interrupt via an INT N instruction, the Military Intel486 processors treat software interrupts as exceptions.

Hardware interrupts occur as the result of an external event and are classified into two types: maskable or non-maskable. Interrupts are serviced after the execution of the current instruction. After the interrupt handler is finished servicing the interrupt, execution proceeds with the instruction immediately **after** the interrupted instruction. Sections 4.8.3, ''Maskable Interrupt,'' and 4.8.4, ''Non-Maskable Interrupt,'' discuss the differences between Maskable and Non-Maskable interrupts.

Exceptions are classified as faults, traps, or aborts, depending on the way they are reported, and whether or not restart of the instruction causing the exception is supported. **Faults** are exceptions that are detected and serviced **before** the execution of the faulting instruction. A fault would occur in a virtual memory system when the processor referenced a page or a segment that was not present. The operating system would fetch the page or segment from disk, and then the Military Intel486 processor would restart the instruction. **Traps** are exceptions that are reported immediately **after** the execution of the instruction that caused the problem. User defined interrupts are examples of traps. **Aborts** are exceptions that do not permit the precise location of the instruction causing the exception to be determined. Aborts are used to report severe errors, such as a hardware error or illegal values in system tables.

Thus, when an interrupt service routine has been completed, execution proceeds from the instruction immediately following the interrupted instruction. On the other hand, the return address from an exception fault routine will always point at the instruction causing the exception and include any leading instruction prefixes. Tables 4-15 and 4-16 summarize the possible interrupts for Military Intel486 processors and shows where the return address points.

Military Intel486 processors can handle up to 256 different interrupts and/or exceptions. In order to service the interrupts, a table with up to 256 interrupt vectors must be defined. The interrupt vectors are simply pointers to the appropriate interrupt service routine. In Real Mode (see section 5.0, ''Real Mode Architecture''), the vectors are 4-byte quantities, a Code Segment plus a 16-bit offset; in Protected Mode, the interrupt vectors are 8-byte quantities, which are put in an Interrupt Descriptor Table. (See section 6.2.3.4, ''Interrupt Descriptor Table.'') Of the 256 possible interrupts, 32 are reserved for use by Intel, the remaining 224 are free to be used by the system designer.

4.8.2 INTERRUPT PROCESSING

When an interrupt occurs, the following actions happen. First, the current program address and the Flags are saved on the stack to allow resumption of the interrupted program. Next, an 8-bit vector is supplied to the Military Intel486 processor which identifies the appropriate entry in the interrupt table. The table contains the starting address of the interrupt service routine. Then, the user supplied interrupt service routine is executed. Finally, when an IRET instruction is executed the old Military Intel486 processor state is restored and program execution resumes at the appropriate instruction.

The 8-bit interrupt vector is supplied to the Military Intel486 processor in several different ways: exceptions supply the interrupt vector internally; software INT instructions contain or imply the vector; maskable hardware interrupts supply the 8-bit vector via the interrupt acknowledge bus sequence. Non-Maskable hardware interrupts are assigned to interrupt vector 2.

4.8.3 MASKABLE INTERRUPT

Maskable interrupts are the most common way used by the Military Intel486 processor to respond to asynchronous external hardware events. A hardware interrupt occurs when the INTR is pulled high and the Interrupt Flag bit (IF) is enabled. The Military Intel486 processor only responds to interrupts between instructions, (REPeat String instructions, have an ''interrupt window,'' between memory moves, which allows interrupts during long string moves). When an interrupt occurs, the Military Intel486 processor reads an 8-bit vector supplied by the hardware which identifies the source of the interrupt, (one of 224 user defined interrupts). The exact nature of the interrupt sequence is discussed in section 10.2.10, ''Interrupt Acknowledge.''

The IF bit in the EFLAG registers is reset when an interrupt is being serviced. This effectively disables servicing additional interrupts during an interrupt service routine. However, the IF may be set explicitly by the interrupt handler, to allow the nesting of interrupts. When an IRET instruction is executed, the original state of the IF is restored.

Table 4-15. Interrupt Vector Assignments

Function	Interrupt Number	Instruction that Can Cause Exception	Return Address Points to Faulting Instruction	Type
Divide Error	0	DIV, IDIV	YES	FAULT
Debug Exception	1	Any instruction	YES	TRAP*
NMI Interrupt	2	INT 2 or NMI	NO	NMI
One Byte Interrupt	3	INT	NO	TRAP
Interrupt on Overflow	4	INTO	NO	TRAP
Array Bounds Check	5	BOUND	YES	FAULT
Invalid OP-Code	6	Any illegal instruction	YES	FAULT
Device Not Available	7	ESC, WAIT	YES	FAULT
Double Fault	8	Any instruction that can generate an exception		ABORT
Intel Reserved	9			
Invalid TSS	10	JMP, CALL, IRET, INT	YES	FAULT
Segment Not Present	1	Segment Register Instructions	YES	FAULT
Stack Fault	12	Stack References	YES	FAULT
General Protection Fault	13	Any Memory Reference	YES	FAULT
Page Fault	14	Any Memory Access or Code Fetch	YES	FAULT
Intel Reserved	15			
Alignment Check Interrupt	17	Unaligned Memory Access	YES	FAULT
Intel Reserved	18–31			
Two Byte Interrupt	0–255	INT n	NO	TRAP

*Some debug exceptions may report both traps on the previous instruction, and faults on the next instruction.

Table 4-16. FPU Interrupt Vector Assignments

Function	Interrupt Number	Instruction Which Can Cause Exception	Return Address Points to Faulting Instruction	Type
Floating Point Error	16	Floating Point, WAIT	YES	FAULT

4.8.4 NON-MASKABLE INTERRUPT

Non-maskable interrupts provide a method of servicing very high priority interrupts. A common example of the use of a non-maskable interrupt (NMI) would be to activate a power failure routine or SMI# to activate a power saving mode. When the NMI input is pulled high, it causes an interrupt with an internally supplied vector value of 2. Unlike a normal hardware interrupt, no interrupt acknowledgment sequence is performed for an NMI.

While executing the NMI servicing procedure, the Military Intel486 processor will not service further NMI requests until an interrupt return (IRET) instruction is executed or the processor is reset (RSM in the case of SMI#). If NMI occurs while currently servicing an NMI, its presence will be saved for servicing after executing the first IRET instruction. The IF bit is cleared at the beginning of an NMI interrupt to inhibit further INTR interrupts.

4.8.5 SOFTWARE INTERRUPTS

A third type of interrupt/exception for the Military Intel486 processor is the software interrupt. An INT n instruction causes the processor to execute the interrupt service routine pointed to by the *n*th vector in the interrupt table.

A special case of the two byte software interrupt INT n is the one byte INT 3, or breakpoint interrupt. By inserting this one byte instruction in a program, the user can set breakpoints in his program as a debugging tool.

A final type of software interrupt is the single step interrupt. It is discussed in section 12.2, ''Single-Step Trap.''

4.8.6 INTERRUPT AND EXCEPTION PRIORITIES

Interrupts are externally-generated events. Maskable Interrupts (on the INTR input) and Non-Maskable Interrupts (on the NMI input or SMI# input) are recognized at instruction boundaries. When more than one interrupt or external event are **both** recognized at the **same** instruction boundary, the Military Intel486 processor invokes the highest priority routine first. (See list below.) If, after the NMI service routine has been invoked, maskable interrupts are still enabled, then the Military Intel486 processor will invoke the appropriate interrupt service routine.

Priority for Servicing External Events for All Military Intel486 Processors

1. RESET/SRESET
2. FLUSH#
3. SMI#
4. NMI
5. INTR
6. STPCLK#

NOTE:
STPCLK# will be recognized while in an interrupt service routine or an SMM handler.

Exceptions are internally-generated events. Exceptions are detected by the Military Intel486 processor if, in the course of executing an instruction, the Military Intel486 processor detects a problematic condition. The IntelDX4 processor then immediately invokes the appropriate exception service routine. The state of the Military Intel486 processor is such that the instruction causing the exception can be restarted. If the exception service routine has taken care of the problematic condition, the instruction will execute without causing the same exception.

It is possible for a single instruction to generate several exceptions (for example, transferring a single operand could generate two page faults if the operand location spans two ''not present'' pages). However, only one exception is generated upon each attempt to execute the instruction. Each exception service routine should correct its corresponding exception, and restart the instruction. In this manner, exceptions are serviced until the instruction executes successfully.

As the Military Intel486 processor executes instructions, it follows a consistent cycle in checking for exceptions. Consider the case of the Military Intel486 processor having just completed an instruction. It then performs the checks listed in Table 4-17 before reaching the point where the next instruction is completed. This cycle is repeated as each instruction is executed, and occurs in parallel with instruction decoding and execution. Checking for EM, TS, or FPU error status only occurs for processors with on-chip floating point units.

Table 4-17. Sequence of Exception Checking

Sequence	Description
1	Check for Exception 1 Traps from the instruction just completed (single-step via Trap Flag, or Data Breakpoints set in the Debug Registers).
2	Check for Exception 1 Faults in the next instruction (Instruction Execution Breakpoint set in the Debug Registers for the next instruction).
3	Check for external NMI and INTR.
4	Check for Segmentation Faults that prevented fetching the entire next instruction (exceptions 11 or 13).
5	Check for Page Faults that prevented fetching the entire next instruction (exception 14).
6	Check for Faults decoding the next instruction (exception 6 if illegal opcode; exception 6 if in Real Mode or in Virtual 8086 Mode and attempting to execute an instruction for Protected Mode only (see section 6.5.4, ''Protection and I/O Permission Bitmap''); or exception 13 if instruction is longer than 15 bytes, or privilege violation in Protected Mode (i.e., not at IOPL or at CPL = 0).
7	If WAIT opcode, check if TS = 1 and MP = 1 (exception 7 if both are 1).
8	If opcode for Floating Point Unit, check if EM = 1 or TS = 1 (exception 7 if either are 1).
9	If opcode for Floating Point Unit (FPU), check FPU error status (exception 16 if error status is asserted).
10	Check in the following order for each memory reference required by the instruction: a. Check for Segmentation Faults that prevent transferring the entire memory quantity (exceptions 11, 12, 13). b. Check for Page Faults that prevent transferring the entire memory quantity (exception 14).

NOTE:
The order stated supports the concept of the paging mechanism being ''underneath'' the segmentation mechanism. Therefore, for any given code or data reference in memory, segmentation exceptions are generated before paging exceptions are generated.

4.8.7 INSTRUCTION RESTART

The Military Intel486 processor fully supports restarting all instructions after faults. If an exception is detected in the instruction to be executed (exception categories 4 through 10 in Table 4-17), the Military Intel486 processor invokes the appropriate exception service routine.

The Military Intel486 processor is in a state that permits restart of the instruction, for all cases except the following. An instruction causes a task switch to a task whose Task State Segment is **partially** ''not present.'' (An entirely ''not present'' TSS is restartable.) Partially present TSSs can be avoided either by keeping the TSSs of such tasks present in memory, or by aligning TSS segments to reside entirely within a single 4K page (for TSS segments of 4 Kbytes or less).

NOTE:
Such cases are easily avoided by proper design of the operating system.

4.8.8 DOUBLE FAULT

A Double Fault (exception 8) results when the Military Intel486 processor attempts to invoke an exception service routine for the segment exceptions (10, 11, 12 or 13), but in the process of doing so, detects an exception other than a Page Fault (exception 14).

A Double Fault (exception 8) will also be generated when the Military Intel486 processor attempts to invoke the Page Fault (exception 14) service routine, and detects an exception other than a second Page Fault. In any functional system, the entire Page Fault service routine must remain ''present'' in memory.

When a Double Fault occurs, the Military Intel486 processor invokes the exception service routine for exception 8.

4.8.9 FLOATING POINT INTERRUPT VECTORS

Several interrupt vectors of the Military Intel486 DX, IntelDX2, and IntelDX4 processors are used to report exceptional conditions while executing numeric programs in either real or protected mode. Table 4-18 shows these interrupts and their causes.

Table 4-18. Interrupt Vectors Used by FPU

Interrupt Number	Cause of Interrupt
7	A Floating Point instruction was encountered when EM or TS of the Military Intel486 DX, IntelDX2, and IntelDX4 processor control register zero (CR0) was set. EM = 1 indicates that software emulation of the instruction is required. When TS is set, either a Floating Point or WAIT instruction causes interrupt 7. This indicates that the current FPU context may not belong to the current task.
13	The first word or doubleword of a numeric operand is not entirely within the limit of its segment. The return address pushed onto the stack of the exception handler points at the Floating Point instruction that caused the exception, including any prefixes. The FPU has not executed this instruction; the instruction pointer and data pointer register refer to a previous, correctly executed instruction.
16	The previous numerics instruction caused an unmasked exception. The address of the faulty instruction and the address of its operand are stored in the instruction pointer and data pointer registers. Only Floating Point and WAIT instructions can cause this interrupt. The Military Intel486 DX, IntelDX2, and IntelDX4 processors return address pushed onto the stack of the exception handler points to a WAIT or Floating Point instruction (including prefixes). This instruction can be restarted after clearing the exception condition in the FPU. The FNINIT, FNCLEX, FNSTSW, FNSTENV, and FNSAVE instructions can not cause this interrupt.

5.0 REAL MODE ARCHITECTURE

5.1 Introduction

When the Military Intel486 processor is reset or powered up, it is initialized in Real Mode. Real Mode has the same base architecture as the 8086 processor, except that it allows access to the 32-bit register set of the Military Intel486 processor. The Military Intel486 processor addressing mechanism, memory size and interrupt handling are identical to those of Real Mode on the 80286 processor.

All of the Military Intel486 processor instructions are available in Real Mode (except those instructions listed in section 6.5.4, ''Protection and I/O Permission Bitmap''). The default operand size in Real Mode is 16 bits, as in the 8086 processor. In order to use the 32-bit registers and addressing modes, override prefixes must be used. Also, the segment size on the Military Intel486 processor in Real Mode is 64 Kbytes, forcing 32-bit effective addresses to have a value less than 0000FFFFH. The primary purpose of Real Mode is to enable Protected Mode Operation.

The LOCK prefix on the Military Intel486 processor, even in Real Mode, is more restrictive than on the 80286 processor. This is due to the addition of paging on the Military Intel486 processor in Protected Mode and Virtual 8086 Mode. Paging makes it impossible to guarantee that repeated string instructions can be LOCKed. The Military Intel486 processor can not require that all pages holding the string be physically present in memory. Hence, a Page Fault (exception 14) might have to be taken during the repeated string instruction. Therefore, the LOCK prefix can not be supported during repeated string instructions.

Table 5-1 lists the only instruction forms where the LOCK prefix is legal on the Military Intel486 processor.

An exception 6 will be generated if a LOCK prefix is placed before any instruction form or opcode not listed above. The LOCK prefix allows indivisible read/modify/write operations on memory operands using the instructions above. For example, even the ADD Reg, Mem is not LOCKable, because the Mem operand is not the destination (and therefore no memory read/modify/operation is being performed).

Because, on the Military Intel486 processor, repeated string instructions are not LOCKable, it is not possible to LOCK the bus for a long period of time. Therefore, the LOCK prefix is not IOPL-sensitive on the Military Intel486 processor. The LOCK prefix can be used at any privilege level, but only on the instruction forms listed above.

Table 5-1. Instruction Forms Where LOCK Prefix Is Legal

Opcode	Operands (Dest, Source)
BIT Test and SET/RESET/COMPLEMENT	Mem, Reg/immed
XCHG	Reg, Mem
CHG	Mem, Reg
ADD, OR, ADC, SBB, AND, SUB, XOR	Mem, Reg/immed
NOT, NEG, INC, DEC	Mem
CMPXCHG, XADD	Mem, Reg

5.2 Memory Addressing

In Real Mode the maximum memory size is limited to 1 megabyte. (See Figure 5-1.) Thus, only address lines A2–A19 are active. (Exception, after RESET address lines A20–A31 are high during CS-relative memory cycles until an intersegment jump or call is executed. See section 9.5, ''Reset and Initialization''.)

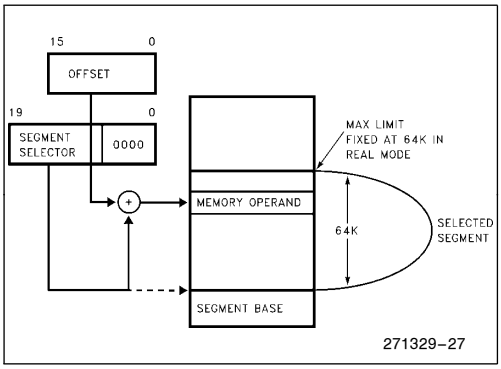


Figure 5-1. Real Address Mode Addressing

Because paging is not allowed in Real Mode, the linear addresses are the same as the physical addresses. Physical addresses are formed in Real Mode by adding the contents of the appropriate segment register, which is shifted left by four bits to an effective address. This addition results in a physi-

cal address from 00000000H to 0010FFEFH. This is compatible with 80286 Real Mode. Because segment registers are shifted left by 4 bits, Real Mode segments always start on 16-byte boundaries.

All segments in Real Mode are exactly 64-Kbytes long, and may be read, written, or executed. The Military Intel486 processor will generate an exception 13 if a data operand or instruction fetch occurs past the end of a segment (i.e., if an operand has an offset greater than FFFFH, for example, a word with a low byte at FFFFH and the high byte at 0000H).

Segments may be overlapped in Real Mode. Thus, if a particular segment does not use all 64 Kbytes, another segment can be overlaid on top of the unused portion of the previous segment. This allows the programmer to minimize the amount of physical memory needed for a program.

5.3 Reserved Locations

There are two fixed areas in memory which are reserved in Real address mode: system initialization area and the interrupt table area. Locations 00000H through 003FFH are reserved for interrupt vectors. Each one of the 256 possible interrupts has a 4-byte jump vector reserved for it. Locations FFFFFFF0H through FFFFFFFFH are reserved for system initialization.

5.4 Interrupts

Many of the exceptions shown in Table 4-16 and discussed in section 4.8.3, ‘‘Maskable Interrupt,’’ are not applicable to Real Mode operation, in particular exceptions 10, 11, 14, 17, which do not happen in Real Mode. Other exceptions have slightly different meanings in Real Mode; Table 5-2 identifies these exceptions.

5.5 Shutdown and Halt

The HALT instruction stops program execution and prevents the Military Intel486 processor from using the local bus until restarted. Either NMI, INTR with interrupts enabled (IF = 1), or RESET will force the Military Intel486 processor out of halt. If interrupted, the saved CS:IP will point to the next instruction after the HLT.

As in the case of protected mode, the shutdown will occur when a severe error is detected that prevents further processing. In Real Mode, shutdown can occur under two conditions, as follows:

- An interrupt or an exception occurs (exceptions 8 or 13) and the interrupt vector is larger than the Interrupt Descriptor Table (i.e., there is not an interrupt handler for the interrupt).
- A CALL, INT or PUSH instruction attempts to wrap around the stack segment when SP is not even (i.e., pushing a value on the stack when SP = 0001 resulting in a stack segment greater than FFFFH).

An NMI input can bring the processor out of shutdown if the Interrupt Descriptor Table limit is large enough to contain the NMI interrupt vector (at least 0017H) and the stack has enough room to contain the vector and flag information (i.e., SP is greater than 0005H). If these conditions are not met, the Military Intel486 processor is unable to execute the NMI and executes another shutdown cycle. In this case, the Military Intel486 processor remains in the shutdown and can only exit via the RESET input.

Table 5-2. Exceptions with Different Meanings in Real Mode (see Table 4-17)

Function	Interrupt Number	Related Instructions	Return Address Location
Interrupt table limit too small	8	INT Vector is not within table limit	Before Instruction
CS, DS, ES, FS, GS Segment overrun exception	13	Word memory reference beyond offset = FFFFH. An attempt to execute past the end of CS segment.	Before Instruction
SS Segment overrun exception	12	Stack Reference beyond offset = FFFFH	Before Instruction

6.0 PROTECTED MODE ARCHITECTURE

The complete capabilities of the Military Intel486 processor are unlocked when the Military Intel486 processor operates in Protected Virtual Address Mode (Protected Mode). Protected Mode vastly increases the linear address space to four Gbytes (2^{32} bytes) and allows the running of virtual memory programs of almost unlimited size (64 terabytes or 2^{46} bytes). In addition Protected Mode allows the Military Intel486 processor to run all of the existing 8086, 80286 and Intel386 processor software, while providing a sophisticated memory management and a hardware-assisted protection mechanism. Protected Mode allows the use of additional instructions especially optimized for supporting multitasking operating systems. The base architecture of the Military Intel486 processor remains the same, the registers, instructions, and addressing modes described in the previous sections are retained. The main difference between Protected Mode and Real Mode from a programmer's view is the increased address space and a different addressing mechanism.

6.1 Addressing Mechanism

Like Real Mode, Protected Mode uses two components to form the logical address, a 16-bit selector is used to determine the linear base address of a segment, the base address is added to a 32-bit effective address to form a 32-bit linear address. The linear address is then either used as the 32-bit physical address, or if paging is enabled the paging mechanism maps the 32-bit linear address into a 32-bit physical address.

The difference between the two modes lies in calculating the base address. In Protected Mode the selector is used to specify an index into an operating system defined table. (See Figure 6-1.) The table contains the 32-bit base address of a given segment. The physical address is formed by adding the base address obtained from the table to the offset.

Paging provides an additional memory management mechanism which operates only in Protected Mode. Paging provides a means of managing the very large segments of the Military Intel486 processor. As such, paging operates beneath segmentation. The paging mechanism translates the protected linear address which comes from the segmentation unit into a physical address. Figure 6-2 shows the complete Military Intel486 processor addressing mechanism with paging enabled.

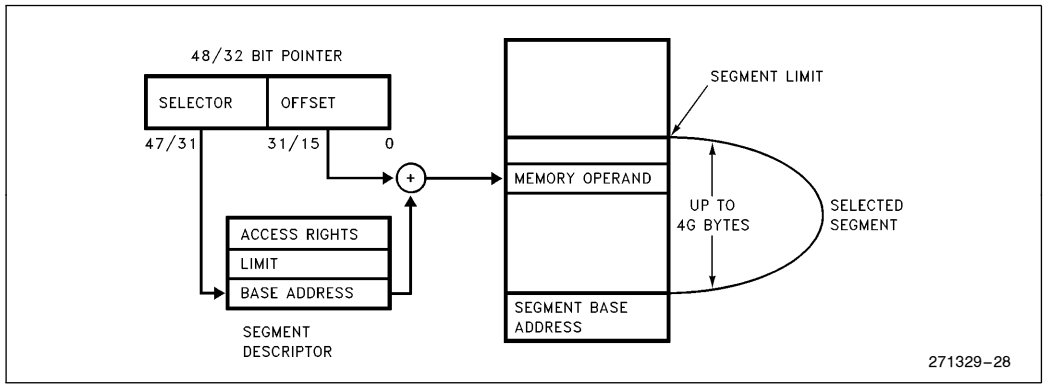


Figure 6-1. Protected Mode Addressing

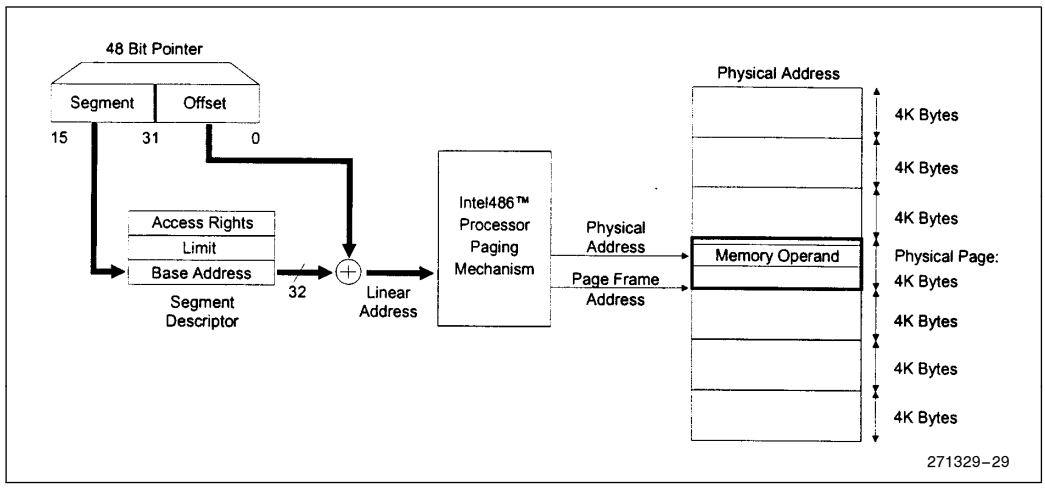


Figure 6-2. Paging and Segmentation

6.2 Segmentation

6.2.1 SEGMENTATION INTRODUCTION

Segmentation is one method of memory management. Segmentation provides the basis for protection. Segments are used to encapsulate regions of memory which have common attributes. For example, all of the code of a given program could be contained in a segment, or an operating system table may reside in a segment. All information about a segment is stored in an 8-byte data structure called a descriptor. All of the descriptors in a system are contained in tables recognized by hardware.

6.2.2 TERMINOLOGY

The following terms are used throughout the discussion of descriptors, privilege levels and protection:

PL: Privilege Level—One of the four hierarchical privilege levels. Level 0 is the most privileged level and level 3 is the least privileged. More privileged levels are numerically smaller than less privileged levels.

RPL: Requester Privilege Level—The privilege level of the original supplier of the selector. RPL is determined by the **least two** significant bits of a selector.

DPL: Descriptor Privilege Level—This is the least privileged level at which a task may access that descriptor (and the segment associated with that descriptor). Descriptor Privilege Level is determined by bits 6:5 in the Access Right Byte of a descriptor.

CPL: Current Privilege Level—The privilege level at which a task is currently executing, which equals the privilege level of the code segment being executed. CPL can also be determined by examining the lowest 2 bits of the CS register, except for conforming code segments.

EPL: Effective Privilege Level—The effective privilege level is the least privileged of the RPL and DPL. Because smaller privilege level **values** indicate greater privilege, EPL is the numerical maximum of RPL and DPL.

Task: One instance of the execution of a program. Tasks are also referred to as processes.

6.2.3 DESCRIPTOR TABLES

6.2.3.1 Descriptor Tables Introduction

The descriptor tables define all of the segments which are used in a Military Intel486 processor system. (See Figure 6-3.) There are three types of tables on the Military Intel486 processor which hold descriptors: the Global Descriptor Table, Local Descriptor Table, and the Interrupt Descriptor Table. All of the tables are variable length memory arrays. They can range in size between 8 bytes and 64 Kbytes. Each table can hold up to 8192 8-byte descriptors. The upper 13 bits of a selector are used as an index into the descriptor table. The tables have registers associated with them which hold the 32-bit linear base address, and the 16-bit limit of each table.

Each of the tables has a register associated with it, the GDTR, LDTR, and the IDTR (see Figure 6-3). The LGDT, LLDT, and LIDT instructions, load the base and limit of the Global, Local, and Interrupt Descriptor Tables, respectively, into the appropriate register. The SGDT, SLDT, and SIDT store the base and limit values. These tables are manipulated by the operating system. Therefore, the load descriptor table instructions are privileged instructions.

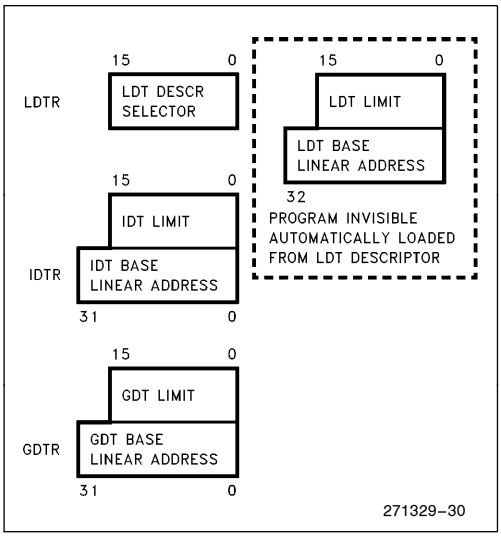


Figure 6-3. Descriptor Table Registers

6.2.3.2 Global Descriptor Table

The Global Descriptor Table (GDT) contains descriptors which are possibly available to all of the tasks in a system. The GDT can contain any type of segment descriptor except for descriptors which are used for servicing interrupts (i.e., interrupt and trap descriptors). Every Military Intel486 processor system contains a GDT. Generally the GDT contains code and data segments used by the operating systems and task state segments, and descriptors for the LDTs in a system.

The first slot of the Global Descriptor Table corresponds to the null selector and is not used. The null selector defines a null pointer value.

6.2.3.3 Local Descriptor Table

LDTs contain descriptors which are associated with a given task. Generally, operating systems are designed so that each task has a separate LDT. The LDT may contain only code, data, stack, task gate, and call gate descriptors. LDTs provide a mechanism for isolating a given task's code and data segments from the rest of the operating system, while the GDT contains descriptors for segments which are common to all tasks. A segment cannot be accessed by a task if its segment descriptor does not exist in either the current LDT or the GDT. This provides both isolation and protection for a task's segments, while still allowing global data to be shared among tasks.

Unlike the 6-byte GDT or IDT registers which contain a base address and limit, the visible portion of the LDT register contains only a 16-bit selector. This selector refers to a Local Descriptor Table descriptor in the GDT.

6.2.3.4 Interrupt Descriptor Table

The third table needed for Military Intel486 processor systems is the Interrupt Descriptor Table. (See Figure 6-4.) The IDT contains the descriptors which point to the location of up to 256 interrupt service routines. The IDT may contain only task gates, interrupt gates, and trap gates. The IDT should be at least 256 bytes in size in order to hold the descriptors for the 32 Intel Reserved Interrupts. Every interrupt used by a system must have an entry in the IDT. The IDT entries are referenced via INT instructions, external interrupt vectors, and exceptions. (See section 4.8, ''Interrupts.'')

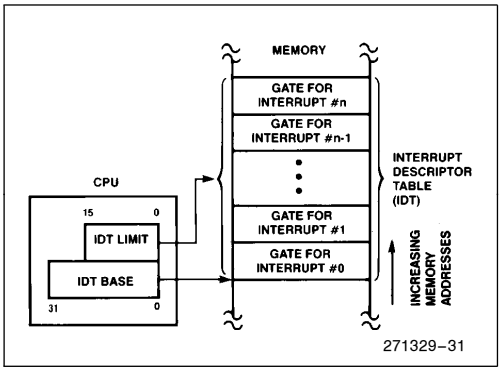


Figure 6-4. Interrupt Descriptor Table Register Use

6.2.4 DESCRIPTORS

6.2.4.1 Descriptor Attribute Bits

The object to which the segment selector points to is called a descriptor. Descriptors are eight-byte quantities that contain attributes about a given region of linear address space (i.e., a segment). These attributes include the 32-bit base linear address of the segment, the 20-bit length and granularity of the segment, the protection level, read, write or execute privileges, the default size of the operands (16-bit or 32-bit), and the type of segment. All of the attribute information about a segment is contained in 12 bits in the segment descriptor. All segments on the Military Intel486 processor have three attribute fields in common: the **P** bit, the **DPL** bit, and the **S** bit. The Present **P** bit is 1 if the segment is loaded in physical memory. If P = 0, any attempt to access this segment will cause a not present exception (exception 11). The Descriptor Privilege Level **DPL** is a two-bit field that specifies the protection level 0–3 associated with a segment.

The Military Intel486 processor has two main categories of segments: system segments and non-system segments (for code and data). The segment **S** bit in the segment descriptor determines if a given segment is a system segment or a code or data segment. If the **S** bit is 1, the segment is either a code or data segment. If it is 0, the segment is a system segment.

6.2.4.2 Military Intel486 Processor Code, Data Descriptors (S = 1)

Figure 6-5 shows the general format of a code and data descriptor and Table 6-1 illustrates how the bits in the Access Rights Byte are interpreted. The Access Rights Bytes is bits 24–31 associated with the segment limit.

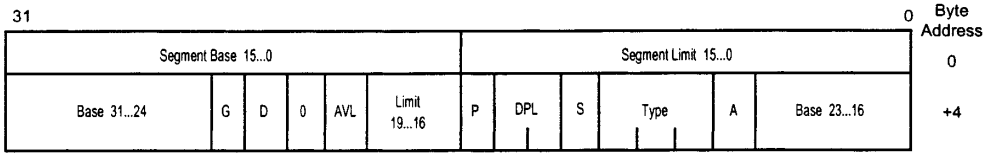
Code and data segments have several descriptor fields in common. The accessed **A** bit is set whenever the processor accesses a descriptor. The **A** bit is used by operating systems to keep usage statistics on a given segment. The **G** bit, or granularity bit, specifies if a segment length is byte-granular or page-granular. Military Intel486 processor segments can be one megabyte long with byte granularity (G = 0) or four gigabytes with page granularity (G = 1), (i.e., 2^{20} pages each page is 4 Kbytes in length). The granularity is totally unrelated to paging. A Military Intel486 processor system can consist of segments with byte granularity, and page granularity, whether or not paging is enabled.

The executable **E** bit tells if a segment is a code or data segment. A code segment (E = 1, S = 1) may be execute-only or execute/read as determined by the Read **R** bit. Code segments are execute only if R = 0, and execute/read if R = 1. Code segments may never be written into.

NOTE:
Code segments may be modified via aliases. Aliases are writeable data segments which occupy the same range of linear address space as the code segment.

The **D** bit indicates the default length for operands and effective addresses. If D = 1 then 32-bit operands and 32-bit addressing modes are assumed. If D = 0 then 16-bit operands and 16-bit addressing modes are assumed. Therefore all existing 80286 code segments will execute on the Military Intel486 processor assuming the D bit is set 0.

Another attribute of code segments is determined by the conforming **C** bit. Conforming segments, C = 1, can be executed and shared by programs at different privilege levels. (See section 6.3, ‘‘Protection.’’)



BASE	Base Address of the segment
LIMIT	The length of the segment
P	Present Bit 1 = Present, 0 = Not Present
DPL	Descriptor Privilege Level 0–3
S	Segment Descriptor 0 = System Descriptor, 1 = Code or Data Segment Descriptor
TYPE	Type of Segment
A	Accessed Bit
G	Granularity Bit 1 = Segment length is page granular, 0 = Segment length is byte granular
D	Default Operation Size (recognized in code segment descriptors only) 1 = 32-bit segment, 0 = 16-bit segment
0	Bit must be zero (0) for compatibility with future processors
AVL	Available field for user or OS

NOTE:
In a maximum-size segment (i.e., a segment with G = 1 and segment limit 19. . .0 = FFFFFH), the lowest 12 bits of the segment base should be zero (i.e., segment base 11. . .000 = 000H).

Figure 6-5. Segment Descriptors

Table 6-1. Access Rights Byte Definition for Code and Data Descriptions

Bit Position	Name	Function	
7	Present (P)	P = 1	Segment is mapped into physical memory.
		P = 0	No mapping to physical memory exits, base and limit are not used.
6–5	Descriptor Privilege Level (DPL)		Segment privilege attribute used in privilege tests.
4	Segment Descriptor (S)	S = 1	Code or Data (includes stacks) segment descriptor.
		S = 0	System Segment Descriptor or Gate Descriptor.
		If Data Segment (S = 1, E = 0)	
3	Executable (E)	E = 0	Descriptor type is data segment:
2	Expansion Direction (ED)	ED = 0	Expand up segment, offsets must be ≤ limit.
		ED = 1	Expand down segment, offsets must be > limit.
1	Writeable (W)	W = 0	Data segment may not be written into.
		W = 1	Data segment may be written into.
		If Code Segment (S = 1, E = 1)	
3	Executable (E)	E = 1	Descriptor type is code segment:
2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged.
1	Readable (R)	R = 0	Code segment may not be read.
		R = 1	Code segment may be read.
0	Accessed (A)	A = 0	Segment has not been accessed.
		A = 1	Segment selector has been loaded into segment register or used by selector test instructions.

Segments identified as data segments (E = 0, S = 1) are used for two types of Military Intel486 processor segments: stack and data segments. The expansion direction **(ED)** bit specifies if a segment expands downward (stack) or upward (data). If a segment is a stack segment all offsets must be greater than the segment limit. On a data segment all offsets must be less than or equal to the limit. In other words, stack segments start at the base linear address plus the maximum segment limit and grow down to the base linear address plus the limit. On the other hand, data segments start at the base linear address and expand to the base linear address plus limit.

The write **W** bit controls the ability to write into a segment. Data segments are read-only if W = 0. The stack segment must have W = 1.

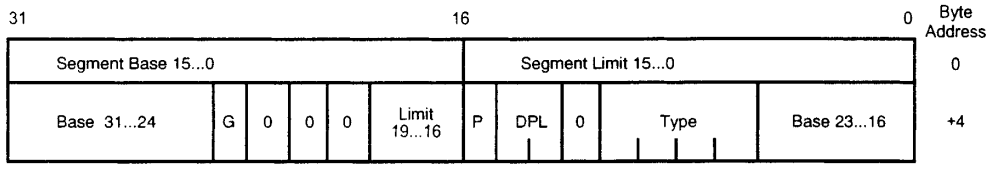
The **B** bit controls the size of the stack pointer register. If B = 1, then PUSHes, POPs, and CALLs all use the 32-bit ESP register for stack references and assume an upper limit of FFFFFFFFH. If B = 0, stack instructions all use the 16-bit SP register and assume an upper limit of FFFFH.

6.2.4.3 System Descriptor Formats

System segments describe information about operating system tables, tasks, and gates. Figure 6-6 shows the general format of system segment descriptors, and the various types of system segments. Military Intel486 processor system descriptors contain a 32-bit base linear address and a 20-bit segment limit. 80286 system descriptors have a 24-bit base address and a 16-bit segment limit. 80286 system descriptors are identified by the upper 16 bits being all zero.

6.2.4.4 LDT Descriptors (S = 0, TYPE = 2)

LDT descriptors (S = 0, TYPE = 2) contain information about Local Descriptor Tables. LDTs contain a table of segment descriptors, unique to a particular task. Because the instruction to load the LDTR is only available at privilege level 0, the DPL field is ignored. LDT descriptors are only allowed in the Global Descriptor Table (GDT).



Type	Defines
0	Invalid
1	Available 80286 TSS
2	LDT
3	Busy 80286 TSS
4	80286 call gate
5	Task Gate (for 80286, Military Intel486™ processor task)
6	80286 interrupt gate
7	80286 trap gate
8	Invalid
9	Available Military Intel486 processor TSS
A	Undefined (Intel Reserved)
B	Busy Military Intel486 processor TSS
C	Military Intel486 processor call gate
D	Undefined (Intel Reserved)
E	Military Intel486 processor
F	Military Intel486 processor

Figure 6-6. System Segment Descriptors

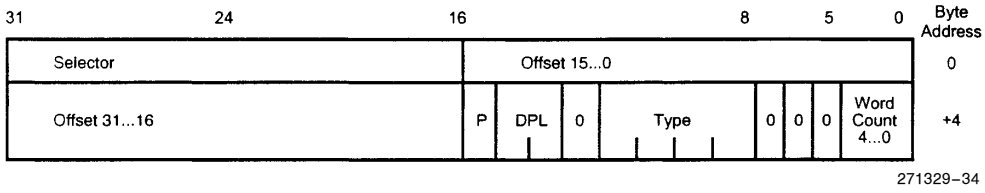
6.2.4.5 TSS Descriptors (S = 0, TYPE = 1, 3, 9, B)

A Task State Segment (TSS) descriptor contains information about the location, size, and privilege level of a Task State Segment (TSS). A TSS in turn is a special fixed format segment which contains all the state information for a task and a linkage field to permit nesting tasks. The TYPE field is used to indicate whether the task is currently BUSY (i.e., on a chain of active tasks) or the TSS is available. The TYPE field also indicates if the segment contains an 80286 processor TSS or a Military Intel486 processor TSS. The Task Register (TR) contains the selector which points to the current Task State Segment.

6.2.4.6 Gate Descriptors (S = 0, TYPE = 4–7, C, F)

Gates are used to control access to entry points within the target code segment. The various types of gate descriptors are **call** gates, **task** gates, **interrupt** gates, and **trap** gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the processor to automatically perform protection checks. It also allows system designers to control entry points to the operating system. Call gates are used to change privilege levels (see section 6.3, ''Protection''), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines.

Figure 6-7 shows the format of the four types of gate descriptors. Call gates are primarily used to transfer program control to a more privileged level. The call gate descriptor consists of three fields: the access byte, a long pointer (selector and offset) which points to the start of a routine and a word count which specifies how many parameters are to be copied from the caller's stack to the stack of the called routine. The word count field is only used by call gates when there is a change in the privilege level, other types of gates ignore the word count field.



Gate Descriptor Fields

Name	Value	Description
Type	4	80286 call gate
	5	Task gate (for 80286 or Military Intel486 processor task)
	6	80286 interrupt gate
	7	80286 trap gate
	C	Military Intel486™ processor call gate
	E	Military Intel486 processor interrupt gate
	F	Military Intel486 processor trap gate
P	0	Descriptor contents are not valid
	1	Descriptor contents are valid

DPL—least privileged level at which a task may access the gate. WORD COUNT 0–31—the number of parameters to copy from caller's stack to the called procedure's stack. The parameters are 32-bit quantities for Military Intel486 processor gates, and 16-bit quantities for 80286 gates.

DESTINATION SELECTOR	16-bit selector	Selector to the target code segment or Selector to the target task state segment for task gate
DESTINATION OFFSET	offset	Entry point within the target code segment
	16-bit 80286	
	32-bit Military Intel486 processor	

Figure 6-7. Gate Descriptor Formats

Interrupt and trap gates use the destination selector and destination offset fields of the gate descriptor as a pointer to the start of the interrupt or trap handler routines. The difference between interrupt gates and trap gates is that the interrupt gate disables interrupts (resets the IF bit), while the trap gate does not.

Task gates are used to switch tasks. Task gates may only refer to a task state segment. (See section 6.3.6, ''Task Switching.'') Therefore, only the destination selector portion of a task gate descriptor is used, and the destination offset is ignored.

Exception 13 is generated when a destination selector does not refer to a correct descriptor type, i.e., a code segment for an interrupt, trap or call gate, a TSS for a task gate.

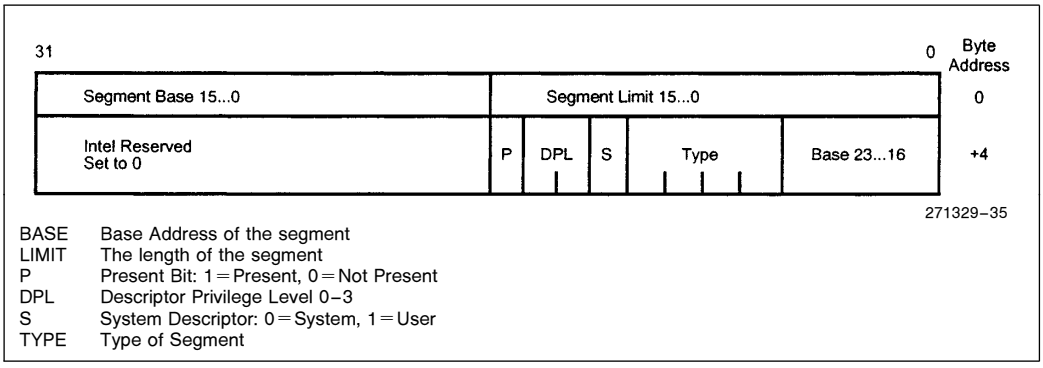
The access byte format is the same for all gate descriptors. P = 1 indicates that the gate contents are valid. P = 0 indicates the contents are not valid and causes exception 11 if referenced. DPL is the descriptor privilege level and specifies when this descriptor may be used by a task. (See section 6.3, ''Protection.'') The S field, bit 4 of the access rights byte, must be 0 to indicate a system control descriptor. The type field specifies the descriptor type as indicated in Figure 6-7.

6.2.4.7 Differences Between Military Intel486 Processor and 80286 Descriptors

In order to provide operating system compatibility between 80286 and Military Intel486 processors, the Military Intel486 processor supports all of the 80286 segment descriptors. Figure 6-8 shows the general format of an 80286 system segment descriptor. The only differences between 80286 and Military Intel486 processor descriptor formats are that the values of the type fields, and the limit and base address fields have been expanded for the Military Intel486 processor. The 80286 system segment descriptors contained a 24-bit base address and 16-bit limit, while the Military Intel486 processor system segment descriptors have a 32-bit base address, a 20-bit limit field, and a granularity bit.

By supporting 80286 system segments the Military Intel486 processor is able to execute 80286 application programs on a Military Intel486 processor operating system. This is possible because the Military Intel486 processor automatically understands which descriptors are 80286-style descriptors and which descriptors are Military Intel486 processor-style descriptors. In particular, if the upper word of a descriptor is zero, then that descriptor is an 80286-style descriptor.

The only other differences between 80286-style descriptors and Military Intel486 processor descriptors is the interpretation of the word count field of call gates and the B bit. The word count field specifies the number of 16-bit quantities to copy for 80286 call gates and 32-bit quantities for Military Intel486 processor call gates. The B bit controls the size of PUSHes when using a call gate; if B = 0 PUSHes are 16 bits, if B = 1 PUSHes are 32 bits.



BASE Base Address of the segment
LIMIT The length of the segment
P Present Bit: 1 = Present, 0 = Not Present
DPL Descriptor Privilege Level 0–3
S System Descriptor: 0 = System, 1 = User
TYPE Type of Segment

Figure 6-8. 80286 Code and Data Segment Descriptors

6.2.4.8 Selector Fields

A selector in Protected Mode has three fields: Local or Global Descriptor Table Indicator (TI), Descriptor Entry Index (Index), and Requester (the selector's) Privilege Level (RPL) as shown in Figure 6-9. The TI bits select one of two memory-based tables of descriptors (the Global Descriptor Table or the Local Descriptor Table). The Index selects one of 8K descriptors in the appropriate descriptor table. The RPL bits allow high speed testing of the selector's privilege attributes.

6.2.4.9 Segment Descriptor Cache

In addition to the selector value, every segment register has a segment descriptor cache register associated with it. Whenever a segment register's contents are changed, the 8-byte descriptor associated with that selector is automatically loaded (cached) on the chip. Once loaded, all references to that segment use the cached descriptor information instead of reaccessing the descriptor. The contents of the descriptor cache are not visible to the programmer. Because descriptor caches only change when a segment register is changed, programs that modify the descriptor tables must reload the appropriate segment registers after changing a descriptor's value.

6.2.4.10 Segment Descriptor Register Settings

The contents of the segment descriptor cache vary depending on the mode the Military Intel486 processor is operating in. When operating in Real Address Mode, the segment base, limit, and other attributes within the segment cache registers are defined as shown in Figure 6-10. For compatibility with the 8086 architecture, the base is set to sixteen times the current selector value, the limit is fixed at 0000FFFFH, and the attributes are fixed so as to indicate the segment is present and fully usable. In Real Address Mode, the internal ''privilege level'' is always fixed to the highest level, level 0, so I/O and other privileged opcodes may be executed.

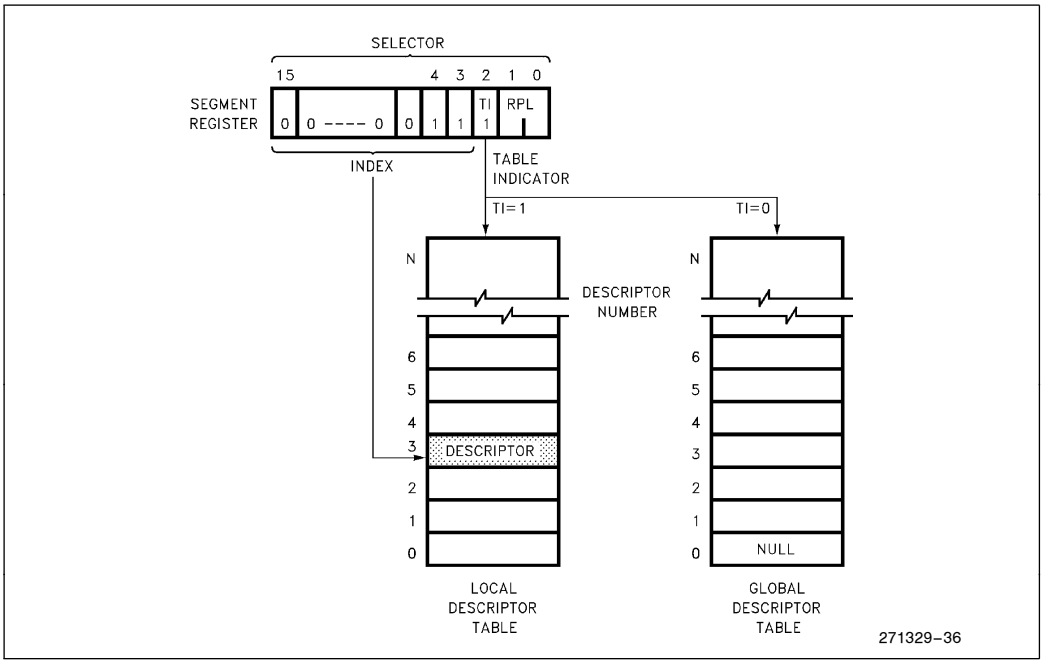
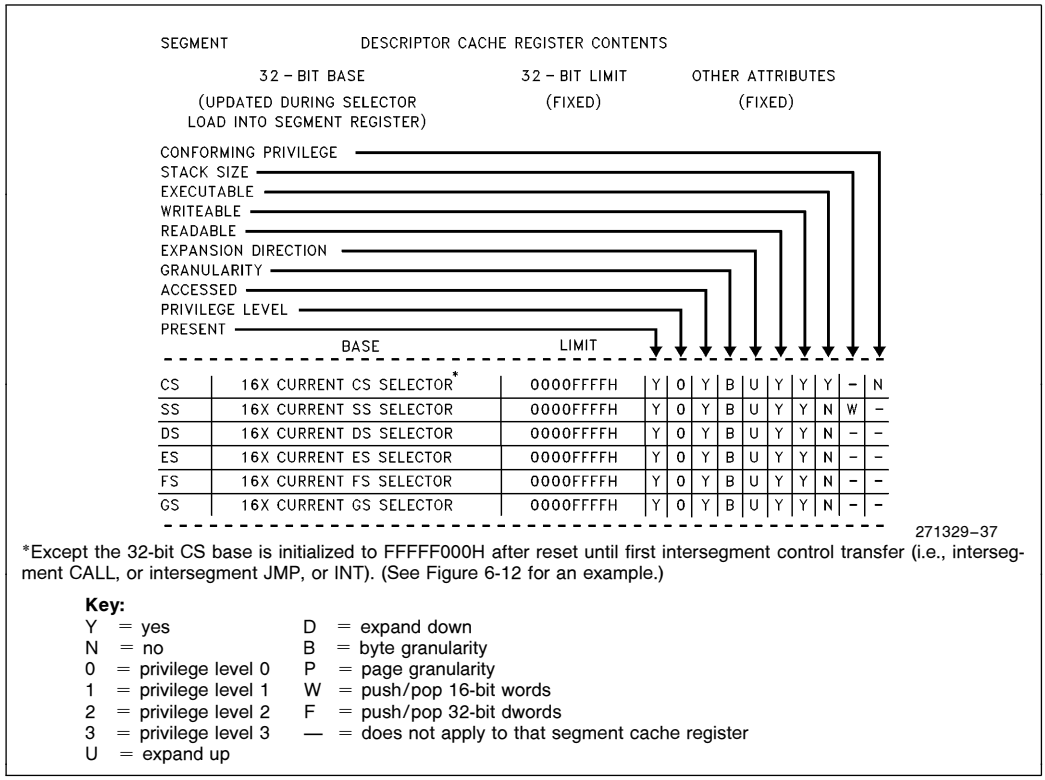


Figure 6-9. Example Descriptor Selection



*Except the 32-bit CS base is initialized to FFFFF000H after reset until first intersegment control transfer (i.e., intersegment CALL, or intersegment JMP, or INT). (See Figure 6-12 for an example.)

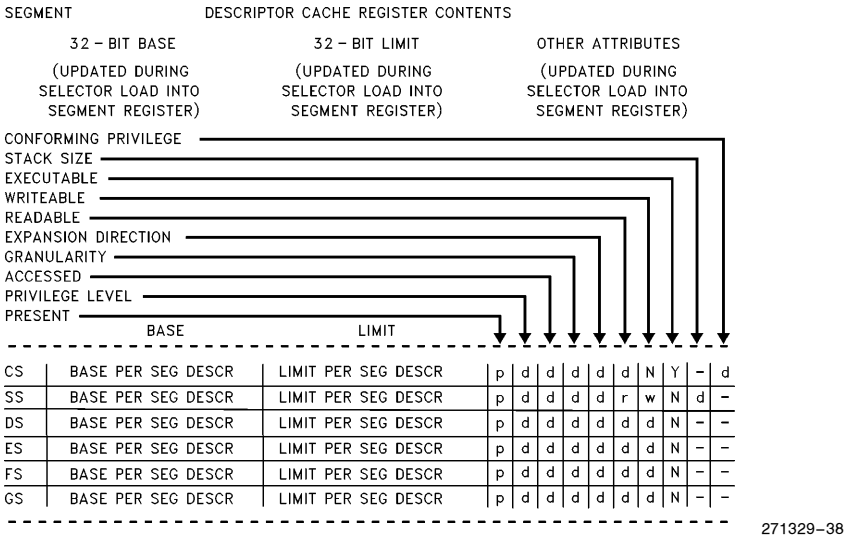
Key:

Y	= yes	D	= expand down
N	= no	B	= byte granularity
0	= privilege level 0	P	= page granularity
1	= privilege level 1	W	= push/pop 16-bit words
2	= privilege level 2	F	= push/pop 32-bit dwords
3	= privilege level 3	—	= does not apply to that segment cache register
U	= expand up		

Figure 6-10. Segment Descriptor Caches for Real Address Mode (Segment Limit and Attributes Are Fixed)

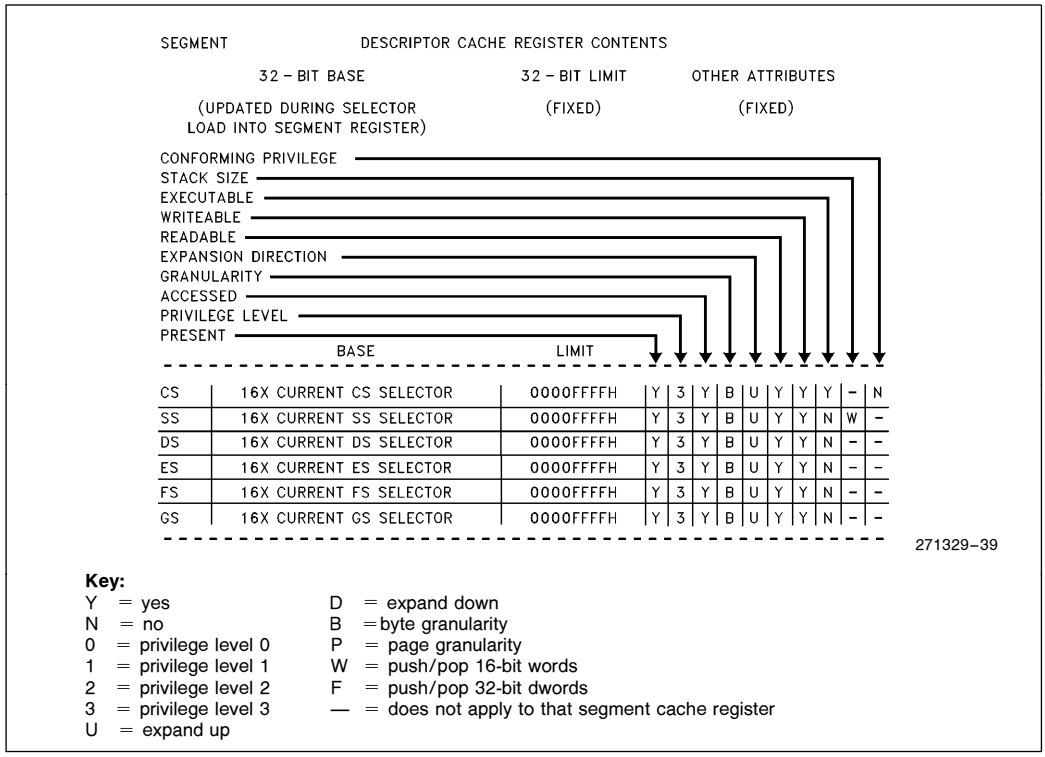
When operating in Protected Mode, the segment base, limit, and other attributes within the segment cache registers are defined as shown in Figure 6-11. In Protected Mode, each of these fields are defined according to the contents of the segment descriptor indexed by the selector value loaded into the segment register.

When operating in a Virtual 8086 Mode within the Protected Mode, the segment base, limit, and other attributes within the segment cache registers are defined as shown in Figure 6-12. For compatibility with the 8086 architecture, the base is set to sixteen times the current selector value, the limit is fixed at 0000FFFFH, and the attributes are fixed so as to indicate the segment is present and fully usable. The virtual program executes at lowest privilege level, level 3, to allow trapping of all IOPL-sensitive instructions and level-0-only instructions.



Key:
Y = fixed yes
N = fixed no
d = per segment descriptor
p = per segment descriptor; descriptor must indicate "present" to avoid exception 11 (exception 12 in case of SS)
r = per segment descriptor, but descriptor must indicate "readable" to avoid exception 13 (special case for SS)
w = per segment descriptor, but descriptor must indicate "writeable" to avoid exception 13 (special case for SS)
— = does not apply to that segment cache register

Figure 6-11. Segment Descriptor Caches for Protected Mode (Loaded per Descriptor)



Key:

Y = yes	D = expand down
N = no	B = byte granularity
0 = privilege level 0	P = page granularity
1 = privilege level 1	W = push/pop 16-bit words
2 = privilege level 2	F = push/pop 32-bit dwords
3 = privilege level 3	— = does not apply to that segment cache register
U = expand up	

Figure 6-12. Segment Descriptor Caches for Virtual 8086 Mode within Protected Mode (Segment Limit and Attributes are Fixed)

6.3 Protection

6.3.1 PROTECTION CONCEPTS

The Military Intel486 processor has four levels of protection which are optimized to support the needs of a multitasking operating system to isolate and protect user programs from each other and the operating system. The privilege levels control the use of privileged instructions, I/O instructions, and access to segments and segment descriptors. Unlike traditional processor-based systems where this protection is achieved only through the use of complex external hardware and software the Military Intel486 processor provides the protection as part of its integrated Memory Management Unit. The Military Intel486 processor offers an additional type of protection on a page basis, when paging is enabled (See section 6.4.3, ''Page Level Protection.'')

The four-level hierarchical privilege system is illustrated in Figure 6-13. It is an extension of the user/supervisor privilege mode commonly used by minicomputers and, in fact, the user/supervisor mode is fully supported by the Military Intel486 processor paging mechanism. The privilege levels (PL) are numbered 0 through 3. Level 0 is the most privileged or trusted level.

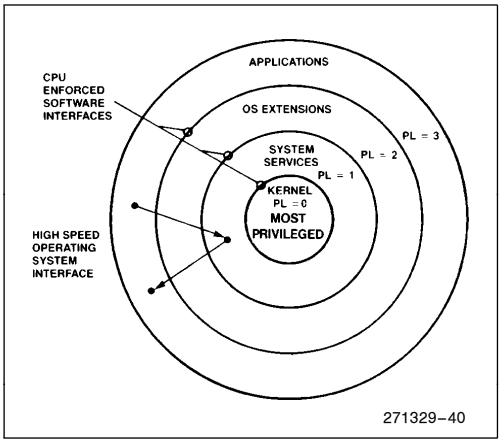


Figure 6-13. Four-Level Hierarchical Protection

6.3.2 RULES OF PRIVILEGE

The Military Intel486 processor controls access to both data and procedures between levels of a task, according to the following rules.

- Data stored in a segment with privilege level **p** can be accessed only by code executing at a privilege level at least as privileged as **p**.
- A code segment/procedure with privilege level **p** can only be called by a task executing at the same or a lesser privilege level than **p**.

6.3.3 PRIVILEGE LEVELS

6.3.3.1 Task Privilege

At any point in time, a task on the Military Intel486 processor always executes at one of the four privilege levels. The Current Privilege Level (CPL) specifies the task's privilege level. A task's CPL may only be changed by control transfers through gate descriptors to a code segment with a different privilege level. (See section 6.3.4, ''Privilege Level Transfers.'') Thus, an application program running at PL = 3 may call an operating system routine at PL = 1 (via a gate) which would cause the task's CPL to be set to 1 until the operating system routine was finished.

6.3.3.2 Selector Privilege (RPL)

The privilege level of a selector is specified by the RPL field. The RPL is the two least significant bits of the selector. The selector's RPL is only used to establish a less trusted privilege level than the current privilege level for the use of a segment. This level is called the task's effective privilege level (EPL). The EPL is defined as being the least privileged (i.e., numerically larger) level of a task's CPL and a selector's RPL. Thus, if selector's RPL = 0 then the CPL always specifies the privilege level for making an access using the selector. On the other hand if RPL = 3 then a selector can only access segments at level 3 regardless of the task's CPL. The RPL is most commonly used to verify that pointers passed to an operating system procedure do not access data that is of higher privilege than the procedure that originated the pointer. Because the originator of a selector can specify any RPL value, the Adjust RPL (ARPL) instruction is provided to force the RPL bits to the originator's CPL.

6.3.3.3 I/O Privilege and I/O Permission Bitmap

The I/O privilege level (IOPL, a 2-bit field in the EFLAG register) defines the least privileged level at which I/O instructions can be unconditionally performed. I/O instructions can be unconditionally performed when CPL $\geq$ IOPL. (The I/O instructions are IN, OUT, INS, OUTS, REP INS, and REP OUTS.) When CPL $>$ IOPL, and the current task is associated with a 286 TSS, attempted I/O instructions cause an exception 13 fault. When CPL $>$ IOPL, and the current task is associated with a Military Intel486 processor TSS, the I/O Permission Bitmap (part of a Military Intel486 processor TSS) is consulted on whether I/O to the port is allowed, or an exception 13 fault is to be generated instead. For diagrams of the I/O Permission Bitmap, refer to Figure 6-14 and Figure 6-15. For further information on how the I/O Permission Bitmap is used in Protected Mode or in Virtual 8086 Mode, refer to section 6.5.4, ''Protection and I/O Permission Bitmap.''

The I/O privilege level (IOPL) also affects whether several other instructions can be executed or cause an exception 13 fault instead. These instructions are called ''IOPL-sensitive'' instructions and they are CLI and STI. (Note that the LOCK prefix is *not* IOPL-sensitive on the Military Intel486 processor.)

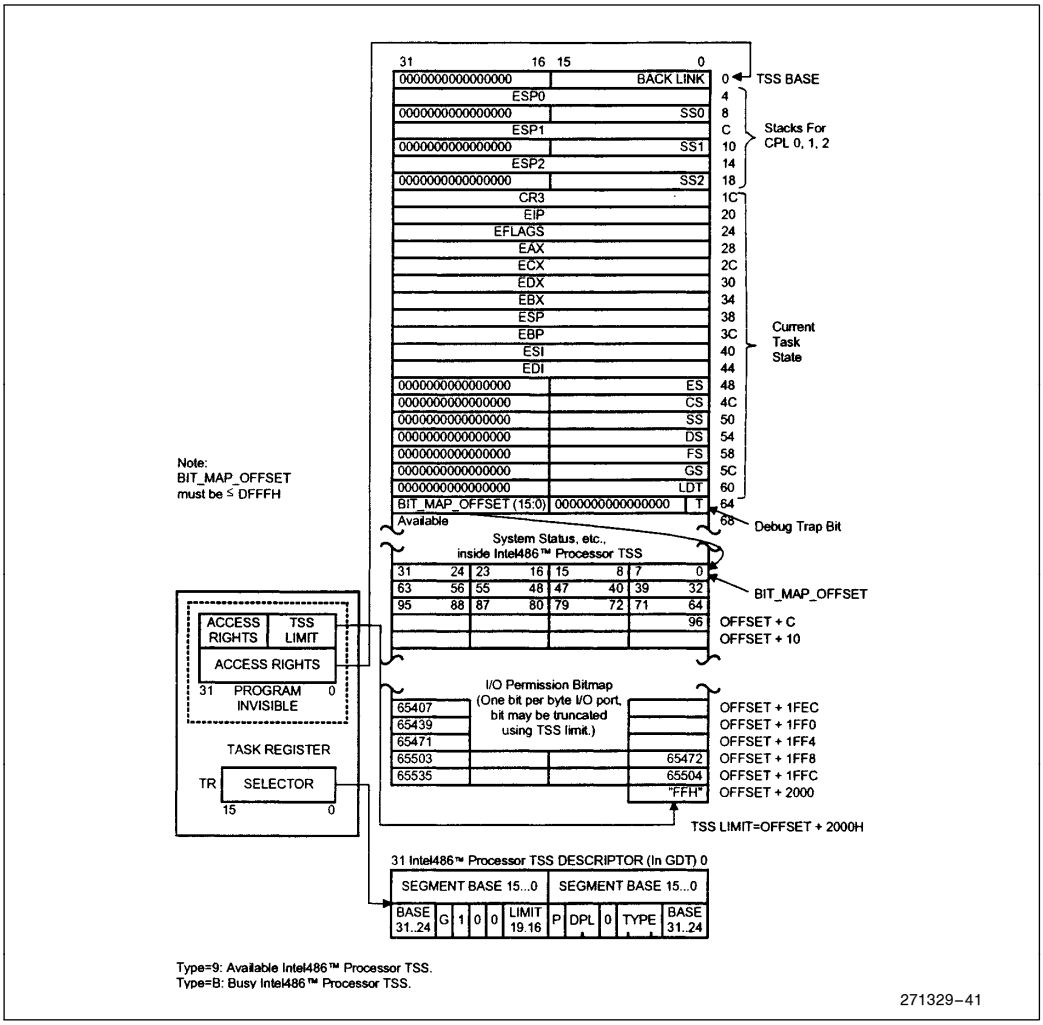
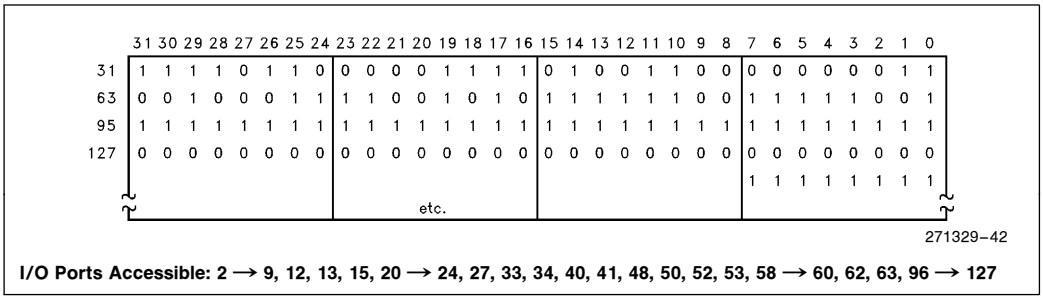


Figure 6-14. Military Intel486™ Processor TSS and TSS Registers



I/O Ports Accessible: 2 ⟶ 9, 12, 13, 15, 20 ⟶ 24, 27, 33, 34, 40, 41, 48, 50, 52, 53, 58 ⟶ 60, 62, 63, 96 ⟶ 127

Figure 6-15. Sample I/O Permission Bit Map

The IOPL also affects whether the IF (interrupts enable flag) bit can be changed by loading a value into the EFLAGS register. When CPL ≥ IOPL, then the IF bit can be changed by loading a new value into the EFLAGS register. When CPL > IOPL, the IF bit cannot be changed by a new value POPed into (or otherwise loaded into) the EFLAGS register; the IF bit merely remains unchanged and no exception is generated.

6.3.3.4 Privilege Validation

The Military Intel486 processor provides several instructions to speed pointer testing and help maintain system integrity by verifying that the selector value refers to an appropriate segment. Table 6-2 summarizes the selector validation procedures available for the Military Intel486 processor.

This pointer verification prevents the common problem of an application at PL = 3 calling a operating systems routine at PL = 0 and passing the operating system routine a ''bad'' pointer which corrupts a data structure belonging to the operating system. If the operating system routine uses the ARPL instruction to ensure that the RPL of the selector has no greater privilege than that of the caller, then this problem can be avoided.

6.3.3.5 Descriptor Access

There are basically two types of segment accesses: those involving code segments such as control transfers, and those involving data accesses. Determining the ability of a task to access a segment involves the type of segment to be accessed, the instruction used, the type of descriptor used and CPL, RPL, and DPL as described above.

Table 6-2. Pointer Test Instructions

Instruction	Operands	Function
ARPL	Selector, Register	Adjust Requested Privilege Level: adjusts the RPL of the selector to the numeric maximum of current selector RPL value and the RPL value in the register. Set zero flag if selector RPL was changed.
VERR	Selector	VERify for Read: sets the zero flag if the segment referred to by the selector can be read.
VERW	Selector	VERify for Write: sets the zero flag if the segment referred to by the selector can be written.
LSL	Register, Selector	Load Segment Limit: reads the segment limit into the register if privilege rules and descriptor type allow. Set zero flag if successful.
LAR	Register, Selector	Load Access Rights: reads the descriptor access rights byte into the register if privilege rules allow. Set zero flag if successful.

Any time an instruction loads data segment registers (DS, ES, FS, GS) the Military Intel486 processor makes protection validation checks. Selectors loaded in the DS, ES, FS, GS registers must refer only to data segments or readable code segments. The data access rules are specified in section 6.3.2, ''Rules of Privilege.'' The only exception to those rules is readable conforming code segments which can be accessed at any privilege level.

Finally the privilege validation checks are performed. The CPL is compared to the EPL and if the EPL is more privileged than the CPL an exception 13 (general protection fault) is generated.

The rules regarding the stack segment are slightly different than those involving data segments. Instructions that load selectors into SS must refer to data segment descriptors for writeable data segments. The DPL and RPL must equal the CPL. All other descriptor types or a privilege level violation will cause exception 13. A stack not present fault causes exception 12. Note that an exception 11 is used for a not-present code or data segment.

6.3.4 PRIVILEGE LEVEL TRANSFERS

Inter-segment control transfers occur when a selector is loaded in the CS register. For a typical system most of these transfers are simply the result of a call or a jump to another routine. There are five types of control transfers which are summarized in Table 6-3. Many of these transfers result in a privilege level transfer. Changing privilege levels is done only via control transfers, by using gates, task switches, and interrupt or trap gates.

Control transfers can only occur if the operation which loaded the selector references the correct descriptor type. Any violation of these descriptor usage rules will cause an exception 13 (e.g., JMP through a call gate, or IRET from a normal subroutine call).

In order to provide further system security, all control transfers are also subject to the privilege rules.

Table 6-3. Descriptor Types Used for Control Transfer

Control Transfer Types	Operation Types	Descriptor Referenced	Descriptor Table
Intersegment within the same privilege level	JMP, CALL, RET, IRET*	Code Segment	GDT/LDT
Intersegment to the same or higher privilege level	CALL	Call Gate	GDT/LDT
Interrupt within task may change CPL	Interrupt Instruction, Exception, External Interrupt	Trap or Interrupt Gate	IDT
Intersegment to a lower privilege level (changes task CPL)	RET, IRET(1)	Code Segment	GDT/LDT
	CALL, JMP	Task State Segment	GDT
Task Switch	CALL, JMP	Task Gate	GDT/LDT
	IRET(2) Interrupt Instruction, Exception, External Interrupt	Task Gate	IDT

NOTES:
1. NT (Nested Task bit of flag register) = 0
2. NT (Nested Task bit of flag register) = 1

The privilege rules require that:

- Privilege level transitions can only occur via gates.
- JMPs can be made to a non-conforming code segment with the same privilege or to a conforming code segment with greater or equal privilege.
- CALLs can be made to a non-conforming code segment with the same privilege or via a gate to a more privileged level.
- Interrupts handled within the task obey the same privilege rules as CALLs.
- Conforming Code segments are accessible by privilege levels which are the same or less privileged than the conforming-code segment's DPL.
- Both the requested privilege level (RPL) in the selector pointing to the gate and the task's CPL must be of equal or greater privilege than the gate's DPL.
- The code segment selected in the gate must be the same or more privileged than the task's CPL.
- Return instructions that do not switch tasks can only return control to a code segment with same or less privilege.
- Task switches can be performed by a CALL, JMP, or INT which references either a task gate or task state segment who's DPL is less privileged or the same privilege as the old task's CPL.

Any control transfer that changes CPL within a task causes a change of stacks as a result of the privilege level change. The initial values of SS:ESP for privilege levels 0, 1, and 2 are retained in the task state segment. (See section 6.3.6, ''Task Switching.'') During a JMP or CALL control transfer, the new stack pointer is loaded into the SS and ESP registers and the previous stack pointer is pushed onto the new stack.

When RETurning to the original privilege level, use of the lower-privileged stack is restored as part of the RET or IRET instruction operation. For subroutine calls that pass parameters on the stack and cross privilege levels, a fixed number of words (as specified in the gate's word count field) are copied from the previous stack to the current stack. The inter-segment RET instruction with a stack adjustment value will correctly restore the previous stack pointer upon return.

6.3.5 CALL GATES

Gates provide protected, indirect CALLs. One of the major uses of gates is to provide a secure method of privilege transfers within a task. Because the operating system defines all of the gates in a system, it can ensure that all gates only allow entry into a few trusted procedures (such as those which allocate memory, or perform I/O).

Gate descriptors follow the data access rules of privilege; that is, gates can be accessed by a task if the EPL, is equal to or more privileged than the gate descriptor's DPL. Gates follow the control transfer rules of privilege and therefore may only transfer control to a more privileged level.

Call Gates are accessed via a CALL instruction and are syntactically identical to calling a normal subroutine. When an inter-level Military Intel486 processor call gate is activated, the following actions occur.

1. Load CS:EIP from gate check for validity
2. SS is pushed zero-extended to 32 bits
3. ESP is pushed
4. Copy Word Count 32-bit parameters from the old stack to the new stack
5. Push Return address on stack

The procedure is identical for 80286 Call gates, except that 16-bit parameters are copied and 16-bit registers are pushed.

Interrupt Gates and Trap gates work in a similar fashion as the call gates, except there is no copying of parameters. The only difference between Trap and Interrupt gates is that control transfers through an Interrupt gate disable further interrupts (i.e., the IF bit is set to 0), and Trap gates leave the interrupt status unchanged.

6.3.6 TASK SWITCHING

A very important attribute of any multitasking/multiuser operating system is its ability to rapidly switch between tasks or processes. The Military Intel486 processor directly supports this operation by providing a task switch instruction in hardware. The Military Intel486 processor task switch operation saves the entire state of the machine (all of the registers, address space, and a link to the previous task), loads a new execution state, performs protection checks,

and commences execution in the new task, in about 10 microseconds. Like transfer of control via gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a Task State Segment (TSS), or a task gate descriptor in the GDT or LDT. An INT n instruction, exception, trap, or external interrupt may also invoke the task switch operation if there is a task gate descriptor in the associated IDT descriptor slot.

The TSS descriptor points to a segment (see Figure 6-14) containing the entire Military Intel486 processor execution state while a task gate descriptor contains a TSS selector. The Military Intel486 processor supports both 80286 and Military Intel486 processor style TSSs. Figure 6-16 shows an 80286 TSS. The limit of a Military Intel486 processor TSS must be greater than 0064H (002BH for an 80286 TSS), and can be as large as 4 Gbytes. In the additional TSS space, the operating system is free to store additional information such as the reason the task is inactive, time the task has spent running, and open files belong to the task.

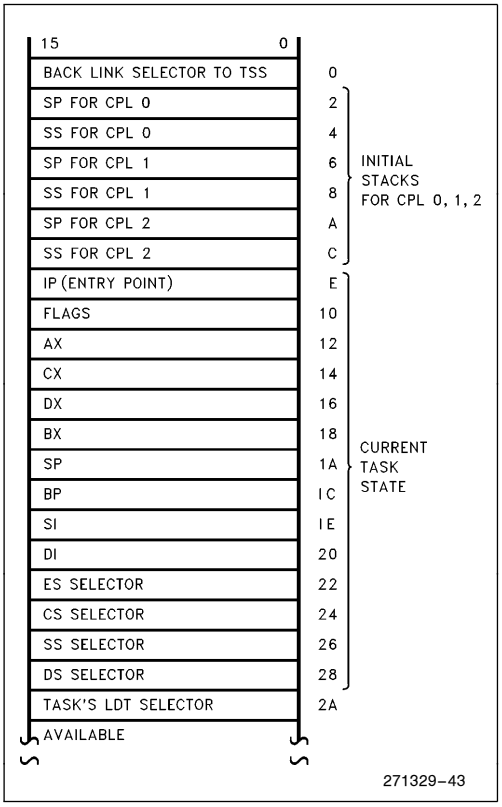


Figure 6-16. 80286 TSS

Each task must have a TSS associated with it. The current TSS is identified by a special register in the Military Intel486 processor called the Task State Segment Register (TR). This register contains a selector referring to the task state segment descriptor that defines the current TSS. A hidden base and limit register associated with TR are loaded whenever TR is loaded with a new selector. Returning from a task is accomplished by the IRET instruction. When IRET is executed, control is returned to the task which was interrupted. The current executing task's state is saved in the TSS and the old task state is restored from its TSS.

Several bits in the flag register and machine status word (CR0) give information about the state of a task which are useful to the operating system. The Nested Task (NT) (bit 14 in EFLAGS) controls the function of the IRET instruction. If NT = 0, the IRET instruction performs the regular return; when NT = 1, IRET performs a task switch operation back to the previous task. The NT bit is set or reset in the following fashion:

When a CALL or INT instruction initiates a task switch, the new TSS will be marked busy and the back link field of the new TSS set to the old TSS selector. The NT bit of the new task is set by CALL or INT initiated task switches. An interrupt that does not cause a task switch will clear NT. (The NT bit will be restored after execution of the interrupt handler) NT may also be set or cleared by POPF or IRET instructions.

The Military Intel486 processor task state segment is marked busy by changing the descriptor type field from TYPE 9H to TYPE BH. An 80286 TSS is marked busy by changing the descriptor type field from TYPE 1 to TYPE 3. Use of a selector that references a busy task state segment causes an exception 13.

The Virtual Mode (VM) bit 17 is used to indicate if a task, is a virtual 8086 task. If VM = 1, then the tasks will use the Real Mode addressing mechanism. The virtual 8086 environment is only entered and exited via a task switch. (See section 6.5, "Virtual 8086 Environment.")

The **T** bit in the Military Intel486 processor TSS indicates that the processor should generate a debug exception when switching to a task. If T = 1, upon entry to a new task, a debug exception 1 will be generated.

6.3.6.1 Floating Point Task Switching

The FPU's state is not automatically saved when a task switch occurs, because the incoming task may not use the FPU. The Task Switched (TS) Bit (bit 3 in the CR0) helps deal with the FPU's state in a multitasking environment. Whenever the Intel OverDrive processors switch tasks, they set the TS bit. The Intel OverDrive processors detect the first use of a processor extension instruction after a task switch and causes the processor extension not available exception 7. The exception handler for exception 7 may then decide whether to save the state of the FPU. A processor extension not present exception (7) will occur when attempting to execute a Floating Point or WAIT instruction if the Task Switched and Monitor coprocessor extension bits are both set (i.e., TS = 1 and MP = 1).

6.3.7 INITIALIZATION AND TRANSITION TO PROTECTED MODE

Because the Military Intel486 processor begins executing in Real Mode immediately after RESET it is necessary to initialize the system tables and registers with the appropriate values.

The GDT and IDT registers must refer to a valid GDT and IDT. The IDT should be at least 256-bytes long, and GDT must contain descriptors for the initial code, and data segments. Figure 6-17 shows the tables and Figure 6-18 the descriptors needed for a simple Protected Mode Military Intel486 processor system. It has a single code and single data/stack segment each four-Gbytes long and a single privilege level PL = 0.

The actual method of enabling Protected Mode is to load CR0 with the PE bit set, via the MOV CR0, R/M instruction. This puts the Military Intel486 processor in Protected Mode.

After enabling Protected Mode, the next instruction should execute an intersegment JMP to load the CS register and flush the instruction decode queue. The final step is to load all of the data segment registers with the initial selector values.

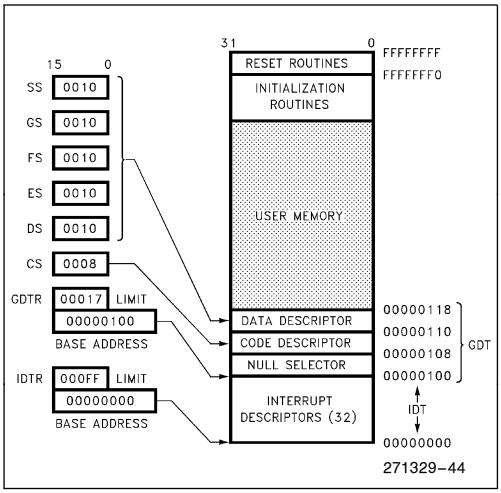


Figure 6-17. Simple Protected System

An alternate approach to entering Protected Mode which is especially appropriate for multitasking operating systems, is to use the built in task-switch to load all of the registers. In this case the GDT would contain two TSS descriptors in addition to the code and data descriptors needed for the first task. The first JMP instruction in Protected Mode would jump to the TSS causing a task switch and loading all of the registers with the values stored in the TSS. Because a task switch saves the state of the current task in a task state segment, the Task State Segment Register should be initialized to point to a valid TSS descriptor.

6.4 Paging

6.4.1 PAGING CONCEPTS

Paging is another type of memory management useful for virtual memory multitasking operating systems. Unlike segmentation which modularizes programs and data into variable length segments, paging divides programs into multiple uniform size pages. Pages bear no direct relation to the logical structure of a program. While segment selectors can be considered the logical ''name'' of a program module or data structure, a page most likely corresponds to only a portion of a module or data structure.

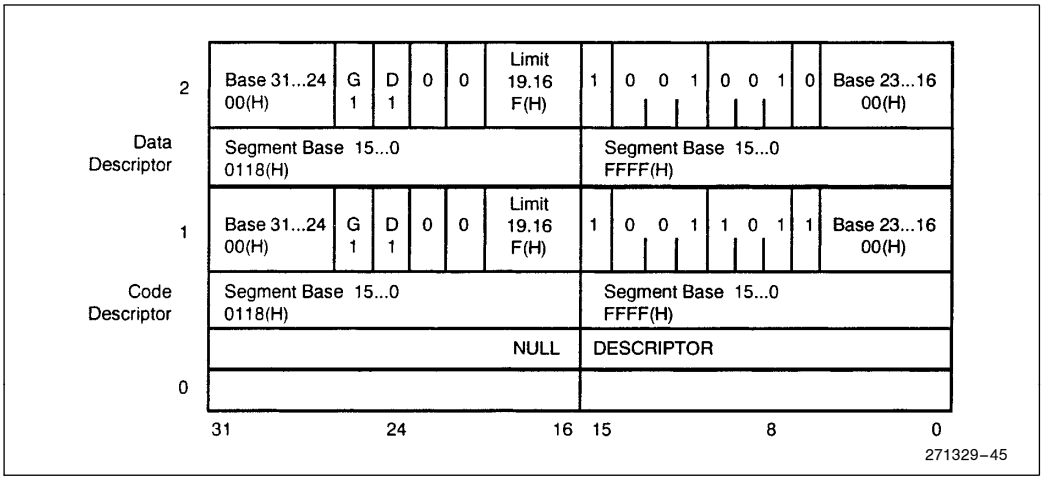


Figure 6-18. GDT Descriptors for Simple System

By taking advantage of the locality of reference displayed by most programs, only a small number of pages from each active task need be in memory at any one moment.

6.4.2 PAGING ORGANIZATION

6.4.2.1 Page Mechanism

The Military Intel486 processor uses two levels of tables to translate the linear address (from the segmentation unit) into a physical address. There are three components to the paging mechanism of the Military Intel486 processor: the page directory, the page tables, and the page itself (page frame). All memory-resident elements of the Military Intel486 processor paging mechanism are the same size, namely, 4 Kbytes. A uniform size for all of the elements simplifies memory allocation and reallocation schemes, because there is no problem with memory fragmentation. Figure 6-19 shows how the paging mechanism works.

6.4.2.2 Page Descriptor Base Register

CR2 is the Page Fault Linear Address register. It holds the 32-bit linear address which caused the last page fault detected.

CR3 is the Page Directory Physical Base Address Register. It contains the physical starting address of the Page Directory. The lower 12 bits of CR3 are always zero to ensure that the Page Directory is always page aligned. Loading it via a MOV CR3 reg instruction causes the Page Table Entry cache to be flushed, as will a task switch through a TSS that **changes** the value of CR0. (See section 6.4.5, "Translation Lookaside Buffer.")

6.4.2.3 Page Directory

The Page Directory is 4-Kbytes long and allows up to 1024 Page Directory Entries. Each Page Directory Entry contains the address of the next level of tables, the Page Tables and information about the page table. The contents of a Page Directory Entry are shown in Figure 6-20. The upper 10 bits of the linear address (A22–A31) are used as an index to select the correct Page Directory Entry.

6.4.2.4 Page Tables

Each Page Table is 4 Kbytes and holds up to 1024 Page Table Entries. Page Table Entries contain the starting address of the page frame and statistical information about the page. (See Figure 6-21.) Address bits A12–A21 are used as an index to select one of the 1024 Page Table Entries. The 20 upper-bit page frame address is concatenated with the lower 12 bits of the linear address to form the physical address. Page tables can be shared between tasks and swapped to disks.

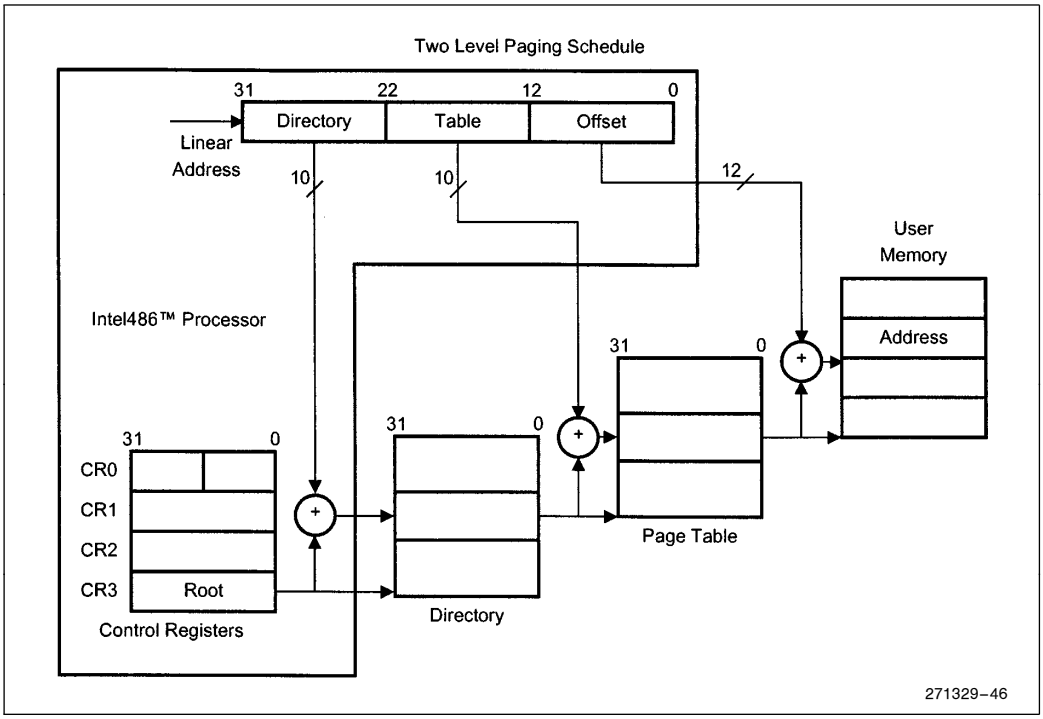


Figure 6-19. Paging Mechanism

31 — 12	11 — 10	9	8	7	6	5	4	3	2	1	0
PAGE TABLE ADDRESS 31 . . . 12	OS RESERVED		0	0	D	A	PCD	PWT	U—S	R—W	P

Figure 6-20. Page Directory Entry (Points to Page Table)

31 — 12	11 — 10	9	8	7	6	5	4	3	2	1	0
PAGE FRAME ADDRESS 31 . . . 12	OS RESERVED		0	0	D	A	PCD	PWT	U—S	R—W	P

Figure 6-21. Page Table Entry (Points to Page)

6.4.2.5 Page Directory/Table Entries

The lower 12 bits of the Page Table Entries and Page Directory Entries contain statistical information about pages and page tables respectively. The **P** (Present) bit 0 indicates if a Page Directory or Page Table entry can be used in address translation. If P = 1 the entry can be used for address translation, if P = 0 the entry cannot be used for translation, and all of the other bits are available for use by the software. For example the remaining 31 bits could be used to indicate where on the disk the page is stored.

The **A** (Accessed) bit 5, is set by the Military Intel486 processor for both types of entries before a read or write access occurs to an address covered by the entry. The **D** (Dirty) bit 6 is set to 1 before a write to an address covered by that page table entry occurs. The D bit is undefined for Page Directory Entries. When the P, A and D bits are updated by the Military Intel486 processor, a Read-Modify-Write cycle is generated which locks the bus and prevents conflicts with other processors or peripherals. Software which modifies these bits should use the LOCK prefix to ensure the integrity of the page tables in multimaster systems.

The 3 bits marked **OS Reserved** in Figure 6-20 and Figure 6-21 (bits 9–11) are software definable. OSs are free to use these bits for whatever purpose they wish. An example use of the **OS Reserved** bits would be to store information about page aging. By keeping track of how long a page has been in memory since being accessed, an operating system can implement a page replacement algorithm such as Least Recently Used.

The (User/Supervisor) U/S bit 2 and the (Read/Write) R/W bit 1 are used to provide protection attributes for individual pages.

6.4.3 PAGE LEVEL PROTECTION (R/W, U/S BITS)

The Military Intel486 processor provides a set of protection attributes for paging systems. The paging mechanism distinguishes between two levels of protection: User which corresponds to level 3 of the segmentation based protection, and supervisor which encompasses all of the other protection levels (0, 1, 2).

The R/W and U/S bits are used in conjunction with the WP bit in the flags register (EFLAGS). The Intel386 processor does not contain the WP bit. The WP bit has been added to the Military Intel486 processor to protect read-only pages from supervisor write accesses. The Intel386 processor allows a read-only page to be written from protection levels 0, 1 or 2. WP = 0 is the Intel386 processor compatible mode. When WP = 0, the supervisor can write to a read-only page as defined by the U/S and R/W bits. When WP = 1, supervisor access to a read-only page (R/W = 0) will cause a page fault (exception 14).

Table 6-4 shows the affect of the WP, U/S and R/W bits on accessing memory. When WP = 0, the supervisor can write to pages regardless of the state of the R/W bit. When WP = 1 and R/W = 0, the supervisor cannot write to a read-only page. A user attempt to access a supervisor only page (U/S = 0) or to write to a read-only page will cause a page fault (exception 14).

Table 6-4. Page Level Protection Attributes

U/S	R/W	WP	User Access	Supervisor Access
0	0	0	None	Read/Write/Execute
0	1	0	None	Read/Write/Execute
1	0	0	Read/Execute	Read/Write/Execute
1	1	0	Read/Write/Execute	Read/Write/Execute
0	0	1	None	Read/Execute
0	1	1	None	Read/Write/Execute
1	0	1	Read/Execute	Read/Execute
1	1	1	Read/Write/Execute	Read/Write/Execute

The R/W and U/S bits provide protection from user access on a page by page basis because the bits are contained in the Page Table Entry and the Page Directory Table. The U/S and R/W bits in the first-level Page Directory Table apply to all entries in the page table pointed to by that directory entry. The U/S and R/W bits in the second-level Page Table Entry apply only to the page described by that entry. The most restrictive of the U/S and R/W bits from the Page Directory Table and the Page Table Entry are used to address a page.

Example: If the U/S and R/W bits for the Page Directory entry were 10 (user read/execute) and the U/S and R/W bits for the Page Table Entry were 01 (no user access at all), the access rights for the page would be 01, the numerically smaller of the two.

Note that a given segment can be easily made read-only for level 0, 1 or 2 via use of segmented protection mechanisms. (Section 6.3, ‘‘Protection’’.)

6.4.4 PAGE CACHEABILITY (PWT AND PCD BITS)

See section 7.6, ‘‘Page Cacheability,’’ for a detailed description of page cacheability and the PWT and PCD bits.

6.4.5 TRANSLATION LOOKASIDE BUFFER

The Military Intel486 processor paging hardware is designed to support demand paged virtual memory systems. However, performance would degrade substantially if the Military Intel486 processor was required to access two levels of tables for every memory reference. To solve this problem, the Military Intel486 processor keeps a cache of the most recently accessed pages. This cache is called the Translation Lookaside Buffer (TLB). The TLB is a four-way set associative 32-entry page table cache. It automatically keeps the most commonly used Page Table Entries in the Military Intel486 processor. The 32-entry TLB coupled with a 4K page size, results in coverage of 128 Kbytes of memory addresses. For many common multitasking systems, the TLB will have a hit rate of about 98%. This means that the Military Intel486 processor will only have to access the two-level page structure on 2% of all memory references. Figure 6-22 illustrates how the TLB complements the Military Intel486 processor’s paging mechanism.

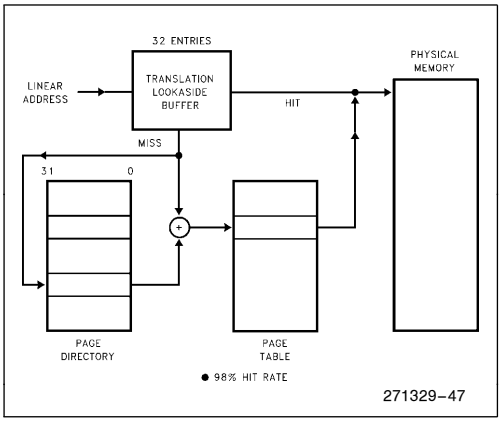


Figure 6-22. Translation Lookaside Buffer

Reading a new entry into the TLB (TLB refresh) is a two step process handled by the Military Intel486 processor hardware. The sequence of data cycles to perform a TLB refresh are the following:

1. Read the correct Page Directory Entry, as pointed to by the page base register and the upper 10 bits of the linear address. The page base register is in control register 3.
   a. Optionally perform a locked read/write to set the accessed bit in the directory entry. The directory entry will actually get read twice if the Military Intel486 processor needs to set any of the bits in the entry. If the page directory entry changes between the first and second reads, the data returned for the second read will be used.
2. Read the correct entry in the Page Table and place the entry in the TLB.
   a. Optionally perform a locked read/write to set the accessed and/or dirty bit in the page table entry. Again, note that the page table entry will actually get read twice if the Military Intel486 processor needs to set any of the bits in the entry. Like the directory entry, if the data changes between the first and second read the data returned for the second read will be used.

Note that the directory entry must always be read into the Military Intel486 processor, because directory entries are never placed in the paging TLB. Page faults can be signaled from either the page directory read or the page table read. Page directory and page table entries may be placed in the Military Intel486 processor on-chip cache just like normal data.

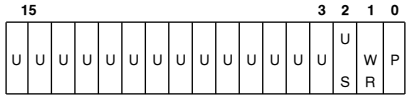
6.4.6 PAGING OPERATION

The paging hardware operates in the following fashion. The paging unit hardware receives a 32-bit linear address from the segmentation unit. The upper 20 linear address bits are compared with all 32 entries in the TLB to determine if there is a match. If there is a match (i.e., a TLB hit), then the 32-bit physical address is calculated and will be placed on the address bus.

However, if the page table entry is not in the TLB, the Military Intel486 processor will read the appropriate Page Directory Entry. If P = 1 on the Page Directory Entry indicating that the page table is in memory, then the Military Intel486 processor will read the appropriate Page Table Entry and set the Access bit. If P = 1 on the Page Table Entry indicating that the page is in memory, the Military Intel486 processor will update the Access and Dirty bits as needed and fetch the operand. The upper 20 bits of the linear address, read from the page table, will be stored in the TLB for future accesses. However, if P = 0 for either the Page Directory Entry or the Page Table Entry, then the Military Intel486 processor will generate a page fault, an Exception 14.

The Military Intel486 processor will also generate an exception 14 page fault if the memory reference violated the page protection attributes (i.e., U/S or R/W) (e.g., trying to write to a read-only page). CR2 will hold the linear address which caused the page fault. If a second page fault occurs, while the Military Intel486 processor is attempting to enter the service routine for the first, then the Military Intel486 processor will invoke the page fault (exception 14) handler a second time, rather than the double fault (exception 8) handler. Because Exception 14 is classified as a fault, CS: EIP will point to the instruction causing the page fault. The 16-bit error code pushed as part of the page fault handler will contain status bits which indicate the cause of the page fault.

The 16-bit error code is used by the operating system to determine how to handle the page fault. The upper portion of Figure 6-23 shows the format of the page-fault error code and the interpretation of the bits.



U/S	W/R	Access Type
0	0	Supervisor* Read
0	1	Supervisor Write
1	0	User Read
1	1	User Write

NOTES:
*Descriptor table access will fault with U/S = 0, even if the program is executing at level 3.

U: UNDEFINED

U/S: The U/S bit indicates whether the access causing the fault occurred when the Military Intel486 processor was executing in User Mode (U/S = 1) or in Supervisor mode (U/S = 0).

W/R: The W/R bit indicates whether the access causing the fault was a Read (W/R = 0) or a Write (W/R = 1).

P: The P bit indicates whether a page fault was caused by a not-present page (P = 0), or by a page level protection violation (P = 1).

Figure 6-23. Page Fault System Information

NOTE:
Even though the bits in the error code (U/S, W/R, and P) have similar names as the bits in the Page Directory/Table Entries, the interpretation of the error code bits is different. Figure 6-23 indicates what type of access caused the page fault.

6.4.7 OPERATING SYSTEM RESPONSIBILITIES

The Military Intel486 processor takes care of the page address translation process, relieving the burden from an operating system in a demand-paged system. The operating system is responsible for

setting up the initial page tables, and handling any page faults. The operating system also is required to invalidate (i.e., flush) the TLB when any changes are made to any of the page table entries. The operating system must reload CR3 to cause the TLB to be flushed.

Setting up the tables is simply a matter of loading CR3 with the address of the Page Directory, and allocating space for the Page Directory and the Page Tables. The primary responsibility of the operating system is to implement a swapping policy and handle all of the page faults.

A final concern of the operating system is to ensure that the TLB cache matches the information in the paging tables. In particular, any time the operating system sets the P present bit of page table entry to zero, the TLB must be flushed. Operating systems may want to take advantage of the fact that CR3 is stored as part of a TSS, to give every task or group of tasks its own set of page tables.

6.5 Virtual 8086 Environment

6.5.1 EXECUTING 8086 PROGRAMS

The Military Intel486 processor allows the execution of 8086 application programs in both Real Mode and in the Virtual 8086 Mode (Virtual Mode). Of the two methods, Virtual 8086 Mode offers the system designer the most flexibility. The Virtual 8086 Mode allows the execution of 8086 applications, while still allowing the system designer to take full advantage of the Military Intel486 processor protection mechanism. In particular, the Military Intel486 processor allows the simultaneous execution of 8086 operating systems and its applications, and a Military Intel486 processor operating system and both 80286 and Military Intel486 processor applications. Thus, in a multi-user Military Intel486 processor computer, one person could be running an MS-DOS* spreadsheet, another person using MS-DOS*, and a third person could be running multiple UNIX utilities and applications. Each person in this scenario would believe that he had the computer completely to himself. Figure 6-24 illustrates this concept.

6.5.2 VIRTUAL 8086 MODE ADDRESSING MECHANISM

One of the major differences between Military Intel486 processor Real and Protected modes is how the segment selectors are interpreted. When the Military Intel486 processor is executing in Virtual 8086 Mode the segment registers are used in an identical fashion to Real Mode. The contents of the segment register is shifted left 4 bits and added to the offset to form the segment base linear address.

The Military Intel486 processor allows the operating system to specify which programs use the 8086 style address mechanism, and which programs use Protected Mode addressing, on a per task basis. Through the use of paging, the one megabyte address space of the Virtual Mode task can be mapped to anywhere in the 4-Gbyte linear address space of the Military Intel486 processor. Like Real Mode, Virtual Mode effective addresses (i.e., segment offsets) that exceed 64 Kbyte will cause an exception 13. However, these restrictions should not prove to be important, because most tasks running in Virtual 8086 Mode will simply be existing 8086 application programs.

6.5.3 PAGING IN VIRTUAL MODE

The paging hardware allows the concurrent running of multiple Virtual Mode tasks, and provides protection and operating system isolation. Although it is not strictly necessary to have the paging hardware enabled to run Virtual Mode tasks, it is needed in order to run multiple Virtual Mode tasks or to relocate the address space of a Virtual Mode task to physical address space greater than one Mbyte.

The paging hardware allows the 20-bit linear address produced by a Virtual Mode program to be divided into up to 256 pages. Each one of the pages can be located anywhere within the maximum 4-Gbyte physical address space of the Military Intel486 processor. In addition, because CR3 (the Page Directory Base Register) is loaded by a task switch, each Virtual Mode task can use a different mapping scheme to map pages to different physical locations. Finally, the paging hardware allows the sharing of the 8086 operating system code between multiple 8086 applications. Figure 6-24 shows how the Military Intel486 processor paging hardware enables multiple 8086 programs to run under a virtual memory demand paged system.

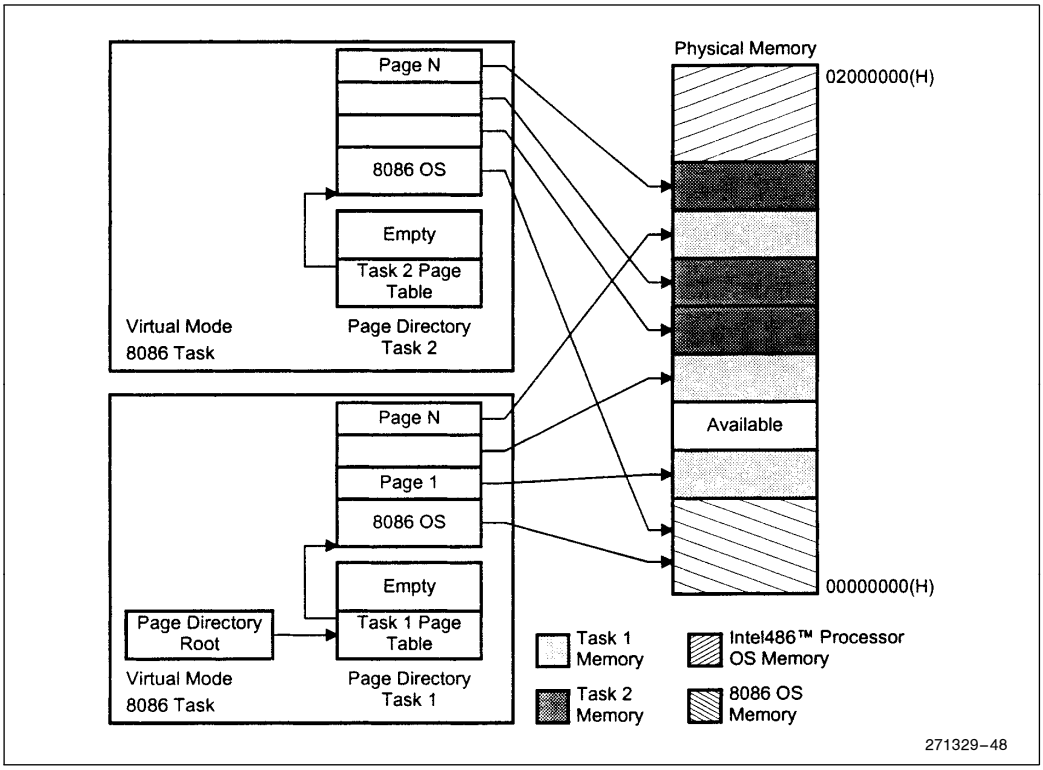


Figure 6-24. Virtual 8086 Environment Memory Management

6.5.4 PROTECTION AND I/O PERMISSION BITMAP

All Virtual 8086 Mode programs execute at privilege level 3, the level of least privilege. As such, Virtual 8086 Mode programs are subject to all of the protection checks defined in Protected Mode. (This is different from Real Mode which implicitly is executing at privilege level 0, the level of greatest privilege.) Thus, an attempt to execute a privileged instruction when in Virtual 8086 Mode will cause an exception 13 fault.

The following are privileged instructions, which may be executed only at Privilege Level 0. Therefore, attempting to execute these instructions in Virtual 8086 Mode (or anytime CPL $>$ 0) causes an exception 13 fault:

```
LIDT; MOV DRn,reg; MOV reg,DRn;
LGDT; MOV TRn,reg; MOV reg,TRn;
LMSW; MOV CRn,reg; MOV reg,CRn.
CLTS;
HLT;
```

Several instructions, particularly those applying to the multitasking model and protection model, are available only in Protected Mode. Therefore, attempting to execute the following instructions in Real Mode or in Virtual 8086 Mode generates an exception 6 fault:

```
LTR;      STR;
LLDT;     SLDT;
LAR;      VERR;
LSL;      VERW;
ARPL.
```

The instructions that are IOPL-sensitive in Protected Mode are:

```
IN;       STI;
OUT;      CLI
INS;
OUTS;
REP INS;
REP OUTS;
```

In Virtual 8086 Mode, a slightly different set of instructions are made IOPL-sensitive. The following instructions are IOPL-sensitive in Virtual 8086 Mode:

```
INT n;    STI;
PUSHF;    CLI;
POPF;     IRET
```

The PUSHF, POPF, and IRET instructions are IOPL-sensitive in Virtual 8086 Mode only. This provision allows the IF flag (interrupt enable flag) to be virtualized to the Virtual 8086 Mode program. The INT n software interrupt instruction is also IOPL-sensitive in Virtual 8086 Mode. Note, however, that the INT 3 (opcode 0CCH), INTO, and BOUND instructions are not IOPL-sensitive in Virtual 8086 mode (they aren't IOPL sensitive in Protected Mode either).

Note that the I/O instructions (IN, OUT, INS, OUTS, REP INS, and REP OUTS) are **not** IOPL-sensitive in Virtual 8086 mode. Rather, the I/O instructions become automatically sensitive to the **I/O Permission Bitmap** contained in the **Military Intel486 processor Task State Segment**. The I/O Permission Bitmap, automatically used by the Military Intel486 processor in Virtual 8086 Mode, is illustrated by Figure 6-14 and Figure 6-15.

The I/O Permission Bitmap can be viewed as a 0–64 Kbit string, which begins in memory at offset Bit__Map__Offset in the current TSS. Bit__Map__Offset must be ≤ DFFFH so the entire bit map and the byte FFH which follows the bit map are all at offsets ≤ FFFFH from the TSS base. The 16-bit pointer Bit__Map__Offset (15:0) is found in the word beginning at offset 66H (102 decimal) from the TSS base, as shown in Figure 6-14.

Each bit in the I/O Permission Bitmap corresponds to a single byte-wide I/O port, as illustrated in Figure 6-14. If a bit is 0, I/O to the corresponding byte-wide port can occur without generating an exception. Otherwise the I/O instruction causes an exception 13 fault. Because every byte-wide I/O port must be protectable, all bits corresponding to a word-wide or dword-wide port must be 0 for the word-wide or dword-wide I/O to be permitted. If all the referenced bits are 0, the I/O will be allowed. If any referenced bits are 1, the attempted I/O will cause an exception 13 fault.

Due to the use of a pointer to the base of the I/O Permission Bitmap, the bitmap may be located anywhere within the TSS, or may be ignored completely by pointing the Bit__Map__Offset (15:0) beyond the limit of the TSS segment. In the same manner, only a small portion of the 64K I/O space need have an associated map bit, by adjusting the TSS limit to truncate the bitmap. This eliminates the commitment of 8K of memory when a complete bitmap is not required, while allowing the fully general case if desired.

Example of Bitmap for I/O Ports 0–255: Setting the TSS limit to {bit__Map__Offset + 31 + 1**} [** see note below] will allow a 32-byte bitmap for the I/O ports #0–255, plus a terminator byte of all 1's [** see note below]. This allows the I/O bitmap to control I/O Permission to I/O port 0–255 while causing an exception 13 fault on attempted I/O to any I/O port 80256 through 65,565.

> ****IMPORTANT IMPLEMENTATION NOTE:** Beyond the last byte of I/O mapping information in the I/O Permission Bitmap **must** be a byte containing all 1's. The byte of all 1's must be within the limit of the Military Intel486 processor TSS segment (see Figure 6-14).

6.5.5 INTERRUPT HANDLING

In order to fully support the emulation of an 8086 machine, interrupts in Virtual 8086 Mode are handled in a unique fashion. When running in Virtual Mode all interrupts and exceptions involve a privilege change back to the host Military Intel486 processor operating system. The Military Intel486 processor operating system determines if the interrupt

comes from a Protected Mode application or from a Virtual Mode program by examining the VM bit in the EFLAGS image stored on the stack.

When a Virtual Mode program is interrupted and execution passes to the interrupt routine at level 0, the VM bit is cleared. However, the VM bit is still set in the EFLAG image on the stack.

The Military Intel486 processor operating system in turn handles the exception or interrupt and then returns control to the 8086 program. The Military Intel486 processor operating system may choose to let the 8086 operating system handle the interrupt or it may emulate the function of the interrupt handler. For example, many 8086 operating system calls are accessed by PUSHing parameters on the stack, and then executing an INT n instruction. If the IOPL is set to 0 then all INT n instructions will be intercepted by the Military Intel486 processor operating system. The Military Intel486 processor operating system could emulate the 8086 operating system's call. Figure 6-25 shows how the Military Intel486 processor operating system could intercept an 8086 operating system's call to ''Open a File.''

A Military Intel486 processor operating system can provide a Virtual 8086 Environment which is totally transparent to the application software via intercepting and then emulating 8086 operating system's calls, and intercepting IN and OUT instructions.

6.5.6 ENTERING AND LEAVING VIRTUAL 8086 MODE

Virtual 8086 mode is entered by executing an IRET instruction (at CPL = 0), or Task Switch (at any CPL) to a Military Intel486 processor task whose Military Intel486 processor TSS has a FLAGS image containing a 1 in the VM bit position while the Military Intel486 processor is executing in Protected Mode. That is, one way to enter Virtual 8086 mode is to switch to a task with a Military Intel486 processor TSS that has a 1 in the VM bit in the EFLAGS image. The other way is to execute a 32-bit IRET instruction at privilege level 0, where the stack has a 1 in the VM bit in the EFLAGS image. POPF does not affect the VM bit, even if the Military Intel486 processor is in Protected Mode or level 0, and so cannot be used to enter Virtual 8086 Mode. PUSHF always pushes a 0 in the VM bit, even if the Military Intel486 processor is in Virtual 8086 Mode, so that a program cannot tell if it is executing in REAL mode, or in Virtual 8086 mode.

The VM bit can be set by executing an IRET instruction only at privilege level 0, or by any instruction or Interrupt which causes a task switch in Protected Mode (with VM = 1 in the new FLAGS image), and can be cleared only by an interrupt or exception in Virtual 8086 Mode. IRET and POPF instructions executed in REAL mode or Virtual 8086 mode will not change the value in the VM bit.

The transition out of virtual 8086 mode to Military Intel486 processor protected mode occurs only on receipt of an interrupt or exception (such as due to a sensitive instruction). In Virtual 8086 mode, all interrupts and exceptions vector through the protected mode IDT, and enter an interrupt handler in protected Military Intel486 processor mode. That is, as part of interrupt processing, the VM bit is cleared.

Because the matching IRET must occur from level 0, if an Interrupt or Trap Gate is used to field an interrupt or exception out of Virtual 8086 mode, the Gate must perform an inter-level interrupt only to level 0. Interrupt or Trap Gates through conforming segments, or through segments with DPL > 0, will raise a GP fault with the CS selector as the error code.

6.5.6.1 Task Switches To and From Virtual 8086 Mode

Tasks which can execute in virtual 8086 mode must be described by a TSS with the new Military Intel486 processor format (TYPE 9 or 11 descriptor).

A task switch out of virtual 8086 mode will operate exactly the same as any other task switch out of a task with a Military Intel486 processor TSS. All of the programmer visible state, including the FLAGS register with the VM bit set to 1, is stored in the TSS.

The segment registers in the TSS will contain 8086 segment base values rather than selectors.

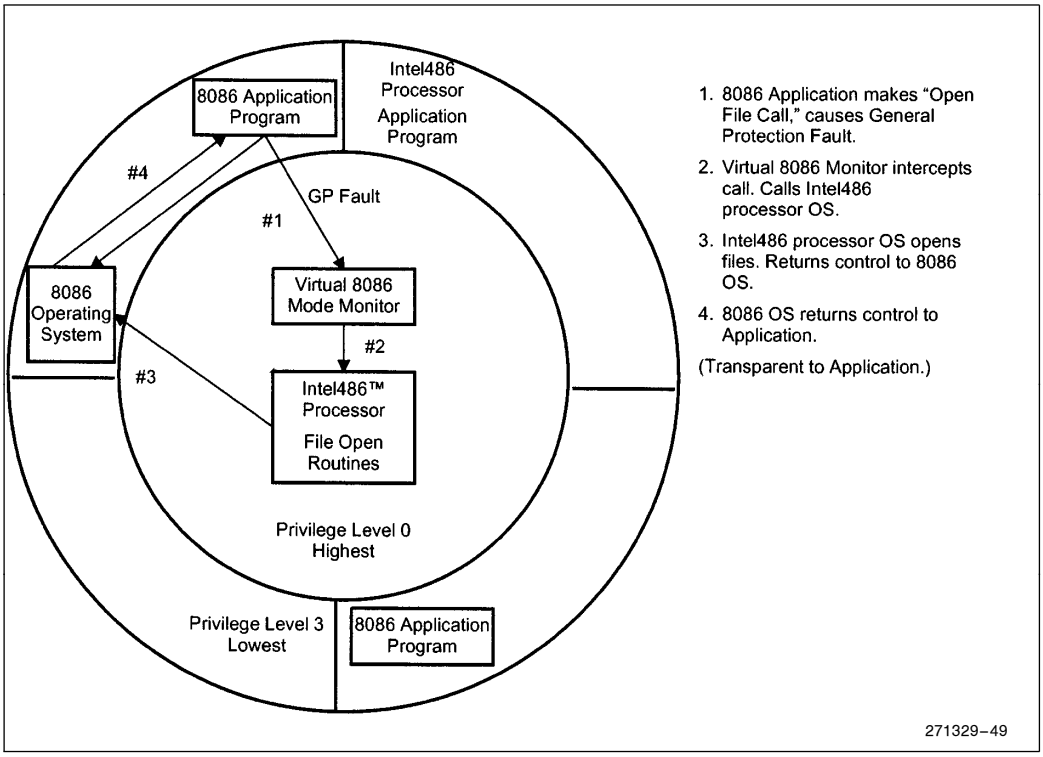


Figure 6-25. Virtual 8086 Environment Interrupt and Call Handling

A task switch into a task described by a Military Intel486 processor TSS will have an additional check to determine if the incoming task should be resumed in virtual 8086 mode. Tasks described by 80286 format TSSs cannot be resumed in virtual 8086 mode, so no check is required there (the FLAGS image in 80286 format TSS has only the low order 16 FLAGS bits). Before loading the segment register images from a Military Intel486 processor TSS, the FLAGS image is loaded, so that the segment registers are loaded from the TSS image as 8086 segment base values. The task is now ready to resume in virtual 8086 execution mode.

6.5.6.2 Transitions Through Trap and Interrupt Gates, and IRET

A task switch is one way to enter or exit virtual 8086 mode. The other method is to exit through a Trap or Interrupt gate, as part of handling an interrupt, and to enter as part of executing an IRET instruction. The transition out must use a Military Intel486 processor Trap Gate (Type 14), or Military Intel486 processor Interrupt Gate (Type 15), which must point to a non-conforming level 0 segment (DPL = 0) in order to permit the trap handler to IRET back to the Virtual 8086 program. The Gate must point to a non-conforming level 0 segment to perform a level switch to level 0 so that the matching IRET can change the VM bit. Military Intel486 processor gates must be used, because 80286 gates save only the low 16 bits of the FLAGS register, so that the VM bit will not be saved on transitions through the 80286 gates. Also, the 16-bit IRET (presumably) used to terminate the 80286 interrupt handler will pop only the lower 16 bits from FLAGS, and will not affect the VM bit. The action taken for a Military Intel486 processor Trap or Interrupt gate if an interrupt occurs while the task is executing in virtual 8086 mode is given by the following sequence.

1. Save the FLAGS register in a temp to push later. Turn off the VM and TF bits, and if the interrupt is serviced by an Interrupt Gate, turn off IF also.
2. Interrupt and Trap gates must perform a level switch from 3 (where the VM86 program executes) to level 0 (so IRET can return). This process involves a stack switch to the stack given in the TSS for privilege level 0. Save the Virtual 8086 Mode SS and ESP registers to push in a later step. The segment register load of SS will be done as a Protected Mode segment load, because the VM bit was turned off above.
3. Push the 8086 segment register values onto the new stack, in the order: GS, FS, DS, ES. These are pushed as 32-bit quantities, with undefined values in the upper 16 bits. Then load these 4 registers with null selectors (0).
4. Push the old 8086 stack pointer onto the new stack by pushing the SS register (as 32-bits, high bits undefined), then pushing the 32-bit ESP register saved above.
5. Push the 32-bit FLAGS register saved in step 1.
6. Push the old 8086 instruction pointer onto the new stack by pushing the CS register (as 32-bits, high bits undefined), then pushing the 32-bit EIP register.
7. Load up the new CS:EIP value from the interrupt gate, and begin execution of the interrupt routine in protected Military Intel486 processor mode.

The transition out of virtual 8086 mode performs a level change and stack switch, in addition to changing back to protected mode. In addition, all of the 8086 segment register images are stored on the stack (behind the SS:ESP image), and then loaded with null (0) selectors before entering the interrupt handler. This will permit the handler to safely save and restore the DS, ES, FS, and GS registers as 80286 selectors. This is needed so that interrupt handlers which don't care about the mode of the interrupted program can use the same prolog and epilog code for state saving (i.e., push all registers in prolog, pop all in epilog) regardless of whether or not a 'native' mode or Virtual 8086 mode program was interrupted. Restoring null selectors to these registers before executing the IRET will not cause a trap in the interrupt handler. Interrupt routines which expect values in the segment registers, or return values in segment registers will have to obtain/return values from the 8086 register images pushed onto the new stack. They will need to know the mode of the interrupted program in order to know where to find/return segment registers, and also to know how to interpret segment register values.

The IRET instruction will perform the inverse of the above sequence. Only the extended Military Intel486 processor IRET instruction (operand size = 32) can be used, and must be executed at level 0 to change the VM bit to 1.

1. If the NT bit in the FLAGs register is on, an intertask return is performed. The current state is stored in the current TSS, and the link field in the current TSS is used to locate the TSS for the interrupted task which is to be resumed. Otherwise, continue with the following sequence.
2. Read the FLAGS image from SS:8[ESP] into the FLAGS register. This will set VM to the value active in the interrupted routine.
3. Pop off the instruction pointer CS:EIP. EIP is popped first, then a 32-bit word is popped which contains the CS value in the lower 16 bits. If VM = 0, this CS load is done as a protected mode segment load. If VM = 1, this will be done as an 8086 segment load.
4. ESP register by 4 to bypass the FLAGS image which was ''popped'' in step 1.
5. If VM = 1, load segment registers ES, DS, FS, and GS from memory locations SS:[ESP + 8], SS:[ESP + 12], SS:[ESP + 16], and SS:[ESP + 20], respectively, where the new value of ESP stored in step 4 is used. Because VM = 1, these are done as 8086 segment register loads. Else if VM = 0, check that the selectors in ES, DS, FS, and GS are valid in the interrupted routine. Null out invalid selectors to trap if an attempt is made to access through them.
6. If (RPL(CS) > CPL), pop the stack pointer SS:ESP from the stack. The ESP register is popped first, followed by 32-bits containing SS in the lower 16 bits. If VM = 0, SS is loaded as a protected mode segment register load. If VM = 1, an 8086 segment register load is used.
7. Resume execution of the interrupted routine. The VM bit in the FLAGS register (restored from the interrupt routine's stack image in step 1) determines whether the Military Intel486 processor resumes the interrupted routine in Protected mode of Virtual 8086 mode.

7.0 ON-CHIP CACHE

All members of the Military Intel486 processor family, except the IntelDX4 processor, contain an on-chip 8-Kbyte cache. (See section 7.1.1, ''IntelDX4 Processor Cache,'' for the IntelDX4 processor cache organization.) The cache is software transparent to maintain binary compatibility with previous generations of the Intel Architecture.

The on-chip cache has been designed for maximum flexibility and performance. The cache has several operating modes offering flexibility during program execution and debugging. Memory areas can be defined as non-cacheable by software and external hardware. Protocols for cache line invalidations and replacement are implemented in hardware, easing system design.

7.1 Cache Organization

The on-chip cache is a unified code and data cache. The cache is used for both instruction and data accesses and acts on physical addresses.

The cache organization is 4-way set associative and each line is 16-bytes wide. The eight Kbytes of cache memory are logically organized as 128 sets, each containing four lines.

The cache memory is physically split into four 2-Kbyte blocks, each containing 128 lines. (See Figure 7-1.) There are 128 21-bit tags associated with each 2-Kbyte block. There is a valid bit for each line in the cache. Each line in the cache is either valid or not valid. There are no provisions for partially valid lines.

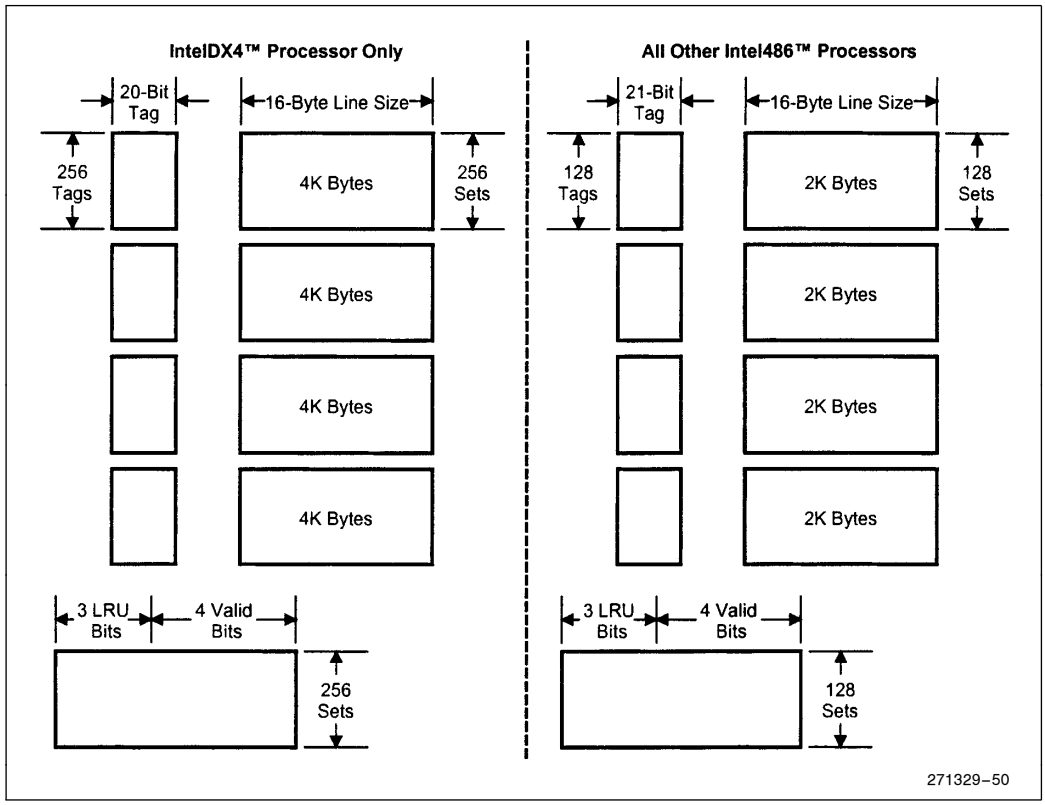


Figure 7-1. On-Chip Cache Physical Organization

For all Military Intel486 processors the on-chip cache is write-through only. All writes will drive an external write bus cycle in addition to writing the information to the internal cache if the write was a cache hit. A write to an address not contained in the internal cache will only be written to external memory. Cache allocations are not made on write misses.

7.1.1 INTELDX4 PROCESSOR CACHE

The IntelDX4 processor contains a 16-Kbyte write-through cache. The 16 Kbytes of cache memory are logically organized as 256 sets, each containing four lines.

The cache memory is physically split into four 4-Kbyte blocks, each containing 256 lines. (See Figure 7-1.) There are 256 20-bit tags associated with each 2-Kbyte block.

All other details listed in section 7.1 for the 8-Kbyte on-chip cache also apply to the IntelDX4 on-chip cache.

7.1.2 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR CACHE

The Write-Back Enhanced IntelDX4 processor implements a unified cache, with a total cache size of 16 Kbytes. The processor's on-chip cache supports a modified MESI (modified/exclusive/shared/invalid) write-back cache consistency protocol.

The Write-Back Enhanced IntelDX4 processor internal cache is configurable as write-back or write-through on a line by line basis, provided the cache is enabled for write-back operation. The cache is enabled for write-back operation by driving the WB/WT# pin to a high state for at least two clocks before and two clocks after the falling edge of the RESET. Cache write-back and invalidations can be initiated by hardware or software. Protocols for cache consistency and line replacement are implemented in hardware to ease system design.

Once the cache configuration is selected, the Write-Back Enhanced IntelDX4 processor will continue to operate in the selected configuration and can only be changed to a different configuration by starting the **RESET** process again. Assertion of **SRESET** will not change the operating mode

Table 7-1. Write-Back Enhanced IntelDX4™ Processor WB/WT# Initialization

State of WB/WT# at Falling Edge of RESET	Effect on Write-Back Enhanced IntelDX4 Processor Operation
WB/WT# = LOW	**Processor is in Standard Bus Mode (Write-Through Cache)** 1. When **FLUSH#** is asserted, the internal cache will be invalidated in one system **CLK**. 2. No Special **FLUSH#** Acknowledge Cycles appear on the bus after the assertion of the **FLUSH#** pin. 3. All write-back specific inputs are ignored (**INV, WB/WT#**) 4. SRESET does not clear the SMBASE register. It behaves much like a RESET (invalidating the on-chip cache and resetting the CR0 register, for example). SRESET is NOT an interrupt.
WB/WT# = HIGH	**Processor is in Enhanced Bus Mode (Write-Back Cache)** 1. Write backs will be performed when a cache flush is requested (via the **FLUSH#** pin or the WBINVD instruction). The system must watch for the **FLUSH#** special cycles to determine the end of the flush. 2. The special **FLUSH#** Acknowledge Cycles will appear on the bus after the assertion of the **FLUSH#** and after all the cache write backs (if any) are completed on the bus. 3. **WB/WT#** is sampled on a line by line basis to determine the state of a line to be allocated in the cache (as a Write Through (S state) or as Write Back (E state)). 4. The **WB/WT#** and **INV** inputs are no longer ignored. **HITM#** and **CACHE#** will be driven during appropriate bus cycles. 5. **PLOCK#** is always driven inactive. 6. **SRESET** is an interrupt. SRESET does not reset the SMBASE register or flush the on-chip cache. The CR0 register gets the same values as after RESET with the exception of the **CD and NW bits.** These two bits retain their previous status. (See section 9.2.18.4, ''Soft Reset (SRESET)'' and Table 3-7 for details on SRESET for write-back enhanced mode.)

of the processor. **WB/WT#** has an internal pull down; If **WB/WT#** is unconnected, the processor will be in Standard Bus Mode, i.e., the on-chip cache is write-through. Table 7-1 lists the two modes of operation and the differences between the two modes.

7.2 Cache Control

Control of the cache is provided by the CD and NW bits in CR0. CD enables and disables the cache. NW controls memory write-through and invalidates.

The CD and NW bits define four operating modes of the on-chip cache as given in Table 7-1. These modes provide flexibility in how the on-chip cache is used.

CD = 1, NW = 1

The cache is completely disabled by setting CD = 1 and NW = 1 and then flushing the cache. This mode may be useful for debugging programs where it is important to see all memory cycles at the pins. Writes that hit in the cache will not appear on the external bus.

It is possible to use the on-chip cache as fast static RAM by ''pre-loading'' certain memory areas into the cache and then setting CD = 1 and NW = 1. Pre-loading can be done by careful choice of memory references with the cache turned on or by use of the testability functions. (See section 11.2, ''On-Chip Cache Testing.'') When the cache is turned off, the memory mapped by the cache is ''frozen'' into the cache because fills and invalidates are disabled.

Table 7-1. Cache Operating Modes

CD	NW	Operating Mode
1	1	Cache fills disabled, write-through and invalidates disabled
1	0	Cache fills disabled, write-through and invalidates enabled
0	1	INVALID. If CR0 is loaded with this configuration of bits, a GP fault with error code of 0 is raised.
0	0	Cache fills enabled, write-through and invalidates enabled

CD = 1, NW = 0

Cache fills are disabled but write-throughs and invalidates are enabled. This mode is the same as if the KEN# pin was strapped HIGH disabling cache fills. Write-throughs and invalidates may still occur to keep the cache valid. This mode is useful if the software must disable the cache for a short period of time, and then re-enable it without flushing the original contents.

CD = 0, NW = 1

Invalid. If CR0 is loaded with this bit configuration, a General Protection fault with error code of 0 will occur.

CD = 0, NW = 0

This is the normal operating mode.

Completely disabling the cache is a two-step process. First, CD and NW must be set to 1, and then the cache must be flushed. If the cache is not flushed, cache hits on reads will still occur and data will be read from the cache.

7.2.1 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR CACHE CONTROL AND OPERATING MODES

The Write-Back Enhanced IntelDX4 processor retains the usage of CR0.CD and CR0.NW, in which the 1,1 state forces a cache-off condition after RESET, and the 0,0 state is the normal run state. Table 7-3 defines these control bits when the cache is enabled for write-back operation. Table 7-3 is also valid when the cache is in write-back mode and some lines are in a write-through state.

CD = 1, NW = 1

The 1,1 state is best used when no lines are allocated, which occurs naturally after RESET (but not SRESET), but must be forced (e.g., by instruction WBINVD) if entered during normal operation. In these cases, the Write-Back Enhanced IntelDX4 processor will operate as if it had no cache at all.

If the 1,1 state is exited, lines that are allocated as write back will be written back upon a snoop hit or replacement cycle. Lines that were allocated as write-through (and later modified while in the 1,1 state) will never appear on the bus.

CD = 1, NW = 0

The only difference from the normal 0,0 ''run'' state is that new line fills (and the line replacements that result from capacity limitations) do not occur. This causes the contents of the cache to be locked in, unless lines are invalidated using snoops.

7.3 Cache Line Fills

Any area of memory can be cached in the Military Intel486 processor. Non-cacheable portions of memory can be defined by the external system or by software. The external system can inform the Military Intel486 processor that a memory address is non-cacheable by returning the KEN# pin inactive during a memory access. (Refer to section 10.2.3, ''Cacheable Cycles.'') Software can prevent certain pages from being cached by setting the PCD bit in the page table entry.

A read request can be generated from program operation or by an instruction pre-fetch. The data will be supplied from the on-chip cache if a cache hit occurs on the read address. If the address is not in the cache, a read request for the data is generated on the external bus.

If the read request is to a cacheable portion of memory, the Military Intel486 processor initiates a cache line fill. During a line fill a 16-byte line is read into the Military Intel486 processor. Cache line fills will only be generated for read misses. Write misses will never cause a line in the internal cache to be allocated. If a cache hit occurs on a write, the line will be updated. Cache line fills can be performed over 8- and 16-bit buses using the dynamic bus sizing feature. Refer to section 10.1.2, ''Dynamic Data Bus Sizing'' for a description of dynamic bus sizing and section 10.2.3, ''Cacheable Cycles'' for further information on cacheable cycles.

7.4 Cache Line Invalidations

The Military Intel486 processor contain both a hardware and software mechanism for invalidating lines in its internal cache. Cache line invalidations are needed to keep the Military Intel486 processor cache contents consistent with external memory.

Refer to section 10.2.8, ''Invalidate Cycles'' for further information on cache line invalidations.

7.4.1 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR SNOOP CYCLES AND WRITE-BACK MODE INVALIDATION

In Enhanced bus mode, the Write-Back Enhanced Intel486 processors perform invalidations differently than other Intel486 processors. Snoop Cycles are initiated by the system to determine if a line is present in the cache, and what the state is. Snoop cycles may further be classified as Inquire cycles or Invalidate cycles. Inquire cycles are driven to the Write-Back Enhanced Intel486 processors when another bus master initiates a memory read cycle, to determine if the processor cache contains the latest data. If the snooped line is in the Write-Back Enhanced Intel486 processors cache and has the most recent information, the processor must schedule a write back of the data. Inquire cycles are driven with INV = ''0''. Invalidate cycles are driven to the Write-Back Enhanced Intel486 processors when the other bus master initiates a memory write cycle to determine if the Write-Back Enhanced Intel486 processors cache contains the snooped line. The Invalidate cycles are driven with INV = ''1'', so that if the snooped line is in the on-chip cache, the line is invalidated. Snoop cycles are described in detail in the ''Bus Functional Description'' section.

The Write-Back Enhanced Intel486 processors have control mechanisms (including snooping) for writing back the modified write-back lines and invalidating the cache. There are special bus cycles associated with write-backs and invalidation. All of the Write-Back Enhanced Intel486 processors special cycles require acknowledgment by RDY# or BRDY#. During the special cycles, the addresses shown in the Table 7-4 are driven onto the address bus and the data bus is left undefined.

Table 7-4. Encoding of the Special Cycles for Write-Back Cache

Cycle Name	M/IO#	D/C#	W/R#	BE3# – BE0#	A4 – A2
Write-Back*	0	0	1	0111	000
First Flush Ack Cycle*	0	0	1	0111	001
Flush*	0	0	1	1101	000
Second Flush Ack Cycle*	0	0	1	1101	001
Shutdown	0	0	1	1110	000
HALT	0	0	1	1011	000
Stop Grant Ack Cycle	0	0	1	1011	100

* For the Write-Back Enhanced Intel486 processors only. FLUSH is present on all Intel486 processors, but differs for Standard Mode. Refer to appropriate sections.

7.5 Cache Replacement

When a line needs to be placed in its internal cache the Military Intel486 processor first checks to see if there is a non-valid line in the set that can be replaced. If all four lines in the set are valid, a pseudo least-recently-used mechanism is used to determine which line should be replaced.

A valid bit is associated with each line in the cache. When a line needs to be placed in a set, the four valid bits are checked to see if there is a non-valid line that can be replaced. If a non-valid line is found, that line is marked for replacement.

The four lines in the set are labeled I0, I1, I2, and I3. The order in which the valid bits are checked during an invalidation is I0, I1, I2 and I3. All valid bits are cleared when the processor is reset or when the cache is flushed.

Replacement in the cache is handled by a pseudo least recently used (LRU) mechanism when all four lines in a set are valid. Three bits, B0, B1 and B2, are defined for each of the 128 sets in the cache. These bits are called the LRU bits. The LRU bits are updated for every hit or replace in the cache.

If the most recent access to the set was to I0 or I1, B0 is set to 1. B0 is set to 0 if the most recent access was to I2 or I3. If the most recent access to I0:I1 was to I0, B1 is set to 1, else B1 is set to 0. If the most recent access to I2:I3 was to I2, B2 is set to 1, else B2 is set to 0.

The pseudo LRU mechanism works in the following manner. When a line must be replaced, the cache will first select which of I0:I1 and I2:I3 was least recently used. Then the cache will determine which of the two lines was least recently used and mark it for replacement. This decision tree is shown in Figure 7-2.

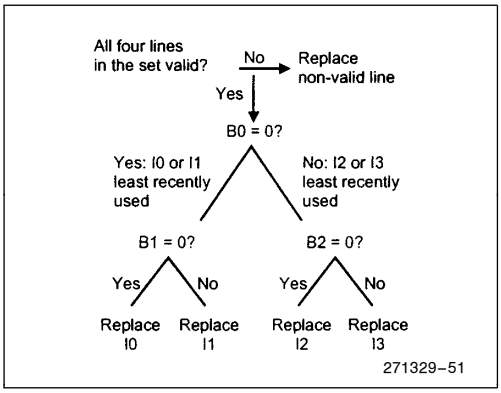


Figure 7-2. On-Chip Cache Replacement Strategy

7.6 Page Cacheability

Two bits for cache control, PWT and PCD, are defined in the page table and page directory entries. The state of these bits are driven out on the PWT and PCD pins during memory access cycles.

The PWT bit controls the write policy for second level caches used with the Military Intel486 processor. Setting PWT = 1 defines a write-through policy for the current page while PWT = 0 defines the possibility of write-back. The state of PWT is ignored internally by the Military Intel486 processor for on-chip cache in write through mode.

The PCD bit controls cacheability on a page by page basis. The PCD bit is internally AND'ed with the KEN# signal to control cacheability on a cycle by cycle basis (see Figure 7-3). PCD = 0 enables caching while PCD = 1 forbids it. Note that cache fills are enabled when PCD = 0 AND KEN# = 0. This logical AND is implemented physically with a NOR gate.

The state of the PCD bit in the page table entry is driven on the PCD pin when a page in external memory is accessed. The state of the PCD pin informs the external system of the cacheability of the requested information. The external system then returns KEN# telling the Military Intel486 processor if the area is cacheable. The Military Intel486 processor initiates a cache line fill if PCD and KEN# indicate that the requested information is cacheable.

The PCD bit is OR'ed with the CD (cache disable) bit in control register 0 to determine the state of the PCD pin. If CD = 1, the Military Intel486 processor forces the PCD pin HIGH. If CD = 0, the PCD pin is driven with the value for the page table entry/directory. (See Figure 7-3.)

The PWT and PCD bits for a bus cycle are obtained from either CR3, the page directory or page table entry. These bits are assumed to be zero during real mode, whenever paging is disabled, or for cycles that bypass paging, (I/O references, interrupt acknowledge and HALT cycles).

When paging is enabled, the bits from the page table entry are cached in the TLB, and are driven any time the page mapped by the TLB entry is referenced. For normal memory cycles, PWT and PCD are taken from the page table entry. During TLB refresh cycles where the page table and directory entries are read, the PWT and PCD bits must be obtained elsewhere. During page table updates the bits are obtained from the page directory. When the page directory is updated the bits are obtained from CR3. PCD and PWT bits are initialized to zero at reset, but can be modified by level 0 software.

7.6.1 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR PAGE CACHEABILITY

In Write-Back Enhanced Intel486 processors-based system, both the processor and the system hardware must determine the cacheability and the configuration (write-back or write-through) on a line by line basis. The system hardware's cacheability is determined by KEN# and the configuration by WB/WT#. The processor's indication of cacheability is determined by PCD and the configuration by PWT. The PWT bit controls the write policy for the second level caches used with the Write-Back Enhanced Intel486 processors. Setting PWT to 1 defines a write-through policy for the current page, while clearing PWT to 0 defines a write-back policy for the current page.

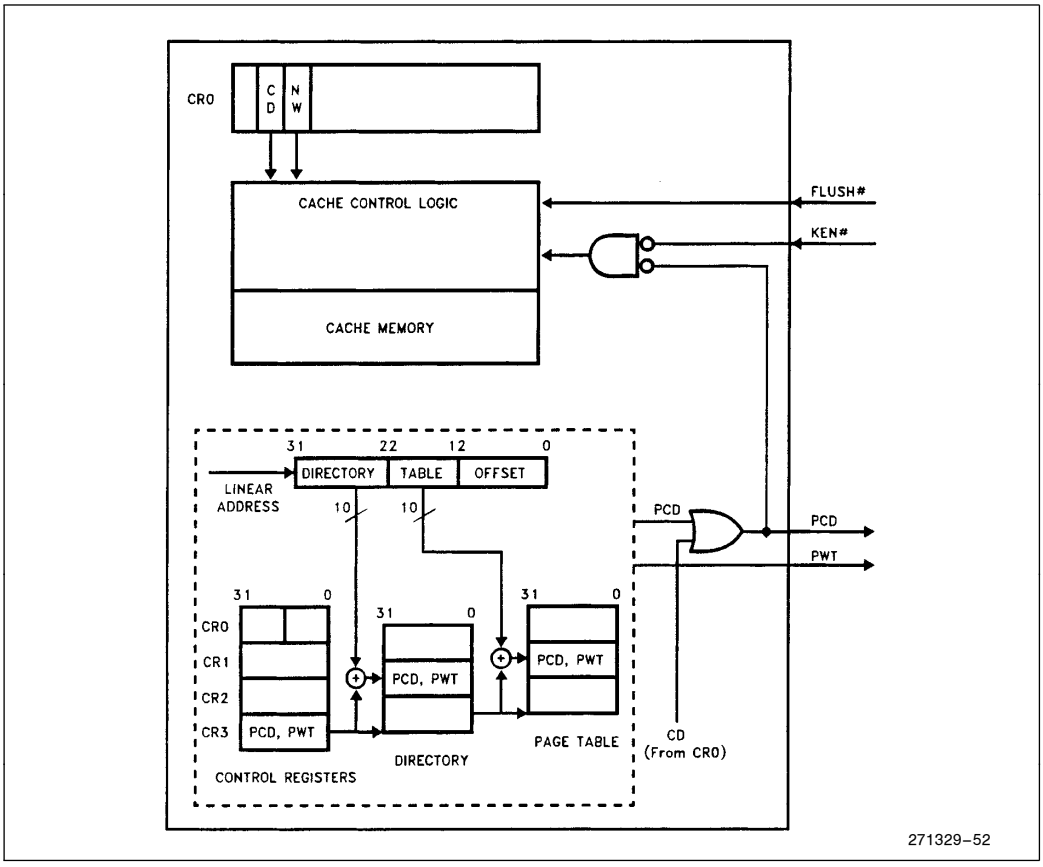


Figure 7-3. Page Cacheability

7.7 Cache Flushing

The on-chip cache can be flushed by external hardware or by software instructions. Flushing the cache clears all valid bits for all lines in the cache. The cache is flushed when external hardware asserts the FLUSH# pin.

The FLUSH# pin needs to be asserted for one clock if driven synchronously or for two clocks if driven asynchronously. FLUSH# is asynchronous, but setup and hold times must be met for recognition in a particular cycle. FLUSH# should be de-asserted before the cache flush is complete. Failure to de-assert the pin will cause execution to stop as the processor will be repeatedly flushing the cache. If external hardware activates flush in response to an I/O write, FLUSH# must be asserted for at least two clocks prior to ready being returned for the I/O write. This ensures that the flush completes before the processor begins execution of the instruction following the OUT instruction.

The instructions INVD and WBINVD cause the on-chip cache to be flushed. External caches connected to the Military Intel486 processor are signaled to flush their contents when these instructions are executed.

WBINVD will also cause an external write-back cache to write back dirty lines before flushing its contents. The external cache is signaled using the bus cycle definition pins and the byte enables (refer to section 9.2.6 ''Bus Cycle Definition'' for the bus cycle definition pins and section 10.2.11 ''Special Bus Cycles'' for special bus cycles). Refer to the *Military Intel486™ Processor Programmers Reference Manual* for detailed instruction definitions.

The results of the INVD and WBINVD instructions are identical for the operation of the non-write-back enhanced Military Intel486 processor on-chip cache because the cache is write-through.

7.7.1 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR CACHE FLUSHING

The on-chip cache can be flushed by external hardware or by software instructions.

Flushing the cache through hardware is accomplished by driving the FLUSH# pin low. This causes the cache to write back all modified lines in the cache and mark the state bits invalid. The First Flush Acknowledge cycle is driven by the Write-Back Enhanced Intel486 processors followed by the Second Flush Acknowledge cycle after all write-backs and invalidations are complete. The two special cycles are issued even if there are no dirty lines to write back.

The INVD and WBINVD instructions cause the on-chip cache to be invalidated. WBINVD causes the modified lines in the internal cache to be written back, and all lines to be marked invalid. After execution of the WBINVD instruction, the Write-back and Flush special cycles are driven to indicate to any external cache that it should write back and invalidate its contents. These two special cycles are issued even if there are no dirty lines to be written back. INVD causes all lines in the cache to be invalidated, so modified lines in the cache are **not** written back. The Flush special cycle is driven after the INVD instruction is executed to indicate to any external cache that it should invalidate its contents. Care should be taken when using the INVD instruction to avoid creating cache consistency problems.

NOTE:
It is recommended to use the WBINVD instruction instead of the INVD instruction if the on-chip cache is configured in the write-back mode.

The assertion of the RESET pin invalidates the entire cache without writing back the modified lines. No special cycles are issued after the invalidation is complete.

Snoop cycles with invalidation (INV = 1) cause the Write-Back Enhanced Intel486 processors to invalidate an individual cache line. If the snooped line is a modified line, then the processor schedules a write-back cycle. Inquire cycles with no-invalidation cause the Write-Back Enhanced Intel486 processors to only write-back the line, if the inquired line is in M-state, and not invalidate the line.

SRESET, STPCLK#, INTR, NMI and SMI# are recognized and latched, but not serviced during the full-cache, modified-line write-backs, caused either by WBINVD instruction or the FLUSH#. However, BOFF#, AHOLD and HOLD are recognized **DURING** the full-cache, modified-line write-backs.

7.8 Write-Back Enhanced IntelDX4™ Processor Write-Back Cache Architecture

This section describes additional features pertaining to the write-back mode of the Write-Back Enhanced Intel486 processors.

7.8.1 WRITE-BACK CACHE COHERENCY PROTOCOL

The Write-Back Enhanced Intel486 processors cache protocol supports a cache line in one of the following four states:

- whether a line is valid and defined as write-back during allocation (E-state),
- if it is valid and defined as write-through during allocation (S-state),
- if it has been modified (M-state),
- if it is invalid (I-state).

These four states are the **M** (Modified line), **E** (write-back line), **S** (write-through line) and the **I** (Invalid line) states and the protocol is referred to as the ''Modified MESI protocol.'' A definition of the states is given below:

M - Modified: An M-state line is modified (different from main memory) and can be accessed (read/written to) without sending a cycle out on the bus.

E - Exclusive: An E-state line is a ''write-back'' line, but the line is not modified (i.e., it is coherent with main memory). An E-state line can be accessed (read/written to) without generating a bus cycle and a write to an E-state line will cause the line to become modified.

S - Shared: An S-state line is a ''write-through'' line, and is coherent with main memory. A read hit to an S-state line will not generate bus activity, but a write hit to an S-state line will generate a write-through cycle on the bus. A write to an S-state line will update the cache and the main memory.

I - Invalid: This state indicates that the line is not in the cache. A read to this line will be a miss and may cause the Write-Back Enhanced Intel486 processors to execute a line fill (fetch the whole line into the cache from main memory). A write to an invalid line will cause the Write-Back Enhanced Intel486 processors to execute a write-through cycle on the bus.

Every line in the Write-Back Enhanced Intel486 processors cache is assigned a state dependent on both Write-Back Enhanced Intel486 processors generated activities and activities generated by the system hardware. As the Write-Back Enhanced Intel486 processors are targeted for uniprocessor systems, a subset of MESI protocol, namely MEI, is used in the Write-Back Enhanced Intel486 processors to maintain cache coherency.

With the modified MESI protocol, it is assumed that in a uniprocessor system lines are defined as write-back or write-through at allocation time. This property associated with a line is never altered. The lines allocated as write-through go to S-state and remain in S-state. A cache line that is allocated as write-back never enters the S-state. The WB/WT# pin is sampled during line allocation and is used strictly to characterize a line as write-back or write-through.

7.8.1.1 State Transition Tables

State transitions are caused by processor-generated transactions (memory reads/writes) and by a set of external input signals and internally-generated variables. The Write-Back Enhanced Intel486 processors also drive certain pins as a consequence of the Cache Consistency Protocol.

Read Cycles

Table 7-5 shows the state transitions for lines in the cache during unlocked read cycles.

Write Cycles

The state transitions of cache lines during Write-Back Enhanced Intel486 processors-generated write cycles are described in Table 7-6.

Table 7-5. Cache State Transitions for Write-Back Enhanced IntelDX4™ Processor Initiated Unlocked Read Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Read hit; data is provided to processor core by cache. No bus cycle is generated.
E	n/a	E	Read hit; data is provided to processor core by cache. No bus cycle is generated.
S	n/a	S	Read hit; Data is provided to the processor by the cache. No bus cycle is generated.
I	CACHE# low AND KEN# low AND WB/WT# high AND PWT low	E	Data item does not exist in cache (MISS). A line fill cycle (read) will be generated by the Write-Back Enhanced IntelDX2™ processor. This state transition will occur if WB/WT# is sampled high with first BRDY#.
I	CACHE# low AND KEN# low AND (WB/WT# low OR PWT high)	S	Same as previous read miss case except that WB/WT# is sampled low with first BRDY# or PWT is high.
I	CACHE# high OR KEN# high	I	KEN# pin inactive; the line is not intended to be cached in the Write-Back Enhanced Intel486 processors.

NOTES:
Locked accesses to the cache will cause the accessed line to transition to the Invalid state.
PCD can also be used by the processor to determine the cacheability, but using the CACHE# pin is recommended. The transition from I to E or S states (based on WB/WT#) occurs only if KEN# is sampled low one clock prior to the first BRDY# and then one clock prior to the last BRDY#, and the cycle is transformed into a line fill cycle. If KEN# is sampled high, the line is not cached and remains in the I state.

Table 7-6. Cache State Transitions for Write-Back Enhanced IntelDX4™ Processor-Initiated Write Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Write hit; update cache. No bus cycle generated to update memory.
E	n/a	M	Write hit; update cache only. No bus cycle generated; line is now modified.
S	n/a	S	Write hit; cache updated with write data item. A write-through cycle is generated on the bus to update memory. Subsequent writes to E-state or M-state lines are held up until this write-through cycle is completed.
I	n/a	I	Write miss; a write-through cycle is generated on the bus to update external memory. No allocation is done. Subsequent writes to the E or M lines are blocked until the write-miss is completed.

Note that even though memory writes are buffered while I/O writes are not, these writes appear at the pins in the same order as they were generated by the processor. Write-Back cycles caused by the replacement of M-state lines are buffered, while Write-Backs due to Snoop hit to M-state lines are not buffered.

Cache Consistency Cycles (Snoop Cycles)

The purpose of Snoop cycles is to check whether the address being presented by another bus master is contained within the cache of the Write-Back Enhanced Intel486 processors. Snoop cycles may be initiated with or without an invalidation request (INV = 1 or 0). If a snoop cycle is initiated with INV = 0 (usually during memory read cycles by another master), it is referred to as an Inquire cycle. If a snoop cycle is initiated with INV = 1 (usually during memory write cycles), it is referred to as an Invalidate cycle. If the address hits a modified line in the cache, the HITM# pin is asserted, and the modified line is written back onto the bus. Table 7-7 describes state transitions for Snoop cycles.

7.8.2 DETECTING ON-CHIP WRITE-BACK CACHE OF THE WRITE-BACK ENHANCED IntelDX4™ PROCESSOR

The write-back policy of the on-chip cache of the Write-Back Enhanced Intel486 processors may be detected by software or hardware. The software mechanism makes use of the CPUID instruction. (See Appendix B, ''Feature Determination,'' for use of the CPUID instruction.) The hardware mechanism makes use of a write-back related output signal from the processor.

A software mechanism to determine if a given processor has write-back support for the on-chip cache should drive the WB/WT# pin to ''1'' during RESET. This pin will be sampled by the processor during the falling edge of the RESET. Execute the CPUID instruction, which returns the model number in the EAX register, EAX[7:4]. If the model number returned is 7 (Write-Back Enhanced Intel486 processors) and the family number is 4, the on-chip cache supports the write-back policy. If the model number returned is in the range 0 through 6 or 8, the on-chip cache only supports the write-through policy.

The following pseudo code/steps give an example of the initialization BIOS that can be used to detect the presence of the write-back on-chip cache:

- Boot Address Cold start
- Load Segment Registers and null IDTR
- Execute CPUID instruction and determine the Family ID and Model ID.
- Compare the Family ID to 4 and the Model ID returned to the values listed in Table B-2.

The hardware mechanism involves using the HITM# signal. For the Write-Back Enhanced Intel486 processors, this signal is driven inactive (high) during RESET. The chipset can sample this output on the falling edge of RESET. If HITM# is sampled high on the falling edge of RESET, the processor supports on-chip write-back cache configuration. For those processors that do not support internal write-back caching, this signal is an INC, and this output is not driven.

Table 7-7. Cache State Transitions During Snoop Cycles

Present State	Next State INV = 1	Next State INV = 0	Description
M	I	E	Snoop hit to a modified line indicated by HITM# pin low. Write-Back Enhanced IntelDX4 Processor schedules the write back of the modified line to memory. The state of the line changes to E provided INV = 0 and changes to I if INV = 1.
E	I	E	Snoop hit, no bus cycle generated. State remains unaltered if INV = 0, and changes to I if INV = 1. There is no external indication of this snoop hit.
S	I	S	Snoop hit, no bus cycle generated. State remains unaltered if INV = 0, and changes to I if INV = 1. There is no external indication of this snoop hit.
I	I	I	Address not in cache.

8.0 SYSTEM MANAGEMENT MODE (SMM) ARCHITECTURES

8.1 SMM Overview

The Military Intel486 processor supports four modes: Real, Virtual-86, Protected, and System Management Mode (SMM). As an operating mode, SMM has a distinct processor environment, interface and hardware/software features.

SMM provides system designers with a means of adding new software-controlled features to computer products that operate transparently to the operating system and software applications. SMM is intended for use only by system firmware, not by applications software or general purpose systems software.

The SMM architectural extension consists of the following elements:

1. System Management Interrupt (SMI#) hardware interface.
2. Dedicated and secure memory space (SMRAM) for SMI# handler code and processor state (context) data with a status signal for the system to decode access to that memory space, SMIACT#. (The SMBASE address is relocatable and could also be relocated to non-cacheable address space.)
3. Resume (RSM) instruction, for exiting the System Management Mode.
4. Special Features such as I/O-Restart, for transparent power management of I/O peripherals, and Auto HALT Restart.

8.2 Terminology

The following terms are used throughout the discussion of System Management Mode.

SMM: System Management Mode. This is the operating environment that the processor (system) enters when the System Management Interrupt is being serviced.

SMI#: System Management Interrupt. This is part of the SMM interface. When SMI# is asserted (SMI# pin asserted low) it causes the processor to invoke SMM. **The SMI# pin is the only means of entering SMM.**

SMM handler: System Management Mode handler. This is the code that will be executed when the processor is in SMM. An example application that this code might implement is a power management control or a system control function.

RSM: Resume instruction. This instruction is used by the SMM handler to exit the SMM and return to the interrupted operating system or application process.

SMRAM: This is the physical memory dedicated to SMM. The SMM handler code and related data reside in this memory. This memory is also used by the processor to store its context before executing the SMM handler. The operating system and applications do not have access to this memory space.

SMBASE: Control register that contains the address of the SMRAM space.

Context: This term refers to the processor state. The SMM discussion refers to the context, or processor state, just before the processor invokes SMM. The context normally consists of the processor registers that fully represent the processor state.

Context Switch: A context switch is the process of either saving or restoring the context. The SMM discussion refers to the context switch as the process of saving/restoring the context while invoking/exiting SMM, respectively.

8.3 System Management Interrupt Processing

The system interrupts the normal program execution and invokes SMM by generating a System Management Interrupt (SMI#) to the processor. The processor will service the SMI# by executing the following sequence (see Figure 8-1):

1. The processor asserts the SMIACT# signal, indicating to the system that it should enable the SMRAM.
2. The processor saves its state (context) to SMRAM, starting at default address location 3FFFFH, proceeding downward in a stack-like fashion.
3. The processor switches to the System Management Mode processor environment (a pseudo-real mode).
4. The processor will then jump to the default absolute address of 38000H in SMRAM to execute the SMI# handler. This SMI# handler performs the system management activities.
5. The SMI# handler will then execute the RSM instruction which restores the processors context from SMRAM, de-asserts the SMIACT# signal, and then returns control to the previously interrupted program execution.

NOTE:
The above sequence is valid for the default SMBASE value only. See the following sections for a description of the SMBASE register and SMBASE relocation.

The System Management Interrupt hardware interface consists of the SMI# interrupt request input and the SMIACT# output used by the system to decode the SMRAM.

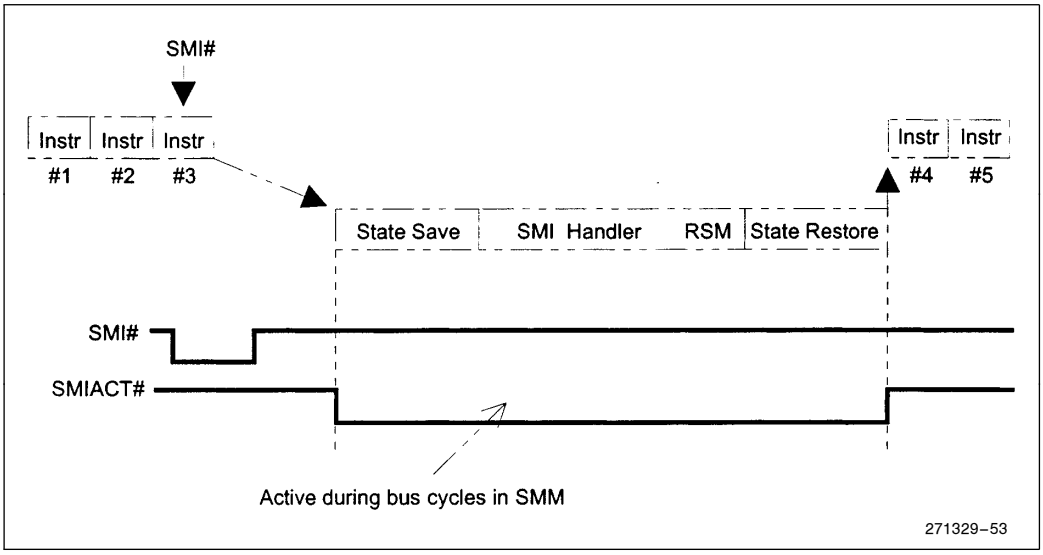


Figure 8-1. Basic SMI# Interrupt Service

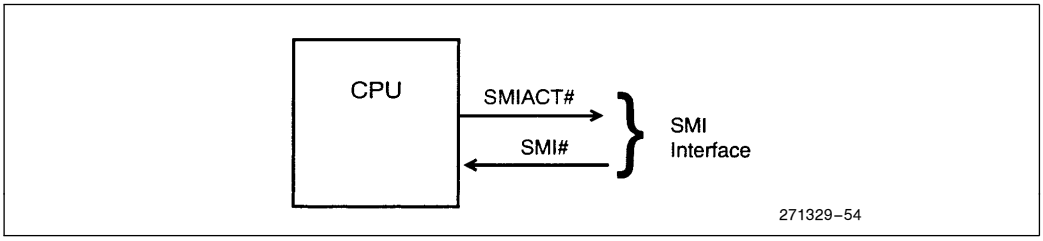


Figure 8-2. Basic SMI# Hardware Interface

8.3.1 SYSTEM MANAGEMENT INTERRUPT (SMI#)

SMI# is a falling-edge triggered, non-maskable interrupt request signal. SMI# is an asynchronous signal, but setup and hold times, t_{20} and t_{21}, must be met in order to guarantee recognition on a specific clock. The SMI# input need not remain active until the interrupt is actually serviced. The SMI# input only needs to remain active for a single clock if the required setup and hold times are met. SMI# will also work correctly if it is held active for an arbitrary number of clocks.

The SMI# input must be held inactive for at least four external clocks after it is asserted to reset the edge triggered logic. A subsequent SMI# might not be recognized if the SMI# input is not held inactive for at least four clocks after being asserted.

SMI#, like NMI, is not affected by the IF bit in the EFLAGS register and is recognized on an instruction boundary. An SMI# will not break locked bus cycles. The SMI# has a higher priority than NMI and is not masked during an NMI. In order for SMI# to be recognized with respect to SRESET, SMI# should not be asserted until two (2) clocks after SRESET becomes inactive.

After the SMI# interrupt is recognized, the SMI# signal will be masked internally until the RSM instruction is executed and the interrupt service routine is complete. Masking the SMI# prevents recursive SMI# calls. SMI# must be de-asserted for at least 4 clocks to reset the edge triggered logic. If another SMI# occurs while the SMI# is masked, the pending SMI# will be recognized and executed on the next instruction boundary after the current SMI# completes. This instruction boundary occurs before execution of the next instruction in the interrupted application code, resulting in back to back SMM handlers. Only one SMI# can be pending while SMI# is masked.

The SMI# signal is synchronized internally and must be asserted at least three (3) CLK periods prior to asserting the RDY# signal in order to guarantee recognition on a specific instruction boundary. This is important for servicing an I/O trap with an SMI# handler. (See Figure 8-3.)

8.3.2 SMI# ACTIVE (SMIACT#)

SMIACT# indicates that the processor is operating in System Management Mode. The processor asserts SMIACT# in response to an SMI# interrupt request on the SMI# pin. SMIACT# is driven active after the processor has completed all pending write cycles (including emptying the write buffers), and before the first access to SMRAM when the processor saves (writes) its state (or context) to SMRAM. SMIACT# remains active until the last access to SMRAM when the processor restores (reads) its state from SMRAM. The SMIACT# signal does not float in response to HOLD. The SMIACT# signal is used by the system logic to decode SMRAM (See Figure 8-2).

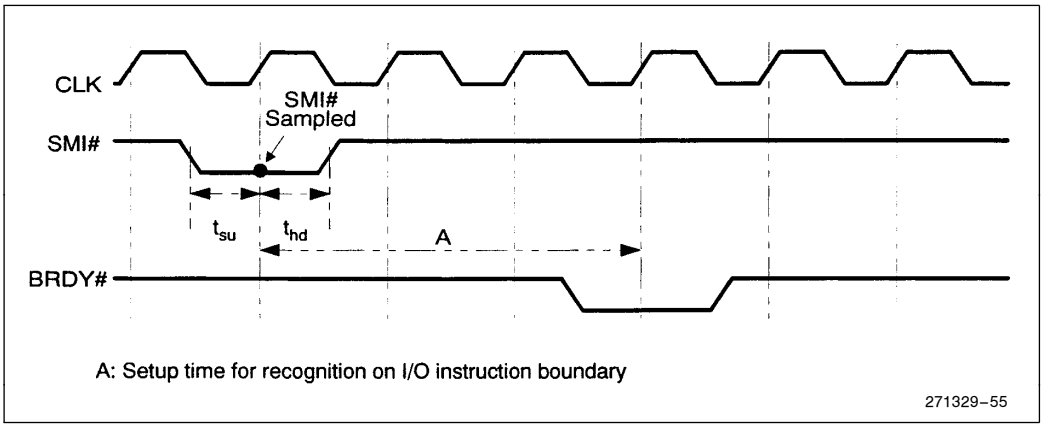


Figure 8-3. SMI# Timing for Servicing an I/O Trap

The number of CLKs required to complete the SMM state save and restore is very dependent on-system memory performance. The values listed in Table 8-1 assume 0 wait-state memory writes (2 CLK cycles), 2-1-1-1 burst read cycles, and 0 wait-state non-burst reads (2 CLK cycles). Additionally, it is assumed that the data read during the SMM state restore sequence is not cacheable.

Figure 8-4 and Table 8-1 can be used for latency calculations. As shown, the minimum time required to enter an SMI# handler routine for the Military Intel486 DX processor (from the completion of the interrupted instruction) is given by:

Latency to beginning of SMI# handler =

A + B + C = 153 CLKs

and the minimum time required to return to the interrupted application (following the final SMM instruction before RSM) is given by:

Latency to continue interrupted application =

E + F + G = 243 CLKs

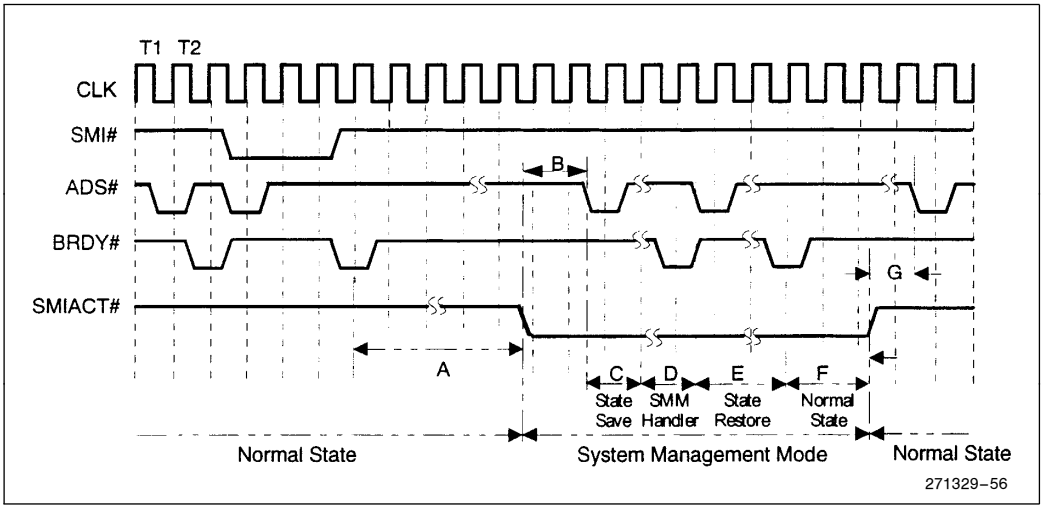


Figure 8-4. Military Intel486™ Processor SMIACT# Timing

Table 8-1. Military Intel486™ Processor SMIACT# Timing

	Military Intel486 DX Processor	IntelDX2™ Processor	IntelDX4™ Processor 3X	IntelDX4 Processor 2X
A:Last RDY# from non-SMM transfer to SMIACT# assertion	2 CLK minimum	1 CLK minimum	1 CLK minimum	1 CLK minimum
B:SMIACT# assertion to first ADS# for SMM state save	40 CLK minimum	20 CLK minimum	13 CLK minimum	20 CLK minimum
C:SMM state save (dependent on memory performance)	Approx. 139 CLKs	Approx. 139 CLKs	Approx. 139 CLKs	Approx. 139 CLKs
D:SMM handler	User determined	User determined	User determined	User determined
E:SMM state restore (dependent on memory performance)	Approx. 236 CLKs	Approx. 236 CLKs	Approx. 236 CLKs	Approx. 236 CLKs
F:Last RDY# from SMM transfer to de-assertion of SMIACT#	4 CLK minimum	2 CLK minimum	1 CLK minimum	1 CLK minimum
G: SMIACT# de-assertion to first non-SMM ADS#	20 CLK minimum	10 CLK minimum	6 CLK minimum	10 CLK minimum

8.3.3 SMRAM

The Military Intel486 processor uses the SMRAM space for state save and state restore operations during an SMI# and RSM. The SMI# handler, which also resides in SMRAM, uses the SMRAM space to store code, data and stacks. In addition, the SMI# handler can use the SMRAM for system management information such as the system configuration, configuration of a powered-down device, and system designer-specific information.

The processor asserts the SMIACT# output to indicate to the memory controller that it is operating in System Management Mode. The system logic should ensure that only the processor has access to this area. Alternate bus masters or DMA devices trying to access the SMRAM space when SMIACT# is active should be directed to system RAM in the respective area.

The system logic is minimally required to decode the physical memory address range from 38000H–3FFFFH as SMRAM area. The processor will save its state to the state save area from 3FFFFH downward to 3FE00H. After saving its state the processor will jump to the address location 38000H to begin executing the SMI# handler. The system logic can choose to decode a larger area of SMRAM as needed. The size of this SMRAM can be between 32 Kbytes and 4 Gbytes.

The system logic should provide a manual method for switching the SMRAM into system memory space when the processor is **not** in SMM. This will enable initialization of the SMRAM space (i.e., loading SMI# handler) before executing the SMI# handler during SMM. (See Figure 8-5.)

8.3.3.1 SMRAM State Save Map

When the SMI# is recognized on an instruction boundary, the processor core first sets the SMIACT# signal LOW indicating to the system logic that accesses are now being made to the system-defined SMRAM areas. The processor then writes its state to the state save area in the SMRAM. The state save area starts at CS Base + [8000H + 7FFFH]. The default CS Base is 30000H, therefore the default state save area is at 3FFFFH. In this case, the CS Base can also be referred to as the SMBASE.

If SMBASE Relocation is enabled, then the SMRAM addresses can change. The following formula is used to determine the relocated addresses where the context is saved. The context will reside at CS Base + [8000H + Register Offset], where the default initial CS Base is 30000H and the Register Offset is listed in the SMRAM state save map (Table 8-2). Reserved spaces will be used to accommodate new registers in future processors. The state save area starts at 7FFFH and continues downward in a stack-like fashion.

Some of the registers in the SMRAM state save area may be read and changed by the SMI# handler, with the changed values restored to the processor registers by the RSM instruction. Some register images are read-only, and must not be modified (modifying these registers will result in unpredictable behavior). The values stored in the areas marked reserved may change in future processors. An SMM handler should not rely on any values stored in an area that is marked as reserved.

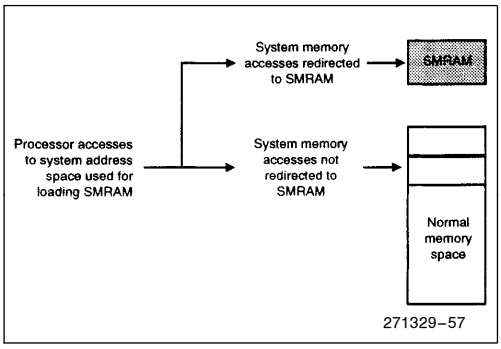


Figure 8-5. Redirecting System Memory Addresses to SMRAM

Table 8-2. SMRAM State Save Map

Register Offset	Register	Writeable?
7FFC	CR0	NO
7FF8	CR3	NO
7FF4	EFLAGS	YES
7FF0	EIP	YES
7FEC	EDI	YES
7FE8	ESI	YES
7FE4	EBP	YES
7FE0	ESP	YES
7FDC	EBX	YES
7FD8	EDX	YES
7FD4	ECX	YES
7FD0	EAX	YES
7FCC	DR6	NO
7FC8	DR7	NO
7FC4	TR*	NO
7FC0	LDTR*	NO
7FBC	GS*	NO
7FB8	FS*	NO
7FB4	DS*	NO
7FB0	SS*	NO
7FAC	CS*	NO
7FA8	ES*	NO
7FA7–7F98	Reserved	NO
7F94	IDT Base	NO
7F93–7F8C	Reserved	NO
7F88	GDT Base	NO
7F87–7F04	Reserved	NO
7F02	Auto HALT Restart Slot (Word)	YES
7F00	I/O Trap Restart Slot (Word)	YES
7EFC	SMM Revision Identifier (Dword)	NO
7EF8	SMBASE Slot (Dword)	YES
7EF7–7E00	Reserved	NO

NOTES:
*Upper two bytes are reserved.
Modifying a value that is marked as not writeable will result in unpredictable behavior.
Words are stored in two consecutive bytes in memory with the low-order byte at the lowest address and the high-order byte in the high address.

The following registers are saved and restored (in areas of the state save that are marked reserved), but are not visible to the system software programmer:

CR1, CR2 and CR4, hidden descriptor registers for CS, DS, ES, FS, GS, and SS.

If an SMI# request is issued for the purpose of powering down the processor, the values of all reserved locations in the SMM state save must be saved to non-volatile memory.

The following registers are not automatically saved and restored by SMI# and RSM:

DR5–DR0, TR7–TR3, FPU registers: STn, FCS, FSW, tag word, FP instruction pointer, FP opcode, and operand pointer.

For all SMI# requests except for suspend/resume, these registers do not have to be saved because their contents will not change. However, during a power down suspend/resume, a resume reset will clear these registers back to their default values. In this case, the suspend SMI# handler should read these registers directly to save them and restore them during the power up resume. Anytime the SMI# handler changes these registers in the processor, it must also save and restore them.

8.3.4 EXIT FROM SMM

The **RSM** instruction is only available to the SMI# handler. The opcode of the instruction is 0FAAH. Execution of this instruction while the processor is executing outside of SMM will cause an invalid opcode error. The last instruction of the SMI# handler will be the RSM instruction.

The RSM instruction restores the state save image from SMRAM back to the processor, then returns control back to the interrupted program execution. There are three SMM features that can be enabled by writing to control ''slots'' in the SMRAM state save area.

Auto HALT Restart. It is possible for the SMI# request to interrupt the HALT state. The SMI# handler can tell the RSM instruction to return control to the HALT instruction **or** to return control to the instruction following the HALT instruction by appropriately setting the Auto HALT Restart slot. The default operation is to restart the HALT instruction.

I/O Trap Restart. If the SMI# interrupt was generated on an I/O access to a powered-down device, the SMI# handler can tell the RSM instruction to re-execute that I/O instruction by setting the I/O Trap Restart slot.

SMBASE Relocation. The system can relocate the SMRAM by setting the SMBASE Relocation slot in the state save area. The RSM instruction will set the SMBASE in the processor based on the value in the SMBASE relocation slot. The SMBASE must be 32K aligned.

For further details on these SMM features, see section 8.5.

If the processor detects invalid state information, it enters the shutdown state. This happens only in the following situations:

- The value stored in the SMBASE slot is not a 32-Kbyte-aligned address.
- A reserved bit of CR4 is set to 1.
- A combination of bits in CR0 is illegal; namely, (PG = 1 and PE = 0) or (NW = 1 and CD = 0).

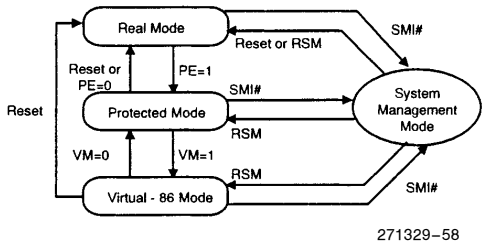
In shutdown mode, the processor stops executing instructions until an NMI interrupt is received or reset initialization is invoked. The processor generates a special bus cycle to indicate it has entered shutdown mode.

NOTE:
INTR and SMI# will also bring the processor out of a shutdown that is encountered due to invalid state information from SMM execution. Make sure that INTR and SMI# are not asserted if SMM routines are written such that a shutdown occurs.

8.4 System Management Mode Programming Model

8.4.1 ENTERING SYSTEM MANAGEMENT MODE

SMM is one of the major operating modes, on a level with Protected mode, Real address mode or virtual-86 mode. Figure 8-6 shows how the processor can enter SMM from any of the three modes and then return.



NOTE:
Reset could occur by asserting the RESET or SRESET pin.

Figure 8-6. Transition to and from System Management Mode

The external signal SMI# causes the processor to switch to SMM. The RSM instruction exits SMM. SMM is transparent to applications programs and operating systems because of the following:

- The only way to enter SMM is via a type of non-maskable interrupt triggered by an external signal.
- The processor begins executing SMM code from a separate address space, referred to earlier as system management RAM (SMRAM).
- Upon entry into SMM, the processor saves the register state of the interrupted program in a part of SMRAM called the SMM context save space.
- All interrupts normally handled by the operating system or by applications are disabled upon entry into SMM
- A special instruction, RSM, restores processor registers from the SMM context save space and returns control to the interrupted program.

SMM is similar to Real address mode in that there are no privilege levels or address mapping. An SMM program can execute all I/O and other system instructions and can address up to four Gbytes of memory.

8.4.2 PROCESSOR ENVIRONMENT

When an SMI# signal is recognized on an instruction execution boundary, the processor waits for all stores to complete, including emptying of the write buffers. The final write cycle is complete when the system returns RDY# or BRDY#. The processor then drives SMIACT# active, saves its register state to SMRAM space, and begins to execute the SMM handler.

SMI# has greater priority than debug exceptions and external interrupts. This means that if more than one of these conditions occur at an instruction boundary, only the SMI# processing occurs, not a debug exception or external interrupt. Subsequent SMI# requests are not acknowledged while the processor is in SMM. The first SMI# interrupt request that occurs while the processor is in SMM is latched, and serviced when the processor exits SMM with the RSM instruction. Only one SMI# will be latched by the processor while it is in SMM.

When the processor invokes SMM, the processor core registers are initialized as shown in Table 8-3.

Table 8-3. SMM Initial Processor Core Register Settings

Register	Contents
General Purpose Registers	Unpredictable
EFLAGS	00000002H
EIP	00008000H
CS Selector	3000H
CS Base	SMM Base (default 30000H)
DS, ES, FS, GS, SS Selectors	0000H
DS, ES, FS, GS, SS Bases	000000000H
DS, ES, FS, GS, SS Limits	0FFFFFFFFH
CR0	Bits 0,2,3 & 31 cleared (PE, EM, TS & PG); others are unmodified
DR6	Unpredictable
DR7	00000000H

The following is a summary of the key features in the SMM environment:

1. Real mode style address calculation
2. 4-Gbyte limit checking
3. IF flag is cleared
4. NMI is disabled
5. TF flag in EFLAGS is cleared; single step traps are disabled
6. DR7 is cleared, except for bits 12 and 13; debug traps are disabled.
7. The RSM instruction no longer generates an invalid opcode error
8. Default 16-bit opcode, register and stack use.

All bus arbitration (HOLD, AHOLD, BOFF#) inputs and bus sizing (BS8#, BS16#) inputs operate normally while the processor is in SMM.

8.4.2.1 Write-Back Enhanced IntelDX4™ Processor Environment

When the Write-Back Enhanced Intel486 processors are in Enhanced Bus Mode, SMI# has greater priority than debug exceptions and external interrupts, except for FLUSH# and SRESET. (See section 4.8.6.)

8.4.3 EXECUTING SYSTEM MANAGEMENT MODE HANDLER

The processor begins execution of the SMM handler at offset 8000H in the CS segment. The CS Base is initially 30000H. However, the CS Base can be changed by using the SMM Base relocation feature.

When the SMM handler is invoked, the processors PE and PG bits in CR0 are reset to 0. The processor is in an environment similar to Real mode, but without the 64-Kbyte limit checking. However, the default operand size and the default address size are set to 16 bits.

The EM bit is cleared so that no exceptions are generated. (If the SMM was entered from Protected mode, the Real mode interrupt and exception support is not available.) The SMI# handler should not use floating point unit instructions until the FPU is properly detected (within the SMI# handler) and the exception support is initialized.

Because the segment bases (other than CS) are cleared to 0 and the segment limits are set to 4 Gbytes, the address space may be treated as a single flat 4-Gbyte linear space that is unsegmented. The processor is still in Real mode and when a segment selector is loaded with a 16-bit value, that value is then shifted left by 4 bits and loaded into the segment base cache. The limits and attributes are not modified.

In SMM, the processor can access or jump anywhere within the 4-Gbyte logical address space. The processor can also indirectly access or perform a near jump anywhere within the 4-Gbyte logical address space.

8.4.3.1 Exceptions and Interrupts within System Management Mode

When the processor enters SMM, it disables INTR interrupts, debug and single-step traps by clearing the EFLAGS, DR6 and DR7 registers. This is done to prevent a debug application from accidentally breaking into an SMM handler. This is necessary because the SMM handler operates from a distinct address space (SMRAM), and hence, the debug trap will not represent the normal system memory space.

If an SMM handler wishes to use the debug trap feature of the processor to debug SMM handler code, it must first ensure that an SMM compliant debug handler is available. The SMM handler must also ensure DR0–DR3 is saved to be restored later. The debug registers DR0–DR3 and DR7 must then be initialized with the appropriate values.

If the processor wishes to use the single step feature of the processor, it must ensure that an SMM compliant single step handler is available and then set the trap flag in the EFLAGS register.

If the system design requires the processor to respond to hardware INTR requests while in SMM, it must ensure that an SMM compliant interrupt handler is available and then set the interrupt flag in the EFLAGS register (using the STI instruction). Software interrupts are not blocked upon entry to SMM, and the system software designer must provide an SMM compliant interrupt handler before attempting to execute any software interrupt instructions. Note that in SMM mode, the interrupt vector table has the same properties and location as the Real mode vector table.

NMI interrupts are blocked upon entry to the SMM handler. If an NMI request occurs during the SMM handler, it is latched and serviced after the processor exits SMM. Only one NMI request will be latched during the SMM handler. If an NMI request is pending when the processor executes the RSM instruction, the NMI is serviced before the next instruction of the interrupted code sequence.

Although NMI requests are blocked when the processor enters SMM, they may be enabled through software by executing an IRET instruction. If the SMM handler requires the use of NMI interrupts, it should invoke a dummy interrupt service routine for the purpose of executing an IRET instruction. Once an IRET instruction is executed, NMI interrupt requests are serviced in the same "real mod" manner in which they are handled outside of SMM.

8.5 SMM Features

8.5.1 SMM REVISION IDENTIFIER

The SMM revision identifier is used to indicate the version of SMM and the SMM extensions that are supported by the processor. The SMM revision identifier is written during SMM entry and can be examined in SMRAM space at Register Offset 7EFCH. The lower word of the SMM revision identifier refers to the version of the base SMM architecture. The upper word of the SMM revision identifier refers to the extensions available. (See Figure 8-7.)

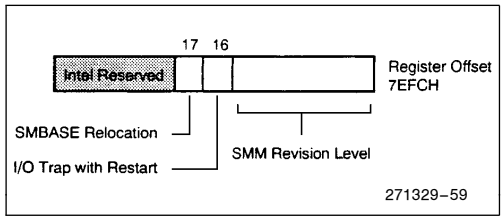


Figure 8-7. SMM Revision Identifier

Table 8-4. Bit Values for SMM Revision Identifier

Bits	Value	Comments
16	0	Processor does not support I/O Trap Restart
16	1	Processor supports I/O Trap Restart
17	0	Processor does not support SMBASE relocation
17	1	Processor supports SMBASE relocation

Bit 16 of the SMM revision identifier is used to indicate to the SMM handler that this processor supports the SMM I/O trap extension. If this bit is high, then this processor supports the SMM I/O trap extension. If this bit is low, then this processor does not support I/O trapping using the I/O trap slot mechanism. (See Table 8-4.)

Bit 17 of this slot indicates whether the processor supports relocation of the SMM jump vector and the SMRAM base address. (See Table 8-4.)

The Military Intel486 processor supports both the I/O Trap Restart and the SMBASE relocation features.

8.5.2 AUTO HALT RESTART

The Auto HALT Restart slot at register offset (word location) 7F02H in SMRAM indicates to the SMM handler that the SMI# interrupted the processor during a HALT state (bit 0 of slot 7F02H is set to 1 if the previous instruction was a HALT). If the SMI# did not interrupt the processor in a HALT state, then the SMI# microcode will set bit 0 of the Auto HALT Restart slot to a value of 0. If the previous instruction was a HALT, the SMM handler can choose to either set or reset bit 0. If this bit is set to 1, the RSM micro code execution will force the processor to re-enter the HALT state. If this bit is set to 0 when the RSM instruction is executed, the processor will continue execution with the instruction just after the interrupted HALT instruction. Note that if the interrupted instruction was not a HALT instruction (bit 0 is set to 0 in the Auto HALT Restart slot upon SMM entry), setting bit 0 to 1 will cause unpredictable behavior when the RSM instruction is executed. (See Figure 8-8 and Table 8-5.)

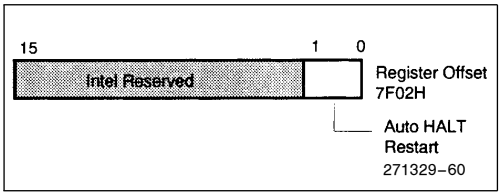


Figure 8-8. Auto HALT Restart

Table 8-5. Bit Values for Auto HALT Restart

Value of Bit 0 at Entry	Value of Bit 0 at Exit	Comments
0	0	Returns to next instruction in interrupted program.
0	1	Unpredictable
1	0	Returns to next instruction after HALT
1	1	Returns to HALT state

If the HALT instruction is restarted, the processor will generate a memory access to fetch the HALT instruction (if it is not in the internal cache), and execute a HALT bus cycle.

8.5.3 I/O INSTRUCTION RESTART

The I/O instruction restart slot (register offset 7F00H in SMRAM) gives the SMM handler the option of causing the RSM instruction to automatically re-execute the interrupted I/O instruction. When the RSM instruction is executed, if the I/O instruction restart slot contains the value 0FFH, then the processor will automatically re-execute the I/O instruction that the SMI# trapped. If the I/O instruction restart slot contains the value 00H when the RSM instruction is executed, then the processor will not re-execute the I/O instruction. The processor automatically initializes the I/O instruction restart slot to 00H during SMM entry. The I/O instruction restart slot should be written only when the processor has generated an SMI# on an I/O instruction boundary. Processor operation is unpredictable when the I/O instruction restart slot is set when the processor is servicing an SMI# that originated on a non-I/O instruction boundary. (See Figure 8-9 and Table 8-6.)

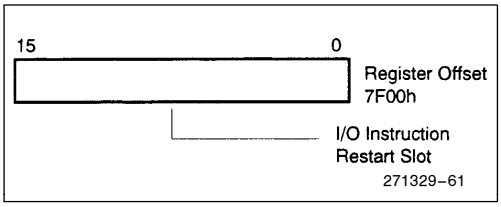


Figure 8-9. I/O Instruction Restart

Table 8-6. I/O Instruction Restart Value

Value at Entry	Value at Exit	Comments
00H	00H	Do not restart trapped I/O instruction
00H	0FFH	Restart trapped I/O instruction

If the system executes back-to-back SMI# requests, the second SMM handler must not set the I/O instruction restart slot (see section 8.6.6 "Nested SMI#s and I/O Restart").

8.5.4 SMM BASE RELOCATION

The Military Intel486 processor provides a control register, SMBASE. The address space used as SMRAM can be modified by changing the SMBASE register before exiting an SMI# handler routine. SMBASE can be changed to any 32K aligned value (values that are not 32K aligned will cause the processor to enter the shutdown state when executing the RSM instruction). SMBASE is set to the default value of 30000H on RESET, but is not changed on SRESET. If the SMBASE register is changed during an SMM handler, all subsequent SMI# requests will initiate a state save at the new SMBASE. (See Figure 8-10.)

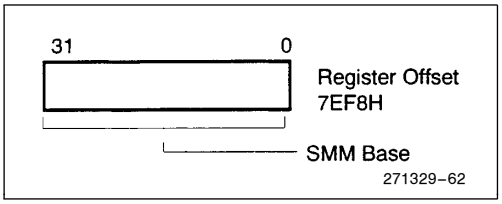


Figure 8-10. SMM Base Location

The SMBASE slot in the SMM state save area is a feature used to indicate and change the SMI# jump vector location and the SMRAM save area. When bit 17 of the SMM Revision Identifier is set then this feature exists and the SMRAM base and consequently the jump vector are as indicated by the SMM Base slot. During the execution of the RSM instruction, the processor will read this slot and initialize the processor to use the new SMBASE during the next SMI#. During an SMI#, the processor will do its context save to the new SMRAM area pointed to by the SMBASE, store the current SMBASE in the SMM Base slot (offset 7EF8H), and then start execution of the new jump vector based on the current SMBASE.

The SMBASE must be a 32-Kbyte aligned, 32-bit integer that indicates a base address for the SMRAM context save area and the SMI# jump vector. For example when the processor first powers up, the minimum SMRAM area is from 38000H–3FFFFH. The default SMBASE is 30000H. Hence the starting address of the jump vector is calculated by:

SMBASE + 8000H

While the starting address for the SMRAM state save area is calculated by:

SMM Base + [8000H + 7FFFH]

Hence, when this feature is enabled, the SMRAM register map is addressed according to the above formulas. (See Figure 8-11.)

To change the SMRAM base address and SMM jump vector location, the SMM handler should modify the SMBASE slot. Upon executing an RSM instruction, the processor will read the SMBASE slot and store it internally. Upon recognition of the next SMI# request, the processor will use the new SMBASE slot for the SMRAM dump and SMI# jump vector.

If the modified SMBASE slot does not contain a 32-Kbyte aligned value, the RSM microcode will cause the processor to enter the shutdown state.

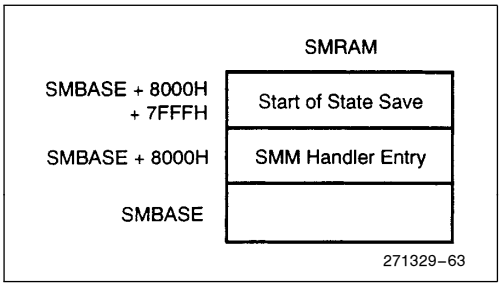


Figure 8-11. SMRAM Usage

8.6 SMM System Design Considerations

8.6.1 SMRAM INTERFACE

The hardware designed to control the SMRAM space must follow these guidelines:

1. A provision should be made to allow for initialization of SMRAM space during system boot up. This initialization of SMRAM space must happen before the first occurrence of an SMI# interrupt. Initializing the SMRAM space must include installation of an SMM handler, and may include installation of related data structures necessary for particular SMM applications. The memory controller providing the interface to the SMRAM should provide a means for the initialization code to manually open the SMRAM space.
2. A minimum initial SMRAM address space of 38000H-3FFFFH should be decoded by the memory controller.
3. Alternate bus masters (such as DMA controllers) should not be allowed to access SMRAM space. Only the processor, either through SMI# or during initialization, should be allowed access to SMRAM.
4. In order to implement a zero-volt suspend function, the system must have access to all of normal system memory from within an SMM handler routine. If the SMRAM is going to overlay normal system memory, there must be a method of accessing any system memory that is located underneath SMRAM.

There are two potential schemes for locating the SMRAM, either overlaid to an address space on top of normal system memory, or placed in a distinct address space. (See Figure 8-12.) When SMRAM is overlaid on the top of normal system memory, the processor output signal SMIACT# must be used to distinguish SMRAM from main system memory. Additionally, if the overlaid normal memory is cacheable, both the processor internal cache and any second level caches must be empty before the first read of an SMM handler routine. If the SMM memory is cacheable, the caches must be empty before the first read of normal memory following an SMM handler routine. This is done by flushing the caches, and is required to maintain cache coherency. When the default SMRAM location is used, SMRAM is overlaid on top of system main memory (at 38000H through 3FFFFH).

If SMRAM is located in its own distinct memory space, which can be completely decoded with only the processor address signals, it is said to be non-overlaid. In this case, there are no new requirements for maintaining cache coherency.

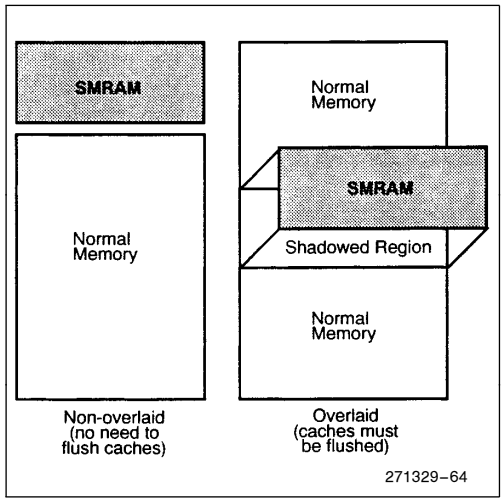


Figure 8-12. SMRAM Location

8.6.2 CACHE FLUSHES

The processor does not unconditionally flush its cache before entering SMM (this option is left to the system designer). If SMRAM is shadowed in a cacheable memory area that is visible to the application or operating system, it is necessary for the system to empty both the processor cache and any second level cache before entering SMM. That is, if SMRAM is in the same physical address location as the normal cacheable memory space, then an SMM read may hit the cache which would contain normal memory space code/data. If the SMM memory is cacheable, the normal read cycles after SMM may hit the cache, which may contain SMM code/data. In this case the cache should be empty before the first memory read cycle during SMM and before the first normal cycle after exiting SMM. (See Figure 8-13.)

The FLUSH# and KEN# signals can be used to ensure cache coherency when switching between normal and SMM modes. Cache flushing during SMM entry is accomplished by asserting the FLUSH# pin when SMI# is driven active. Cache flushing during SMM exit is accomplished by asserting the FLUSH# pin after the SMIACT# pin is deasserted (within 1 CLK). To guarantee this behavior, the constraints on setup and hold timings on the interaction of FLUSH# and SMIACT# as specified for a processor should be followed.

If the SMRAM area is overlaid over normal memory and if the system designer does not want to flush the caches upon leaving SMM then references to the SMRAM area should not be cached. It is the obligation of the system designer to ensure that the KEN# pin is sampled inactive during all references to the SMRAM area. Figures 8-14 and 8-15 illustrate a cached and non-cached SMM using FLUSH# and KEN#.

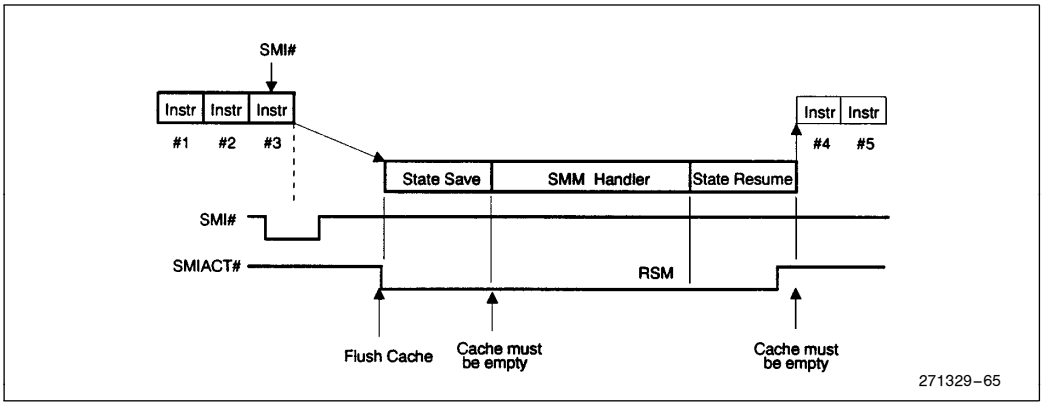


Figure 8-13. FLUSH# Mechanism during SMM

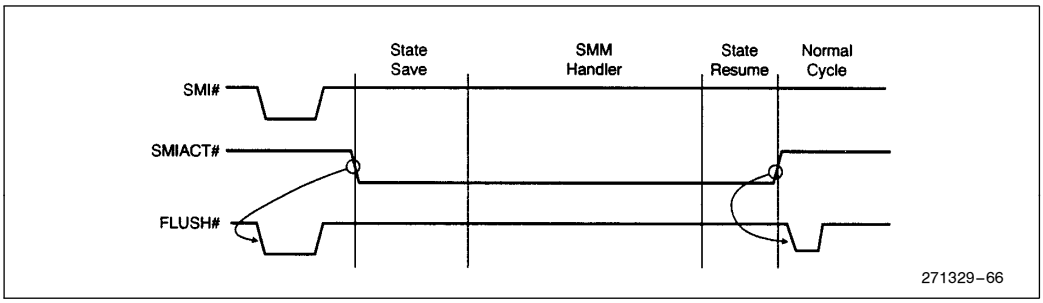


Figure 8-14. Cached SMM

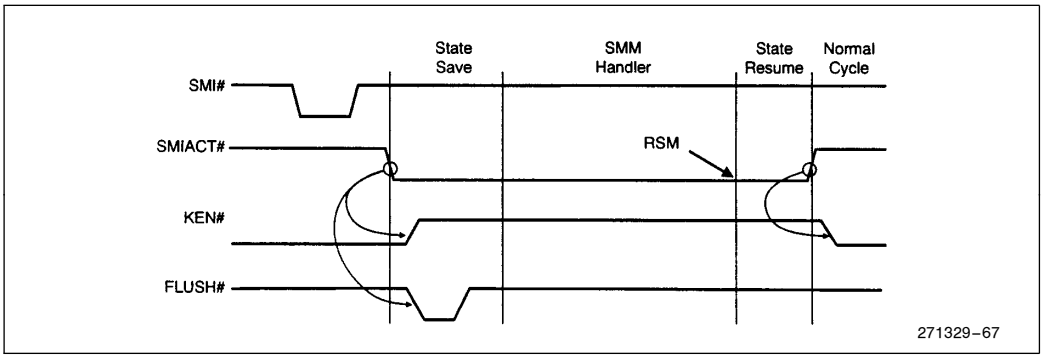


Figure 8-15. Non-Cached SMM

8.6.3 A20M# PIN AND SMBASE RELOCATION

Systems based on a PC-compatible architecture contain a feature that enables the processor address bit A20 to be forced to 0. This limits physical memory to a maximum of 1 Mbyte, and is provided to ensure compatibility with those programs that relied on the physical address wrap around functionality of the 8088 processor. The A20M# pin on Military Intel486 processors provides this function. When A20M# is active, all external bus cycles will drive A20M# low, and all internal cache accesses will be performed with A20M# low.

The A20M# pin is recognized while the processor is in SMM. The functionality of the A20M# input must be recognized in the following two instances:

1. If the SMM handler needs to access system memory space above 1 Mbyte (for example, when saving memory to disk for a zero-volt suspend), the A20M# pin must be de-asserted before the memory above 1 Mbyte is addressed.
2. If SMRAM has been relocated to address space above 1 Mbyte, and A20M# is active upon entering SMM, the processor will attempt to access SMRAM at the relocated address, but with A20 low. This could cause the system to crash, because there would be no valid SMM interrupt handler at the accessed location.

In order to account for the above two situations, the system designer must ensure that A20M# is de-asserted on entry to SMM. A20M# must be driven inactive before the first cycle of the SMM state save, and must be returned to its original level after the last cycle of the SMM state restore. This can be done by blocking the assertion of A20M# whenever SMIACT# is active.

8.6.4 PROCESSOR RESET DURING SMM

The system designer should take into account the following restrictions while implementing the processor RESET logic.

1. When running software written for the 80286 processor a processor SRESET is used to switch the processor from Protected mode to Real mode. Note that SRESET has a higher interrupt priority than SMIACT#. When the processor is in SMM, the SRESET to the processor during SMM should be blocked until the processor exits SMM. SRESET must be blocked beginning from the time when SMI# is driven active and ending at least 20 CLK cycles after SMIACT# is de-asserted. Be careful not to block the global system RESET, which may be necessary to recover from a system crash.
2. During execution of the RSM instruction to exit SMM, there is a small time window between the de-assertion of SMIACT# and the completion of the RSM microcode. If SRESET is asserted during this window, it is possible that the SMRAM space will be violated. The system designer must guarantee that SRESET is blocked until at least 20 processor clock cycles after SMIACT# has been driven inactive.
3. Any request for a processor SRESET for the purpose of switching the processor from Protected mode to Real mode must be acknowledged after the processor has exited SMM. In order to maintain software transparency, the system logic must latch any SRESET signals that are blocked during SMM.

8.6.5 SMM AND SECOND LEVEL WRITE BUFFERS

Before a Military Intel486 processor enters SMM, it empties its internal write buffers. This is necessary so that the data in the write buffers is written to normal memory space, not SMM space. Once the processor is ready to begin writing an SMM state save to SMRAM, it asserts the SMIACT# signal. SMIACT# may be driven active by the processor before the system memory controller has had an opportunity to empty the second level write buffers.

To prevent the data from these second level write buffers from being written to the wrong location, the system memory controller needs to direct the memory write cycles to either SMM space or normal memory space. This can be accomplished by saving the status of SMIACT# along with the address for each word in the write buffers.

8.6.6 NESTED SMI#s AND I/O RESTART

Special care must be taken when executing an SMM handler for the purpose of restarting an I/O instruction. When the processor executes a RSM instruction with the I/O restart slot set, the restored EIP is modified to point to the instruction immediately preceding the SMI# request, so that the I/O instruction

can be re-executed. If a new SMI# request is received while the processor is executing an SMM handler, the processor will service this SMI# request before restarting the original I/O instruction. If the I/O restart slot is set when the processor executes the RSM instruction for the second SMM handler, the RSM microcode will decrement the restored EIP again. EIP now points to an address different from the originally interrupted instruction, and the processor will begin execution of the interrupted application code at an incorrect entry point.

To prevent this from occurring, the SMM handler routine must not set the I/O restart slot during the second of two consecutive SMM handlers.

8.7 SMM Software Considerations

8.7.1 SMM CODE CONSIDERATIONS

The default operand size and the default address size are 16 bits; however, operand-size override and address-size override prefixes can be used as needed to directly access data anywhere within the 4-Gbyte logical address space.

With operand-size override prefixes, the SMM handler can use jumps, calls, and returns, to transfer control to any location within the 4-Gbyte space. Note, however, the following restrictions:

- Any control transfer that does not have an operand-size override prefix truncates EIP to 16 low-order bits.
- Due to the Real mode style of base-address formation, a far jump or call cannot transfer control to a segment with a base address of more than 20 bits (one megabyte).

8.7.2 EXCEPTION HANDLING

Upon entry into SMM, external interrupts that require handlers are disabled (the IF bit in the EFLAGS is cleared). This is necessary because, while the processor is in SMM, it is running in a separate memory space. Consequently the vectors stored in the interrupt descriptor table (IDT) for the prior mode are not applicable. Before allowing exception handling (or software interrupts), the SMM program must initialize new interrupt and exception vectors. The interrupt vector table for SMM has the same format as for Real mode. Until the interrupt vector table is correctly initialized, the SMM handler must not generate an exception (or software interrupt). Even though hardware interrupts are disabled, exceptions and software interrupts can still occur. Only a correctly written SMM handler can prevent internal exceptions. When new exception vectors are initialized, internal exceptions can be serviced. The following are the restrictions:

1. Due to the Real mode style of base address formation, an interrupt or exception cannot transfer control to a segment with a base address of more that 20 bits.
2. An interrupt or exception cannot transfer control to a segment offset of more than 16 bits (64 Kbytes).
3. If exceptions or interrupts are allowed to occur, only the low order 16 bits of the return address (EIP) are pushed onto the stack. If the offset of the interrupted procedure is greater than 64 Kbytes, it is not possible for the interrupt/exception handler to return control to that procedure. (One work-around could be to perform software adjustment of the return address on the stack.)
4. The SMBASE Relocation feature affects the way the processor will return from an interrupt or exception during an SMI# handler.

8.7.3 HALT DURING SMM

HALT should not be executed during SMM, unless interrupts have been enabled (see section 8.7.2. ‘‘Exception Handling’’). Interrupts are disabled in SMM and INTR, NMI, and SMI# are the only events that take the processor out of HALT.

8.7.4 RELOCATING SMRAM TO AN ADDRESS ABOVE ONE MEGABYTE

Within SMM (or Real mode), the segment base registers can only be updated by changing the segment register. The segment registers contain only 16 bits, which allows only 20 bits to be used for a segment base address (the segment register is shifted left four bits to determine the segment base address). If SMRAM is relocated to an address above one megabyte, the segment registers can no longer be initialized to point to SMRAM.

These areas can still be accessed by using address override prefixes to generate an offset to the correct address. For example, if the SMBASE has been relocated immediately below 16M, the DS and ES registers are still initialized to 0000 0000H. We can still access data in SMRAM by using 32-bit displacement registers:

```
mov    esi, 00FFxxxxH      ;64K segment
                           ;immediately
                           ;below 16M
mov    ax,ds:[esi]
```

9.0 HARDWARE INTERFACE

9.1 Introduction

The Military Intel486 processor has separate parallel buses for data and addresses. The bidirectional data bus is 32 bits in width. The address bus consists of two components: 30 address lines (A2–A31) and 4-byte enable lines (BE0#–BE3#). The address lines form the upper 30 bits of the address and the byte enables select individual bytes within a 4-byte location. The address lines are bidirectional for use in cache line invalidations. (See Figure 9-1.)

The Military Intel486 processor's burst bus mechanism enables high-speed cache fills from external memory. Burst cycles can strobe data into the processor at a rate of one item every clock. Non-burst cycles have a maximum rate of one item every two clocks. Burst cycles are not limited to cache fills: all read bus cycles requiring more than a single data cycle can be bursted.

During bus hold, the Military Intel486 processor relinquishes control of the local bus by floating its address, data and control buses. The Military Intel486 processor has an address hold feature in addition to bus hold. During address hold, only the address bus is floated, the data and control buses can remain active. Address hold is used for cache line invalidations.

The Military Intel486 supports the IEEE 1149.1 boundary scan.

This section provides a brief description of the Military Intel486 processor input and output signals arranged by functional groups. The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # is not present after the signal name, the signal is active at high voltage level. The term ''ready'' is used to indicate that the cycle is terminated with RDY# or BRDY#.

This section and section 10, ''Bus Operation,'' describe bus cycles and data cycles. A bus cycle is at least two-clocks long and begins with ADS# active in the first clock and RDY# and/or BRDY# active in the last clock. Data is transferred to or from the Military Intel486 processor during a data cycle. A bus cycle contains one or more data cycles.

9.2 Signal Descriptions

9.2.1 CLOCK (CLK)

CLK provides the fundamental timing and the internal operating frequency for the Military Intel486 processor. All external timing parameters are specified with respect to the **rising edge** of CLK.

The Military Intel486 processor can operate over a wide frequency range, however the CLK frequency cannot change rapidly while RESET is inactive. The CLK frequency must be stable for proper chip operation because a single edge of CLK is used internally to generate two phases. CLK only needs TTL levels for proper operation. Figure 9-2 illustrates the CLK waveform.

9.2.2 INTELDX4 PROCESSOR CLOCK MULTIPLIER SELECTABLE INPUT (CLKMUL)

The IntelDX4 processor differs from the IntelDX2 processor in that it provides for two internal clock multiplier ratios: speed doubled mode and speed tripled mode. Speed doubled mode is identical to the IntelDX2 processor mode of operation where the internal core is operating at twice the external bus frequency. Selecting speed tripled mode causes the internal core frequency to operate at three times the external bus frequency. The IntelDX4 processor determines the desired clock multiplier ratio by sampling the status of the CLKMUL input during cold (power on) processor resets. **The clock multiplier ratio cannot be changed during warm resets. Also, SRESET cannot be used to select the clock multiplier ratio.**

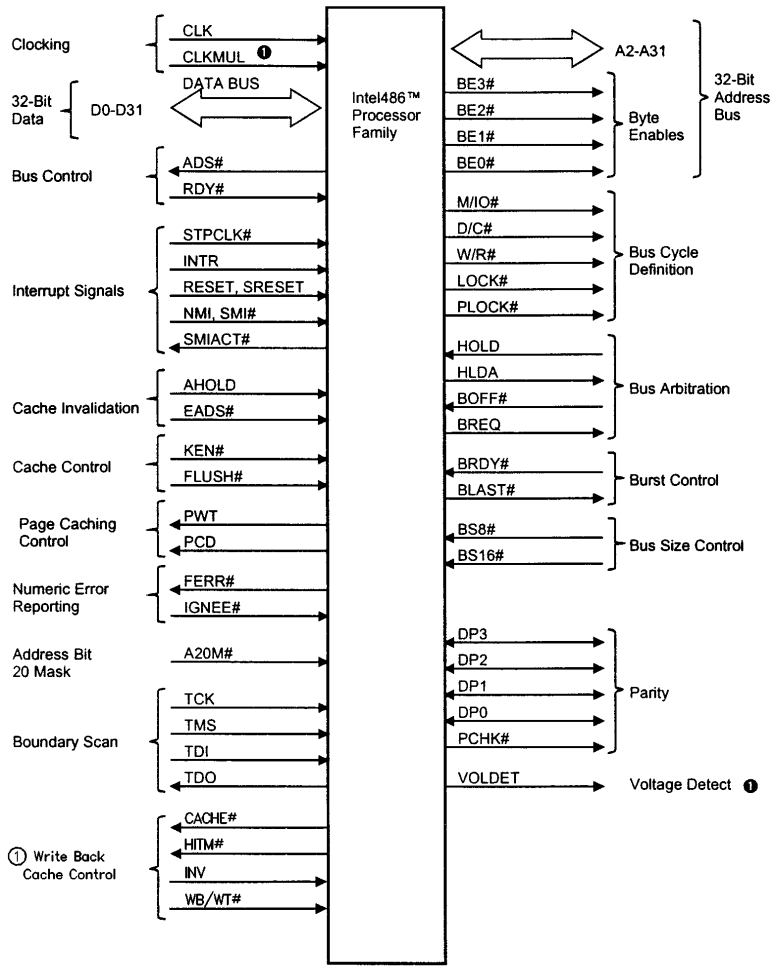
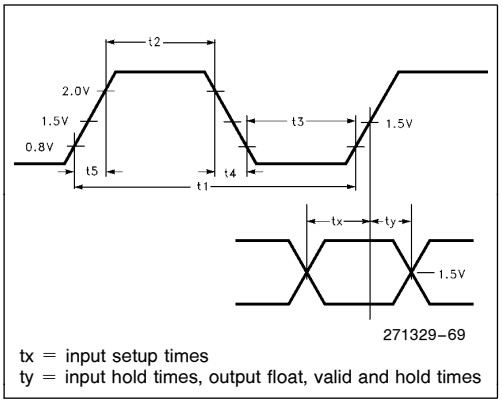


Figure 9-1. Functional Signal Groupings



tx = input setup times
ty = input hold times, output float, valid and hold times

Figure 9-2. CLK Waveform

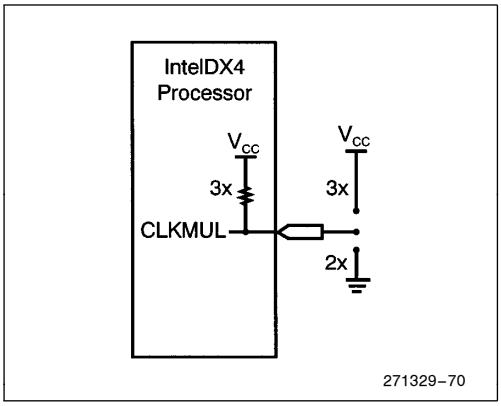


Figure 9-3. Voltage Detect (VOLDET) Sense Pin

To determine which clock multiplier is desired, the IntelDX4 processor samples the status of CLKMUL while RESET is active. If the CLKMUL input is driven low during RESET, the frequency of the core will be twice the external bus frequency (speed doubled mode). If driven high or left floating, speed tripled mode is selected. (See Table 9-1.) In order to allow maximum flexibility, CLKMUL can be jumper-configurable to either V_{CC} (speed tripled mode) or V_{SS} (speed doubled mode). (See Figure 9-3.)

Table 9-1. Clock Multiplier Selection

CLKMUL at RESET	Clock Multiplier	External Clock Freq. (MHz)	Internal Clock Freq. (MHz)
V_{CC} or Not Driven	3	25 33	75 100
V_{SS}	2	25 33	50 66

The clock multiplier selection method is fully backward compatible with Military Intel486 processor-based system designs. The CLKMUL signal occupies a pin which is labeled as an 'INC' on other Military Intel486 processors. Therefore, this pin is not driven in other Military Intel486 processor system designs. The IntelDX4 processor contains an internal pull-up resistor on the CLKMUL signal. As shown in Table 9-1, when CLKMUL is not driven, the internal core frequency defaults to speed tripled mode.

The internal pull-up resistor on the CLKMUL pin is disabled while the IntelDX4 processor is in the Stop Grant or Stop Clock modes. This prevents a low level DC current path from drawing current while in the Stop Grant or Stop Clock states on a system with CLKMUL connected to V_{SS}.

9.2.3 ADDRESS BUS (A31–A2, BE0#–BE3#)

A31–A2 and BE0#–BE3# form the address bus and provide physical memory and I/O port addresses. The Military Intel486 processor is capable of addressing 4 gigabytes of physical memory space (00000000H through FFFFFFFFH), and 64 Kbytes of I/O address space (00000000H through 0000FFFFH). A31–A2 identify addresses to a 4-byte location. BE0#–BE3# identify which bytes within the 4-byte location are involved in the current transfer.

Addresses are driven back into the Military Intel486 processor over A31–A4 during cache line invalidations. The address lines are active HIGH. When used as inputs into the processor, A31–A4 must meet the setup and hold times, t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.

The byte enable outputs, BE0#–BE3#, determine which bytes must be driven valid for read and write cycles to external memory.

- BE3# applies to D24–D31
- BE2# applies to D16–D23
- BE1# applies to D8–D15
- BE0# applies to D0–D7

BE0#–BE3# can be decoded to generate A0, A1 and BHE# signals used in 8- and 16-bit systems (see Table 10-5). BE0#–BE3# are active LOW and are not driven during bus hold.

9.2.4 DATA LINES (D31–D0)

The bidirectional lines, D31–D0, form the data bus for the Military Intel486 processor D0–D7 define the least significant byte and D24–D31 the most significant byte. Data transfers to 8- or 16-bit devices are possible using the data bus sizing feature controlled by the BS8# or BS16# input pins. D31–D0 are active HIGH. For reads, D31–D0 must meet the setup and hold times, t_{22} and t_{23}. D31–D0 are not driven during read cycles and bus hold.

9.2.5 PARITY

Data Parity Input/Outputs (DP0–DP3)

DP0–DP3 are the data parity pins for the processor. There is one pin for each byte of the data bus. Even parity is generated or checked by the parity generators/checkers. Even parity means that there are an even number of HIGH inputs on the eight corresponding data bus pins and parity pin.

Data parity is generated on all write data cycles with the same timing as the data driven by the Military Intel486 processor. Even parity information must be driven back to the Military Intel486 processor on these pins with the same timing as read information to insure that the correct parity check status is indicated by the Military Intel486 processor.

The values read on these pins do not affect program execution. It is the responsibility of the system to take appropriate actions if a parity error occurs.

Input signals on DP0–DP3 must meet setup and hold times t_{22} and t_{23} for proper operation.

Parity Status Output (PCHK#)

Parity status is driven on the PCHK# pin, and a parity error is indicated by this pin being LOW. PCHK# is driven the clock after ready for read operations to indicate the parity status for the data sampled at the end of the previous clock. Parity is checked during code reads, memory reads and I/O reads. Parity is not checked during interrupt acknowledge cycles. PCHK# only checks the parity status for enabled bytes as indicated by the byte enable and bus size signals. It is valid only in the clock immediately after read data is returned to the Military Intel486 processor. At all other times it is inactive (HIGH). PCHK# is never floated.

Driving PCHK# is the only effect that bad input parity has on the Military Intel486 processor. The Military Intel486 processor will not vector to a bus error interrupt when bad data parity is returned. In systems that will not employ parity, PCHK# can be ignored. In systems not using parity, DP0–DP3 should be connected to V_{CC} through a pull-up resistor.

9.2.6 BUS CYCLE DEFINITION

M/IO#, D/C#, W/R# Outputs

M/IO#, D/C# and W/R# are the primary bus cycle definition signals. They are driven valid as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles, D/C# distinguishes between data and control cycles and W/R# distinguishes between write and read cycles.

Bus cycle definitions as a function of M/IO#, D/C# and W/R# are given in Table 9-2. Note there is a difference between the Military Intel486 processor and Intel386™ processor bus cycle definitions. The halt bus cycle type has been moved to location 001 in the Military Intel486 processor from location 101 in the Intel386 processor. Location 101 is now reserved and will never be generated by the Military Intel486 processor.

Special bus cycles are discussed in section 10.2.11, ‘‘Special Bus Cycles’’.

Table 9-2. ADS# Initiated Bus Cycle Definitions

M/IO#	D/C#	W/R#	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

Bus Lock Output (LOCK#)

LOCK# indicates that the Military Intel486 processor is running a read-modify-write cycle where the external bus must not be relinquished between the read and write cycles. Read-modify-write cycles are used to implement memory-based semaphores. Multiple reads or writes can be locked.

When LOCK# is asserted, the current bus cycle is locked and the Military Intel486 processor should be allowed exclusive access to the system bus. LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after ready is returned indicating the last locked bus cycle.

The Military Intel486 processor will not acknowledge bus hold when LOCK# is asserted (though it will allow an address hold). LOCK# is active LOW and is floated during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active. Refer to section 10.2.6, ''Locked Cycles,'' for a detailed discussion of Locked bus cycles.

Pseudo-Lock Output (PLOCK#)

The pseudo-lock feature allows atomic reads and writes of memory operands greater than 32 bits. These operands require more than one cycle to transfer. The Military Intel486 processor asserts PLOCK# during segment table descriptor reads (64 bits) and cache line fills (128 bits).

When PLOCK# is asserted no other master will be given control of the bus between cycles. A bus hold request (HOLD) is not acknowledged during pseudo-locked reads and writes, with one exception. During non-cacheable non-bursted code prefetches, HOLD is recognized on memory cycle boundaries even though PLOCK# is asserted. The Military Intel486 processor will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether BRDY# or RDY# are returned.

A pseudo-locked transfer is meaningful only if the memory operand is aligned and if its completely contained within a single cache line.

Because PLOCK# is a function of the bus size and KEN# inputs, PLOCK# should be sampled only in the clock ready is returned. This pin is active LOW and is not driven during bus hold. Refer to section 10.2.7, ''Pseudo-Locked Cycles.''

9.2.6.1 PLOCK# Floating Point Considerations

For processors with an on-chip FPU, the following must be noted for PLOCK# operation. A 64-bit floating point number must be aligned to an 8-byte boundary to guarantee an atomic access. Normally PLOCK# and BLAST# are inverse of each other. However, during the first cycle of a 64-bit floating point write, both PLOCK# and BLAST# will be asserted. Military Intel486 processors with on-chip FPUs also assert PLOCK# during floating point long reads and writes (64 bits), segmentable description reads (64 bits) and code line fills (128 bits).

9.2.7 BUS CONTROL

The bus control signals allow the Military Intel486 processor to indicate when a bus cycle has begun, and allow other system hardware to control burst cycles, data bus width and bus cycle termination.

Address Status Output (ADS#)

The ADS# output indicates that the address and bus cycle definition signals are valid. This signal will go active in the first clock of a bus cycle and go inactive in the second and subsequent clocks of the cycle. ADS# is also inactive when the bus is idle.

ADS# is used by the external bus circuitry as the indication that the Military Intel486 processor has started a bus cycle. The external circuit must sample the bus cycle definition pins on the next rising edge of the clock after ADS# is driven active.

ADS# is active LOW and is not driven during bus hold.

Non-burst Ready Input (RDY#)

RDY# indicates that the current bus cycle is complete. In response to a read, RDY# indicates that the external system has presented valid data on the data pins. In response to a write request, RDY# indicates that the external system has accepted the Military Intel486 processor data. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. Because RDY# is sampled during address hold, data can be returned to the processor when AHOLD is active.

RDY# is active LOW, and is not provided with an internal pull-up resistor. This input must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

9.2.8 BURST CONTROL

Burst Ready Input (BRDY#)

BRDY# performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Military Intel486 processor data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle.

During a burst cycle, BRDY# will be sampled each clock, and if active, the data presented on the data bus pins will be strobed into the Military Intel486 processor. ADS# is negated during the second through last data cycles in the burst, but address lines A2–A3 and byte enables will change to reflect the next data item expected by the Military Intel486 processor.

If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely aborted. An additional complete bus cycle will be initiated after an aborted burst cycle if the cache line fill was not complete. BRDY# is treated as a normal ready for the last data cycle in a burst transfer or for non-burstable cycles. Refer to section 10.2.2, ''Multiple and Burst Cycle Bus Transfers,'' for burst cycle timing.

BRDY# is active LOW and is provided with a small internal pull-up resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.

Burst Last Output (BLAST#)

BLAST# indicates that the next time BRDY# is returned it will be treated as a normal RDY#, terminating the line fill or other multiple-data-cycle transfer. BLAST# is active for all bus cycles regardless of whether they are cacheable or not. This pin is active LOW and is not driven during bus hold.

9.2.9 INTERRUPT SIGNALS

The interrupt signals can interrupt or suspend execution of the processor's current instruction stream.

Reset Input (RESET)

The RESET input must be used at power-up to initialize the processor. The Reset input forces the processor to begin execution at a known state. The processor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to ensure proper processor operation. However, for warm boot-ups RESET should remain active for at least 15 CLK periods. RESET is active HIGH. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

RESET will reset SMBASE to the default value of 30000H. If SMBASE relocation is not used, the RESET signal can be used as the only reset. (See section 8, ''System Management Mode Architecture.'')

The Military Intel486 processor will be placed in the Power Down Mode if UP# is sampled active at the falling edge of RESET.

Soft Reset Input (SRESET)

The SRESET (Soft RESET) input, has the same functions as RESET, but does not change the SMBASE, and UP# is not sampled on the falling edge of SRESET. If SMBASE relocation is used by the system, the soft resets should be handled using the SRESET input. The SRESET signal should not be used for the cold boot-up power-on reset.

The SRESET input pin is provided to save the status of SMBASE during Intel 286 processor-compatible mode change. SRESET leaves the location of

SMBASE intact while resetting other units, including the on-chip cache. For compatibility, the system should use SRESET to flush the on-chip cache. The FLUSH# input pin should be used to flush the on-chip cache. SRESET should not be used to initiate test modes.

System Management Interrupt Request Input (SMI#)

SMI# is the system management mode interrupt request signal. The SMI# request is acknowledged by the SMIACT# signal. After the SMI# interrupt is recognized, the SMI# signal will be masked internally until the RSM instruction is executed and the interrupt service routine is complete. SMI# is falling-edge sensitive after internal synchronization.

The SMI# input must be held inactive for at least four clocks after it is asserted to reset the edge triggered logic. SMI# is provided with a pull-up resistor to maintain compatibility with designs which do not use this feature. SMI# is an asynchronous signal, but setup and hold times, t_{20} and t_{21}, must be met in order to guarantee recognition on a specific clock.

System Management Mode Active Output (SMIACT#)

SMIACT# indicates that the processor is operating in System Management Mode. The processor asserts SMIACT# in response to an SMI interrupt request on the SMI# pin. SMIACT# is driven active after the processor has completed all pending write cycles (including emptying the write buffers), and before the first access to SMRAM when the processor saves (writes) its state (or context) to SMRAM. SMIACT# remains active until the last access to SMRAM when the processor restores (reads) its state from SMRAM. The SMIACT# signal does not float in response to HOLD. The SMIACT# signal is used by the system logic to decode SMRAM.

Maskable Interrupt Request Input (INTR)

INTR indicates that an external interrupt has been generated. Interrupt processing is initiated if the IF flag is active in the EFLAGS register.

The Military Intel486 processor will generate two locked interrupt acknowledge bus cycles in response to asserting the INTR pin. An 8-bit interrupt number will be latched from an external interrupt controller at the end of the second interrupt acknowledge cycle. INTR must remain active until the interrupt acknowledges have been performed to assure program interruption. Refer to section 10.2.10, ''Interrupt Acknowledge,'' for a detailed discussion of interrupt acknowledge cycles.

The INTR pin is active HIGH and is not provided with an internal pull-down resistor. INTR is asynchronous, but the INTR setup and hold times, t_{20} and t_{21}, must be met to assure recognition on any specific clock.

Non-maskable Interrupt Request Input (NMI)

NMI is the non-maskable interrupt request signal. Asserting NMI causes an interrupt with an internally supplied vector value of 2. External interrupt acknowledge cycles are not generated because the NMI interrupt vector is internally generated. When NMI processing begins, the NMI signal will be masked internally until the IRET instruction is executed.

NMI is rising edge sensitive after internal synchronization. NMI must be held LOW for at least four CLK periods before this rising edge for proper operation. NMI is not provided with an internal pull-down resistor. NMI is asynchronous but setup and hold times, t_{20} and t_{21} must be met to assure recognition on any specific clock.

Stop Clock Interrupt Request Input (STPCLK#)

The Military Intel486 processor provides an interrupt mechanism, STPCLK#, that allows system hardware to control the power consumption of the processor by stopping the internal clock (output of the PLL) to the processor core in a controlled manner. This low-power state is called the Stop Grant state. In addition, the STPCLK# interrupt allows the system to change the input frequency within the specified range or completely stop the CLK input frequency (input to the PLL). If the CLK input is completely stopped, the processor enters into the Stop Clock state–the lowest power state. If the frequency is changed or stopped, the Military Intel486 processor will not return to the Stop Grant state until the CLK input has been running at a constant frequency for the time period necessary to stabilize the PLL (minimum of 1 ms).

The Military Intel486 processor will generate a Stop Grant bus cycle in response to the STPCLK#

interrupt request. STPCLK# is active LOW and is provided with an internal pull-up resistor. STPCLK# is an asynchronous signal, but must remain active until the processor issues the Stop Grant bus cycle. (Refer to section 10.2.11.3, ''Stop Grant Indication Cycle.'')

9.2.10 BUS ARBITRATION SIGNALS

This section describes the mechanism by which the processor relinquishes control of its local bus when requested by another bus master.

Bus Request Output (BREQ)

The Military Intel486 processor asserts BREQ whenever a bus cycle is pending internally. Thus, BREQ is always asserted in the first clock of a bus cycle, along with ADS#. Furthermore, if the Military Intel486 processor is currently not driving the bus (due to HOLD, AHOLD, or BOFF#), BREQ is asserted in the same clock that ADS# would have been asserted if the Military Intel486 processor were driving the bus. After the first clock of the bus cycle, BREQ may change state. It will be asserted if additional cycles are necessary to complete a transfer (via BS8#, BS16#, KEN#), or if more cycles are pending internally. However, if no additional cycles are necessary to complete the current transfer, BREQ can be negated before ready comes back for the current cycle. External logic can use the BREQ signal to arbitrate among multiple processors. This pin is driven regardless of the state of bus hold or address hold. BREQ is active HIGH and is never floated. During a hold state, internal events may cause BREQ to be de-asserted prior to any bus cycles.

Bus Hold Request Input (HOLD)

HOLD allows another bus master complete control of the Military Intel486 processor bus. The Military Intel486 processor will respond to an active HOLD signal by asserting HLDA and placing most of its output and input/output pins in a high impedance state (floated) after completing its current bus cycle, burst cycle, or sequence of locked cycles. In addition, if the Military Intel486 processor receives a HOLD request while performing a code fetch, and that cycle is backed off (BOFF#), the Military Intel486 processor will recognize HOLD before restarting the cycle. The code fetch can be non-cacheable or cacheable and non-bursted or bursted. The BREQ, HLDA, PCHK# and FERR# pins are not floated during bus hold. The Military Intel486 processor will maintain its bus in this state until the HOLD is de-asserted. Refer to section 10.2.9, ''Bus Hold,'' for timing diagrams for bus hold cycles and HOLD request acknowledge during BOFF#.

Unlike the Intel386 processor, the Military Intel486 processor will recognize HOLD during reset. Pull-up resistors are not provided for the outputs that are floated in response to HOLD. HOLD is active HIGH and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper chip operation.

Bus Hold Acknowledge Output (HLDA)

HLDA indicates that the Military Intel486 processor has given the bus to another local bus master. HLDA goes active in response to a hold request presented on the HOLD pin. HLDA is driven active in the same clock that the Military Intel486 processor floats its bus.

HLDA will be driven inactive when leaving bus hold and the Military Intel486 processor will resume driving the bus. The Military Intel486 processor will not cease internal activity during bus hold because the internal cache will satisfy the majority of bus requests. HLDA is active HIGH and remains driven during bus hold.

Backoff Input (BOFF#)

Asserting the BOFF# input forces the Military Intel486 processor to release control of its bus in the next clock. The pins floated are exactly the same as in response to HOLD. The response to BOFF# differs from the response to HOLD in two ways: First, the bus is floated immediately in response to BOFF# while the Military Intel486 processor completes the current bus cycle before floating its bus in response to HOLD. Second the Military Intel486 processor does not assert HLDA in response to BOFF#.

The Military Intel486 processor remains in bus hold until BOFF# is negated. Upon negation, the Military Intel486 processor restarts the bus cycle aborted when BOFF# was asserted. To the internal execution engine the effect of BOFF# is the same as inserting a few wait states to the original cycle. Refer to section 10.2.12, ''Bus Cycle Restart,'' for a description of bus cycle restart.

Any data returned to the Military Intel486 processor while BOFF# is asserted is ignored. BOFF# has higher priority than RDY# or BRDY#. If both BOFF# and ready are returned in the same clock, BOFF# takes effect. If BOFF# is asserted while the bus is idle, the Military Intel486 processor will float its bus in the next clock. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper chip operation.

9.2.11 CACHE INVALIDATION

The AHOLD and EADS# inputs are used during cache invalidation cycles. AHOLD conditions the Military Intel486 processor address lines, A4–A31, to accept an address input. EADS# indicates that an external address is actually valid on the address inputs. Activating EADS# will cause the Military Intel486 processor to read the external address bus and perform an internal cache invalidation cycle to the address indicated. Refer to section 10.2.8, ''Invalidate Cycle,'' or cache invalidation cycle timing.

Address Hold Request Input (AHOLD)

AHOLD is the address hold request. It allows another bus master access to the Military Intel486 processor address bus for performing an internal cache invalidation cycle. Asserting AHOLD will force the Military Intel486 processor to stop driving its address bus in the next clock. While AHOLD is active only the address bus will be floated, the remainder of the bus can remain active. For example, data can be returned for a previously specified bus cycle when AHOLD is active. The Military Intel486 processor will not initiate another bus cycle during address hold. Because the Military Intel486 processor floats its bus immediately in response to AHOLD, an address hold acknowledge is not required. If AHOLD is asserted while a bus cycle is in progress, and no readies are returned during the time AHOLD is asserted, the Military Intel486 processor will redrive the same address (that it originally sent out) once AHOLD is negated.

AHOLD is recognized during reset. Because the entire cache is invalidated by reset, any invalidation cycles run during reset will be unnecessary. AHOLD is active HIGH and is provided with a small internal pull-down resistor. It must satisfy the setup and hold times t_{18} and t_{19} for proper chip operation. AHOLD also determines whether or not the built in self test features of the Military Intel486 processor will be exercised on assertion of RESET. (See section 11.1, ''Built-In Self Test.'')

External Address Valid Input (EADS#)

EADS# indicates that a valid external address has been driven onto the Military Intel486 processor address pins. This address will be used to perform an internal cache invalidation cycle. The external address will be checked with the current cache contents. If the address specified matches any areas in the cache, that area will immediately be invalidated.

An invalidation cycle may be run by asserting EADS# regardless of the state of AHOLD, HOLD and BOFF#. EADS# is active LOW and is provided with an internal pull-up resistor. EADS# must satisfy the setup and hold times t_{12} and t_{13} for proper chip operation.

9.2.12 CACHE CONTROL

Cache Enable Input (KEN#)

KEN# is the cache enable pin. KEN# is used to determine whether the data being returned by the current cycle is cacheable. When KEN# is active and the Military Intel486 processor generates a cycle that can be cached (most any memory read cycle), the cycle will be transformed into a cache line fill cycle.

A cache line is 16 bytes long. During the first cycle of a cache line fill the byte-enable pins should be ignored and data should be returned as if all four byte enables were asserted. The Military Intel486 processor will run between 4 and 16 contiguous bus cycles to fill the line depending on the bus data width selected by BS8# and BS16#. Refer to section 10.2.3, ''Cacheable Cycles,'' for a description of cache line fill cycles.

The KEN# input is active LOW and is provided with a small internal pull-up resistor. It must satisfy the setup and hold times t_{14} and t_{15} for proper chip operation.

Cache Flush Input (FLUSH#)

The FLUSH# input forces the Military Intel486 processor to flush its entire internal cache. FLUSH# is active LOW and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition on any specific clock.

FLUSH# also determines whether or not the tri-state test mode of the Military Intel486 processor will be invoked on assertion of RESET. (See section 11.4, ''Tri-State Output Test Mode.'')

9.2.13 PAGE CACHEABILITY (PWT, PCD)

The PWT and PCD output signals correspond to two user attribute bits in the page table entry. When paging is enabled, PWT and PCD correspond to bits 3 and 4 of the page table entry respectively. For cycles that are not paged when paging is enabled (for example I/O cycles) PWT and PCD correspond to bits 3 and 4 in control register 3. When paging is disabled, the Military Intel486 processor ignores the PCD and PWT bits and assumes they are zero for the purpose of caching and driving PCD and PWT.

PCD is masked by the CD (cache disable) bit in control register 0 (CR0). When CD = 1 (cache line fills disabled) the Military Intel486 processor forces PCD HIGH. When CD = 0, PCD is driven with the value of the page table entry/directory.

The purpose of PCD is to provide a cacheable/non-cacheable indication on a page by page basis. The Military Intel486 processor will not perform a cache fill to any page in which bit 4 of the page table entry is set. PWT corresponds to the write-back bit and can be used by an external cache to provide this functionality. PCD and PWT bits are assigned to be zero during real mode or whenever paging is disabled. Refer to section 7.6, ''Page Cacheability,'' for a discussion of non-cacheable pages.

PCD and PWT have the same timing as the cycle definition pins (M/IO#, D/C#, W/R#). PCD and PWT are active HIGH and are not driven during bus hold.

9.2.14 NUMERIC ERROR REPORTING (FERR#, IGNNE#)

To allow PC-type floating point error reporting, Military Intel486 DX, IntelDX2, and IntelDX4 processors provide two pins, FERR# and IGNNE#.

Floating Point Error Output (FERR#)

The processor asserts FERR# whenever an unmasked floating point error is encountered. FERR# is similar to the ERROR# pin on the Intel387 math coprocessor. FERR# can be used by external logic for PC-type floating point error reporting in systems with a Military Intel486 DX, IntelDX2, or IntelDX4 processor. FERR# is active LOW and is not floated during bus hold.

In some cases, FERR# is asserted when the next floating point instruction is encountered. In other cases, it is asserted before the next floating point instruction is encountered, depending on the execution state of the instruction that caused the exception.

The following class of floating point exceptions drive FERR# at the time the exception occurs (i.e., before encountering the next floating point instruction):

1. The stack fault, invalid operation, and denormal exceptions on all transcendental instructions, integer arithmetic instructions, FSQRT, FSCALE, FPREM(1), FXTRACT, FBLD, and FBSTP.
2. Any exceptions on store instructions (including integer store instructions).

The following class of floating point exceptions drive FERR# only after encountering the next floating point instruction:

1. Exceptions other than on all transcendental instructions, integer arithmetic instructions, FSQRT, FSCALE, FPREM(1), FXTRACT, FBLD, and FBSTP.
2. Any exception on all basic arithmetic, load, compare, and control instructions (i.e., all other instructions).

Ignore Numeric Error Input (IGNNE#)

Military Intel486 DX, IntelDX2, and IntelDX4 processors will ignore a numeric error and continue executing non-control floating point instructions when IGNNE# is asserted, and FERR# is still activated. When de-asserted, the processor will freeze on a non-control floating point instruction if a previous instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set.

The IGNNE# input is active LOW and provided with a small internal pull-up resistor. This input is asynchronous, but must meet setup and hold times t_{20} and t_{21} to insure recognition on any specific clock.

9.2.15 BUS SIZE CONTROL (BS16#, BS8#)

The BS16# and BS8# inputs allow external 16- and 8-bit buses to be supported with a small number of external components. The Military Intel486 processor samples these pins every clock. The value sampled in the clock before ready determines the bus size. When asserting BS16# or BS8# only 16 or 8 bits of the data bus need be valid. If both BS16# and BS8# are asserted, an 8-bit bus width is selected.

When BS16# or BS8# are asserted, the Military Intel486 processor will convert a larger data request to the appropriate number of smaller transfers. The byte enables will also be modified appropriately for the bus size selected.

BS16# and BS8# are active LOW and are provided with small internal pull-up resistors. BS16# and BS8# must satisfy the setup and hold times t_{14} and t_{15} for proper chip operation.

9.2.16 ADDRESS BIT 20 MASK (A20M#)

Asserting the A20M# input causes the Military Intel486 processor to mask physical address bit 20 before performing a lookup in the internal cache and before driving a memory cycle to the outside world. When A20M# is asserted, the Military Intel486 processor emulates the 1-Mbyte address wraparound that occurs on the 8086. A20M# is active LOW and must be asserted only when the processor is in real mode. The A20M# is not defined in Protected Mode. A20M# is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For correct operation of the chip, A20M# should not be active at the falling edge of RESET.

A20M# exhibits a minimum 4 clock latency, from time of assertion to masking of the A20 bit. A20M# is ignored during cache invalidation cycles. I/O writes require A20M# to be asserted a minimum of 2 clocks prior to RDY being returned for the I/O write. This insures recognition of the address mask before the Military Intel486 processor begins execution of the instruction following OUT. If A20M# is asserted after the ADS# of a data cycle, the A20 address signal is not masked during this cycle but is masked in the next cycle. During a prefetch (cacheable or not), if A20M# is asserted after the first ADS#, A20 is not masked for the duration of the prefetch; even if BS16# or BS8# is asserted.

9.2.17 INTELDX4 PROCESSOR VOLTAGE DETECT SENSE OUTPUT (VOLDET)

A voltage detect sense pin (VOLDET) has been added to the IntelDX4 processor PGA package. This pin allows external system logic to distinguish between a 5V Military Intel486 DX or IntelDX2 processor and the 3.3V IntelDX4 processor. The pin passively indicates to external logic whether the installed PGA processor requires 5V (in the case of the Military Intel486 DX or IntelDX2 processor) or 3.3V (in the case of the IntelDX4 processor). Pin S4 has been defined as the VOLDET pin because this pin is defined as an NC pin on the Military Intel486 DX and IntelDX2 processor.

To utilize this feature, a weak, external pull-up resistor should be connected to the VOLDET pin. This pin samples high (logic 1) if the installed processor is a 5V Military Intel486 DX or IntelDX2 processor. This pin samples low (logic 0) if a IntelDX4 processor is installed. Upon sampling the logic level of this pin, external logic can then enable the proper V_{CC} level to the processor. In power sensitive applications, an active element is preferred for the pull-up device because it could be disabled after sampling, thereby eliminating the resulting DC current path when the installed processor is the IntelDX4 processor.

Figure 9-4 shows a logical representation of the Voltage Detect sense mechanism.

This pin can remain not connected for those system designs that do not wish to utilize this voltage detect feature.

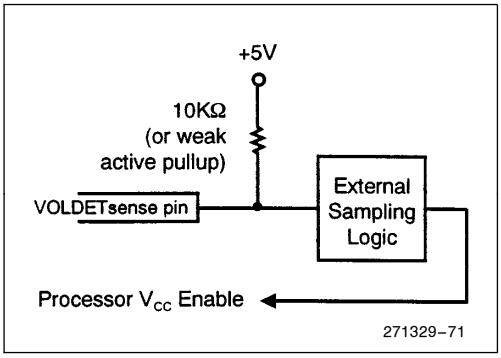


Figure 9-4. Voltage Detect (VOLDET) Sense Pin

9.2.18 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR SIGNALS AND OTHER ENHANCED BUS FEATURES

This section describes the pins that interface with the system to support the Enhanced Bus mode/ write-back features at system level.

9.2.18.1 Cacheability (CACHE#)

The CACHE# output indicates the internal cacheability on read cycles and a burst write-back on write cycles. CACHE# is asserted for cacheable reads, cacheable code fetches and write-backs. It is driven inactive for non-cacheable reads, special cycles, I/O cycles and write-through cycles. This is different from the PCD (page cache disable) pin. The operational differences between CACHE# and PCD are listed in Table 9-3. See Table 9-4 for operational differences between CACHE# and other Intel486 processor signals.

Table 9-3. Differences between CACHE# and PCD

Bus Operation	CACHE#	PCD
All reads (1)	same as PCD(3)	same as PCD(3)
Replacement write-back	low	low
Snoop-forced write-back	low	low
S-state write-through	high	same as PCD(3)
I-state write-through (2)	high	same as PCD(3)

NOTES:
1. Includes line fills and non-cacheable reads. During locked read cycles CACHE# is inactive. The non-cacheable reads may or may not be burst.
2. Due to the non-allocate on write policy, this includes both cacheable and non-cacheable writes. PCD will distinguish between the two, but CACHE# does not.
3. This behavior is the same as the existing specification of the Intel486 processor in write-through mode.

Table 9-4. CACHE# vs. Other Intel486™ Processor Signals

Pin Symbol	Relation To This Signal
ADS#	CACHE# is driven to valid state with ADS#
RDY#, BRDY#	CACHE# is de-asserted with the first RDY# or BRDY#
HLDA, BOFF#	CACHE# floats under these signals.
KEN#	The combination of CACHE# and KEN# determines if a read miss is converted into a cache line fill.

9.2.18.2 Cache Flush (FLUSH#)

FLUSH# is an existing pin that operates differently if the processor is configured as Enhanced Bus mode (write-back). In Enhanced Bus mode, it acts similar to the WBINVD instruction. In Enhanced Bus mode, FLUSH# is treated as an interrupt. It is sampled at each clock, but is recognized only on instruction boundary. Pending writes are completed before FLUSH# is serviced, and all prefetching is stopped. Depending on the number of modified lines in the cache, the flush could take up to a minimum of 1280 bus Clocks or 2560 processor clocks and a maximum of 5000+ bus clocks to scan the cache, perform the write backs, invalidate the cache and run two special cycles. After all modified lines are written back to memory, two special bus cycles, ''First Flush ACK Cycle'' and ''Second Flush ACK Cycle,'' are issued, in that order. These cycles differ from the special cycles issued after WBINVD only in that A2=1 (address line 2 = 1). SRESET, STPCLK#, INTR, NMI and SMI# are not recognized during a flush write-back, while BOFF#, AHOLD and HOLD are recognized.

FLUSH# may be asserted just for a single clock, or may be retained asserted, but should be de-asserted at or prior to the RDY# returned from the ''First Flush ACK'' special bus cycle. If asserted during INVD or WBINVD, FLUSH# will be recognized. If asserted simultaneously with SMI#, then SMI# is recognized after FLUSH# is serviced.

FLUSH# may be driven at any time. If driven during SRESET, it must be held for one clock after SRESET is de-asserted to be recognized.

9.2.18.3 Hit/Miss to a Modified Line (HITM#)

HITM# is a cache coherency protocol pin that is driven only in Enhanced Bus mode. When a snoop cycle is run by the system (with INV = ''0'' or INV = ''1''), HITM# indicates if the processor contains the snooped line in the M-state. Assertion of HITM# indicates that the line will be written back in total, unless the processor is already in the process of doing a replacement write-back of the same line.

HITM# will be valid on the bus two system clocks after EADS# is asserted on the bus. If asserted, HITM# remains asserted until the last RDY# or BRDY# of the snoop write-back cycle is returned. It will be de-asserted before the next following ADS#. (See Table 9-5.)

Table 9-5. HITM# vs. Other Intel486™ Processor Signals

Pin Symbol	Relation To This Signal
EADS#	HITM# is asserted due to an EADS#-driven snoop, provided the snooped line is in the M-state in the cache.
HLDA, BOFF#	HITM# does not float under these signals.
ADS#, CACHE#	The beginning of a snoop write-back cycle is identified by the assertion of ADS#, CACHE#, and HITM#.

9.2.18.4 Soft Reset (SRESET)

When in Enhanced Bus mode, SRESET has the following differences: SRESET, unlike RESET, does not cause AHOLD, A20M#, FLUSH#, UP#, and WB/WT# pins to be sampled (i.e., special test modes and on-chip cache configuration can not be accessed with SRESET).

On SRESET, the internal SMRAM base register retains its previous value and the processor does not flush, write-back or disable the internal cache. CR0.CD and CR0.NW retain previous values, CR0.4 is set to ''1'', and the remaining bits are cleared. Because SRESET is treated as an interrupt, it is possible to have a bus cycle while SRESET is asserted. A bus cycle could be due to an on-going instruction, emptying the write buffers of the processor, or snoop write-back cycles if there is a snoop hit to an M-state line while SRESET is asserted.

NOTE:
For both Standard Bus mode and Enhanced Bus mode:

- SMI# must be blocked during SRESET. It must also be blocked for a minimum of 2 clocks after SRESET is de-asserted.
- SRESET must be blocked during SMI#. It must also be blocked for a minimum of 20 clocks after SMIACT# is de-asserted.

9.2.18.5 Invalidation Request (INV)

INV is a cache coherency protocol pin that is used only in Enhanced Bus mode. It is sampled by the processor on EADS#-driven snoop cycles. **It is necessary to assert this pin to simulate the standard mode processor invalidate cycle on write-through-only lines.** INV also invalidates the write-back lines. However, if the snooped line is in the M-state, the line will be written back and then invalidated.

INV is sampled when EADS# is asserted. If INV is not asserted with EADS#, the snoop cycle will have no effect on a write-through-only line or a line allocated as write-back, but not yet modified. If the line is write-back and modified, it will be written back to memory, but will not be de-allocated (invalidated) from the internal cache. The address of the snooped cache line is provided on the address bus. (See Table 9-6.)

Table 9-6. INV vs. Other Intel486™ Processor Signals

Pin Symbol	Relation To This Signal
EADS#	EADS# determines when INV is sampled.
A31–A4	The address of the snooped cache line is provided on these pins.

9.2.18.6 Write-Back/Write-Through (WB/WT#)

WB/WT# enables Enhanced Bus mode (write-back cache). It also allows the system to define a cached line as write-through or write-back.

WB/WT# is sampled at the falling edge of RESET to determine if Enhanced Bus mode is enabled (WB/WT# must be driven for two clocks before and two clocks after RESET for recognition by the processor). If sampled low or floated, the Write-Back Enhanced Intel486 processors operate in the Intel486 processor standard mode. For write-through only operation, i.e. standard mode, WB/WT# does not need to be connected.

In Enhanced Bus mode, WB/WT# allows the system-hardware to force any allocated line to be treated as write-through or write-back. As with cacheability, both the processor and the external system must agree that a line may be treated as write-back for the internal cache to be allocated as write-back. The default is always write-through. **The processor's indication of write-back vs. write-through is from the PWT pin, in which function and timing are the same as in the standard mode Intel486 processor.**

To define write-back or write-through configuration of a line, WB/WT# is sampled in the same clock as the first RDY# or BRDY# is returned during a line fill (allocation) cycle. (See Table 9-7.)

Table 9-7. WB/WT# vs. Other Intel486™ Processor Signals

Pin Symbol	Relation to This Signal
RDY#, BRDY#	WB/WT# is sampled with the first RDY# or BRDY#.
PWT	The combination of WB/WT# and PWT determine if the Write-Back Enhanced IntelDX2™ processor will treat the line as WB.
PCD, CACHE#, KEN#	The state of WB/WT# does not matter if PCD, CACHE# or KEN# define the line to be non-cacheable.
W/R#	WB/WT# is significant only on read fill cycles.
RESET	WB/WT# is sampled on the falling edge of RESET to define the cache configuration.

9.2.18.7 Pseudo-Lock Output (PLOCK#)

In the Enhanced bus mode, PLOCK# is always driven inactive. In this mode, a 64-bit data read (caused by an FP operand access or a segment descriptor read) is treated as a multiple cycle read request, which may be a burst or a non-burst access based on whether BRDY# or RDY# is returned by the system. Because only write-back cycles (caused by Snoop write-back or replacement write-back) are burstable, a 64-bit write will be driven out as two non-burst bus cycles. BLAST# is asserted during both writes. Refer to section 10.2, ''Bus Functional Description'' for details on Pseudo-Locked bus cycles.

9.2.19 BOUNDARY SCAN TEST SIGNALS

Test Clock (TCK)

TCK is an input to the Military Intel486 processor and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the part on the falling edge of TCK on TDO.

In addition to using TCK as a free running clock, it may be stopped in a low, O, state, indefinitely as described in IEEE 1149.1. While TCK is stopped in the low state, the boundary scan latches retain their state.

When boundary scan is not used, TCK should be tied high or left as a NC. (This is important during power up to avoid the possibility of glitches on the TCK which could prematurely initiate boundary scan operations.) TCK is supplied with an internal pull-up resistor.

TCK is a clock signal and is used as a reference for sampling other JTAG signals. On the rising edge of TCK, TMS and TDI are sampled. On the falling edge of TCK, TDO is driven.

Test Mode Select (TMS)

TMS is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic, as described in section 11.5.4, ''Test Access Port Controller.''

To guarantee deterministic behavior of the TAP controller TMS is provided with an internal pull-up resistor. If boundary scan is not used, TMS may be tied high or left unconnected. TMS is sampled on the rising edge of TCK. TMS is used to select the internal TAP states required to load boundary scan instructions to data on TDI. For proper initialization of the JTAG logic, TMS should be driven high, ''1,'' for at least four TCK cycles following the rising edge of RESET.

Test Data Input (TDI)

TDI is the serial input used to shift JTAG instructions and data into the component. The shifting of instructions and data occurs during the SHIFT-IR and SHIFT-DR TAP controller states, respectively. These states are selected using the TMS signal as described in section 11.5.4, ''Test Access Port Controller.''

An internal pull-up resistor is provided on TDI to ensure a known logic state if an open circuit occurs on the TDI path. Note that when ''1'' is continuously shifted into the instruction register, the BYPASS instruction is selected. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and the SHIFT-DR states. During all other TAP controller states, TDI is a ''don't care.'' TDI is only sampled

when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller. For proper initialization of JTAG logic, TDI should be driven high, ''1,'' for at least four TCK cycles following the rising edge of RESET.

Test Data Output (TDO)

TDO is the serial output used to shift JTAG instructions and data out of the component. The shifting of instructions and data occurs during the SHIFT-IR and SHIFT-DR TAP controller states, respectively. These states are selected using the TMS signal as described in section 11.5.4, ''Test Access Port Controller''. When not in SHIFT-IR or SHIFT-DR state, TDO is driven to a high impedance state to allow connecting TDO of different devices in parallel. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times TDO is driven to the high impedance state. TDO is only driven when TMS and TCK have been used to select the SHIFT-IR or SHIFT-DR states in the TAP controller.

9.3 Interrupt and Non-Maskable Interrupt Interface

The Military Intel486 processor provides four asynchronous interrupt inputs: INTR (interrupt request), NMI (non-maskable interrupt input), SMI# (system management interrupt) and STPCLK# (stop clock interrupt). This section describes the hardware interface between the instruction execution unit and the pins. For a description of the algorithmic response to interrupts refer to section 4.8, ''Interrupts''. For interrupt timings refer to section 10.2.10, ''Interrupt Acknowledge''.

9.3.1 INTERRUPT LOGIC

The Military Intel486 processor contains a two-clock synchronizer on the interrupt line. An interrupt request will reach the internal instruction execution unit two clocks after the INTR pin is asserted, if proper setup is provided to the first stage of the synchronizer.

There is no special logic in the interrupt path other than the synchronizer. The INTR signal is level sensitive and must remain active for the instruction execution unit to recognize it. The interrupt will not be serviced by the Military Intel486 processor if the INTR signal does not remain active.

The instruction execution unit will look at the state of the synchronized interrupt signal at specific clocks during the execution of instructions (if interrupts are enabled). These specific clocks are at instruction boundaries, or iteration boundaries in the case of string move instructions. Interrupts will only be accepted at these boundaries.

An interrupt must be presented to the Military Intel486 processor INTR pin three clocks before the end of an instruction for the interrupt to be acknowledged. Presenting the interrupt 3 clocks before the end of an instruction allows the interrupt to pass through the two clock synchronizer leaving one clock to prevent the initiation of the next sequential instruction and to begin interrupt service. If the interrupt is not received in time to prevent the next instruction, it will be accepted at the end of next instruction, assuming INTR is still held active.

The longest latency between when an interrupt request is presented on the INTR pin and when the interrupt service begins is: longest instruction used + the two clocks for synchronization + one clock required to vector into the interrupt service microcode.

9.3.2 NMI LOGIC

The NMI pin has a synchronizer like that used on the INTR line. Other than the synchronizer, the NMI logic is different from that of the maskable interrupt.

NMI is edge triggered as opposed to the level triggered INTR signal. The rising edge of the NMI signal is used to generate the interrupt request. The NMI input need not remain active until the interrupt is actually serviced. The NMI pin only needs to remain active for a single clock if the required setup and hold times are met. NMI will operate properly if it is held active for an arbitrary number of clocks.

The NMI input must be held inactive for at least four clocks after it is asserted to reset the edge triggered logic. A subsequent NMI may not be generated if the NMI is not held inactive for at least four clocks after being asserted.

The NMI input is internally masked whenever the NMI routine is entered. The NMI input will remain masked until an IRET (return from interrupt) instruction is executed. Masking the NMI signal prevents recursive NMI calls. If another NMI occurs while the NMI is masked off, the pending NMI will be executed after the current NMI is done. Only one NMI can be pending while NMI is masked.

9.3.3 SMI# LOGIC

SMI# is edge triggered like NMI, but the interrupt request is generated on the falling-edge. SMI# is an asynchronous signal, but setup and hold times, t_{20} and t_{21}, must be met in order to guarantee recognition on a specific clock. The SMI# input need not remain active until the interrupt is actually serviced. The SMI# input only needs to remain active for a single clock if the required setup and hold times are met. SMI# will also work correctly if it is held active for an arbitrary number of clocks.

The SMI# input must be held inactive for at least four clocks after it is asserted to reset the edge triggered logic. A subsequent SMI# might not be recognized if the SMI# input is not held inactive for at least four clocks after being asserted.

SMI#, like NMI, is not affected by the IF bit in the EFLAGS register and is recognized on an instruction boundary. An SMI# will not break locked bus cycles.

The SMI# has a higher priority than NMI and is not masked during an NMI.

After the SMI# interrupt is recognized, the SMI# signal will be masked internally until the RSM instruction is executed and the interrupt service routine is complete. Masking the SMI# prevents recursive SMI# calls. The SMI# input must be de-asserted for at least 4 clocks to reset the edge triggered logic. If another SMI# occurs while the SMI# is masked, the pending SMI# will be recognized and executed on the next instruction boundary after the current SMI# completes. This instruction boundary occurs before execution of the next instruction in the interrupted application code, resulting in back to back SMM handlers. Only one SMI# can be pending while SMI# is masked.

The SMI# signal is synchronized internally and should be asserted at least three (3) CLK periods prior to asserting the RDY# signal in order to guarantee recognition on a specific instruction boundary. This is important for servicing an I/O trap with an SMI# handler.

9.3.4 STPCLK# LOGIC

STPCLK# is level triggered and active LOW. STPCLK# is an asynchronous signal, but must remain active until the processor issues the Stop Grant bus cycle. STPCLK# may be de-asserted at any time after the processor has issued the Stop Grant bus cycle. When the processor enters the Stop Grant state, the internal pull-up resistor of STPCLK#, CLKMUL (for IntelDX4 processor), and UP# are disabled so that the processor power consumption is reduced. The STPCLK# input must be driven high (not floated) in order to exit the Stop Grant state. **STPCLK# must be de-asserted for a minimum of 5 clocks after RDY# or BRDY# is returned active for the Stop Grant Bus Cycle before being asserted again.**

When the processor recognizes a STPCLK# interrupt, the processor will stop execution on the next instruction boundary (unless superseded by a higher priority interrupt), stop the pre-fetch unit, empty all internal pipelines and the write buffers, generate a Stop Grant bus cycle, and then stop the internal clock. At this point the processor is in the Stop Grant state.

The processor cannot respond to a STPCLK# request from an HLDA state because it cannot empty the write buffers and, therefore, cannot generate a Stop Grant cycle.

The rising edge of STPCLK# will tell the processor that it can return to program execution at the instruction following the interrupted instruction.

Unlike the normal interrupts, INTR and NMI, the STPCLK# interrupt does not initiate acknowledge cycles or interrupt table reads. Among external interrupts, the STPCLK# order of priority is shown in section 4.8.

9.4 Write Buffers

The Military Intel486 processor contains four write buffers to enhance the performance of consecutive writes to memory. The buffers can be filled at a rate of one write per clock until all four buffers are filled.

When all four buffers are empty and the bus is idle, a write request will propagate directly to the external bus bypassing the write buffers. If the bus is not available at the time the write is generated internally, the write will be placed in the write buffers and propagate to the bus as soon as the bus becomes available. The write is stored in the on-chip cache immediately if the write is a cache hit.

Writes will be driven onto the external bus in the same order in which they are received by the write buffers. Under certain conditions a memory read will go onto the external bus before the memory writes pending in the buffer even though the writes occurred earlier in the program execution.

A memory read will only be reordered in front of all writes in the buffers under the following conditions: If all writes pending in the buffers are cache hits and the read is a cache miss. Under these conditions the Military Intel486 processor will not read from an external memory location that needs to be updated by one of the pending writes.

Reordering of a read with the writes pending in the buffers can only occur once before all the buffers are emptied. Reordering read once only maintains cache consistency. Consider the following example: The processor writes to location X. Location X is in the internal cache, so it is updated there immediately. However, the bus is busy so the write out to main memory is buffered (see Figure 9-5). At this point, any reads to location X would be cache hits and most up-to-date data would be read.

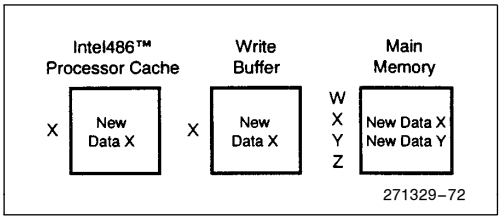


Figure 9-5. Reordering of a Reads with Write Buffers

The next instruction causes a read to location Y. Location Y is not in the cache (a cache miss). Because the write in the write buffer is a cache hit, the read is reordered. When location Y is read, it is put into the cache. The possibility exists that location Y will replace location X in the cache. If this is true, location X would no longer be cached (see Figure 9-6).

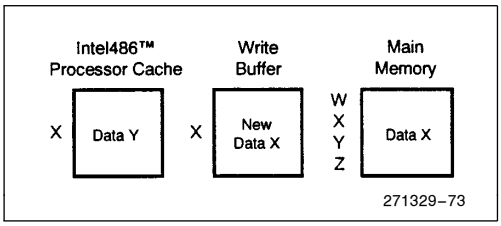


Figure 9-6. Reordering of a Reads with Write Buffers

Cache consistency has been maintained up to this point. If a subsequent read is to location X (now a cache miss) and it was reordered in front of the buffered write to location X, stale data would be read. This is why only 1 read is allowed to be reordered. Once a read is reordered, all the writes in the write buffer are flagged as cache misses to ensure that no more reads are reordered. Because one of the conditions to reorder a read is that all writes in the write buffer must be cache hits, no more reordering is allowed until all of those flagged writes propagate to the bus. Similarly, if an invalidation cycle is run all entries in the write buffer are flagged as cache misses.

For multiple processor systems and/or systems using DMA techniques, such as bus snooping, locked semaphores should be used to maintain cache consistency.

9.4.1 WRITE BUFFERS AND I/O CYCLES

Input/Output (I/O) cycles must be handled in a different manner by the write buffers.

I/O reads are never reordered in front of buffered memory writes. This insures that the Military Intel486 processor will update all memory locations before reading status from an I/O device.

The Military Intel486 processor never buffers single I/O writes. When processing an OUT instruction, internal execution stops until the I/O write actually completes on the external bus. This allows time for the external system to drive an invalidate into the Military Intel486 processor or to mask interrupts before the processor progresses to the instruction following OUT. REP OUTS instructions will be buffered.

A read cycle must be explicitly generated to a non-cacheable location in memory to guarantee that a read bus cycle is performed. This read will not be allowed to proceed to the bus until after the I/O write has completed because I/O writes are not buffered. The I/O device will have time to recover to accept another write during the read cycle.

9.4.2 WRITE BUFFERS IMPLICATIONS ON LOCKED BUS CYCLES

Locked bus cycles are used for read-modify-write accesses to memory. During a read-modify-write access, a memory base variable is read, modified and then written back to the same memory location. It is important that no other bus cycles, generated by other bus masters or by the Military Intel486 processor itself, be allowed on the external bus between the read and write portion of the locked sequence.

During a locked read cycle, the Military Intel486 processor will always access external memory, it will never look for the location in the on-chip cache, but for write cycles, data is written in the internal cache (if cache hit) and in the external memory. All data pending in the Military Intel486 processor's write buffers will be written to memory before a locked cycle is allowed to proceed to the external bus.

The Military Intel486 processor will assert the LOCK# pin after the write buffers are emptied during a locked bus cycle. With the LOCK# pin asserted, the processor will read the data, operate on the data and place the results in a write buffer. The contents of the write buffer will then be written to external memory. LOCK# will become inactive after the write part of the locked cycle.

9.5 Reset and Initialization

The Military Intel486 processor has a built in self test (BIST) that can be run during reset. BIST is invoked if the AHOLD pin is asserted for 1 clock before and 1 clock after RESET is de-asserted. RESET must be active for 15 clocks with or without BIST being enabled. To ensure proper results, neither FLUSH# nor SRESET can be asserted while BIST is executing. Refer to section 11.0, ''Testability,'' for information on Military Intel486 processor testability.

The Military Intel486 processor registers have the values shown in Table 9-3 after RESET is performed. The EAX register contains information on the success or failure of the BIST if the self test is executed. The DX register always contains a component identifier at the conclusion of RESET. The upper byte of DX (DH) will contain 04 and the lower byte (DL) will contain the revision identifier. (See Table 9-4.)

RESET forces the Military Intel486 processor to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active.

All entries in the cache are invalidated by RESET.

9.5.1 FLOATING POINT REGISTER VALUES

In addition to the register values listed above, Military Intel486 DX, IntelDX2, and IntelDX4 processors have the floating point register values shown in Table 9-5.

The floating point registers are initialized as if the FINIT/FNINIT (initialize processor) instruction was executed if the BIST was performed. If the BIST is not executed, the floating point registers are unchanged.

The Military Intel486 processor will start executing instructions at location FFFFFFF0H after RESET. When the first Inter Segment Jump or Call is executed, address lines A20–A31 will drop LOW for CS-relative memory cycles, and the Military Intel486 processor will only execute instructions in the lower one Mbyte of physical memory. This allows the system designer to use a ROM at the top of physical memory to initialize the system and take care of RESETs.

Table 9-3. Register Values after Reset

Register	Initial Value (BIST)	Initial Value (No BIST)
EAX	Zero (Pass)	Undefined
ECX	Undefined	Undefined
EDX	0400 + Revision ID	0400 + Revision ID
EBX	Undefined	Undefined
ESP	Undefined	Undefined
EBP	Undefined	Undefined
ESI	Undefined	Undefined
EDI	Undefined	Undefined
EFLAGS	00000002h	00000002h
EIP	0FFF0h	0FFF0h
ES	0000h	0000h
CS	F000h*	F000h*
SS	0000h	0000h
DS	0000h	0000h
FS	0000h	0000h
GS	0000h	0000h
IDTR	Base = 0, Limit = 3FFh	Base = 0, Limit = 3FFh
CR0	60000010h	60000010h
DR7	00000000h	00000000h

Table 9-4. Military Intel486™ Processor Revision ID

Product	Component ID (DH)	Revision ID (DL)
Military Intel486™ DX Processor	04	0x 1x
IntelDX2™ Processor	04	3x
IntelDX4™ Processor	04	9x

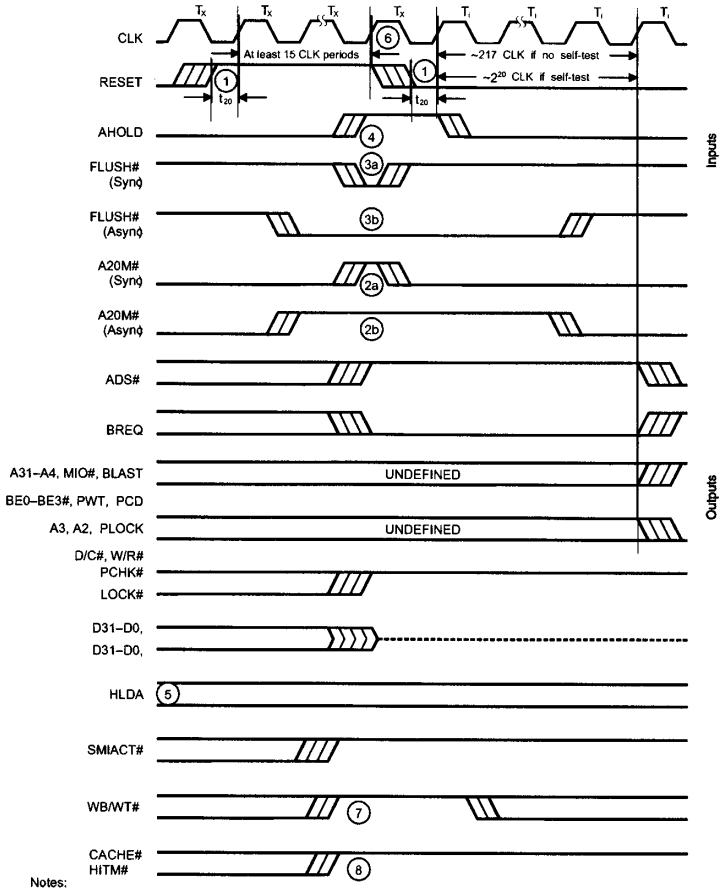
Table 9-5. Floating Point Values after Reset

Register	Initial Value (BIST)	Initial Value (No BIST)
CW	037Fh	Unchanged
SW	0000h	Unchanged
TW	FFFFh	Unchanged
FIP	00000000h	Unchanged
FEA	00000000h	Unchanged
FCS	0000h	Unchanged
FDS	0000h	Unchanged
FOP	000h	Unchanged
FSTACK	Undefined	Unchanged

9.5.2 PIN STATE DURING RESET

The Military Intel486 processor recognizes and can respond to HOLD, AHOLD, and BOFF# requests regardless of the state of RESET. Thus, even though the processor is in reset, it can still float its bus in response to any of these requests.

While in reset, the Military Intel486 processor bus is in the state shown in Figure 9-7 if the HOLD, AHOLD and BOFF# requests are inactive. The figure shows the bus state for the Military Intel486 processor. Note that the address (A31–A2, BE3#–BE0#) and cycle definition (M/IO#, D/C#, W/R#) pins are undefined from the time reset is asserted up to the start of the first bus cycle. All undefined pins **(except FERR#)** assume known values at the beginning of the first bus cycle. The first bus cycle is always a code fetch to address FFFFFFF0H.



Notes:

1. RESET is an asynchronous input. t_{20} must be met only to guarantee recognition on a specific clock edge.

2a. When A20M# is driven synchronously, it must be driven high (inactive) for the CLK edge prior to the falling edge of RESET to ensure proper operation. A20M# setup and hold times must be met.

2b. When A20M# is driven asynchronously, it should be driven low (active) for two CLKs prior to and two CLKs after the falling edge of RESET to ensure proper operation.

3a. When FLUSH# is driven synchronously, it must be driven low (high) for the CLK edge prior to the falling edge of RESET to invoke the 3-state Output Test Mode. All outputs are guaranteed 3-stated within 10 CLKs of RESETR being deasserted. FLUSH# setup and hold times must be met.

3b. When FLUSH# is driven asynchronously, it must be driven low (active) for two CLKs period prior to and two CLKs after the falling edge of RESET to invoke the 3-state Output Test Mode. All outputs are guaranteed 3-stated within 10 CLKs of RESET being deasserted.

4. AHOLD should be driven high (active) for the CLK edge prior to the falling edge of RESET to invoke the Built-In-Self-Test (BIST). AHOLD setup and hold times must be met.

5. Hold is recognized normally during RESET. On power-up HLDA is indeterminate until RESET is recognized by the processor.

6. 15 CLKs RESET pulse width for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

7. WB/WT# should be driven high for at least one CLK before falling edge of RESET and at least one CLK after falling edge of RESET to enable the Enhanced Bus Mode. The Standard Bus Mode will be enabled if WB/WT# is sampled low or left floating at the falling edge of RESET.

8. The system may sample HITM# to detect the presence of the Enhanced Bus Mode. If HITM# is HIGH for one CLK after reset is inactive, the Enhanced Bus Mode is present.

271329–74

Figure 9-7. Pin States during RESET

9.5.2.1 Controlling the CLK Signal in the Processor during Power On

The power on requirements of the Military Intel486 processor with regards to allowable CLK input during the power on sequence have never been specified. Clocking the processor before Vcc has reached its normal operating level can cause unpredictable results on Military Intel486 processors. While Intel will maintain original clock and power specifications (none), this section reflects what Intel considers to be a good clock design.

Intel strongly recommends that system designers ensure that a clock signal is not presented to the Military Intel486 processor until Vcc has stabilized at its normal operating level. This design recommendation can easily be met by gating the clock signal with a POWERGOOD signal. The POWERGOOD signal should reflect the status of Vcc at the Military Intel486 processor (which may be different from the power supply status in designs that provide power to the processor through the use of a voltage regulator or converter).

Most clock synthesizers and some clock oscillators contain on-board gating logic. If external gating logic is implemented, it should be done on the original clock signal output from the clock oscillator/synthesizer. Gating the clock to the processor independently of the clock to the rest of the motherboard will cause clock skew, which may violate processor or chipset timing requirements. If the clock signal to the motherboard is enabled with a POWERGOOD signal, it is also important to verify that the motherboard logic does not require a clock input prior to this POWERGOOD signal. Some chipsets also gate the clock to the processor only after a POWERGOOD signal, which inherently meets the requirements of this design note. Designs should implement this design note, so as to maintain maximum flexibility with all Military Intel486 processor steppings.

9.5.2.2 FERR# Pin State During Reset for Military Intel486 DX, IntelDX2, and IntelDX4 Processors

FERR# reflects the state of the ES (error summary status) bit in the floating point unit status word. The ES bit is initialized whenever the floating point unit state is initialized. The floating point unit's status word register can be initialized by BIST or by executing FINIT/FNINIT instruction. Thus, after reset and before executing the first FINIT or FNINIT instruction, the values of the FERR# and the numeric status word register bits 0–7 depends on whether or not BIST is performed. Table 9-6 shows the state of FERR# signal after reset and before the execution of the FINIT/FNINIT instruction.

Table 9-6. FERR# Pin State after Reset and before FP Instructions

BIST Performed	FERR# Pin	FPU Status Word Register Bits 0–7
YES	Inactive (High)	Inactive (Low)
NO	Undefined (Low or High)	Undefined (Low or High)

After the first FINIT or FNINIT instruction, FERR# pin and the FPU status word register bits (07) will be inactive irrespective of the Built-In Self-Test (BIST).

9.6 Clock Control

The Military Intel486 processor provides an interrupt mechanism (STPCLK#) that allows system hardware to control the power consumption of the processor by stopping the internal clock (output of the PLL) to the processor core in a controlled manner. This low-power state is called the Stop Grant state. In addition, the STPCLK# interrupt allows the system to change the input frequency within the specified range or completely stop the CLK input frequency (input to the PLL). If the CLK input is completely stopped, the processor enters into the Stop Clock statethe lowest power state.

There are two targets for the low-power mode supply current:

- ~20–100 mA in the **Stop Grant state** (fast wake-up, frequency-and voltage-dependent), and
- ~100–1000 μA in the full **Stop Clock state** (slow wake-up, voltage-dependent).

See section 9.6.3.2 and 9.6.3.3, for a detailed description of the Stop Grant and Stop Clock states.

9.6.1 STOP GRANT BUS CYCLE

A special Stop Grant bus cycle will be driven to the bus after the processor recognizes the STPCLK# interrupt. The definition of this bus cycle is the same as the HALT cycle definition for the standard Military Intel486 processor, with the exception that the Stop Grant bus cycle drives the value 0000 0010H on the address pins. The system hardware must acknowledge this cycle by returning RDY# or BRDY#. **The processor will not enter the Stop Grant state until either RDY# or BRDY# has been returned.**

The Stop Grant bus cycle is defined as follows:

M/IO# = 0, D/C# = 0, W/R# = 1, Address Bus = 0000 0010H (A_4 = 1), BE3#–BE0# = 1011, Data bus = undefined

The latency between a STPCLK# request and the Stop Grant bus cycle is dependent on the current instruction, the amount of data in the processor write buffers, and the system memory performance. (See Figure 9-8.)

9.6.2 PIN STATE DURING STOP GRANT

During the Stop Grant state, most output and input/output signals of the processor will maintain their previous condition (the level they held when entering the Stop Grant state). The data and data parity signals will be tri-stated. In response to HOLD being driven active during the Stop Grant state (when the CLK input is running), the processor will generate HLDA and tri-state all output and input/output signals that are tri-stated during the HOLD/HLDA state. After HOLD is de-asserted all signals will return to their prior state before the HOLD/HLDA sequence.

In order to achieve the lowest possible power consumption during the Stop Grant state, the system designer must ensure the input signals with pull-up resistors are not driven LOW and the input signals with pull-down resistors are not driven HIGH. (See Table 3-11 in the Quick Pin Reference section for signals with internal pull-up and pull-down resistors.)

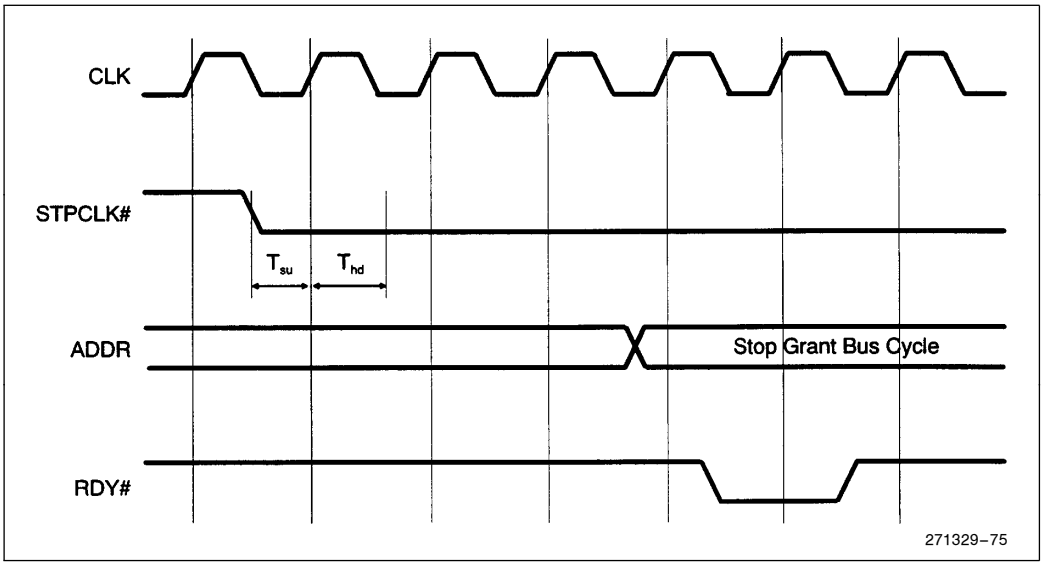


Figure 9-8. Stop Clock Protocol

All inputs, except the data bus pins must be driven to the power supply rails to ensure the lowest possible current consumption during Stop Grant or Stop Clock modes. For compatibility with future processors, data pins should be driven low to achieve the lowest possible power consumption. Pull-down resistors/bus keepers are needed to minimize leakage current.

If HOLD is asserted during the Stop Grant state, all pins that are normally floated during HLDA will still be floated by the processor. The floated pins should be driven to a low level. (See Table 9-7.)

Table 9-7. Pin State during Stop Grant Bus State

Signal	Type	State
A3-A2	O	Previous state
A31–A4	I/O	Previous state
D31–D0	I/O	Floated
BE3#–BE0#	O	Previous state
DP3–DP0	I/O	Floated
W/R#, D/C#, M/IO#	O	Previous state
ADS#	O	Inactive
LOCK#, PLOCK#	O	Inactive
BREQ	O	Previous state
HLDA	O	As per HOLD
BLAST#	O	Previous state
FERR#	O	Previous state
PCD, PWT	O	Previous state
PCHK#	O	Previous state
PWT, PCD	O	Previous state
SMIACT#	O	Previous state

9.6.3 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR PIN STATES DURING STOP GRANT

During the Stop Grant state, most output signals of the processor will maintain their previous condition, which is the level they held when entering the Stop Grant state. The data bus and data parity signals also maintain their previous state. In response to HOLD being driven active during the Stop Grant state when the CLK input is running, the Write-Back Enhanced Intel486 processors will generate HLDA and tri-state all output and input/output signals that are tri-stated during the HOLD/HLDA state. After HOLD is de-asserted all signals will return to the state they were in prior to the HOLD/HLDA sequence.

All inputs should be driven to the power supply rails to ensure the lowest possible current consumption during the Stop Grant or Stop Clock states. (See Table 9-8.)

The Write-Back Enhanced Intel486 processors have bus keepers features. The data bus and data parity pins have bus keepers that maintain the previous state while in the Stop Grant state. External resistors are no longer required, which prevents excess current during the Stop Grant state. (If external resistors are present, they should be strong enough to ‘‘flip’’ the bus hold circuitry and eliminate potential DC paths. Alternately, ‘‘weak’’ resistors may also be added to prevent excessive current flow.) See section 17.3.3, ‘‘External Resistors Recommended to Minimize Leakage Currents,’’ for external register values.

In order to obtain the lowest possible power consumption during the Stop Grant state, system designers must ensure that the input signals with pull-up resistors are not driven LOW, and the input signals with pull-down resistors are not driven HIGH. (See the Table 3-11 for signals with internal pull-up and pull-down resistors).

Table 9-8. Write-Back Enhanced IntelDX4™ Processor Pin States during Stop Grant Bus Cycle

Signal	Type	State
A3-A2	O	Previous state
A31-A4	I/O	Previous state
D31-D0	I/O	Previous state
BE3#–BE0#	O	Previous state
DP3–DP0	I/O	Previous state
W/R#, D/C#, M/IO#	O	Previous state
ADS#	O	Inactive (high)
LOCK#, PLOCK#	O	Inactive (high)
BREQ	O	Previous state
HLDA	O	As per HOLD
BLAST#	O	Previous state
FERR#	O	Previous state
PCHK#	O	Previous state
PWT, PCD	O	Previous state
CACHE#	O	Inactive(1) (high)
HITM#	O	Inactive(1) (high)
SMIACT#	O	Previous state

NOTES:
1. For the case of snoop cycles (via EADS#) during Stop Grant state, both HITM# and CACHE# may go active depending on the snoop hit in the internal cache. During Stop Grant state, AHOLD, HOLD, BOFF# and EADS# are serviced normally.

9.6.4 CLOCK CONTROL STATE DIAGRAM

The following state descriptions and diagram show the state transitions during a Stop Clock cycle for the Military Intel486 processor. (Refer to Figure 9-9 for a Stop Clock state diagram.)

9.6.4.1 Normal State

This is the normal operating state of the processor.

9.6.4.2 Stop Grant State

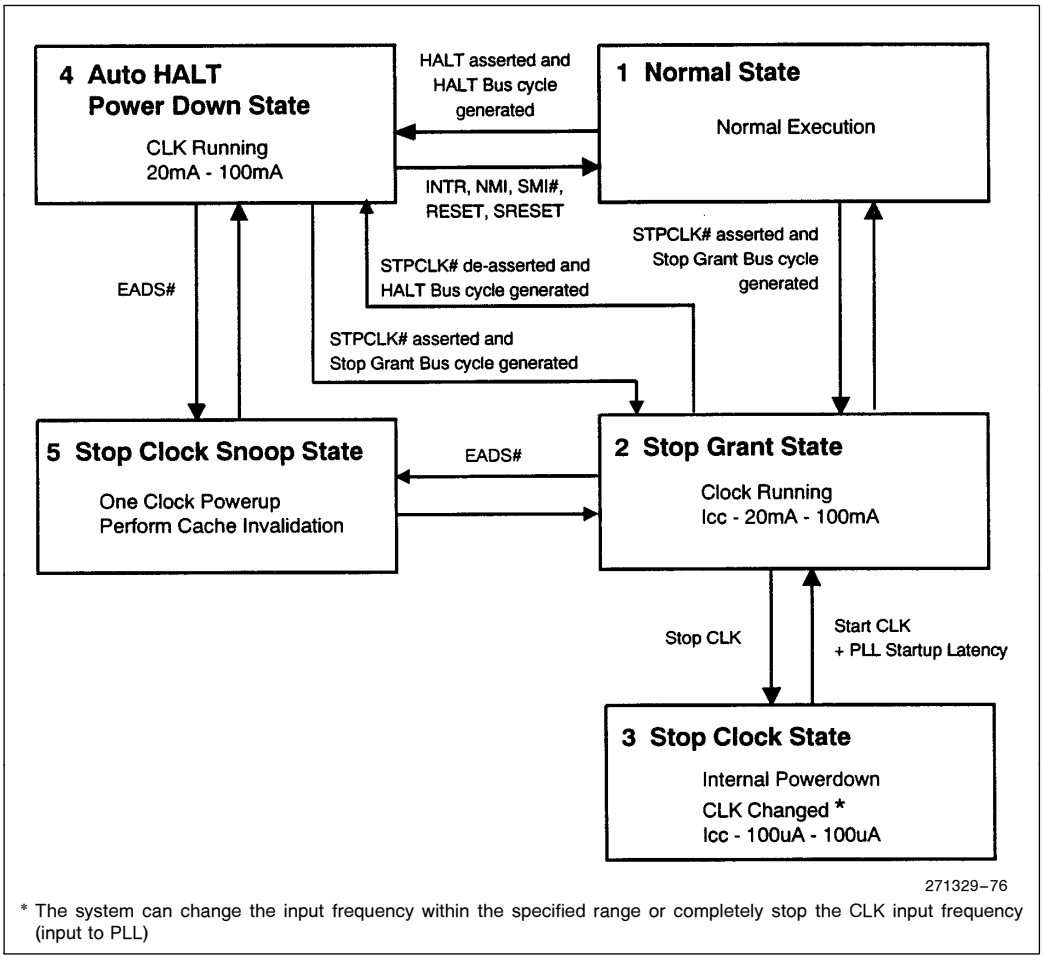
The **Stop Grant** state provides a fast wake-up state that can be entered by simply asserting the external STPCLK# interrupt pin. Once the Stop Grant bus cycle has been placed on the bus, and either RDY# or BRDY# is returned, the processor is in this state (depending on the CLK input frequency). The processor returns to the normal execution state 10–20 clock periods after STPCLK# has been de-asserted.

While in the Stop Grant state, the pull-up resistors on STPCLK#, CLKMUL (for the IntelDX4 processor) and UP# are disabled internally. The system must continue to drive these inputs to the state they were in immediately before the processor entered the Stop Grant state. For minimum processor power consumption, all other input pins should be driven to their inactive level while the processor is in the Stop Grant state.

A RESET or SRESET will bring the processor from the Stop Grant state to the Normal state. The processor will recognize the inputs required for cache invalidation's (HOLD, AHOLD, BOFF# and EADS#) as explained later in this section. The processor will not recognize any other inputs while in the Stop Grant state. Input signals to the processor will not be recognized until 1 CLK after STPCLK# is de-asserted (see Figure 9-10).

While in the Stop Grant state, the processor will not recognize transitions on the interrupt signals (SMI#, NMI, and INTR). Driving an active edge on either SMI# or NMI will not guarantee recognition and service of the interrupt request following exit from the Stop Grant state. However, if one of the interrupt signals (SMI#, NMI, or INTR) is driven active while the processor is in the Stop Grant state, and held active for at least one CLK after STPCLK# is de-asserted, the corresponding interrupt will be serviced. The Military Intel486 processor requires INTR to be held active until the processor issues an interrupt acknowledge cycle in order to guarantee recognition. (See Figure 9-10).

When the processor is in the Stop Grant state, the system is allowed to stop or change the CLK input. When the CLK input to the processor is stopped (or changed), the Military Intel486 processor requires the CLK input to be held at a constant frequency for a minimum of 1 ms before de-asserting STPCLK#. This 1-ms time period is necessary so that the PLL can stabilize, and it must be met before the processor will return to the Stop Grant state.



* The system can change the input frequency within the specified range or completely stop the CLK input frequency (input to PLL)

Figure 9-9. Military Intel486™ Processor Family Stop Clock State Machine

The processor will generate a Stop Grant bus cycle only when entering that state from the Normal or the Auto HALT Power Down state. When the processor enters the Stop Grant state from the Stop Clock state or the Stop Clock Snoop state, the processor will not generate a Stop Grant bus cycle.

9.6.4.3 Stop Clock State

Stop Clock state is entered from the Stop Grant state by stopping the CLK input (either logic high or logic low). None of the processor input signals should change state while the CLK input is stopped. Any transition on an input signal (with the exception of INTR, NMI and SMI#) before the processor has returned to the Stop Grant state will result in unpredictable behavior. If INTR is driven active while the CLK input is stopped, and held active until the processor issues an interrupt acknowledge bus cycle, it will be serviced in the normal manner. The system design must ensure the processor is in the correct state prior to asserting cache invalidation or interrupt signals to the processor.

The processor will return to the Stop Grant state after the CLK input has been running at a constant frequency for a period of time equal to the PLL start-up latency (see section 9.6.3.2). The CLK input can be restarted to any frequency between the minimum and maximum frequency listed in the AC timing specifications.

9.6.4.4 Auto HALT Power Down State

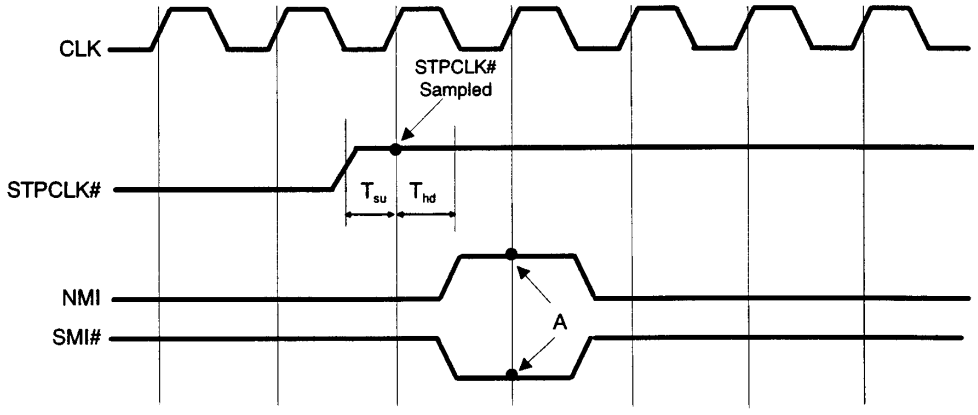
The execution of a HALT instruction will also cause the processor to automatically enter the **Auto HALT Power Down** state. The processor will issue a normal HALT bus cycle before entering this state. The processor will transition to the Normal state on the occurrence of INTR, NMI, SMI#, RESET, or SRESET.

The system can generate a STPCLK# while the processor is in the Auto HALT Power Down state. The processor will generate a Stop Grant bus cycle when it enters the Stop Grant state from the HALT state.

When the system de-asserts the STPCLK# interrupt, the processor will return execution to the HALT state. The processor will generate a new HALT bus cycle when it re-enters the HALT state from the Stop Grant state.

9.6.4.5 Stop Clock Snoop State (Cache Invalidations)

When the processor is in the Stop Grant state or the Auto HALT Power Down state, the processor will recognize HOLD, AHOLD, BOFF# and EADS# for cache invalidation. When the system asserts HOLD, AHOLD, or BOFF#, the processor will float the bus accordingly. When the system then asserts EADS#, the processor will transparently enter the **Stop Clock Snoop state** and will power up for 1 full core



A. Earliest time at which NMI or SMI# will be recognized.

Figure 9-10. Recognition of Inputs when Exiting Stop Grant State

clock in order to perform the required cache snoop cycle. It will then re-freeze the clock to the processor core and return to the previous state. The processor does not generate a bus cycle when it returns to the previous state.

A FLUSH# event during the Stop Grant state or the Auto HALT Power Down state will be latched and acted upon by asserting the internal FLUSH# signal for one clock upon re-entering the Normal state.

9.6.4.6 Auto Idle Power Down State

When the chip is known to be truly idle and waiting for a RDY# or BRDY# from a memory or I/O bus cycle read, the Military Intel486 processor will reduce its core clock rate to be equal to the external CLK frequency without affecting performance. When any RDY# or BRDY# is asserted, the part will return to clocking the core at the specified multiplier of the external CLK frequency. This functionality is transparent to software and external hardware.

9.6.5 WRITE-BACK ENHANCED IntelDX4™ PROCESSOR CLOCK CONTROL STATE DIAGRAM

Figure 9-11 (state diagram) shows the state transitions during Stop Clock for the Write-Back Enhanced Intel486 processors.

NOTE:
The Stop Clock State Machine in the Standard bus configuration is identical to that of other Intel486 processors. (See section 9.6.4, ''Clock Control State Diagram''.)

9.6.5.1 Normal State

This is the normal operating state of the processor. When the processor is executing program/instruction and the STPCLK# pin is not asserted, the processor is said to be in its normal state.

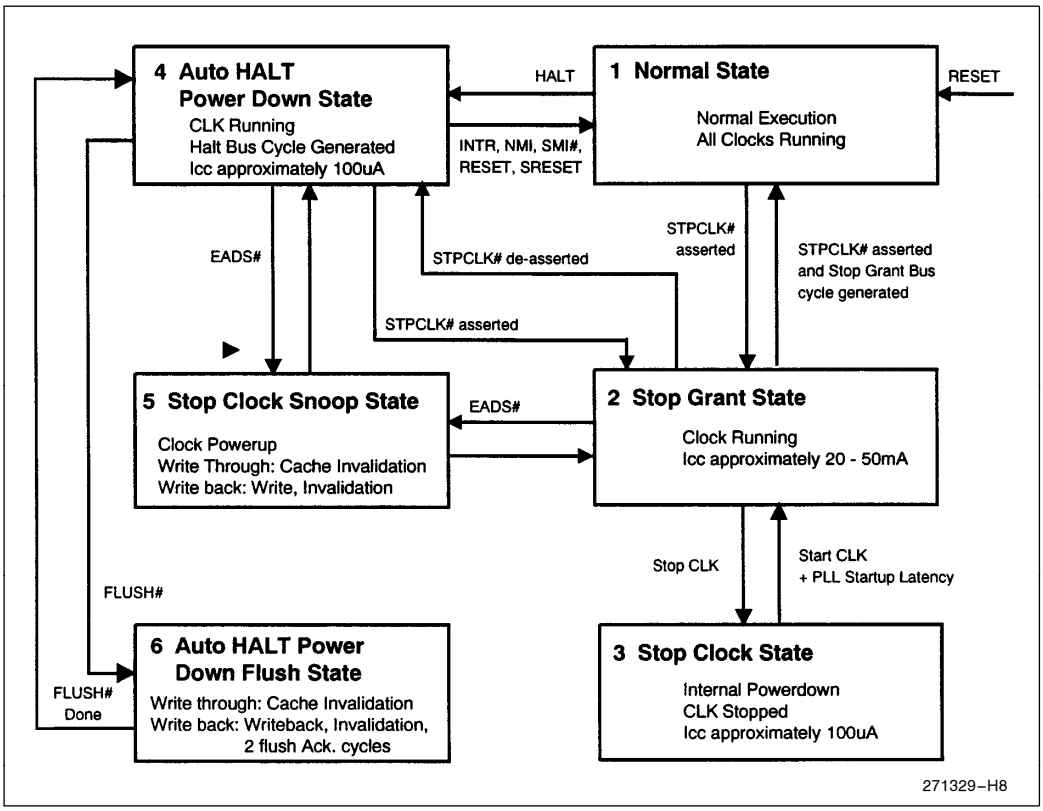


Figure 9-11. Write-Back Enhanced IntelDX4™ Processor Stop Clock State Machine (Enhanced Bus Configuration)

9.6.5.2 Stop Grant State

For minimum processor power consumption, all other input pins should be driven to their inactive level while the processor is in the Stop Grant state excepting data bus, data parity, WB/WT# and INV pins. WB/WT# should be driven low and INV should be driven high.

In both the Standard mode and Enhanced mode states, the following conditions exist:

- A RESET, SRESET or de-assertion of STPCLK# will bring the processor from the Stop Grant state to the Normal state.
- While in the Stop Grant state, the processor will not recognize transitions on the interrupt signals (SMI#, NMI, and INTR). This means SMI#, NMI, INTR are not Stop Break events. The external logic should de-assert STPCLK# before issuing interrupts or if an interrupt is asserted it should be kept asserted for at least 1 clock after STPCLK# is removed. (Note that the Write-Back Enhanced Intel486 processors require that INTR must be held active until the processor issues an interrupt acknowledge cycle in order to guarantee recognition.)
- FLUSH# is not a Stop Break event. But if FLUSH# is asserted during the Stop Grant state, it is latched by the Write-Back Enhanced Intel486 processors and serviced later when STPCLK# is deasserted.
- The processor will latch and respond to the inputs BOFF#, EADS#, AHOLD, and HOLD. The processor will not recognize any other inputs while in the Stop Grant state except FLUSH#. Other input signals to the processor will not be recognized until the CLK following the CLK in which STPCLK# is de-asserted. (See Figure 9-11.)
- The processor will generate a Stop Grant bus cycle only when entering that state from the Normal or the Auto HALT Power Down state. The Stop Grant bus cycle is not generated when the processor enters the Stop Grant state from the Stop Clock state or the Stop Clock Snoop state.
- The processor will not enter the Stop Grant state until all the pending writes are completed, all pending interrupts are serviced and the processor is idle.

9.6.5.3 Stop Clock State

Stop Clock state is the lowest power consumption mode in the processor, because it allows removal of the external clock. It also has the longest latency for returning to normal state. The **Stop Clock** state is entered from the Stop Grant state by stopping the CLK input. In the Stop Clock state, total processor power consumption drops to 100 μA, which is approximately 200–250 times lower than the Stop Grant state. None of the processor input signals should change state while the CLK input is stopped. Any transition on an input signal before the processor has returned to the Stop Grant state will result in unpredictable behavior. If INTR is driven active, it must be held active until the processor issues an interrupt acknowledge cycle.

In the Stop Clock state, the processor is dormant. It does not respond to any transitions on any of the input pins including snoops, flushes and interrupts. It is recommended that this mode only be entered if the processor cache is coherent with main memory and the processor is not processing any interrupts. If this mode is entered with a dirty cache, no alternate master cycles can be allowed while the processor is in the Stop Clock state.

The processor will return to the Stop Grant state after the CLK input has been running at a constant frequency for a period of time equal to the PLL start-up latency. The CLK input can be restarted to any frequency between the minimum and maximum frequency listed in the AC timing specifications.

In Enhanced Bus Mode

If the processor is taken into the Stop Clock state with a dirty cache, alternate bus master cycles are not allowed while the processor remains in the Stop Clock state. In order to take the processor into the Stop Clock state with a clean cache, the cache must be flushed. During the time the cache is being flushed, the system must block interrupts to the processor. With all interrupts other than STPCLK# blocked, the processor does not write into the cache during the time from the completion of the flush and time it enters the Stop Grant state. This is necessary for the cache to be coherent. To ensure this, the system should drive KEN# inactive from the time the flush starts until the Stop Grant cycle is issued. The system can then put the processor in the Stop Clock state by stopping the CLOCK.

If the processor is already in the Stop Grant state and entering the Stop Clock state is desired, the system must de-assert STPCLK# before flushing the cache in order to ensure the cache coherency. The 5-clock de-assertion specification for STPCLK# must also be met before the above sequence can occur.

9.6.5.4 Auto HALT Power Down State

Upon execution of a HALT instruction, the processor will automatically enter a low power state, called the **Auto HALT Power Down state.** The processor will issue a normal HALT bus cycle when entering this state. Because interrupts are HALT break events, the processor will transition to the Normal state on the occurrence of INTR, NMI, SMI# or RESET (SRESET is also a HALT break event). If there is a FLUSH# while the processor is in this state, the FLUSH# will be serviced by transitioning to the Stop Clock Flush state. After the FLUSH# is completed, the processor returns back to the Auto HALT Power Down state.

The system can generate a STPCLK# while the processor is in the Auto HALT Power Down state. The processor will then generate a Stop Grant bus cycle and enter the Stop Grant state from the Auto HALT Power Down state. When the system de-asserts the STPCLK# interrupt, the processor will return to the Auto HALT Power Down state. The processor will not generate a new HALT bus cycle when it re-enters the Auto HALT Power Down state from the Stop Grant state.

9.6.6 STOP CLOCK SNOOP STATE (CACHE INVALIDATIONS)

When the processor is in the Stop Grant state or the Auto HALT Power Down state, the processor will recognize HOLD, AHOLD, BOFF#, and EADS# for cache invalidation. When the system asserts HOLD, AHOLD, or BOFF#, the processor will float the bus accordingly. When the system asserts EADS#, the processor will transparently enter the **Stop Clock Snoop state** and will power up in order to perform the required cache snoop cycle and write-back cycles. It will then refreeze the CLK to the processor core and return to the previous state (i.e., either the Stop Grant state or the Auto HALT Power Down state). The processor does not generate a bus cycle when it returns to the previous state.

9.6.6.1 Auto HALT Power Down Flush State (Cache Flush) for the Write-Back Enhanced IntelDX4™ Processor

If the Write-Back Enhanced Intel486 processor is in either Standard or Enhanced Bus mode, and a FLUSH# event occurs during Auto HALT Power Down state, the processor will transition to the Auto HALT Power Down Flush state. If the on-chip cache is configured as a write-back cache, the CLK to the processor core is turned on until all the dirty lines are written back, the cache is invalidated, and the two flush acknowledge cycles are completed. If the on-chip cache is configured as a write-through cache, the CLK to the processor core is turned on until the cache is invalidated. The processor then refreezes the CLK and returns to the previous state (i.e., the Auto HALT Power Down state). Auto HALT Power Down Flush state is entered only from the Auto HALT Power Down state and not from the Stop Grant state.

9.6.7 SUPPLY CURRENT MODEL FOR STOP CLOCK MODES AND TRANSITIONS

Figures 9-12 and 9-13 illustrate the effect of different Stop Clock state transitions on the supply current of the Military Intel486 processor.

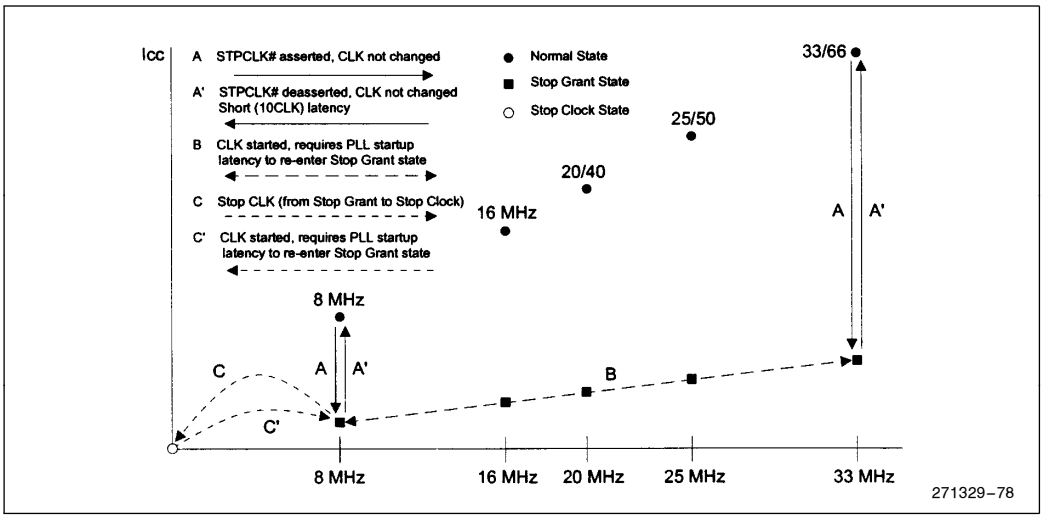


Figure 9-12. Supply Current Model for Stop Clock Modes and Transitions for the Military Intel486™ Processor

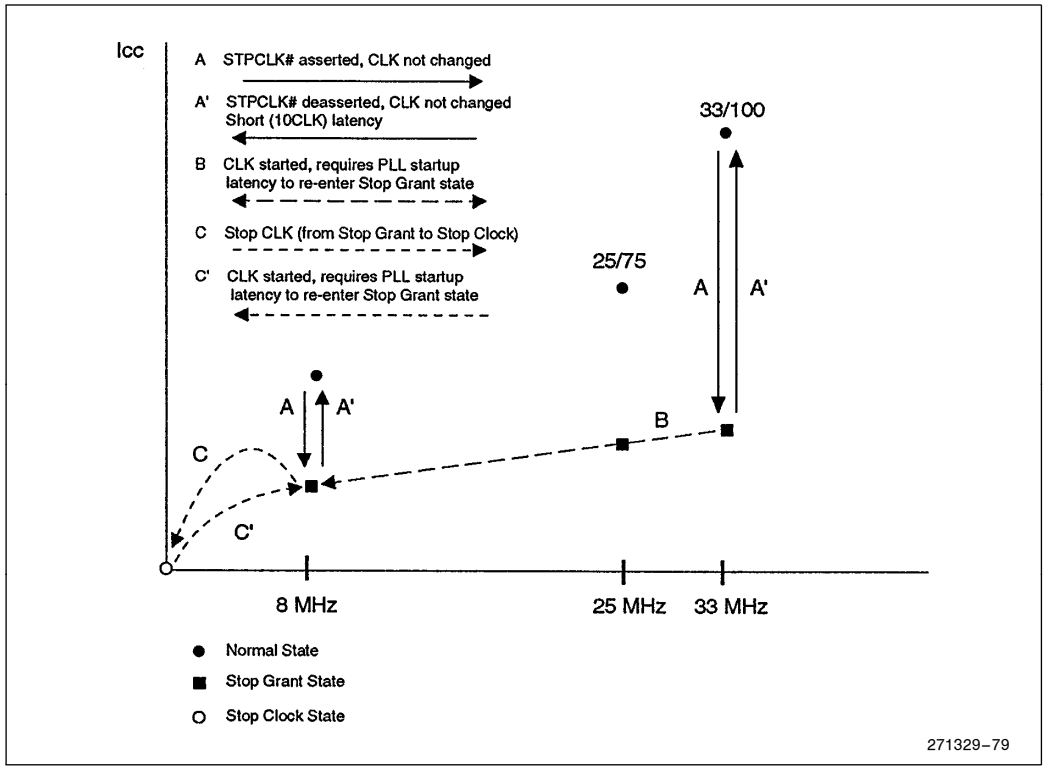


Figure 9-13. Supply Current Model for Stop Clock Modes and Transitions for the IntelDX4™ Processor

10.0 BUS OPERATION

10.1 Data Transfer Mechanism

All data transfers occur as a result of one or more bus cycles. Logical data operands of byte, word and doubleword lengths may be transferred without restrictions on physical address alignment. Data may be accessed at any byte boundary but two or three cycles may be required for unaligned data transfers. (See section 10.1.2, ''Dynamic Data Bus Sizing,'' and section 10.1.5, ''Operand Alignment.'')

The Military Intel486 processor address signals are split into two components. High-order address bits are provided by the address lines, A2–A31. The byte enables, BE0#–BE3#, form the low-order address and provide linear selects for the four bytes of the 32-bit address bus.

The byte enable outputs are asserted when their associated data bus bytes are involved with the present bus cycle, as listed in Table 10-1. Byte enable patterns that have a negated byte enable separating two or three asserted byte enables will never occur (see Table 10-5). All other byte enable patterns are possible.

Table 10-1. Byte Enables and Associated Data and Operand Bytes

Byte Enable Signal	Associated Data Bus Signals	
BE0#	D0–D7	(byte 0–least significant)
BE1#	D8–D15	(byte 1)
BE2#	D16–D23	(byte 2)
BE3#	D24–D31	(byte 3–most significant)

Address bits A0 and A1 of the physical operand's base address can be created when necessary. Use of the byte enables to create A0 and A1 is shown in Table 10-2. The byte enables can also be decoded to generate BLE# (byte low enable) and BHE# (byte high enable). These signals are needed to address 16-bit memory systems. (See section 10.1.3, ''Interfacing with 8-, 16-, and 32-Bit Memories.'')

10.1.1 MEMORY AND I/O SPACES

Bus cycles may access physical memory space or I/O space. Peripheral devices in the system may either be memory-mapped, or I/O-mapped, or both. Physical memory addresses range from 00000000H to FFFFFFFFH (4 gigabytes). I/O addresses range from 00000000H to 0000FFFFH (64 Kbytes) for programmed I/O. (See Figure 10-1.)

Table 10-2. Generating A0–A31 from BE0#–BE3# and A2–A31

Military Intel486™ Processor Address Signals								
A31	**. . .**	**A2**			**BE3#**	**BE2#**	**BE1#**	**BE0#**
	Physical Base Address							
A31	. . .	A2	A1	A0				
A31	. . .	A2	0	0	X	X	X	Low
A31	. . .	A2	0	1	X	X	Low	High
A31	. . .	A2	1	0	X	Low	High	High
A31	. . .	A2	1	1	Low	High	High	High

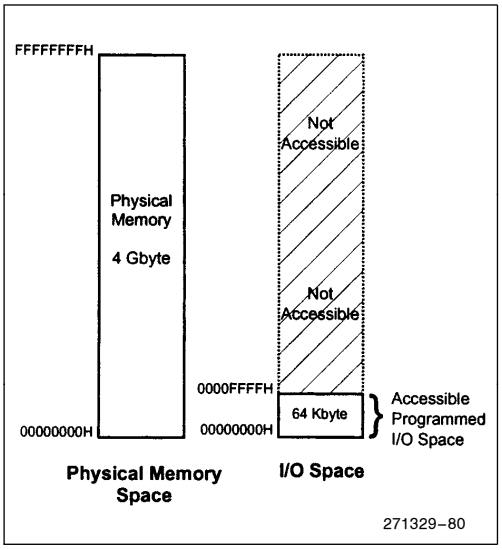


Figure 10-1. Physical Memory and I/O Spaces

10.1.1.1 Memory and I/O Space Organization

The Military Intel486 processor datapath to memory and input/output (I/O) spaces can be 32-, 16- or 8-bits wide. The byte enable signals, BE0# – BE3#, allow byte granularity when addressing any memory or I/O structure whether 8, 16 or 32 bits wide.

The Military Intel486 processor includes bus control pins, BS16# and BS8#, which allow direct connection to 16- and 8-bit memories and I/O devices. Cycles to 32-, 16- and 8-bit may occur in any sequence, since the BS8# and BS16# signals are sampled during each bus cycle.

32-bit wide memory and I/O spaces are organized as arrays of physical 4-byte words. Each memory or I/O 4-byte word has four individually addressable bytes at consecutive byte addresses (see Figure 10-2). The lowest addressed byte is associated with data signals D0–D7; the highest-addressed byte with D24–D31. Physical 4-byte words begin at addresses divisible by four.

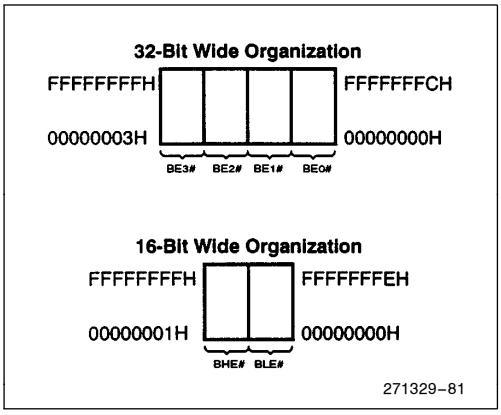


Figure 10-2. Physical Memory and I/O Space Organization

16-bit memories are organized as arrays of physical 2-byte words. Physical 2-byte words begin at addresses divisible by two. The byte enables BE0# – BE3#, must be decoded to A1, BLE# and BHE# to address 16-bit memories. (See section 10.1.3, ''Interfacing with 8-, 16- and 32-Bit Memories.'')

To address 8-bit memories, the two low order address bits A0 and A1, must be decoded from BE0# – BE3#. The same logic can be used for 8- and 16-bit memories, because the decoding logic for BLE# and A0 are the same. (See section 10.1.3, ''Interfacing with 8-, 16-, and 32-Bit Memories.'')

10.1.2 DYNAMIC DATA BUS SIZING

Dynamic data bus sizing is a feature allowing processor connection to 32-, 16- or 8-bit buses for memory or I/O. The Military Intel486 processor may connect to all three bus sizes. Transfers to or from 32-, 16- or 8-bit devices are supported by dynamically determining the bus width during each bus cycle. Address decoding circuitry may assert BS16# for 16-bit devices, or BS8# for 8-bit devices during each bus cycle. BS8# and BS16# must be negated when addressing 32-bit devices. An 8-bit bus width is selected if both BS16# and BS8# are asserted.

BS16# and BS8# force the Military Intel486 processor to run additional bus cycles to complete requests larger than 16- or 8 bits. A 32-bit transfer will be converted into two 16-bit transfers (or 3 transfers if the data is misaligned) when BS16# is asserted. Asserting BS8# will convert a 32-bit transfer into four 8-bit transfers.

Extra cycles forced by BS16# or BS8# should be viewed as independent bus cycles. BS16# or BS8# must be driven active during each of the extra cycles unless the addressed device has the ability to change the number of bytes it can return between cycles.

The Military Intel486 processor will drive the byte enables appropriately during extra cycles forced by BS8# and BS16#. A2–A31 will not change if accesses are to a 32-bit aligned area. Table 10-3 shows the set of byte enables that will be generated on the next cycle for each of the valid possibilities of the byte enables on the current cycle.

The dynamic bus sizing feature of the Military Intel486 processor is significantly different than that of the Intel386 processor. Unlike the Intel386 processor, the Military Intel486 processor requires that data bytes be driven on the addressed data pins. The simplest example of this function is a 32-bit aligned, BS16# read. When the Military Intel486 processor reads the two high order bytes, they must be driven on the data bus pins D16–D31. The Military Intel486 processor expects the two low order bytes on D0–D15. The Intel386 processor expects both the high and low order bytes on D0–D15. The Intel386 processor always reads or writes data on the lower 16 bits of the data bus when BS16# is asserted.

The external system must contain buffers to enable the Military Intel486 processor to read and write data on the appropriate data bus pins. Table 10-4 shows the data bus lines to which the Military Intel486 processor expects data to be returned for each valid combination of byte enables and bus sizing options.

Table 10-3. Next Byte Enable Values for BSn# Cycles

Current				Next with BS8#				Next with BS16#			
BE3#	BE2#	BE1#	BE0#	BE3#	BE2#	BE1#	BE0#	BE3#	BE2#	BE1#	BE0#
1	1	1	0	n	n	n	n	n	n	n	n
1	1	0	0	1	1	0	1	n	n	n	n
1	0	0	0	1	0	0	1	1	0	1	1
0	0	0	0	0	0	0	1	0	0	1	1
1	1	0	1	n	n	n	n	n	n	n	n
1	0	0	1	1	0	1	1	1	0	1	1
0	0	0	1	0	0	1	1	0	0	1	1
1	0	1	1	n	n	n	n	n	n	n	n
0	0	1	1	0	1	1	1	n	n	n	n
0	1	1	1	n	n	n	n	n	n	n	n

NOTE:
''n'' means that another bus cycle will not be required to satisfy the request.

Table 10-4. Data Pins Read with Different Bus Sizes

BE3#	BE2#	BE1#	BE0#	w/o BS8#/BS16#	w BS8#	w BS16#
1	1	1	0	D7–D0	D7–D0	D7–D0
1	1	0	0	D15–D0	D7–D0	D15–D0
1	0	0	0	D23–D0	D7–D0	D15–D0
0	0	0	0	D31–D0	D7–D0	D15–D0
1	1	0	1	D15–D8	D15–D8	D15–D8
1	0	0	1	D23–D8	D15–D8	D15–D8
0	0	0	1	D31–D8	D15–D8	D15–D8
1	0	1	1	D23–D16	D23–D16	D23–D16
0	0	1	1	D31–D16	D23–D16	D31–D16
0	1	1	1	D31–D24	D31–D24	D31–D24

Valid data will only be driven onto data bus pins corresponding to active byte enables during write cycles. Other pins in the data bus will be driven but they will not contain valid data. Unlike the Intel386 processor, the Military Intel486 processor will not duplicate write data onto parts of the data bus for which the corresponding byte enable is negated.

10.1.3 INTERFACING WITH 8-, 16- AND 32-BIT MEMORIES

In 32-bit physical memories, such as the one shown in Figure 10-3, each 4-byte word begins at a byte address that is a multiple of four. A2–A31 are used as a 4-byte word select. BE0# –BE3# select individual bytes within the 4-byte word. BS8# and BS16# are negated for all bus cycles involving the 32-bit array.

16- and 8-bit memories require external byte swapping logic for routing data to the appropriate data lines and logic for generating BHE#, BLE# and A1. In systems where mixed memory widths are used, extra address decoding logic is necessary to assert BS16# or BS8#.

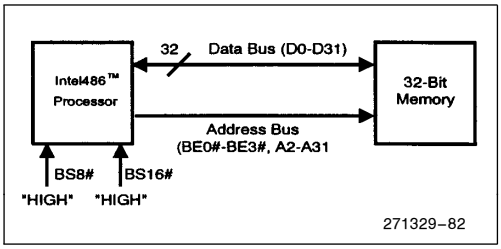


Figure 10-3. Military Intel486™ Processor with 32-Bit Memory

Figure 10-4 shows the Military Intel486 processor address bus interface to 32-, 16- and 8-bit memories. To address 16-bit memories the byte enables must be decoded to produce A1, BHE# and BLE# (A0). For 8-bit wide memories the byte enables must be decoded to produce A0 and A1. The same byte select logic can be used in 16- and 8-bit systems, because BLE# is exactly the same as A0. (See Table 10-5.)

BE0# –BE3# can be decoded as shown in Table 10-5 to generate A1, BHE# and BLE#. The byte select logic necessary to generate BHE# and BLE# is shown in Figure 10-5.

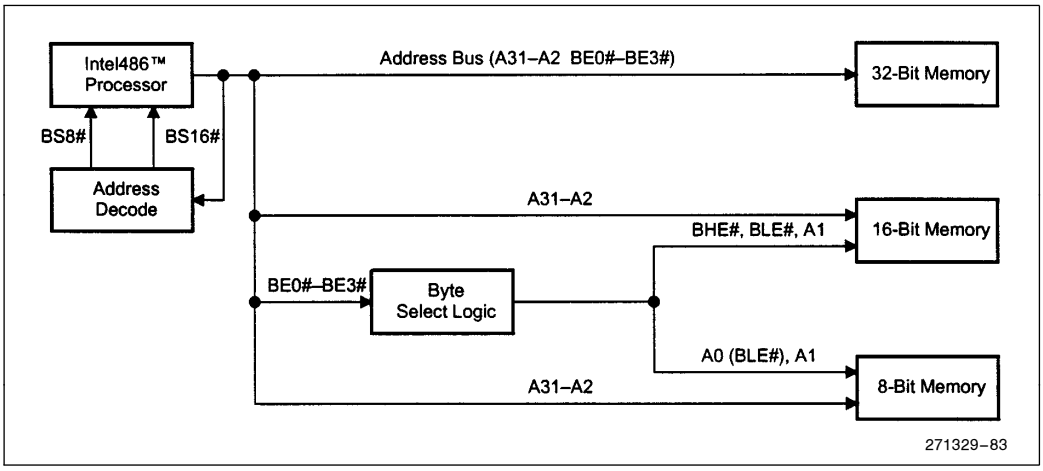


Figure 10-4. Addressing 16- and 8-Bit Memories

Table 10-5. Generating A1, BHE# and BLE# for Addressing 16-Bit Devices

Military Intel486™ Processor				8-, 16-Bit Bus Signals			Comments
BE3#	BE2#	BE1#	BE0#	A1	BHE#	BLE# (A0)	
H*	H*	H*	H*	x	x	x	x–no active bytes
H	H	H	L	L	H	L	
H	H	L	H	L	L	H	
H	H	L	L	L	L	L	
H	L	H	H	H	H	L	
H*	L*	H*	L*	x	x	x	x–not contiguous bytes
H	L	L	H	L	L	H	
H	L	L	L	L	L	L	
L	H	H	H	H	L	H	
L*	H*	H*	L*	x	x	x	x–not contiguous bytes
L*	H*	L*	H*	x	x	x	x–not contiguous bytes
L*	H*	L*	L*	x	x	x	x–not contiguous bytes
L		H	H	H	L	L	
L*	L*	H*	L*	x	x	x	x–not contiguous bytes
L	L	L	H	L	L	H	
L	L	L	L	L	L	L	

BLE# asserted when D0–D7 of 16-bit bus is active.
BHE# asserted when D8–D15 of 16-bit bus is active.
A1 low for all even words; A1 high for all odd words.

Key:
x = don't care H = high voltage level L = low voltage level
* = a non-occurring pattern of Byte Enables; either none are asserted or the pattern has Byte Enables asserted for non-contiguous bytes

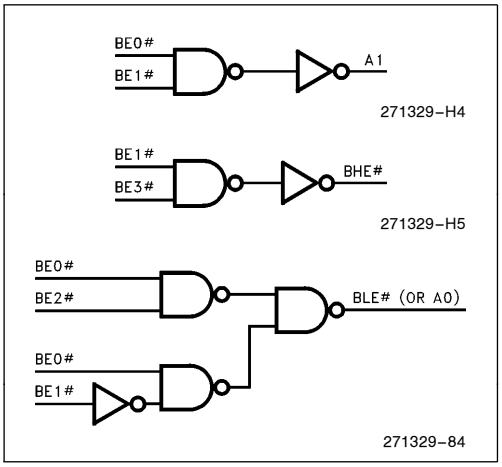


Figure 10-5. Logic to Generate A1, BHE# and BLE# for 16-Bit Buses

Combinations of BE0#–BE3# that never occur are those in which two or three asserted byte enables are separated by one or more negated byte enables. These combinations are "don't care" conditions in the decoder. A decoder can use the non-occurring BE0#–BE3# combinations to its best advantage.

Figure 10-6 shows a Military Intel486 processor data bus interface to 16- and 8-bit wide memories. External byte swapping logic is needed on the data lines so that data is supplied to and received from the Military Intel486 processor on the correct data pins (see Table 10-4).

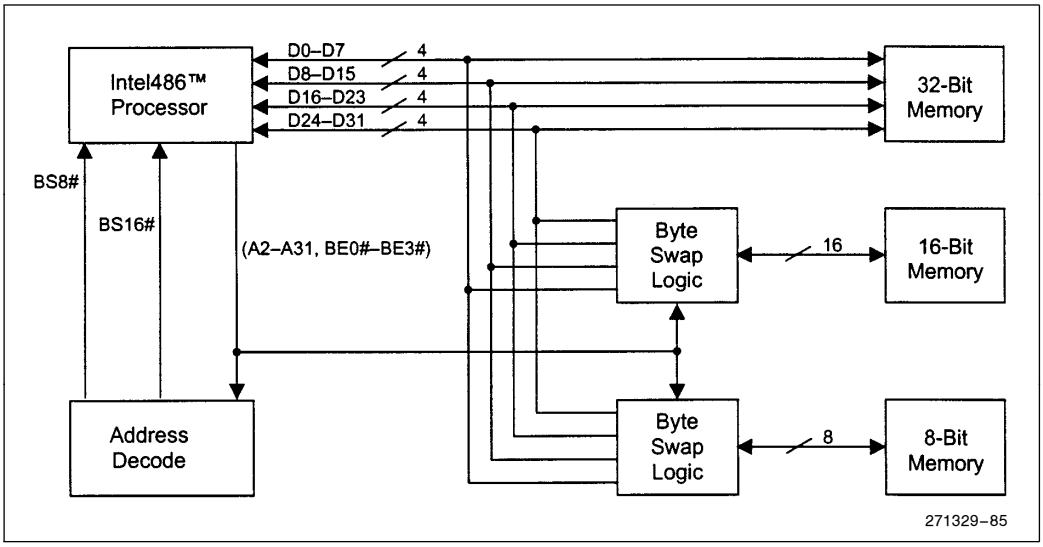


Figure 10-6. Data Bus Interface to 16- and 8-Bit Memories

10.1.4 DYNAMIC BUS SIZING DURING CACHE LINE FILLS

BS8# and BS16# can be driven during cache line fills. The Military Intel486 processor will generate enough 8- or 16-bit cycles to fill the cache line. This can be up to sixteen 8-bit cycles.

The external system should assume that all byte enables are active for the first cycle of a cache line fill. The Military Intel486 processor will generate proper byte enables for subsequent cycles in the line fill. Table 10-6 shows the appropriate A0 (BLE#), A1 and BHE# for the various combinations of the Military Intel486 processor byte enables on both the first and subsequent cycles of the cache line fill. The "*" marks all combinations of byte enables that will be generated by the Military Intel486 processor during a cache line fill.

10.1.5 OPERAND ALIGNMENT

Physical 4-byte words begin at addresses that are multiples of four. It is possible to transfer a logical operand that spans more than one physical 4-byte word of memory or I/O at the expense of extra cycles. Examples are 4-byte operands beginning at addresses that are not evenly divisible by 4, or 2-byte words split between two physical 4-byte words. These are referred to as unaligned transfers.

Operand alignment and data bus size dictate when multiple bus cycles are required. Table 10-7 describes the transfer cycles generated for all combinations of logical operand lengths, alignment, and data bus sizing. When multiple cycles are required to transfer a multibyte logical operand, the highest-order bytes are transferred first. For example, when the processor does a 4-byte unaligned read beginning at location x11 in the 4-byte aligned space, the three high order bytes are read in the first bus cycle. The low byte is read in a subsequent bus cycle.

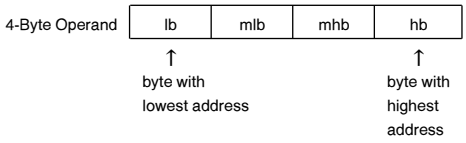
Table 10-6. Generating A0, A1 and BHE# from the Military Intel486™ Processor Byte Enables

				First Cache Fill Cycle			Any Other Cycle		
BE3#	BE2#	BE1#	BE0#	A0	A1	BHE#	A0	A1	BHE#
1	1	1	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
*0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	1	0	0
1	0	0	1	0	0	0	1	0	0
*0	0	0	1	0	0	0	1	0	0
1	0	1	1	0	0	0	0	1	1
*0	0	1	1	0	0	0	0	1	0
*0	1	1	1	0	0	0	1	1	0

Table 10-7. Transfer Bus Cycles for Bytes, Words and Dwords

	Byte-Length of Logical Operand								
	1	2				4			
Physical Byte Address in Memory (Low Order Bits)	xx	00	01	10	11	00	01	10	11
Transfer Cycles over 32-Bit Bus	b	w	w	w	hb lb	d	hb l3	hw lw	h3 lb
Transfer Cycles over 16-Bit Bus († = BS#16 asserted)	b	w	lb † hb†	w	hb lb	lw † hw†	hb lb† mw†	hw lw	mw† hb† lb
Transfer Cycles over 8-Bit Bus (‡ = BS8# Asserted)	b	lb ‡ hb ‡	lb ‡ hb‡	lb ‡ hb ‡	hb lb	lb ‡ mlb ‡ mhb ‡ hb ‡	hb lb ‡ mlb ‡ mhb ‡	mhb ‡ hb ‡ lb ‡ mlb ‡	mlb ‡ mhb ‡ hb ‡ kb

KEY:
b = byte transfer
w = 2-byte transfer
3 = 3-byte transfer
d = 4-byte transfer
h = high-order portion
l = low-order portion
m = mid-order portion



The function of unaligned transfers with dynamic bus sizing is not obvious. When the external systems asserts BS16# or BS8# forcing extra cycles, low-order bytes or words are transferred first (opposite to the example above). When the Military Intel486 processor requests a 4-byte read and the external system asserts BS16#, the lower 2 bytes are read first followed by the upper 2 bytes.

In the unaligned transfer described above, the processor requested three bytes on the first cycle. If the external system asserted BS16# during this 3-byte transfer, the lower word is transferred first followed by the upper byte. In the final cycle the lower byte of the 4-byte operand is transferred as in the 32-bit example above.

10.2 Bus Functional Description

The Military Intel486 processor supports a wide variety of bus transfers to meet the needs of high performance systems. Bus transfers can be single cycle or multiple cycle, burst or non-burst, cacheable or non-cacheable, 8-, 16- or 32-bit, and pseudo-locked.

To support multiprocessing systems there are cache invalidation cycles and locked cycles.

This section begins with basic non-cacheable non-burst single cycle transfers. It moves on to multiple cycle transfers and introduces the burst mode. Cacheability is introduced in section 10.2.3, ''Cacheable Cycles.'' The remaining sections describe locked, pseudo-locked, invalidate, bus hold and interrupt cycles.

Bus cycles and data cycles are discussed in this section. A bus cycle is at least two clocks long and begins with ADS# active in the first clock and ready active in the last clock. Data is transferred to or from the Military Intel486 processor during a data cycle. A bus cycle contains one or more data cycles.

Refer to section 10.2.13, ''Bus States,'' for a description of the bus states shown in the timing diagrams.

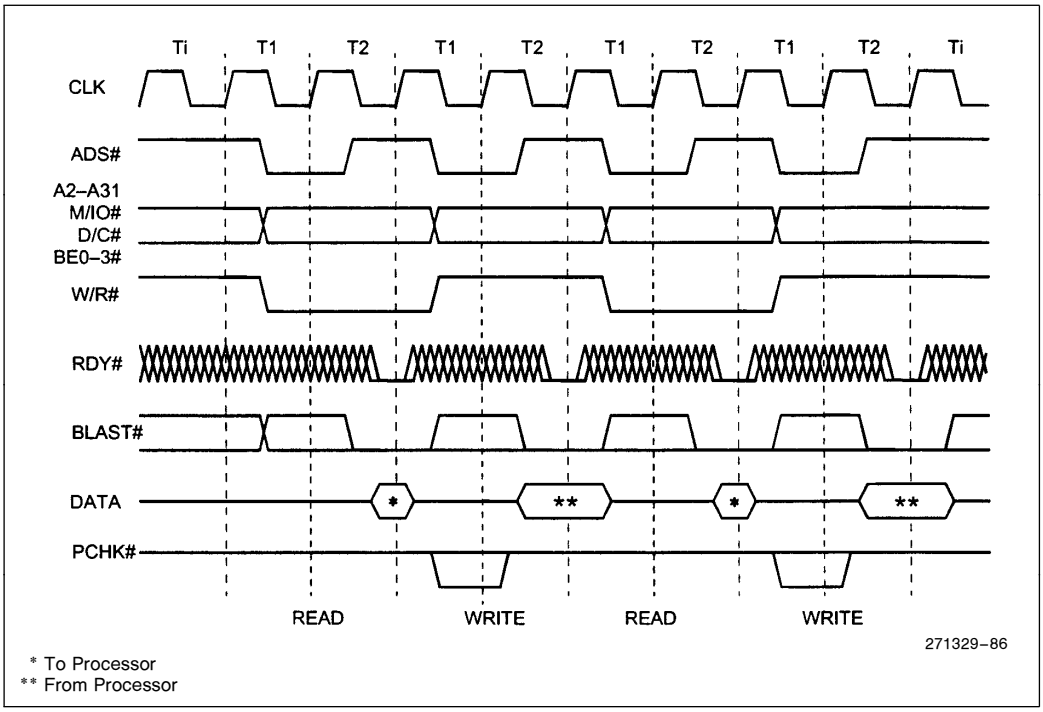
10.2.1 NON-CACHEABLE NON-BURST SINGLE CYCLE

10.2.1.1 No Wait States

The fastest non-burst bus cycle that the Military Intel486 processor supports is two clocks long. These cycles are called 2-2 cycles because reads and writes take two cycles each. The first ''2'' refers to reads and the second to writes.

For example, if a wait state needs to be added to the write, the cycle would be called 2-3.

Basic two clock read and write cycles are shown in Figure 10-7. The Military Intel486 processor initiates a cycle by asserting the address status signal (ADS#) at the rising edge of the first clock. The ADS# output indicates that a valid bus cycle definition and address is available on the cycle definition lines and address bus.



* To Processor
** From Processor

Figure 10-7. Basic 2-2 Bus Cycle

The non-burst ready input (RDY#) is returned by the external system in the second clock. RDY# indicates that the external system has presented valid data on the data pins in response to a read or the external system has accepted data in response to a write.

The Military Intel486 processor samples RDY# at the end of the second clock. The cycle is complete if RDY# is active (LOW) when sampled. Note that RDY# is ignored at the end of the first clock of the bus cycle.

The burst last signal (BLAST#) is asserted (LOW) by the Military Intel486 processor during the second clock of the first cycle in all bus transfers illustrated in Figure 10-7. This indicates that each transfer is complete after a single cycle. The Military Intel486 processor asserts BLAST# in the last cycle of a bus transfer.

The timing of the parity check output (PCHK#) is shown in Figure 10-7. The Military Intel486 processor drives the PCHK# output one clock after ready terminates a read cycle. PCHK# indicates the parity status for the data sampled at the end of the previous clock. The PCHK# signal can be used by the external system. The Military Intel486 processor does nothing in response to the PCHK# output.

10.2.1.2 Inserting Wait States

The external system can insert wait states into the basic 2-2 cycle by driving RDY# inactive at the end of the second clock. RDY# must be driven inactive to insert a wait state. Figure 10-8 illustrates a simple non-burst, non-cacheable signal with one wait state added. Any number of wait states can be added to a Military Intel486 processor bus cycle by maintaining RDY# inactive.

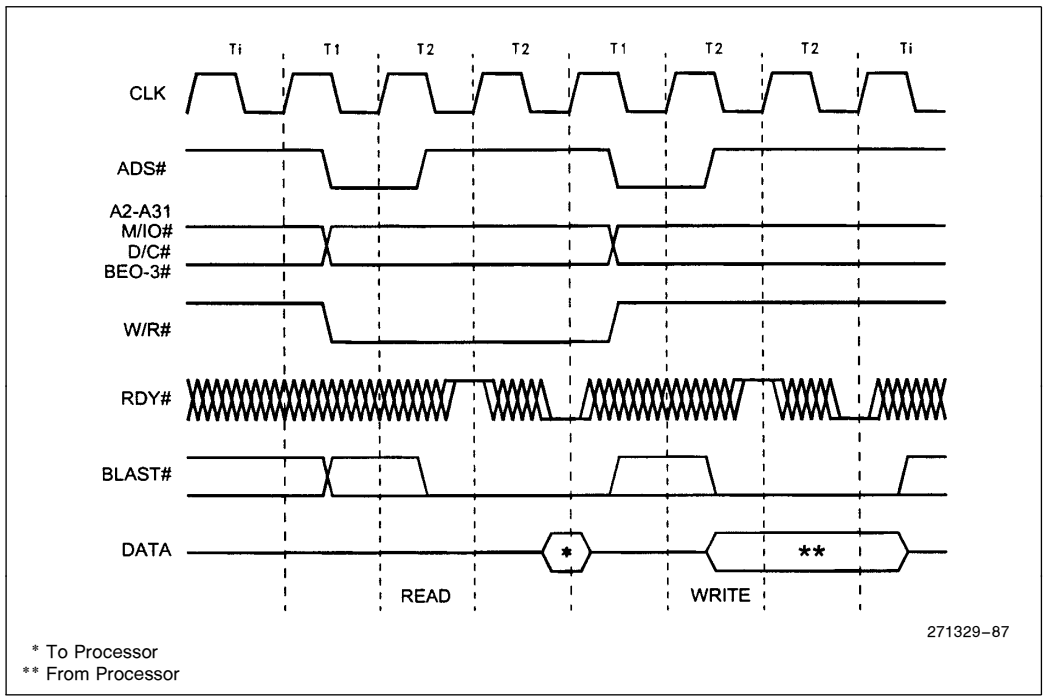


Figure 10-8. Basic 3-3 Bus Cycle

The burst ready input (BRDY#) must be driven inactive on all clock edges where RDY# is driven inactive for proper operation of these simple non-burst cycles.

10.2.2 MULTIPLE AND BURST CYCLE BUS TRANSFERS

Multiple cycle bus transfers can be caused by internal requests from the Military Intel486 processor or by the external memory system. An internal request for a 128-bit pre-fetch must take more than one cycle. Internal requests for unaligned data may also require multiple bus cycles. A cache line fill requires multiple cycles to complete.

The external system can cause a multiple cycle transfer when it can only supply 8- or 16-bits per cycle.

Only multiple cycle transfers caused by internal requests are considered in this section. Cacheable cycles and 8- and 16-bit transfers are covered in section 10.2.3, ''Cacheable Cycles'' and section 10.2.5, ''8- and 16-Bit Cycles.''

Internal Requests from Military Intel486 DX, IntelDX2, and IntelDX4 Processors

An internal request by a Military Intel486 DX, IntelDX2, or IntelDX4 processor for a 64-bit floating point load must take more than one internal cycle.

10.2.2.1 Burst Cycles

The Military Intel486 processor can accept burst cycles for any bus requests that require more than a single data cycle. During burst cycles, a new data item is strobed into the Military Intel486 processor every clock rather than every other clock as in non-burst cycles. The fastest burst cycle requires 2 clocks for the first data item with subsequent data items returned every clock.

The Military Intel486 processor is capable of bursting a maximum of 32 bits during a write. Burst writes can only occur if BS8# or BS16# is asserted. For example, the Military Intel486 processor can burst write four 8-bit operands or two 16-bit operands in a single burst cycle. But the Military Intel486 processor cannot burst multiple 32-bit writes in a single burst cycle.

Burst cycles begin with the Military Intel486 processor driving out an address and asserting ADS# in the same manner as non-burst cycles. The Military Intel486 processor indicates that it is willing to perform a burst cycle by holding the burst last signal (BLAST#) inactive in the second clock of the cycle. The external system indicates its willingness to do a burst cycle by returning the burst ready signal (BRDY#) active.

The addresses of the data items in a burst cycle will all fall within the same 16-byte aligned area (corresponding to an internal Military Intel486 processor cache line). A 16-byte aligned area begins at location XXXXXXX0 and ends at location XXXXXXXF. During a burst cycle, only BE0–3#, A_2, and A_3 may change. A_4–A_{31}, M/IO#, D/C#, and W/R# will remain stable throughout a burst. Given the first address in a burst, external hardware can easily calculate the address of subsequent transfers in advance. An external memory system can be designed to quickly fill the Military Intel486 processor internal cache lines.

Burst cycles are not limited to cache line fills. Any multiple cycle read request by the Military Intel486 processor can be converted into a burst cycle. The Military Intel486 processor will only burst the number of bytes needed to complete a transfer.

For example, the Military Intel486 DX, IntelDX2, Write-Back Enhanced IntelDX2 or IntelDX4 processor will burst eight bytes for a 64-bit floating point non-cacheable read.

The external system converts a multiple cycle request into a burst cycle by returning BRDY# active rather than RDY# (non-burst ready) in the first cycle of a transfer. For cycles that cannot be burst, such as interrupt acknowledge and halt, BRDY# has the same effect as RDY#. BRDY# is ignored if both BRDY# and RDY# are returned in the same clock. Memory areas and peripheral devices that cannot perform bursting must terminate cycles with RDY#.

10.2.2.2 Terminating Multiple and Burst Cycle Transfers

The Military Intel486 processor drives BLAST# inactive for all but the last cycle in a multiple cycle transfer. BLAST# is driven inactive in the first cycle to inform the external system that the transfer could take additional cycles. BLAST# is driven active in the last cycle of the transfer indicating that the next time BRDY# or RDY# is returned the transfer is complete.

BLAST# is not valid in the first clock of a bus cycle. It should be sampled only in the second and subsequent clocks when RDY# or BRDY# is returned.

The number of cycles in a transfer is a function of several factors including the number of bytes the Military Intel486 processor needs to complete an internal request (1, 2, 4, 8, or 16), the state of the bus size inputs (BS8# and BS16#), the state of the cache enable input (KEN#) and alignment of the data to be transferred.

When the Military Intel486 processor initiates a request it knows how many bytes will be transferred and if the data is aligned. The external system must indicate whether the data is cacheable (if the transfer is a read) and the width of the bus by returning the state of the KEN#, BS8# and BS16# inputs one clock before RDY# or BRDY# is returned. The Military Intel486 processor determines how many cycles a transfer will take based on its internal information and inputs from the external system.

BLAST# is not valid in the first clock of a bus cycle because the Military Intel486 processor cannot determine the number of cycles a transfer will take until the external system returns KEN#, BS8# and BS16#. BLAST# should only be sampled in the second and subsequent clocks of a cycle when the external system returns RDY# or BRDY#.

The system may terminate a burst cycle by returning RDY# instead of BRDY#. BLAST# will remain deasserted until the last transfer. However, any transfers required to complete a cache line fill will follow the burst order, e.g., if burst order was 4, 0, C, 8 and RDY# was returned at after 0, the next transfers will be from C and 8.

10.2.2.3 Non-Cacheable, Non-Burst, Multiple Cycle Transfers

Figure 10-9 illustrates a 2 cycle non-burst, non-cacheable multiple cycle read. This transfer is simply a sequence of two single cycle transfers. The Military Intel486 processor indicates to the external system that this is a multiple cycle transfer by driving BLAST# inactive during the second clock of the first cycle. The external system returns RDY# active indicating that it will not burst the data. The external system also indicates that the data is not cacheable by returning KEN# inactive one clock before it returns RDY# active. When the Military Intel486 processor samples RDY# active it ignores BRDY#.

Each cycle in the transfer begins when ADS# is driven active and the cycle is complete when the external system returns RDY# active.

The Military Intel486 processor indicates the last cycle of the transfer by driving BLAST# active. The next RDY# returned by the external system terminates the transfer.

10.2.2.4 Non-Cacheable Burst Cycles

The external system converts a multiple cycle request into a burst cycle by returning BRDY# active rather than RDY# in the first cycle of the transfer. This is illustrated in Figure 10-10.

There are several features to note in the burst read. ADS# is only driven active during the first cycle of the transfer. RDY# must be driven inactive when BRDY# is returned active.

BLAST# behaves exactly as it does in the non-burst read. BLAST# is driven inactive in the second clock of the first cycle of the transfer indicating more cycles to follow. In the last cycle, BLAST# is driven active telling the external memory system to end the burst after returning the next BRDY#.

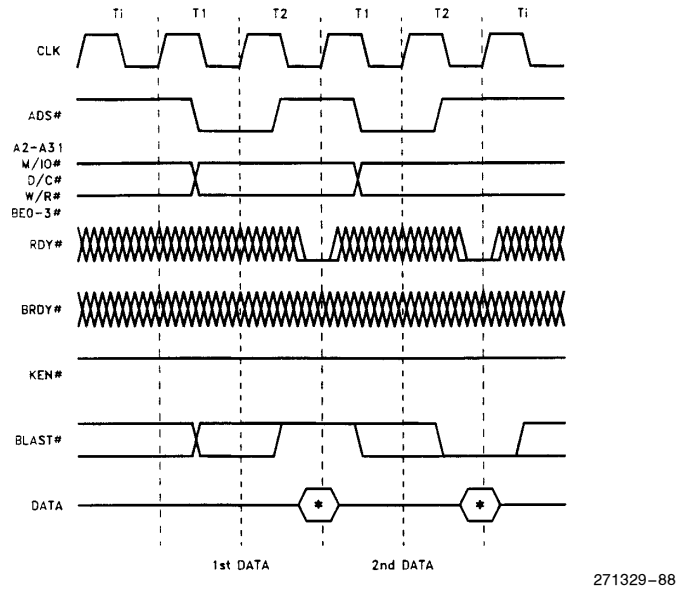


Figure 10-9. Non-Cacheable, Non-Burst, Multiple-Cycle Transfers

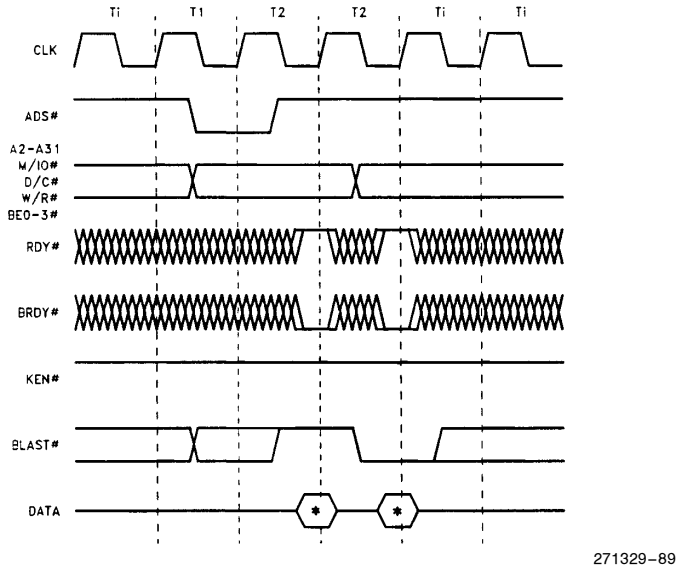


Figure 10-10. Non-Cacheable Burst Cycle

10.2.3 CACHEABLE CYCLES

Any memory read can become a cache fill operation. The external memory system can allow a read request to fill a cache line by returning KEN# active one clock before RDY# or BRDY# during the first cycle of the transfer on the external bus. Once KEN# is asserted and the remaining three requirements described below are met, the Military Intel486 processor will fetch an entire cache line regardless of the state of KEN#. KEN# must be returned active in the last cycle of the transfer for the data to be written into the internal cache. The Military Intel486 processor will only convert memory reads or prefetches into a cache fill.

KEN# is ignored during write or I/O cycles. Memory writes will only be stored in the on-chip cache if there is a cache hit. I/O space is never cached in the internal cache.

To transform a read or a prefetch into a cache line fill the following conditions must be met:

1. The KEN# pin must be asserted one clock prior to RDY# or BRDY# being returned for the first data cycle.
2. The cycle must be of the type that can be internally cached. (Locked reads, I/O reads, and interrupt acknowledge cycles are never cached).
3. The page table entry must have the page cache disable bit (PCD) set to 0. To cache a page table entry, the page directory must have PCD = 0. To cache reads or prefetches when paging is disabled, or to cache the page directory entry, control register 3 (CR3) must have PCD = 0.
4. The cache disable (CD) bit in control register 0 (CR0) must be clear.

External hardware can determine when the Military Intel486 processor has transformed a read or prefetch into a cache fill by examining the KEN#, M/IO#, D/C#, W/R#, LOCK#, and PCD pins. These pins convey to the system the outcome of conditions 1–3 in the above list. In addition, the Military Intel486 processor drives PCD high whenever the CD bit in CR0 is set, so that external hardware can evaluate condition 4.

Cacheable cycles can be burst or non-burst.

10.2.3.1 Byte Enables during a Cache Line Fill

For the first cycle in the line fill, the state of the byte enables should be ignored. In a non-cacheable memory read, the byte enables indicate the bytes actually required by the memory or code fetch.

The Military Intel486 processor expects to receive valid data on its entire bus (32 bits) in the first cycle of a cache line fill. Data should be returned with the assumption that all the byte enable pins are driven active. However if BS8# is asserted only one byte need be returned on data lines D0–D7. Similarly if BS16# is asserted two bytes should be returned on D0–D15.

The Military Intel486 processor will generate the addresses and byte enables for all subsequent cycles in the line fill. The order in which data is read during a line fill depends on the address of the first item read. Byte ordering is discussed in section 10.2.4, ‘‘Burst Mode Details.’’

10.2.3.2 Non-Burst Cacheable Cycles

Figure 10-11 shows a non-burst cacheable cycle. The cycle becomes a cache fill when the Military Intel486 processor samples KEN# active at the end of the first clock. The Military Intel486 processor drives BLAST# inactive in the second clock in response to KEN#. BLAST# is driven inactive because a cache fill requires 3 additional cycles to complete. BLAST# remains inactive until the last transfer in the cache line fill. KEN# must be returned active in the last cycle of the transfer for the data to be written into the internal cache.

Note that this cycle would be a single bus cycle if KEN# was not sampled active at the end of the first clock. The subsequent three reads would not have happened since a cache fill was not requested.

The BLAST# output is invalid in the first clock of a cycle. BLAST# may be active during the first clock due to earlier inputs. Ignore BLAST# until the second clock.

During the first cycle of the cache line fill the external system should treat the byte enables as if they are all active. In subsequent cycles in the burst, the Military Intel486 processor drives the address lines and byte enables. (See section 10.2.4.2, ''Burst and Cache Line Fill Order'') .

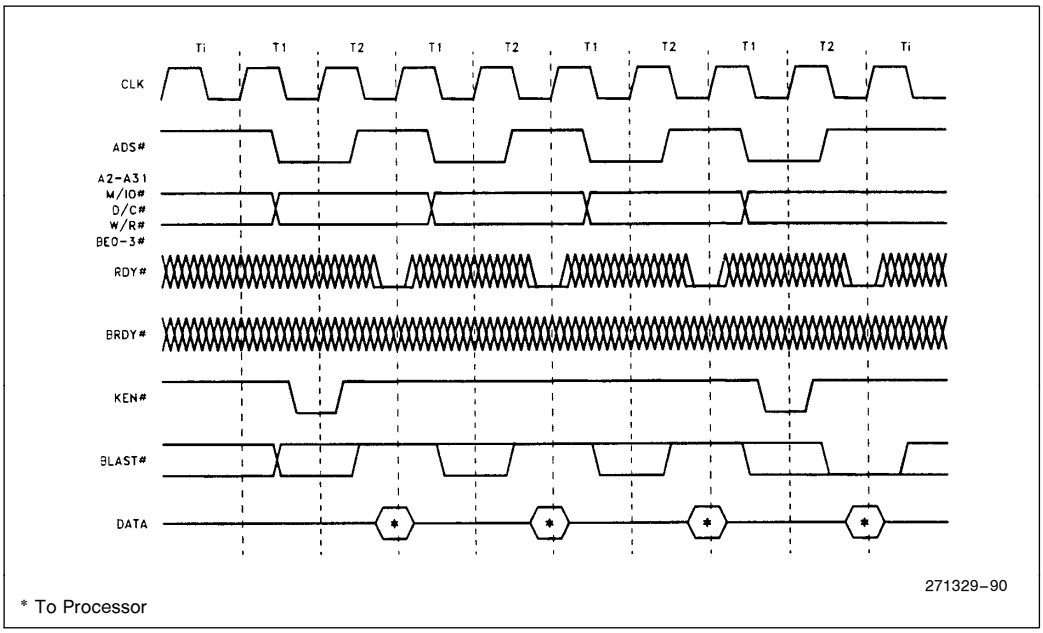


Figure 10-11. Non-Burst, Cacheable Cycles

10.2.3.3 Burst Cacheable Cycles

Figure 10-12 illustrates a burst mode cache fill. As in Figure 10-11, the transfer becomes a cache line fill when the external system returns KEN# active at the end of the first clock in the cycle.

The external system informs the Military Intel486 processor that it will burst the line in by driving BRDY# active at the end of the first cycle in the transfer.

Note that during a burst cycle, ADS# is only driven with the first address.

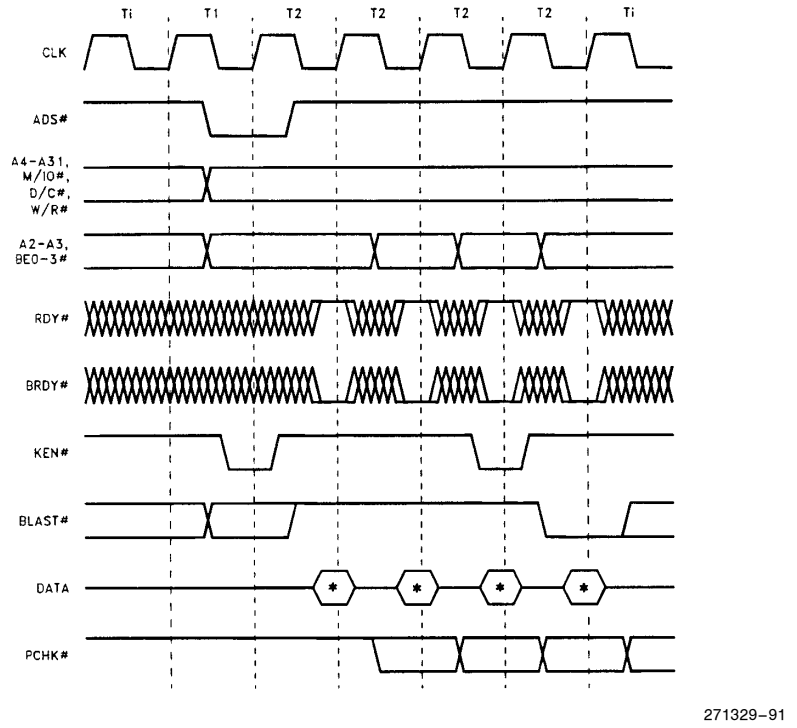


Figure 10-12. Burst Cacheable Cycle

10.2.3.4 Effect of Changing KEN# during a Cache Line Fill

KEN# can change multiple times as long as it arrives at its final value in the clock before RDY# or BRDY# is returned. This is illustrated in Figure 10-13. Note that the timing of BLAST# follows that of KEN# by one clock. The Military Intel486 processor samples KEN# every clock and uses the value returned in the clock before ready to determine if a bus cycle would be a cache line fill. Similarly, it uses the value of KEN# in the last cycle before early RDY# to load the line just retrieved from memory into the cache. KEN# is sampled every clock and it must satisfy setup and hold time.

KEN# can also change multiple times before a burst cycle, as long as it arrives at its final value one clock before ready is returned active.

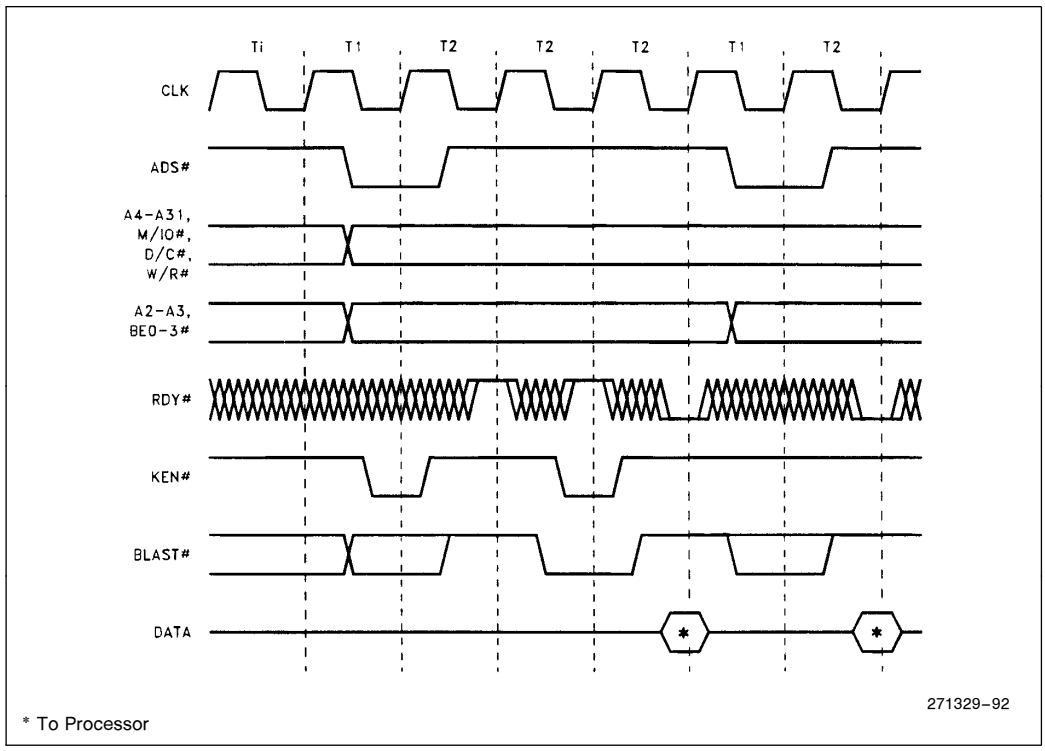


Figure 10-13. Effect of Changing KEN#

10.2.4 BURST MODE DETAILS

10.2.4.1 Adding Wait States to Burst Cycles

Burst cycles need not return data on every clock. The Military Intel486 processor will only strobe data into the chip when either RDY# or BRDY# are active. Driving BRDY# and RDY# inactive adds a wait state to the transfer. A burst cycle where two clocks are required for every burst item is shown in Figure 10-14.

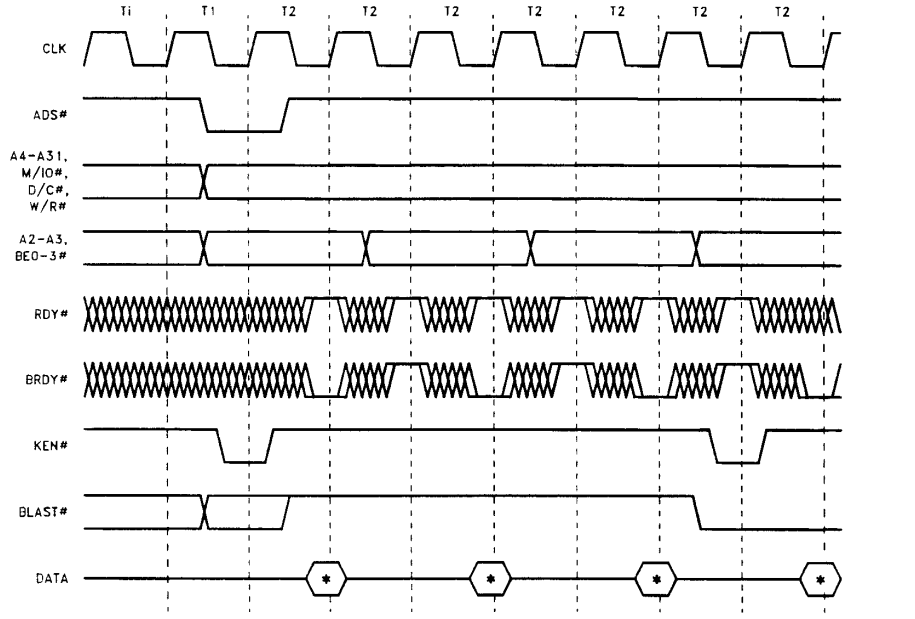


Figure 10-14. Slow Burst Cycle

10.2.4.2 Burst and Cache Line Fill Order

The burst order used by the Military Intel486 processor is shown in Table 10-8. This burst order is followed by any burst cycle (cache or not), cache line fill (burst or not) or code prefetch.

The Military Intel486 processor presents each request for data in an order determined by the first address in the transfer. For example, if the first address was 104 the next three addresses in the burst will be 100, 10C and 108. An example of burst address sequencing is shown in Figure 10-15.

Table 10-8. Burst Order (Both Read and Write Bursts)

First Addr.	Second Addr.	Third Addr.	Fourth Addr.
0	4	8	C
4	0	C	8
8	C	0	4
C	8	4	0

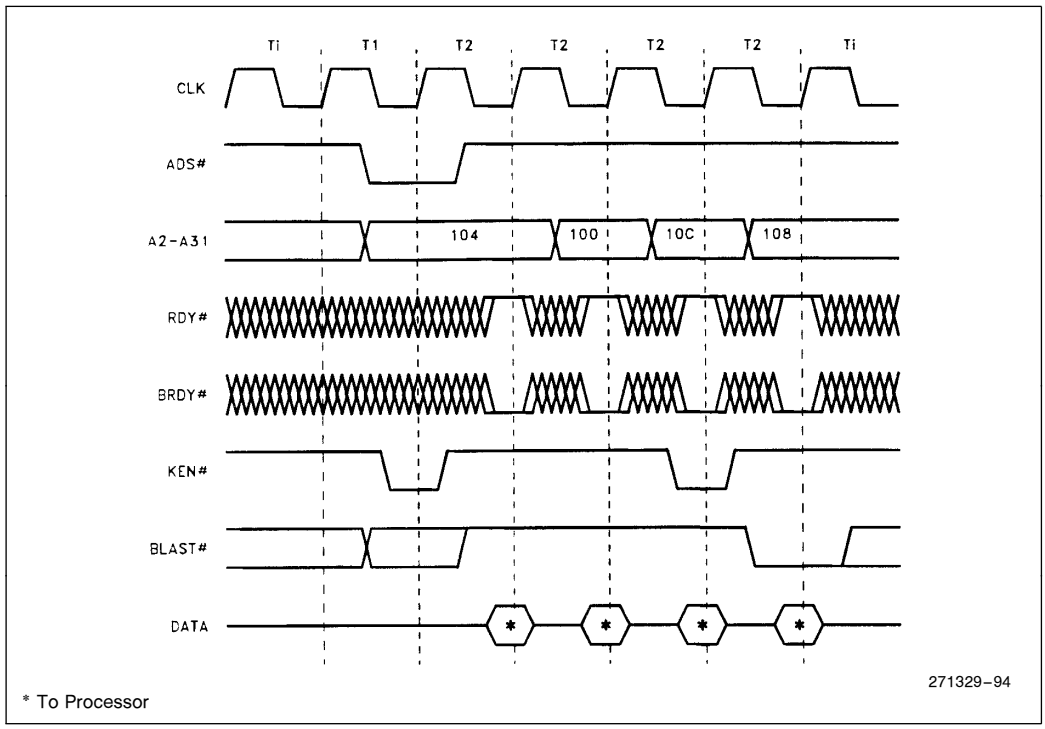


Figure 10-15. Burst Cycle Showing Order of Addresses

The sequences shown in Table 10-8 accommodate systems with 64-bit buses as well as systems with 32-bit data buses. The sequence applies to all bursts, regardless of whether the purpose of the burst is to fill a cache line, do a 64-bit read, or do a pre-fetch. If either BS8# or BS16# is returned active, the Military Intel486 processor completes the transfer of the current 32-bit word before progressing to the next 32-bit word. For example, a BS16# burst to address 4 has the following order: 4-6-0-2-C-E-8-A.

10.2.4.3 Interrupted Burst Cycles

Some memory systems may not be able to respond with burst cycles in the order defined in Table 10-8. To support these systems the Military Intel486 processor allows a burst cycle to be interrupted at any time. The Military Intel486 processor will automatically generate another normal bus cycle after being interrupted to complete the data transfer. This is called an interrupted burst cycle. The external system can respond to an interrupted burst cycle with another burst cycle.

The external system can interrupt a burst cycle by returning RDY# instead of BRDY#. RDY# can be returned after any number of data cycles terminated with BRDY#.

An example of an interrupted burst cycle is shown in Figure 10-16. The Military Intel486 processor immediately drives ADS# active to initiate a new bus cycle after RDY# is returned active. BLAST# driven inactive one clock after ADS# begins the second bus cycle indicating that the transfer is not complete.

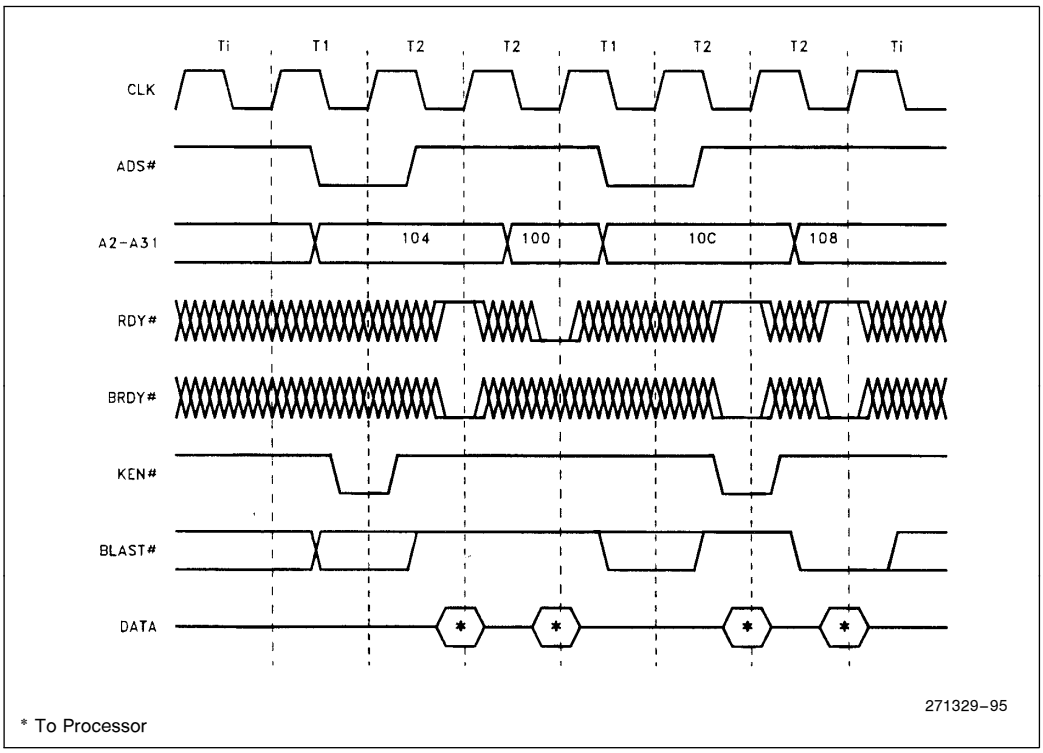


Figure 10-16. Interrupted Burst Cycle

KEN# need not be returned active in the first data cycle of the second part of the transfer in Figure 10-16. The cycle had been converted to a cache fill in the first part of the transfer and the Military Intel486 processor expects the cache fill to be completed. Note that the first half and second half of the transfer in Figure 10-16 are each two cycle burst transfers.

The order in which the Military Intel486 processor requests operands during an interrupted burst transfer is determined by Table 10-7. Mixing RDY# and BRDY# does not change the order in which operand addresses are requested by the Military Intel486 processor.

An example of the order in which the Military Intel486 processor requests operands during a cycle in which the external system mixes RDY# and BRDY# is shown in Figure 10-17. The Military Intel486 processor initially requests a transfer beginning at location 104. The transfer becomes a cache line fill when the external system returns KEN# active. The first cycle of the cache fill transfers the contents of location 104 and is terminated with RDY#. The Military Intel486 processor drives out a new request (by asserting ADS#) to address 100. If the external system terminates the second cycle with BRDY#, the Military Intel486 processor will next request/expect address 10C. The correct order is determined by the first cycle in the transfer, which may not be the first cycle in the burst if the system mixes RDY# with BRDY#.

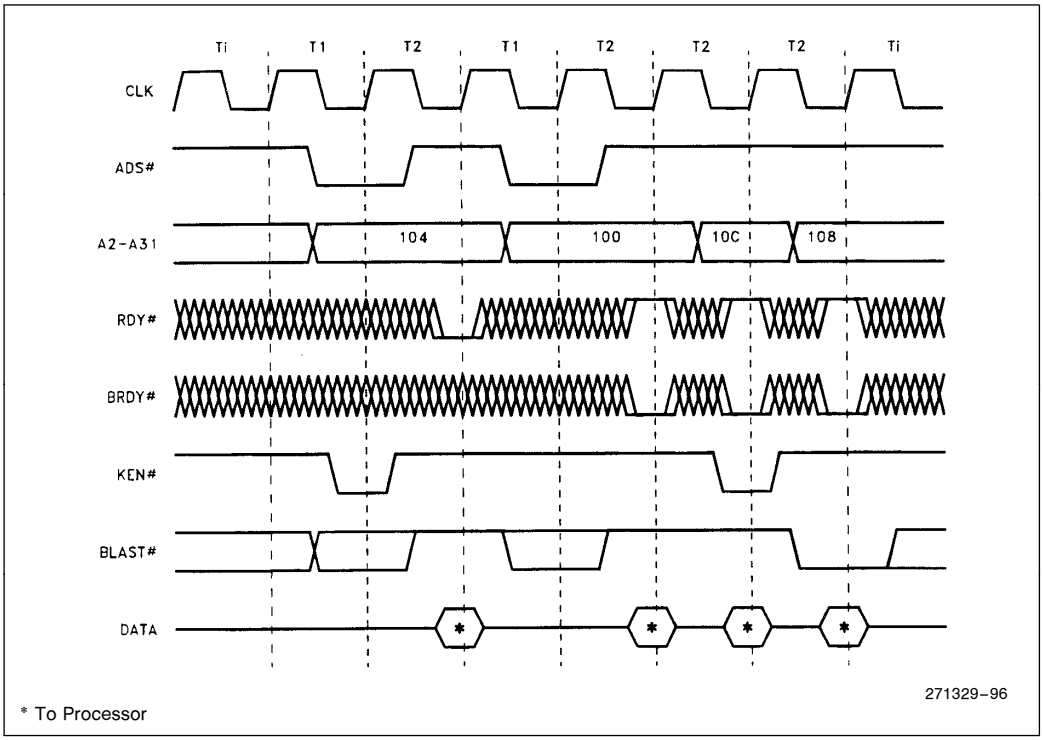


Figure 10-17. Interrupted Burst Cycle with Unobvious Order of Addresses

10.2.5 8- AND 16-BIT CYCLES

The Military Intel486 processor supports both 16- and 8-bit external buses through the BS16# and BS8# inputs. BS16# and BS8# allow the external system to specify, on a cycle by cycle basis, whether the addressed component can supply 8, 16 or 32 bits. BS16# and BS8# can be used in burst cycles as well as non-burst cycles. If both BS16# and BS8# are returned active for any bus cycle, the Military Intel486 processor will respond as if only BS8# were active.

The timing of BS16# and BS8# is the same as that of KEN#. BS16# and BS8# must be driven active before the first RDY# or BRDY# is driven active. Driving the BS16# and BS8# active can force the Military Intel486 processor to run additional cycles to complete what would have been only a single 32-bit cycle. BS8# and BS16# may change the state of BLAST# when they force subsequent cycles from the transfer.

Figure 10-18. shows an example in which BS8# forces the Military Intel486 processor to run two extra cycles to complete a transfer. The Military Intel486 processor issues a request for 24 bits of information. The external system drives BS8# active indicating that only eight bits of data can be supplied per cycle. The Military Intel486 processor issues two extra cycles to complete the transfer.

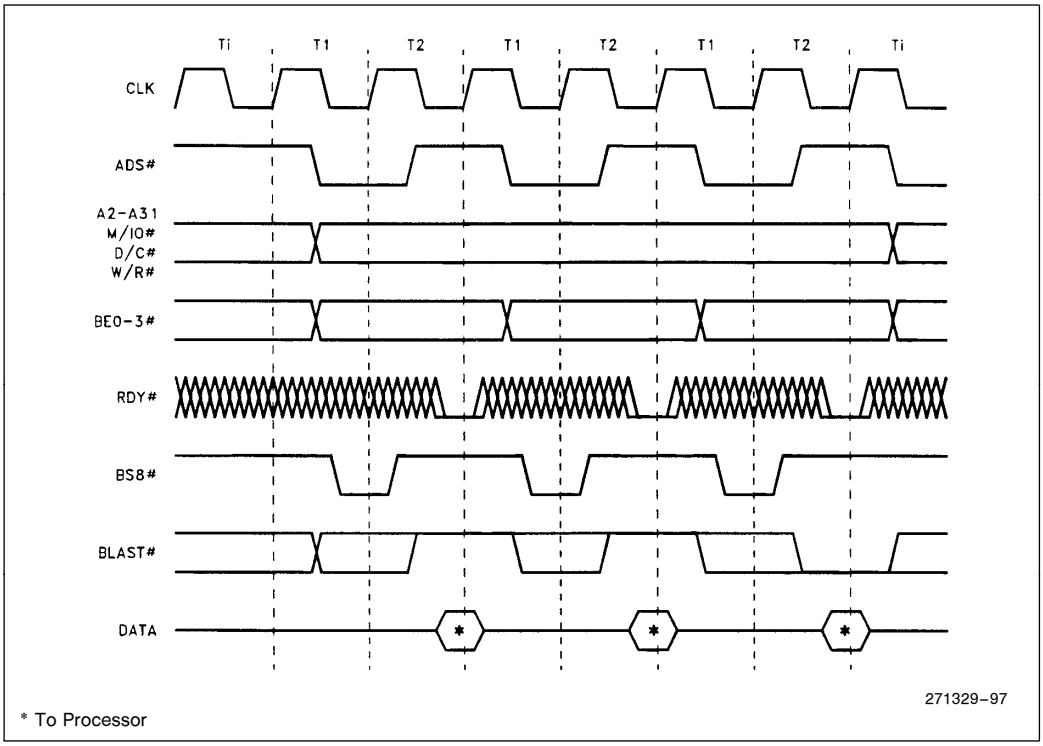


Figure 10-18. 8-Bit Bus Size Cycle

Extra cycles forced by the BS16# and BS8# should be viewed as independent bus cycles. BS16# and BS8# should be driven active for each additional cycle unless the addressed device has the ability to change the number of bytes it can return between cycles. The Military Intel486 processor will drive BLAST# inactive until the last cycle before the transfer is complete.

Refer to section 10.1.2, ''Dynamic Data Bus Sizing,'' for the sequencing of addresses while BS8# or BS16# are active.

BS8# and BS16# operate during burst cycles in exactly the same manner as non-burst cycles. For example, a single non-cacheable read could be transferred by the Military Intel486 processor as four 8-bit burst data cycles. Similarly, a single 32-bit write could be written as four 8-bit burst data cycles. An example of a burst write is shown in Figure 10-19. Burst writes can only occur if BS8# or BS16# is asserted.

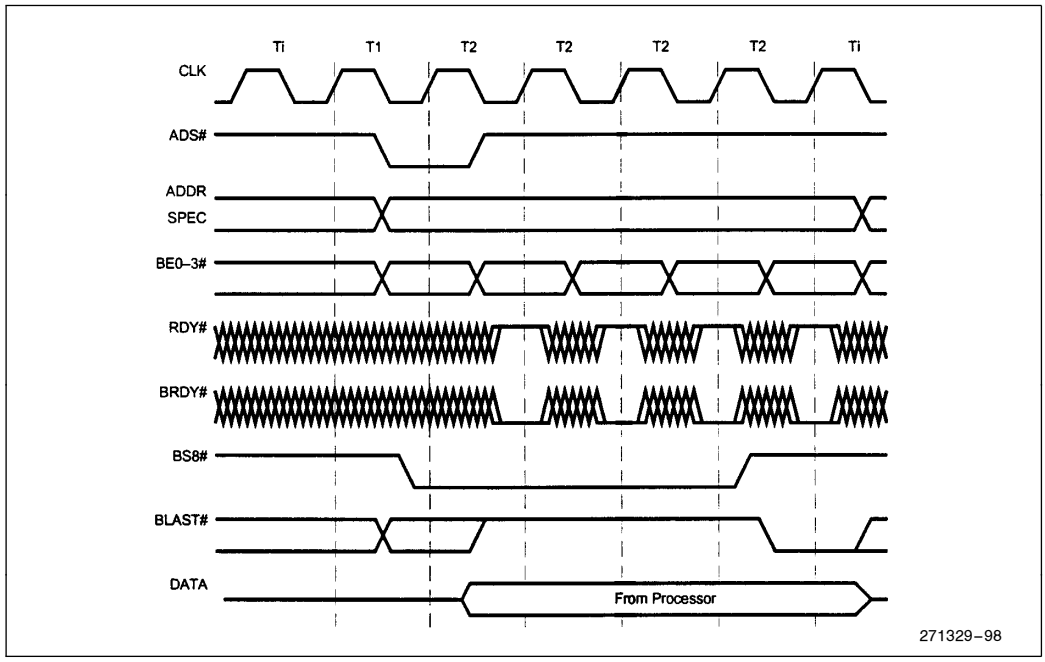


Figure 10-19. Burst Write as a Result of BS8# or BS16#

10.2.6 LOCKED CYCLES

Locked cycles are generated in software for any instruction that performs a read-modify-write operation. During a read-modify-write operation the Military Intel486 processor can read and modify a variable in external memory and be assured that the variable is not accessed between the read and write.

Locked cycles are automatically generated during certain bus transfers. The XCHG (exchange) instruction generates a locked cycle when one of its operands is memory based. Locked cycles are generated when a segment or page table entry is updated and during interrupt acknowledge cycles. Locked cycles are also generated when the LOCK instruction prefix is used with selected instructions.

Locked cycles are implemented in hardware with the LOCK# pin. When LOCK# is active, the Military Intel486 processor is performing a read-modify-write operation and the external bus should not be relinquished until the cycle is complete. Multiple reads or writes can be locked. A locked cycle is shown in Figure 10-20. LOCK# goes active with the address and bus definition pins at the beginning of the first read cycle and remains active until RDY# is returned for the last write cycle. For unaligned 32 bits read-modify-write operation, the LOCK# remains active for the entire duration of the multiple cycle. It will go inactive when RDY# is returned for the last write cycle.

When LOCK# is active, the Military Intel486 processor will recognize address hold and backoff but will not recognize bus hold. It is left to the external system to properly arbitrate a central bus when the Military Intel486 processor generates LOCK#.

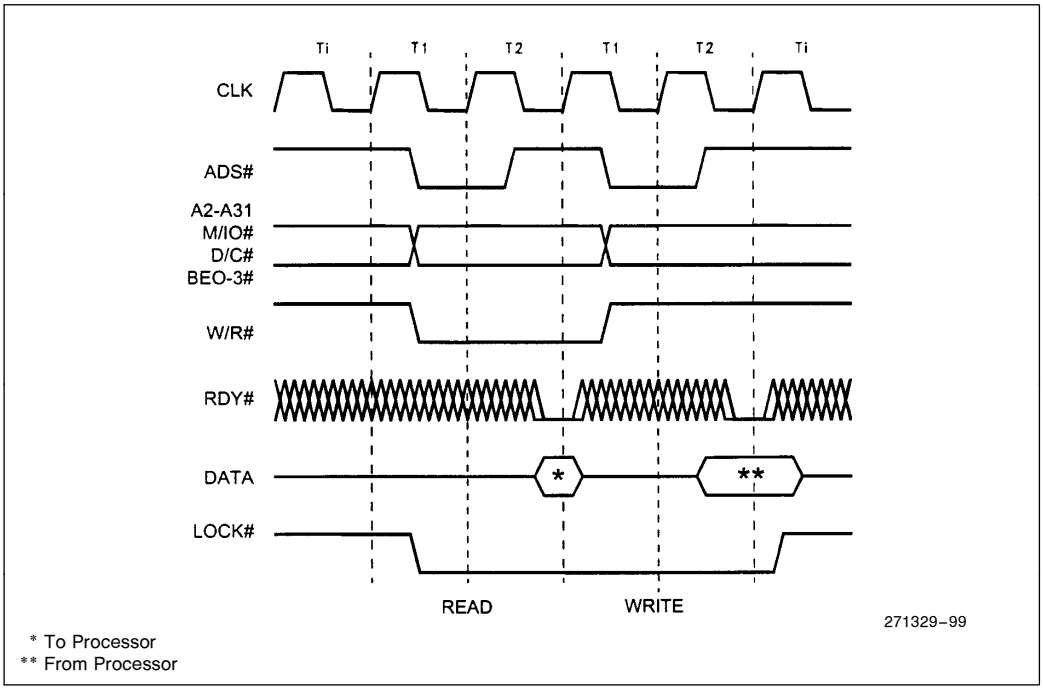


Figure 10-20. Locked Bus Cycle

10.2.7 PSEUDO-LOCKED CYCLES

Pseudo-locked cycles assure that no other master will be given control of the bus during operand transfers which take more than one bus cycle.

For the Military Intel486 processor, examples include 64-bit description loads and cache line fills.

Pseudo-locked transfers are indicated by the PLOCK# pin. The memory operands must be aligned for correct operation of a pseudo-locked cycle.

PLOCK# need not be examined during burst reads. A 64-bit aligned operand can be retrieved in one burst (note: this is only valid in systems that do not interrupt bursts).

The system must examine PLOCK# during 64-bit writes since the Military Intel486 processor cannot burst write more than 32 bits. However, burst can be used within each 32-bit write cycle if BS8# or BS16# is asserted. BLAST will be de-asserted in response to BS8# or BS16#. A 64-bit write will be driven out as two non-burst bus cycles. BLAST# is asserted during both writes since a burst is not possible. PLOCK# is asserted during the first write to indicate that another write follows. This behavior is shown in Figure 10-21.

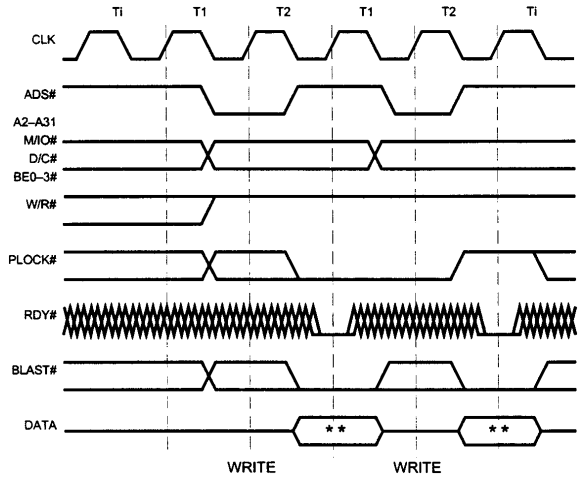
The first cycle of a 64-bit floating point write is the only case in which both PLOCK# and BLAST# are asserted. Normally PLOCK# and BLAST# are the inverse of each other.

During all of the cycles where PLOCK# is asserted, HOLD is not acknowledged until the cycle completes. This results in a large HOLD latency, especially when BS8# or BS16# is asserted. To reduce the HOLD latency during these cycles, windows are available between transfers to allow HOLD to be acknowledged during non-cacheable code prefetches. PLOCK# will be asserted since BLAST# is negated, but it is ignored and HOLD is recognized during the prefetch.

PLOCK# can change several times during a cycle settling to its final value in the clock ready is returned.

10.2.7.1 Floating Point Read and Write Cycles

For Military Intel486 DX, IntelDX2, Write-Back Enhanced IntelDX2, and IntelDX4 processors, 64-bit floating point read and write cycles are also examples of operand transfers that take more than one bus cycle.



** From Processor

Figure 10-21. Pseudo Lock Timing

10.2.8 INVALIDATE CYCLES

Invalidate cycles are needed to keep the Military Intel486 processor internal cache contents consistent with external memory. The Military Intel486 processor contains a mechanism for listening to writes by other devices to external memory. When the Military Intel486 processor finds a write to a section of external memory contained in its internal cache, the Military Intel486 processor's internal copy is invalidated.

Invalidations use two pins, address hold request (AHOLD) and valid external address (EADS#). There are two steps in an invalidation cycle. First, the external system asserts the AHOLD input forcing the Military Intel486 processor to immediately relinquish its address bus. Next, the external system asserts EADS# indicating that a valid address is on the Military Intel486 processor address bus. Figure 10-22 shows the fastest possible invalidation cycle. The Military Intel486 processor recognizes AHOLD on one CLK edge and floats the address bus in response. To allow the address bus to float and avoid contention, EADS# and the invalidation address should not be driven until the following CLK edge. The Military Intel486 processor reads the address over its address lines. If the Military Intel486 processor finds this address in its internal cache, the cache entry is invalidated. Note that the Military Intel486 processor address bus is input/output, unlike the Intel386 processor's bus, which is output only.

The Military Intel486 processor immediately relinquishes its address bus in the next clock upon assertion of AHOLD. For example, the bus could be 3 wait states into a read cycle. If AHOLD is activated, the Military Intel486 processor will immediately float its address bus before ready is returned terminating the bus cycle.

When AHOLD is asserted only the address bus is floated, the data bus can remain active. Data can be returned for a previously specified bus cycle during address hold. (See Figure 10-22 and Figure 10-23.)

EADS# is normally asserted when an external master drives an address onto the bus. AHOLD need not be driven for EADS# to generate an internal invalidate. If EADS# alone is asserted while the Military Intel486 processor is driving the address bus, it is possible that the invalidation address will come from the Military Intel486 processor itself.

Note that it is also possible to run an invalidation cycle by asserting EADS# when BOFF# is asserted or after HLDA has been returned, following the assertion of HOLD.

Running an invalidate cycle prevents the Military Intel486 processor cache from satisfying other internal requests, so invalidations should be run only when necessary. The fastest possible invalidate cycle is shown in Figure 10-22, while a more realistic invalidation cycle is shown in Figure 10-23. Both of the examples take one clock of cache access from the Military Intel486 processor.

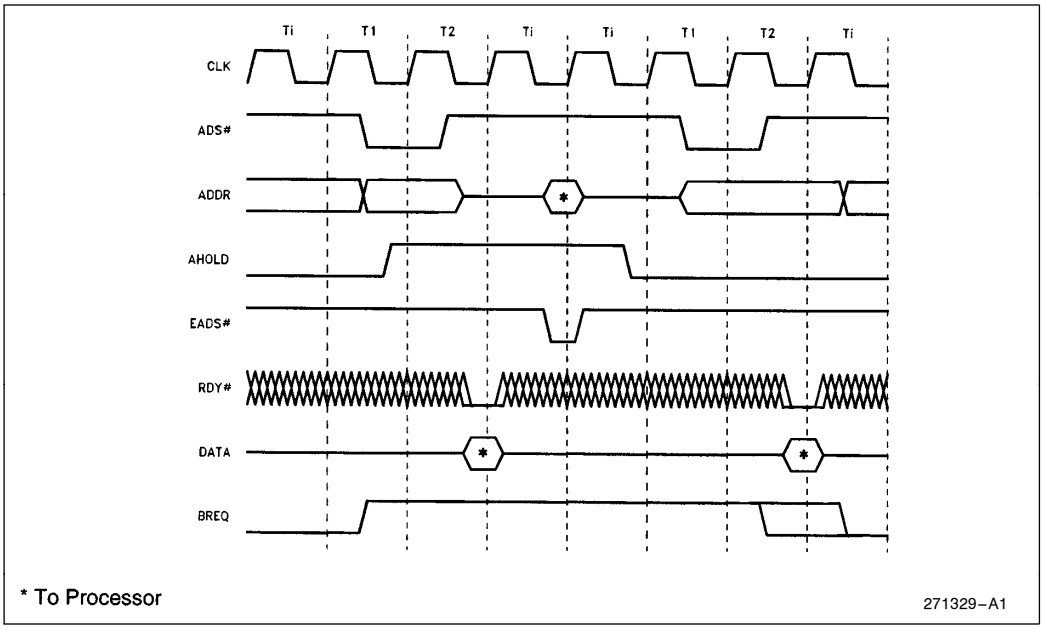


Figure 10-22. Fast Internal Cache Invalidation Cycle

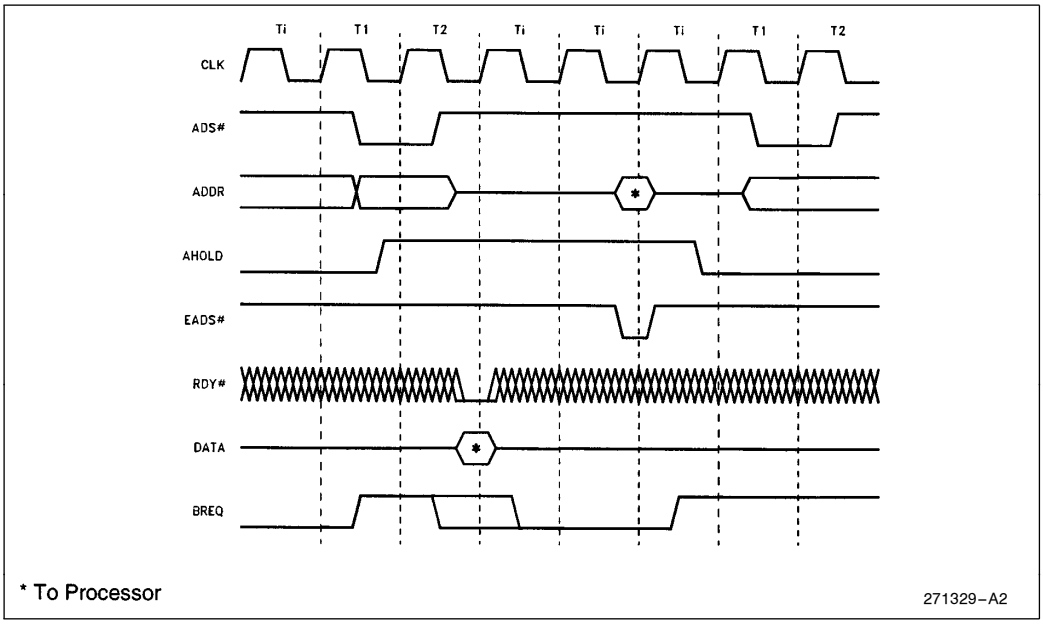


Figure 10-23. Typical Internal Cache Invalidation Cycle

10.2.8.1 Rate of Invalidate Cycles

The Military Intel486 processor can accept one invalidate per clock except in the last clock of a line fill. One invalidate per clock is possible as long as EADS# is negated in ONE or BOTH of the following cases:

1. In the clock RDY# or BRDY# is returned for the last time.
2. In the clock following RDY# or BRDY# being returned for the last time.

This definition allows two system designs. Simple designs can restrict invalidates to one every other clock. The simple design need not track bus activity. Alternatively, systems can request one invalidate per clock provided that the bus is monitored.

10.2.8.2 Running Invalidate Cycles Concurrently with Line Fills

Precautions are necessary to avoid caching stale data in the Military Intel486 processor cache in a system with a second level cache. An example of a system with a second level cache is shown in Figure 10-24.

An external device can be writing to main memory over the system bus while the Military Intel486 processor is retrieving data from the second level cache.

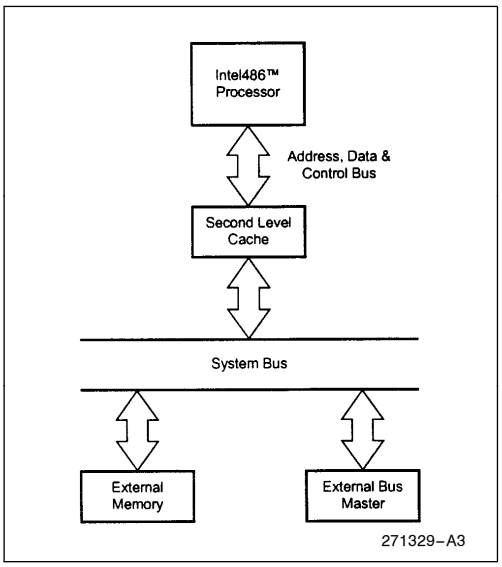


Figure 10-24. System with Second Level Cache

The Military Intel486 processor will need to invalidate a line in its internal cache if the external device is writing to a main memory address also contained in the Military Intel486 processor cache.

A potential problem exists if the external device is writing to an address in external memory, and at the same time the Military Intel486 processor is reading data from the same address in the second level cache. The system must force an invalidation cycle to invalidate the data that the Military Intel486 processor has requested during the line fill.

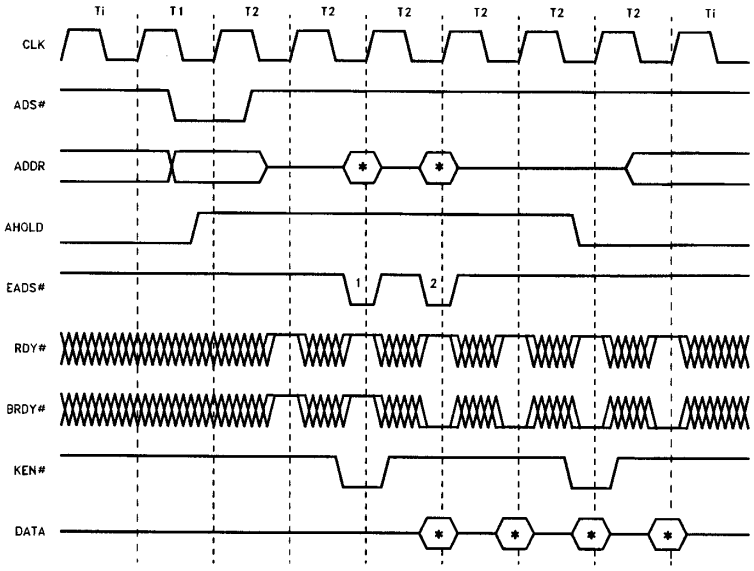
If the system asserts EADS# before the first data in the line fill is returned to the Military Intel486 processor, the system must return data consistent with the new data in the external memory upon resumption of the line fill after the invalidation cycle. This is illustrated by the asserted EADS# signal labeled 1 in Figure 10-25.

If the system asserts EADS# at the same time or after the first data in the line fill is returned (in the same clock that the first RDY# or BRDY# is returned or any subsequent clock in the line fill) the data will be read into the Military Intel486 processor input buffers but it will not be stored in the on-chip cache. This is illustrated by asserted EADS# signal labeled 2 in Figure 10-25. The stale data will be used to satisfy the request that initiated the cache fill cycle.

10.2.9 BUS HOLD

The Military Intel486 processor provides a bus hold, hold acknowledge protocol using the bus hold request (HOLD) and bus hold acknowledge (HLDA) pins. Asserting the HOLD input indicates that another bus master desires control of the Military Intel486 processor bus. The Military Intel486 processor will respond by floating its bus and driving HLDA active when the current bus cycle, or sequence of locked cycles is complete. An example of a HOLD/HLDA transaction is shown in Figure 10-26. Unlike the Intel386 processor, the Military Intel486 processor can respond to HOLD by floating its bus and asserting HLDA while RESET is asserted.

Note that HOLD will be recognized during un-aligned writes (less than or equal to 32-bits) with BLAST# being active for each write. For greater than 32-bit or un-aligned write, HOLD# recognition is prevented by PLOCK# getting asserted. However, HOLD is recognized during non-cacheable, non-burstable code prefetches even though PLOCK# is active.

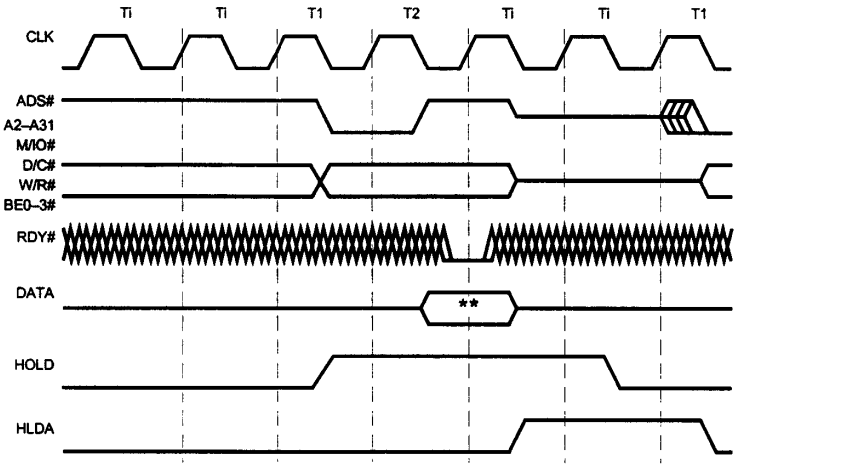


NOTES:
1. Data returned must be consistent if its address equals the invalidation address in this clock
2. Data returned will not be cached if its address equals the invalidation address in this clock

Figure 10-25. Cache Invalidation Cycle Concurrent with Line Fill

For cacheable and non-bursted or bursted cycles, HOLD is acknowledged during backoff only if HOLD and BOFF# are asserted during an active bus cycle (after ADS# asserted) and before the first RDY# or BRDY# has been returned (see Figure 10-27). The order in which HOLD and BOFF# go active is unimportant (so long as both are active prior to the first RDY#/BRDY# returned by the system). Figure 10-27 shows the case where HOLD is asserted first; HOLD could be asserted simultaneously or after BOFF# and still be acknowledged.

The pins floated during bus hold are: BE0#–BE3#, PCD, PWT, W/R#, D/C#, M/IO#, LOCK#, PLOCK#, ADS#, BLAST#, D0–D31, A2–A31, DP0–DP3.



** From Processor

Figure 10-26. HOLD/HLDA Cycles

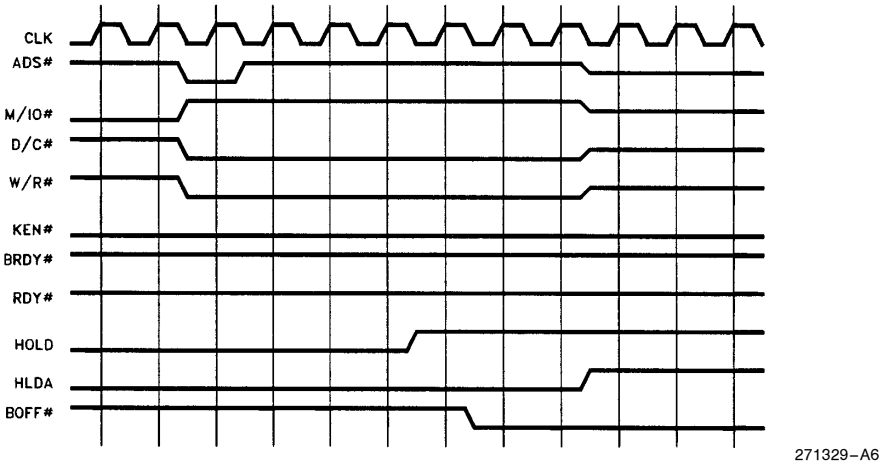


Figure 10-27. HOLD Request Acknowledged during BOFF#

10.2.10 INTERRUPT ACKNOWLEDGE

The Military Intel486 processor generates interrupt acknowledge cycles in response to maskable interrupt requests generated on the interrupt request input (INTR) pin. Interrupt acknowledge cycles have a unique cycle type generated on the cycle type pins.

An example of an interrupt acknowledge transaction is shown in Figure 10-28. Interrupt acknowledge cycles are generated in locked pairs. Data returned during the first cycle is ignored. The interrupt vector is returned during the second cycle on the lower 8 bits of the data bus. The Military Intel486 processor has 256 possible interrupt vectors.

The state of A2 distinguishes the first and second interrupt acknowledge cycles. The byte address driven during the first interrupt acknowledge cycle is 4 (A31–A3 low, A2 high, BE3#–BE1# high, and BE0# low). The address driven during the second interrupt acknowledge cycle is 0 (A31–A2 low, BE3#–BE1# high, BE0# low).

Each of the interrupt acknowledge cycles are terminated when the external system returns RDY# or BRDY#. Wait states can be added by withholding RDY# or BRDY#. The Military Intel486 processor automatically generates four idle clocks between the first and second cycles to allow for 8259A recovery time.

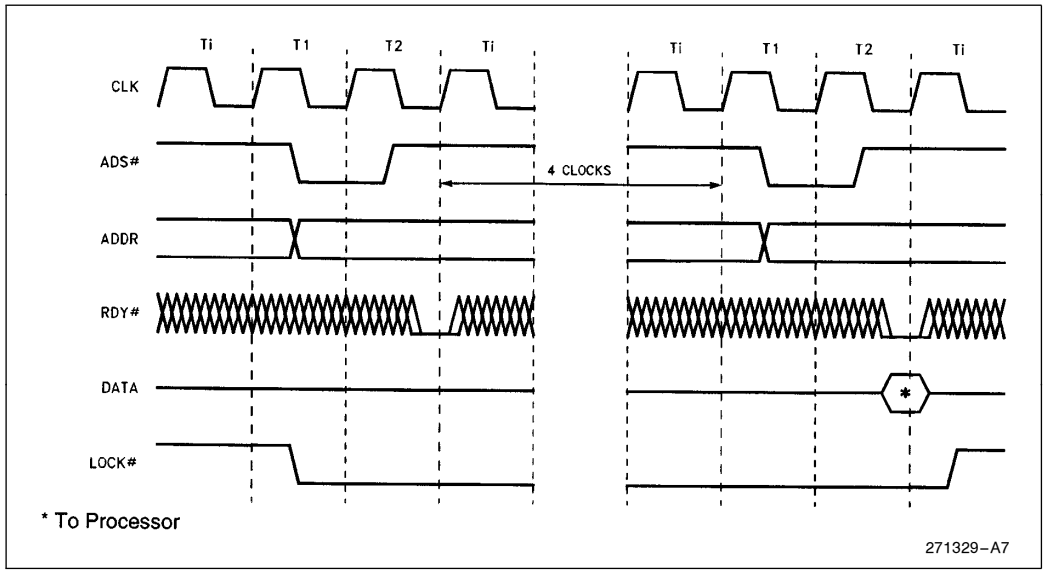


Figure 10-28. Interrupt Acknowledge Cycles

10.2.11 SPECIAL BUS CYCLES

The Military Intel486 processor provides special bus cycles to indicate that certain instructions have been executed, or certain conditions have occurred internally. The special bus cycles in Table 10-9 are defined when the bus cycle definition pins are in the following state: M/IO# = 0, D/C# = 0 and W/R# = 1.

During these cycles the address bus is driven low while the data bus is undefined.

Two of the special cycles indicate halt or shutdown. Another special cycle is generated when the Military Intel486 processor executes an INVD (invalidate data cache) instruction and could be used to flush an external cache. The Write Back cycle is generated when the Military Intel486 processor executes the WBINVD (write-back invalidate data cache) instruction and could be used to synchronize an external write-back cache.

The external hardware must acknowledge these special bus cycles by returning RDY# or BRDY#.

Table 10-9. Special Bus Cycle Encoding

Cycle Name	M/IO#	D/C#	W/R#	BE3#–BE0#	A4–A2
Write-Back	0	0	1	0111	000
Flush	0	0	1	1101	000
Shutdown	0	0	1	1110	000
HALT	0	0	1	1011	000
Stop Grant Ack Cycle	0	0	1	1011	001

NOTE:
1. See section 9.6.1, ''Stop Grant Bus Cycle,'' for details.

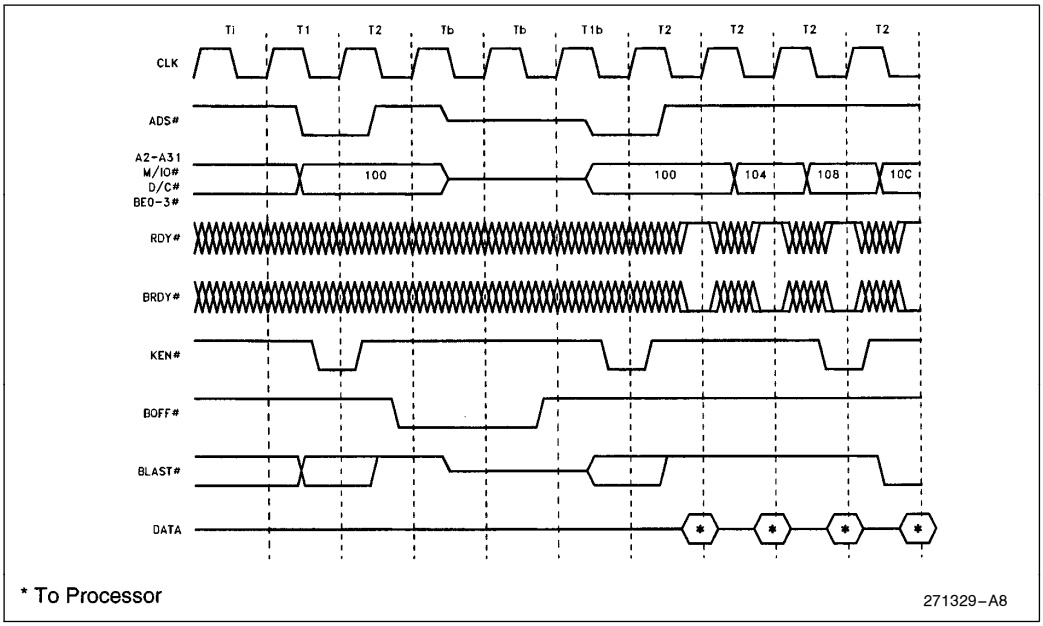


Figure 10-29. Restarted Read Cycle

10.2.11.1 HALT Indication Cycle

The Military Intel486 processor halts as a result of executing a HALT instruction. Signaling its entrance into the HALT state, a HALT indication cycle is performed. The HALT indication cycle is identified by the bus definition signals in special bus cycle state and a byte address of 2. BE0# and BE2# are the only signals distinguishing HALT indication from shutdown indication, which drives an address of 0. During the HALT cycle, undefined data is driven on D0–D31. The HALT indication cycle must be acknowledged by RDY# asserted.

A halted Military Intel486 processor resumes execution when INTR (if interrupts are enabled) or NMI or RESET is asserted.

10.2.11.2 Shutdown Indication Cycle

The Military Intel486 processor shuts down as a result of a protection fault while attempting to process a double fault. Signaling its entrance into the shutdown state, a shutdown indication cycle is performed. The shutdown indication cycle is identified by the bus definition signals in special bus cycle state and a byte address of 0.

10.2.11.3 Stop Grant Indication Cycle

A special Stop Grant bus cycle will be driven to the bus after the processor recognizes the STPCLK# interrupt. The definition of this bus cycle is the same as the HALT cycle definition for the Military Intel486 processor, with the exception that the Stop Grant bus cycle drives the value 0000 0010H on the address pins. The system hardware must acknowledge this cycle by returning RDY# or BRDY#. The processor will not enter the Stop Grant state until either RDY# or BRDY# has been returned. (See Figure 10-31.)

The Stop Grant Bus Cycle is defined as follows:

M/IO# = 0, D/C# = 0, W/R# = 1, Address Bus = 0000 0010H (A_4 = 1), BE3#–BE0# = 1011, Data bus = undefined.

The latency between a STPCLK# request and the Stop Grant bus cycle is dependent on the current instruction, the amount of data in the processor write buffers, and the system memory performance.

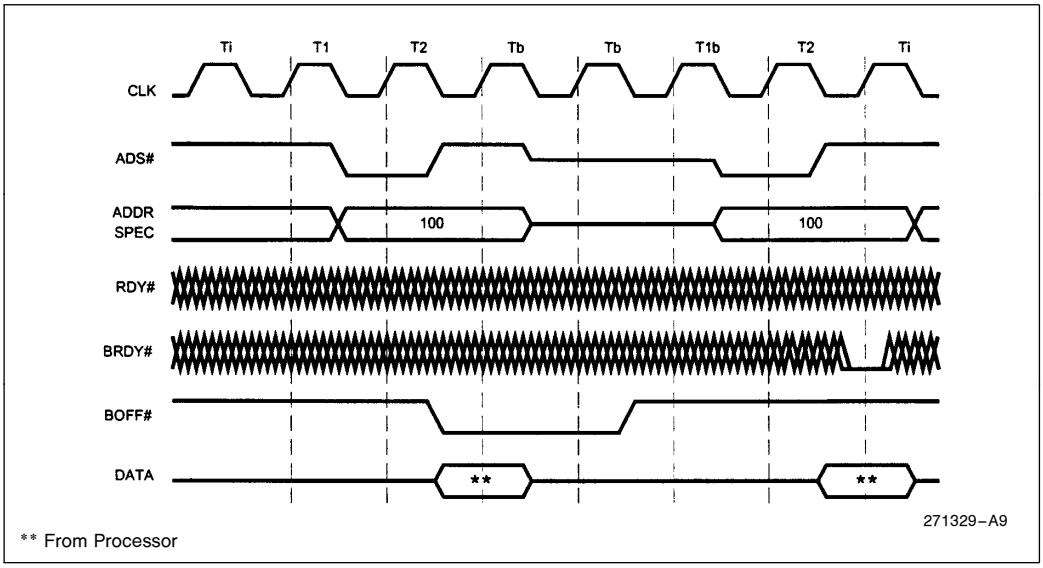


Figure 10-30. Restarted Write Cycle

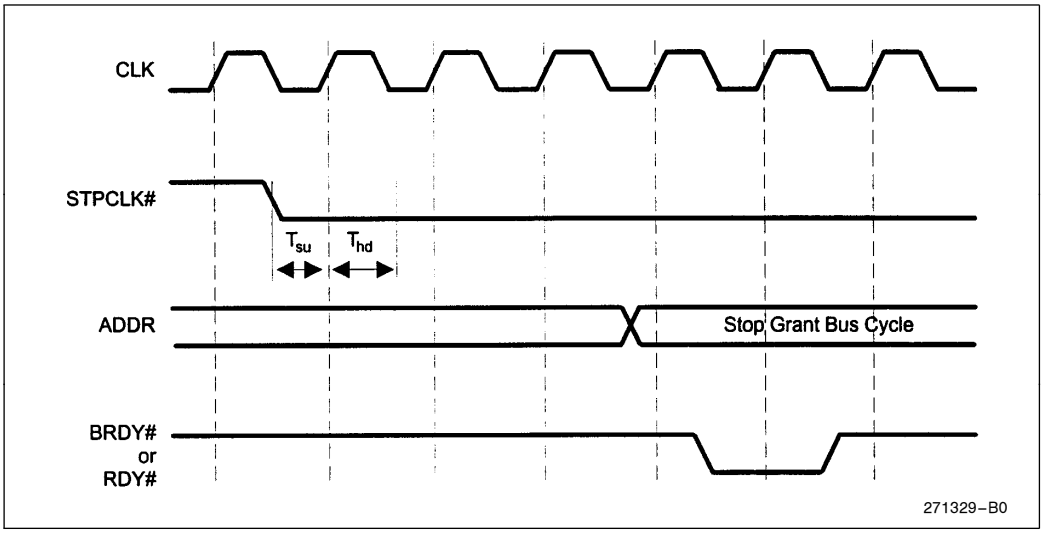


Figure 10-31. Stop Grant Bus Cycle

10.2.12 BUS CYCLE RESTART

In a multi-master system another bus master may require the use of the bus to enable the Military Intel486 processor to complete its current bus request. In this situation the Military Intel486 processor will need to restart its bus cycle after the other bus master has completed its bus transaction.

A bus cycle may be restarted if the external system asserts the backoff (BOFF#) input. The Military Intel486 processor samples the BOFF# pin every clock. The Military Intel486 processor will immediately (in the next clock) float its address, data and status pins when BOFF# is asserted (see Figures 10-29 and 10-34). Any bus cycle in progress when BOFF# is asserted is aborted and any data returned to the processor is ignored. The same pins are floated in response to BOFF# as are floated in response to HOLD. HLDA is not generated in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#. If either RDY# or BRDY# are returned in the same clock as BOFF#, BOFF# takes effect.

The device asserting BOFF# is free to run any cycles it wants while the Military Intel486 processor bus is in its high impedance state. If backoff is requested after the Military Intel486 processor has started a cycle, the new master should wait for memory to return RDY# or BRDY# before assuming control of the bus. Waiting for ready provides a handshake to insure that the memory system is ready to accept a new cycle. If the bus is idle when BOFF# is asserted, the new master can start its cycle two clocks after issuing BOFF#.

The external memory can view BOFF# in the same manner as BLAST#. Asserting BOFF# tells the external memory system that the current cycle is the last cycle in a transfer.

The bus remains in the high impedance state until BOFF# is negated. Upon negation, the Military Intel486 processor restarts its bus cycle by driving out the address and status and asserting ADS#. The bus cycle then continues as usual.

Asserting BOFF# during a burst, BS8# or BS16# cycle will force the Military Intel486 processor to ignore data returned for that cycle only. Data from previous cycles will still be valid. For example, if BOFF# is asserted on the third BRDY# of a burst, the Military Intel486 processor assumes the data returned with the first and second BRDY# is correct and restarts the burst beginning with the third item. The same rule applies to transfers broken into multiple cycle by BS8# or BS16#.

Asserting BOFF# in the same clock as ADS# will cause the Military Intel486 processor to float its bus in the next clock and leave ADS# floating low. Because ADS# is floating low, a peripheral may think that a new bus cycle has begun even-though the cycle was aborted. There are two possible solutions to this problem. The first is to have all devices recognize this condition and ignore ADS# until ready comes back. The second approach is to use a "two clock" backoff: in the first clock AHOLD is asserted, and in the second clock BOFF# is asserted. This guarantees that ADS# will not be floating low. This is only necessary in systems where BOFF# may be asserted in the same clock as ADS#.

10.2.13 BUS STATES

A bus state diagram is shown in Figure 10-32. A description of the signals used in the diagram is given in Table 10-10.

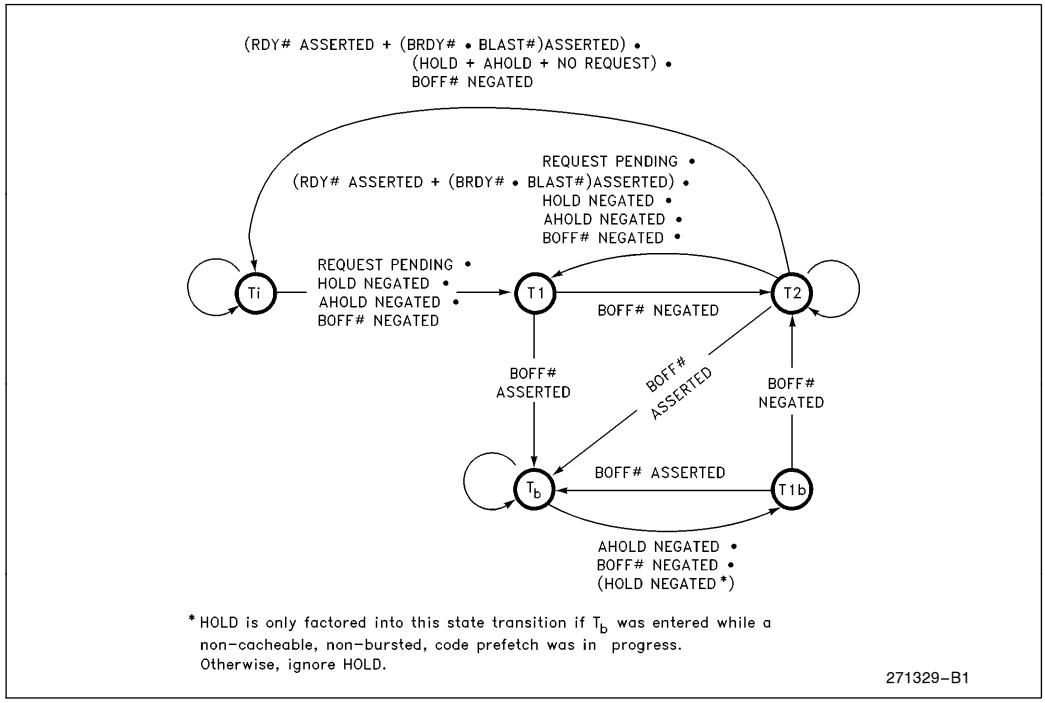


Figure 10-32. Bus State Diagram

Table 10-10. Bus State Description

State	Means
Ti	Bus is idle. Address and status signals may be driven to undefined values, or the bus may be floated to a high impedance state.
T1	First clock cycle of a bus cycle. Valid address and status are driven and ADS# is asserted.
T2	Second and subsequent clock cycles of a bus cycle. Data is driven if the cycle is a write, or data is expected if the cycle is a read. RDY# and BRDY# are sampled.
T1b	First clock cycle of a restarted bus cycle. Valid address and status are driven and ADS# is asserted.
Tb	Second and subsequent clock cycles of an aborted bus cycle.

10.2.14 FLOATING POINT ERROR HANDLING FOR THE MILITARY INTEL486 DX, INTELDX2, AND INTELDX4 PROCESSORS

The Military Intel486 DX, IntelDX2, and IntelDX4 processors provide two options for reporting floating point errors. The simplest method is to raise interrupt 16 whenever an unmasked floating point error occurs. This option may be enabled by setting the NE bit in control register 0 (CR0).

The Military Intel486 DX, IntelDX2, and IntelDX4 processors also provide the option of allowing external hardware to determine how floating point errors are reported. This option is necessary for compatibility with the error reporting scheme used in DOS based systems. The NE bit must be cleared in CR0 to enable user-defined error reporting. User-defined error reporting is the default condition because the NE bit is cleared on reset.

Two pins, floating point error (FERR#) and ignore numeric error (IGNNE#), are provided to direct the actions of hardware if user-defined error reporting is used. The Military Intel486 DX, IntelDX2, and IntelDX4 processors assert the FERR# output to indicate that a floating point error has occurred. FERR# corresponds to the ERROR# pin on the Intel387™ math coprocessor. However, there is a difference in the behavior of the two.

In some cases FERR# is asserted when the next floating point instruction is encountered, and in other cases it is asserted before the next floating point instruction is encountered depending upon the execution state of the instruction causing the exception.

The following class of floating point exceptions drive FERR# at the time the exception occurs (i.e., before encountering the next floating point instruction).

1. The stack fault, invalid operation, and denormal exceptions on all transcendental instructions, integer arithmetic instructions, FSQRT, FSEALE, FPREM(1), FXTRACT, FBLD, and FBSTP.
2. Any exceptions on store instructions (including integer store instructions).

The following class of floating point exceptions drive FERR# only after encountering the next floating point instruction.

1. Exceptions other than on all transcendental instructions, integer arithmetic instructions, FSQRT, FSCALE, FPREM(1), FXTRACT, FBLD, and FBSTP.
2. Any exception on all basic arithmetic, load, compare, and control instructions (i.e., all other instructions).

For both sets of exceptions above, the Intel387 math coprocessor asserts ERROR# when the error occurs and does not wait for the next floating point instruction to be encountered.

IGNNE# is an input to the Military Intel486 DX, IntelDX2, and IntelDX4 processors. When the NE bit in CR0 is cleared, and IGNNE# is asserted, the Military Intel486 DX, IntelDX2, and IntelDX4 processors will ignore a user floating point error and continue executing floating point instructions. When IGNNE# is negated, the IGNNE# is an input to these processors that will freeze on floating point instructions which get errors (except for the control instructions FNCLEX, FNINIT, FNSAVE, FNSTENV, FNSTCW, FNSTSW, FNSTSW AX, FNENI, FNDISI and FNSETPM). IGNNE# may be asynchronous to the Military Intel486 DX, IntelDX2, and IntelDX4 processor clock.

In systems with user-defined error reporting, the FERR# pin is connected to the interrupt controller. When an unmasked floating point error occurs, an interrupt is raised. If IGNNE# is high at the time of this interrupt, the Military Intel486 DX, IntelDX2, and IntelDX4 processors will freeze (disallowing execution of a subsequent floating point instruction) until the interrupt handler is invoked. By driving the IGNNE# pin low (when clearing the interrupt request), the interrupt handler can allow execution of a floating point instruction, within the interrupt handler, before the error condition is cleared (by FNCLEX, FNINIT, FNSAVE or FNSTENV). If execution of a non-control floating point instruction, within the floating point interrupt handler, is not needed, the IGNNE# pin can be tied HIGH.

10.2.15 MILITARY INTEL486 DX, INTELDX2, AND INTELDX4 PROCESSORS FLOATING POINT ERROR HANDLING IN AT-COMPATIBLE SYSTEMS

The Military Intel486 DX, IntelDX2, and IntelDX4 processors provide special features to allow the implementation of an AT-compatible numerics error reporting scheme. These features DO NOT replace the external circuit. Logic is still required that decodes the OUT F0 instruction and latches the FERR# signal. What follows is a description of the use of these Intel Processor features.

The features provided by the Military Intel486 DX, IntelDX2, and IntelDX4 processors are the NE bit in the Machine Status Register, the IGNNE# pin, and the FERR# pin.

The NE bit determines the action taken by the Military Intel486 DX, IntelDX2, and IntelDX4 processors when a numerics error is detected. When set this bit signals that non-DOS compatible error handling will be implemented. In this mode the Military Intel486 DX, IntelDX2, and IntelDX4 processors take a software exception (16) if a numerics error is detected.

If the NE bit is reset, the Military Intel486 DX, IntelDX2, and IntelDX4 processors use the IGNNE# pin to allow an external circuit to control the time at which non-control numerics instructions are allowed to execute. Note that floating point control instructions such as FNINIT and FNSAVE can be executed during a floating point error condition regardless of the state of IGNNE#.

To process a floating point error in the DOS environment the following sequence must take place:

1. The error is detected by the Military Intel486 DX, IntelDX2, and IntelDX4 processor that activates the FERR# pin.
2. FERR# is latched so that it can be cleared by the OUT F0 instruction.
3. The latched FERR# signal activates an interrupt at the interrupt controller. This interrupt is usually handled on IRQ13.
4. The Interrupt Service Routine (ISR) handles the error and then clears the interrupt by executing an OUT instruction to port F0. The address F0 is decoded externally to clear the FERR# latch. The IGNNE# signal is also activated by the decoder output.
5. Usually the ISR then executes an FNINIT instruction or other control instruction before restarting the program. FNINIT clears the FERR# output.

Figure 10-33 illustrates a sample circuit that will perform the function described above. Note that this circuit has not been tested and is included as an example of required error handling logic.

Note that the IGNNE# input allows non-control instructions to be executed prior to the time the FERR# signal is reset by the Military Intel486 DX, IntelDX2, and IntelDX4 processors. This function is implemented to allow exact compatibility with the AT implementation. Most programs reinitialize the floating point unit before continuing after an error is detected. The floating point unit can be reinitialized using one of the following four instructions: FCLEX, FINIT, FSAVE and FSTENV.

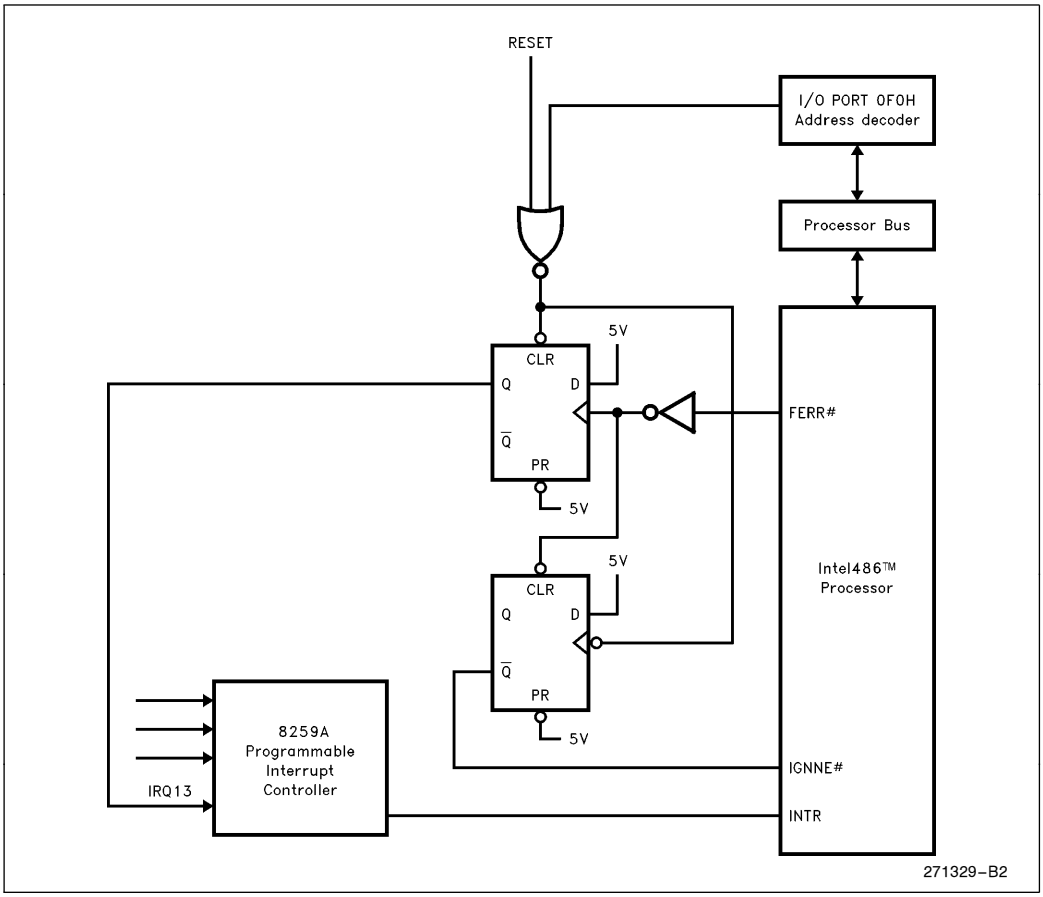


Figure 10-33. DOS-Compatible Numerics Error Circuit

10.3 Enhanced Bus Mode Operation (Write-Back Mode) for the Write-Back Enhanced IntelDX4™ Processor

This section describes how the Write-Back enhanced Intel486 processor bus operation changes for the Enhanced Bus mode when the internal cache is configured in write-back mode.

10.3.1 SUMMARY OF BUS DIFFERENCES

The following is a list of the differences between the Enhanced and Standard Bus modes:

1. Burst write capability is extended to four double-word burst cycles (for write-back cycles only)
2. Four new signals: INV, WB/WT#, HITM#, and CACHE#, have been added to support the write-back operation of the internal cache. These signals function the same as the equivalent signals on the Pentium® OverDrive® Processor pins.
3. The SRESET signal has been modified so that it neither writes back, invalidates, nor disables the cache. Special test modes are also not initiated through SRESET.
4. The FLUSH# signal behaves the same as the WBINVD instruction. Upon assertion, FLUSH# writes back all modified lines, invalidates the cache, and issues two special bus cycles.
5. The PLOCK# signal remains inactive in the Enhanced Bus mode.

10.3.2 BURST CYCLES

Figure 10-34 shows a basic burst read cycle of the Write-Back Enhanced Intel486 processors. In the Enhanced Bus mode, both PCD and CACHE# are asserted if the cycle is internally cacheable. The Write-Back Enhanced Intel486 processors sample KEN# in the clock before the first BRDY#. If KEN# is returned active by the system, this cycle is transformed into a multiple-transfer cycle. With each data item returned from external memory, the data is ''cached'' only if KEN# is returned active again in the clock before the last BRDY# signal. Data is sampled only in the clock in which BRDY# is returned. If the data is not sent to the processor every clock, it causes a ''slow burst'' cycle.

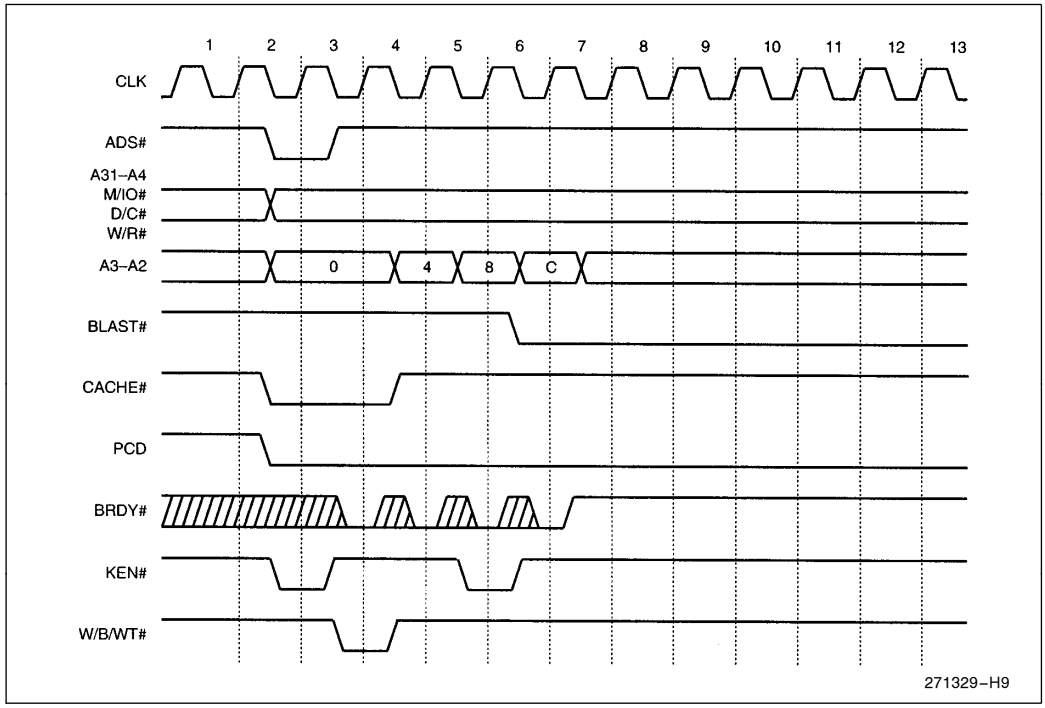


Figure 10-34. Basic Burst Read Cycle

10.3.2.1 Non-Cacheable Burst Operation

If CACHE# is asserted on a read cycle, it indicates that the processor will follow with BLAST# high if KEN# is returned active. However, the converse is not true. The Write-Back Enhanced Intel486 processors may elect to read-burst data, which are identified as non-cacheable by either CACHE# or KEN#. In this case, BLAST# is also high in the same cycle as the first BRDY# (in clock four). To improve performance, the memory controller should try to complete the cycle as a burst cycle.

The assertion of CACHE# on a write cycle signifies a replacement or snoop write-back cycle. These cycles consist of four doubleword transfers (either bursts or non-burst). The signals KEN# and WB/WT# are not sampled during write-back cycles because the processor does not attempt to redefine the cacheability of the line.

10.3.2.2 Burst Cycle Signal Protocol

The signals from ADS# through BLAST#, which are shown in Figure 10-34, have the same function and timing in both Standard and Enhanced Bus modes. Burst cycles can be up to 16-bytes long (four aligned doublewords) and can start with any one of the four doublewords. The sequence of the addresses are determined by the first address and the sequence follows the order shown previously in Table 10-8. The burst order for reads is the same as the burst order for writes. (See section 10.2.4.2, ''Burst and Cache Line Fills.'')

An attempted line fill, which is caused by a read miss, is indicated by the assertion of CACHE# and W/R# to low. For a line fill to occur, the system must assert KEN# twice: one clock prior to the first BRDY# and one clock prior to last BRDY#. It takes only one assertion of KEN# to mark the line as non-cacheable. A write-back cycle of a cache line, due to replacement or snoop, is indicated by the assertion of CACHE# low and W/R# high. KEN# has no effect during write-back cycles. CACHE# is valid from the assertion of ADS# through the clock in which the first RDY# or BRDY# is returned. CACHE# is inactive at all other times. PCD behaves the same in Enhanced Bus mode as in Standard Bus mode, **except that it is low during write-back cycles.**

The Write-Back Enhanced Intel486 processors samples WB/WT# once, in the *same* clock as the first BRDY#. This sampled value of WB/WT# is combined with PWT to bring the line into the internal cache, either as a write-back line or write-through line.

10.3.3 CACHE CONSISTENCY CYCLES

The system performs snooping to maintain cache consistency. Snoop cycles can be performed under AHOLD, BOFF#, or HOLD, described in Table 10-11.

The snoop cycle begins by checking whether a particular cache line has been ''cached'' and invalidates the line based on the state of the INV pin. If the Write-Back Enhanced Intel486 processors are configured in Enhanced Bus mode, the system must drive INV high to invalidate a particular cache line. The Write-Back Enhanced Intel486 processors do not have an output pin to indicate a snoop hit to an S-state line or an E-state line. However, the Write-Back Enhanced Intel486 processors will invalidate the line if the system snoop hits an S-state, E-state, or M-state line, provided INV was driven high during snooping. If INV is driven low during a snoop, a modified line will be written back to memory and will remain in the cache as a write-back line; a write-through line also will remain in the cache as a write-through line.

Table 10-11. Snoop Cycles under AHOLD, BOFF#, or HOLD

AHOLD	Floats the address bus. ADS# is asserted under AHOLD only to initiate a snoop write-back cycle. An ongoing burst cycle is completed under AHOLD. For non-burst cycles, a specific non-burst transfer (ADS#-RDY# transfer) is completed under AHOLD and fractured before the next assertion of ADS#. A snoop write-back cycle is reordered ahead of a fractured non-burst cycle and the non-burst cycle is completed only after the snoop write-back cycle is completed, provided there are no other snoop write-back cycles scheduled.
BOFF#	Overrides AHOLD and takes effect in the next clock. On-going bus cycles will stop in the clock following the assertion of BOFF# and resume when BOFF# is de-asserted. A snoop is the only bus cycle the Write-Back Enhanced IntelDX2™ processor responds to under BOFF#. Snoop write-back will be reordered ahead of the backed-off cycle. The snoop write-back cycle begins after BOFF# is de-asserted followed by the backed-off cycle.
HOLD	HOLD is acknowledged only between bus cycles, except for a non-cacheable, non-bursted code prefetch cycle. In a non-cacheable, non-bursted code prefetch cycle, HOLD is acknowledged after the system returns RDY#. Once HOLD is active, the processor blocks all bus activities until the system releases the bus (by de-asserting HOLD).

After asserting AHOLD or BOFF#, the external bus master driving the snoop cycle must wait for two clocks before driving the snoop address and asserting EADS#. If snooping is done under HOLD, the master performing the snoop must wait for at least one clock cycle before driving the snoop addresses and asserting EADS#. **INV should be driven low during read operations to minimize invalidations, and INV should be driven high to invalidate a cache line during write operations.** The Write-Back Enhanced Intel486 processors assert HITM# if the cycle hits a modified line in the cache. This output signal becomes valid two clock periods after EADS# is valid on the bus. HITM# remains asserted until the modified line is written back and will remain asserted until the RDY# or BRDY# of the snoop cycle is returned. Snoop operations could interrupt an ongoing bus operation in both the Standard Bus and Enhanced Bus modes. **The Write-Back Enhanced Intel486 processors can accept EADS# in every clock period while in Standard Bus mode. In Enhanced Bus mode, the Write-Back Enhanced Intel486 processors can accept EADS# every other clock period or until a snoop hits an M-state line.** The Write-Back Enhanced Intel486 processors will not accept any further snoop cycles input until the previous snoop write-back operation is completed.

All write-back cycles adhere to the burst address sequence of 0-4-8-C. The CACHE#, PWT, and PCD output pins are asserted and the KEN# and WB/WT# input pins are ignored. Write-back cycles can be either bursted or non-bursted. All write-back operations write 16 bytes of data to memory corresponding to the modified line that hit during the snoop. **Note that the Write-Back Enhanced Intel486 processors will accept BS8# and BS16# line-fill cycles, but not on replacement or snoop-forced write-back cycles.**

10.3.3.1 Snoop Collision with a Current Cache Line Operation

The system can also perform snooping concurrent with a cache access and may collide with a current cache bus cycle. Table 10-12 lists some scenarios and the results of a snoop operation colliding with an on-going cache fill or replacement cycle.

Table 10-12. Various Scenarios of a Snoop Write-Back Cycle Colliding with an On-Going Cache Fill or Replacement Cycle

Arbitration Control	Snoop to the Line That Is Being Filled	Snoop to a Different Line from the Line Being Filled	Snoop to the Line That Is Being Replaced	Snoop to a Different Line from the Line Being Replaced
AHOLD	Read all line fill data into cache line buffer. Update cache only if snoop occurred with INV = "0" No write-back cycle because the line has not been modified yet	Complete fill if the cycle is bursted. Start snoop write-back. If the cycle is non-bursted, the snoop write-back will be reordered ahead of the line fill. After the snoop write-back cycle is completed, continue with line fill	Complete replacement write-back if the cycle is bursted. Processor does not initiate a snoop write-back, but asserts HITM# until the replacement write-back is completed. If the replacement cycle is non-bursted, the snoop write-back is re-ordered ahead of the replacement write-back cycle. The processor does not continue with the replacement write-back cycle.	Complete replacement write-back if it is a burst cycle. Initiate snoop write-back. If the replacement write-back is a non-burst cycle, the snoop write-back cycle is re-ordered in front of the replacement cycle. After the snoop write-back, the replacement write-back is continued from the interrupt point.
BOFF#	Stop reading line fill data Wait for BOFF# to go inactive. Continue read from backed off point Update cache only if snoop occurred with INV = "0"	Stop fill Wait for BOFF# to go inactive Do snoop write-back Continue fill from interrupt point	Stop replacement write-back Wait for BOFF# to go inactive Initiate snoop write-back Processor does not continue replacement write-back	Stop replacement write-back Wait for BOFF# to be de-asserted Initiate snoop write-back Continue replacement write-back from point of interrupt
HOLD	HOLD is not acknowledged until the current bus cycle (i.e., the line operation) is completed, except for a non-cacheable, non-bursted code prefetch cycle. Consequently there can be no collision with the snoop cycles using HOLD, except as mentioned earlier. In this case the snoop write-back is re-ordered ahead of an on-going non-burst, non-cached code prefetch cycle. After the write-back cycle is completed, the code prefetch cycle continues from the point of interrupt.			

10.3.3.2 Snoop under AHOLD

Snooping under AHOLD begins by asserting AHOLD to force the Write-Back Enhanced Intel486 processors to float its address bus, as shown in Figure 10-35. **The ADS# for the write-back cycle is guaranteed to occur no sooner than the second clock following the assertion of HITM# (i.e., there is a dead clock between the assertion of HITM# and the first ADS# of the snoop write-back cycle.)**

When a line is written back, KEN#, WB/WT#, BS8#, and BS16# are ignored, and PWT and PCD are always low during write-back cycles.

The next ADS# for a new cycle can occur immediately after the last RDY# or BRDY# of the write-back cycle. The Write-Back Enhanced Intel486 processors do not guarantee a dead clock between cycles **unless** the **second** cycle is a snoop-forced write-back cycle. This allows snoop-forced write-backs to be backed off (BOFF#) when snooping under AHOLD.

HITM# is guaranteed to remain asserted until the RDY# or BRDY# corresponding to the last double-word of the write-back cycle is returned. HITM# will be de-asserted from the clock edge in which the last BRDY# or RDY# for the snoop write-back cycle is returned. The write-back cycle could be a bursted or non-bursted. In either case, 16 bytes of data corresponding to the modified line that has a snoop hit is written back.

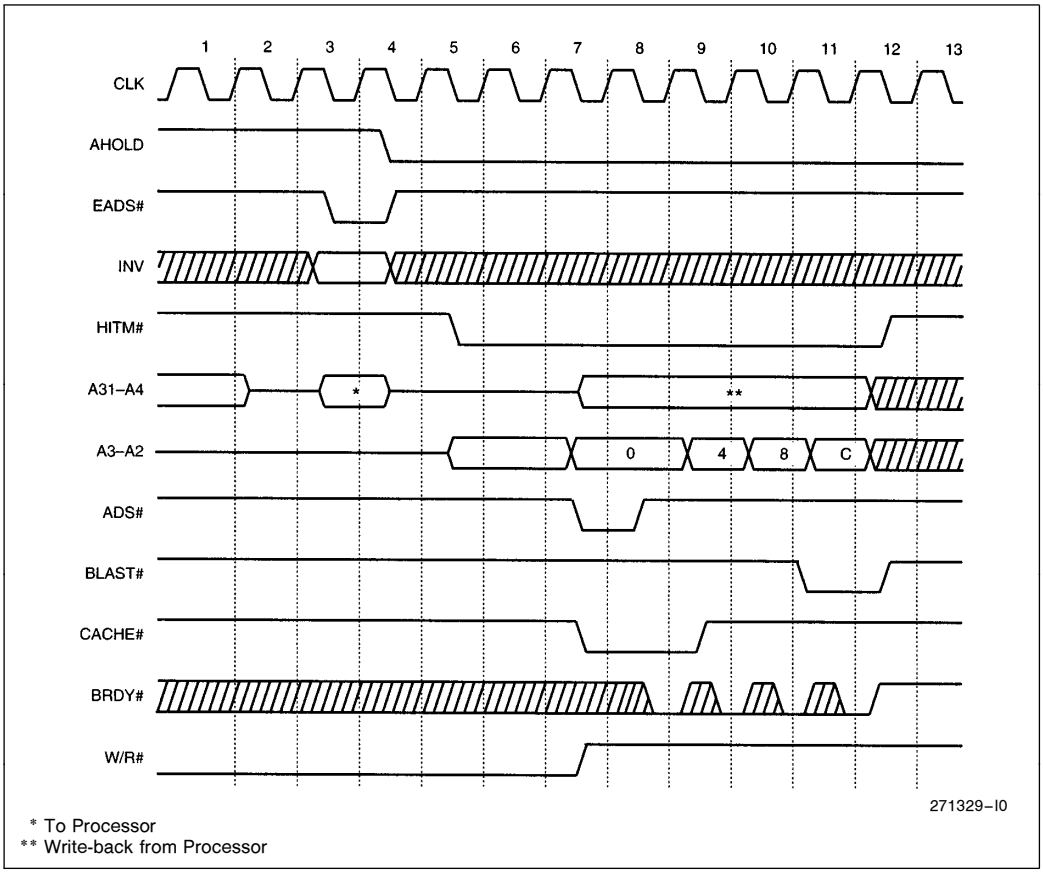


Figure 10-35. Snoop Cycle Invalidating a Modified Line

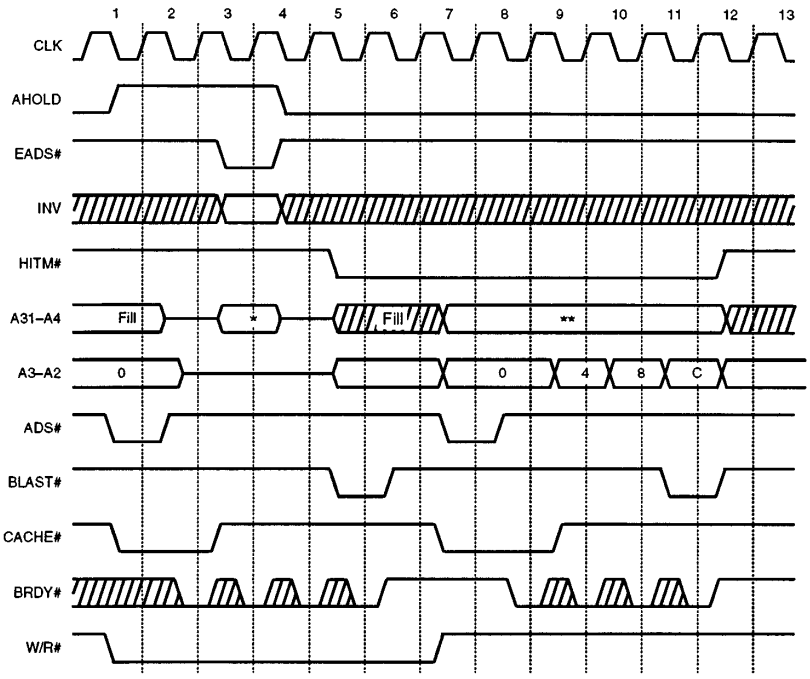
Snoop under AHOLD Overlaying a Line-Fill Cycle

The assertion of AHOLD during a line fill is allowed on the Write-Back Enhanced Intel486 processors. In this case, when a snoop cycle is overlaid by an on-going line-fill cycle, the chipset must generate the burst addresses internally for the line fill to complete, because the address bus will have the valid snoop address. The write-back mode is more complex compared to the write-through mode because of the possibility of a line being written back. Figure 10-36 shows a snoop cycle overlaying a line-fill cycle, when the snooped line is not the same as the line being filled.

In Figure 10-36, the snoop to an M-state line causes a snoop write-back cycle. The Write-Back Enhanced Intel486 processors will assert HITM# two clocks after the EADS#, but will delay the snoop write-back cycle until the line fill is completed, because the line fill shown in Figure 10-36 is a burst cycle. In this figure, AHOLD is asserted one clock after ADS#. In the clock after AHOLD is asserted, the Write-Back Enhanced Intel486 processors will float the address bus (not the Byte Enables). Hence, the memory controller must determine burst addresses in this period. The chipset must comprehend the special ordering required by all burst sequences of the Write-Back Enhanced Intel486 processors. HITM# is guaranteed to remain active until the write-back cycle completes.

If AHOLD continues to be asserted over the forced write-back cycle, the memory controller also must supply the write-back addresses to the memory. The Write-Back Enhanced Intel486 processors always run the write-back with an address sequence of 0-4-8-C.

In general, if the snoop cycle overlays any burst cycle (not necessarily a line-fill cycle) the snoop write-back will be delayed because of the on-going burst cycle. First, the burst cycle goes to completion and only then does the snoop write-back cycle start.



* To Processor
** Write-back from Processor

Figure 10-36. Snoop Cycle Overlaying a Line-Fill Cycle

AHOLD Snoop Overlaying a Non-Burst Cycle

When AHOLD overlays a non-burst cycle, snooping is based on the completion of the current non-burst-ed transfer (ADS#-RDY# transfer). Figure 10-37 shows a snoop cycle under AHOLD overlaying a non-burst line-fill cycle. HITM# is asserted two clocks after EADS#, and the non-burst cycle is fractured after the RDY# for a specific single transfer is returned. The snoop write-back cycle is re-ordered ahead of an on-going non-burst cycle. After the write-back cycle is completed, the fractured non-burst cycle will continue. The snoop write-back ALWAYS precedes the completion of a fractured cycle, regardless of the point at which AHOLD is de-asserted, and AHOLD must be de-asserted before the fractured non-burst cycle can complete.

AHOLD Snoop to the Same Line That Is Being Filled

A system snoop will not cause a write-back cycle to occur if the snoop hits a line while the line is being filled. The processor does not allow a line to be modified until the fill is completed (and a snoop will only produce a write-back cycle for a modified line). Although a snoop to a line that is being filled will not produce a write-back cycle, the snoop still has an effect based on the following rules:

1. The processor always snoops the line being filled.
2. In all cases, the processor uses the operand that triggered the line fill.
3. If the snoop occurs when INV = ''1'', the processor never updates the cache with the fill data.
4. If the snoop occurs when INV = ''0'', the processor loads the line into the internal cache.

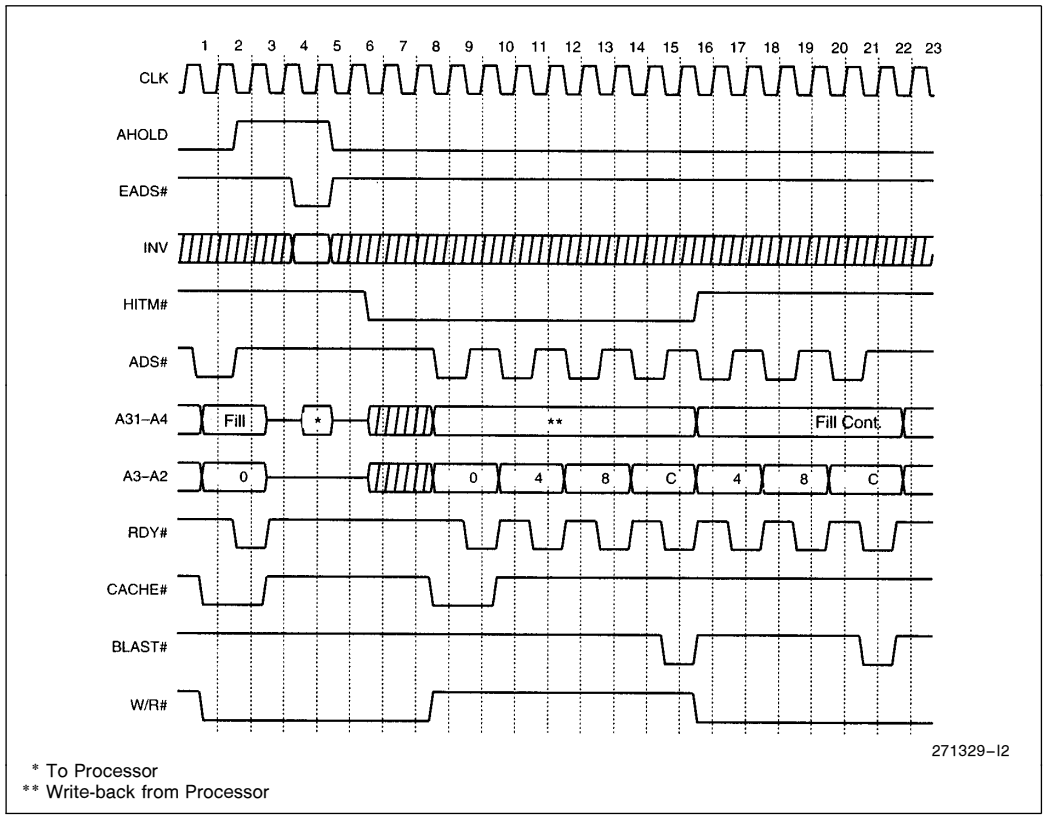


Figure 10-37. Snoop Cycle Overlaying a Non-Burst Cycle

Snoop during Replacement Write-Back

If the cache contains valid data during a line fill, one of the cache lines may be replaced as determined by the LRU algorithm. If the line being replaced is modified, this line will be written back to maintain cache coherency. When a replacement write-back cycle is in progress, it might be necessary to snoop the line that is being written back. (See Figure 10-38.)

If the replacement write-back cycle is bursted and there is a snoop hit to the same line as the line that is being replaced, the on-going replacement cycle runs to completion. HITM# is asserted until the line is written back and the snoop write-back will not be initiated. In this case, the replacement write-back is converted to the snoop write-back, and HITM# is asserted and de-asserted without a specific ADS# to initiate the write-back cycle.

If there is a snoop hit to a different line from the line being replaced, and if the replacement write-back cycle is bursted, the replacement cycle goes to completion. Only then is the snoop write-back cycle initiated.

If the replacement write-back cycle is a non-burst cycle, and if there is a snoop hit to the same line as the line being replaced, it will fracture the replacement write-back cycle after the RDY# for the current non-burst transfer is returned. The snoop write-back cycle will be reordered in front of the fractured replacement write-back cycle and will be completed under HITM#. However, after AHOLD is de-asserted the replacement write-back cycle is not completed.

If there is a snoop hit to the line that is different from the one being replaced, the non-burst replacement write-back cycle will be fractured, and the snoop write-back cycle will be reordered ahead of the replacement write-back cycle. After the snoop write-back is completed, the replacement write-back cycle will continue.

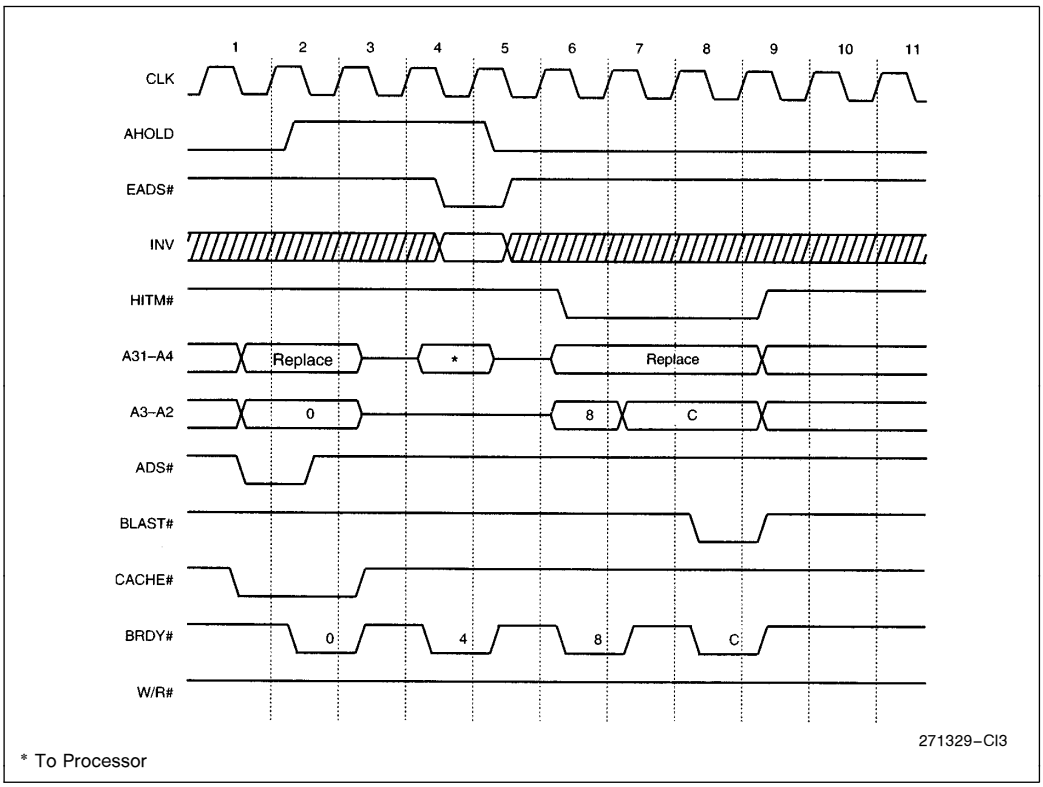


Figure 10-38. Snoop to the Line That Is Being Replaced

10.3.3.3 Snoop under BOFF#

BOFF# is capable of fracturing any transfer, burst or non-burst. The output pins (see Table 3-8 and Table 3-9) of the Write-Back Enhanced Intel486 processors will be floated in the clock period following the assertion of BOFF#. If the system snoop hits a modified line using BOFF#, the snoop write-back cycle will be reordered ahead of the current cycle. BOFF# must be de-asserted for the processor to perform a snoop write-back cycle and resume the fractured cycle. The fractured cycle resumes with a new ADS# and begins with the first uncompleted transfer. Snoops are permitted under BOFF#, but write-back cycles will not be started until BOFF# is de-asserted. Consequently, multiple snoop cycles can occur under a continuously asserted BOFF#, but only up to the first asserted HITM#.

Snoop under BOFF# during Cache Line Fill

As shown in Figure 10-39, BOFF# fractured the second transfer of a non-burst cache line-fill cycle. The system begins snooping by driving EADS# and INV in clock six. The assertion of HITM# in clock eight indicates that the snoop cycle hit a modified line and the cache line will be written back to memory. The assertion of HITM# in clock eight and CACHE# and ADS# in clock ten identifies the beginning of the snoop write-back cycle. ADS# is guaranteed to be asserted no sooner than two clock periods after the assertion of HITM#. Write-back cycles always use the four-doubleword address sequence of 0-4-8-C (burst or non-burst). The snoop write-back cycle begins upon the de-assertion of BOFF# with HITM# asserted throughout the duration of the snoop write-back cycle.

If the snoop cycle hits a line that is different from the line being filled, the cache line fill will resume after the snoop write-back cycle completes, as shown in Figure 10-39.

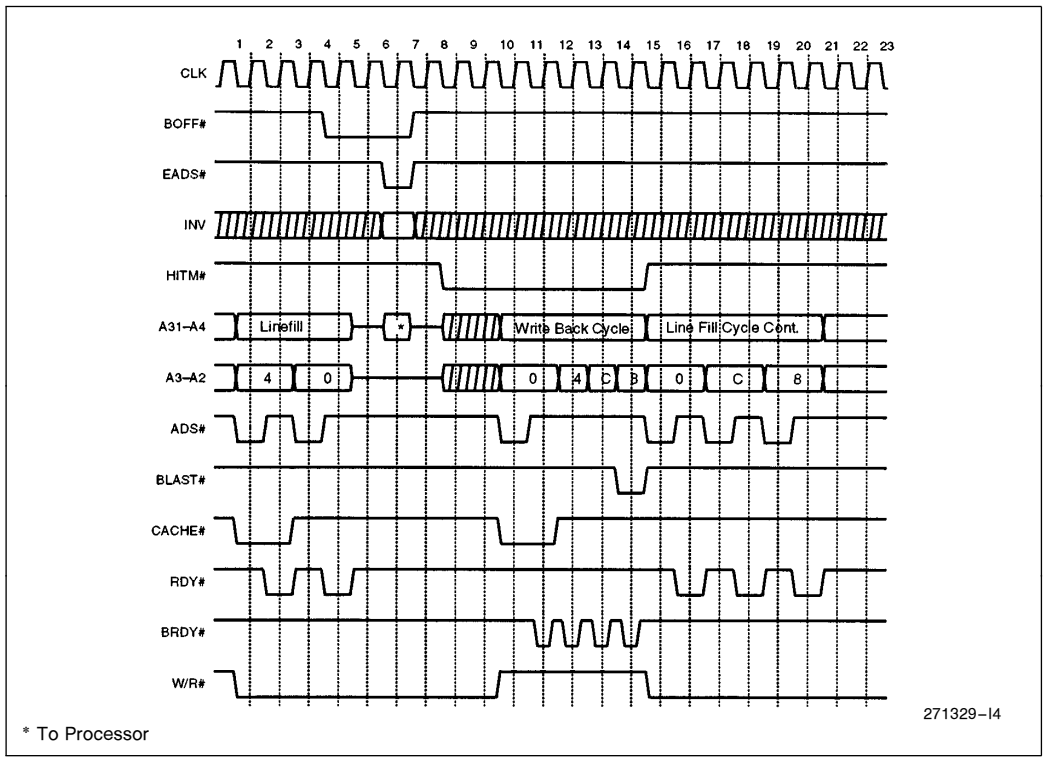


Figure 10-39. Snoop under BOFF# during a Cache Line-Fill Cycle

An ADS# is always issued when a cycle resumes after being fractured by BOFF#. The address of the fractured data transfer is reissued under this ADS#, and CACHE# is not issued unless the fractured operation resumes from the first transfer (e.g., first doubleword). If the system asserts BOFF# and RDY# simultaneously, as shown in clock four on Figure 10-39, BOFF# dominates and RDY# is ignored. Consequently, the Write-Back Enhanced Intel486 processors accept only up to the x4h doubleword, and the line fill resumes with the x0h doubleword. ADS# initiates the resumption of the line-fill operation in clock period 15. HITM# is de-asserted in the clock period following the clock period in which the last RDY# or BRDY# of the write-back cycle is returned. Hence, HITM# is guaranteed to be de-asserted before the ADS# of the next cycle.

Figure 10-39 also shows the system returning RDY# to indicate a non-burst line-fill cycle. Bursted cache line-fill cycles behave similar to non-bursted cache line-fill cycles when snooping using BOFF#. If the system snoop hits the same line as the line being filled (burst or non-burst), the Write-Back Enhanced Intel486 processors will not assert HITM# and will not issue a snoop write-back cycle, because it did not modify the line, and the line fill resumes upon the de-assertion of BOFF#. However, the line fill will be cached only if INV is driven low during the snoop cycle.

Snoop under BOFF# during Replacement Write-Back

If the system snoop under BOFF# hits the line that is currently being replaced (burst or non-burst), the entire line is written back as a snoop write-back line, and the replacement write-back cycle is not continued. However, if the system snoop hits to a different line than the one currently being replaced, the replacement write-back cycle will continue after the snoop write-back cycle has been completed. Figure 10-40 shows a system snoop hit to the same line as the one being replaced (non-burst).

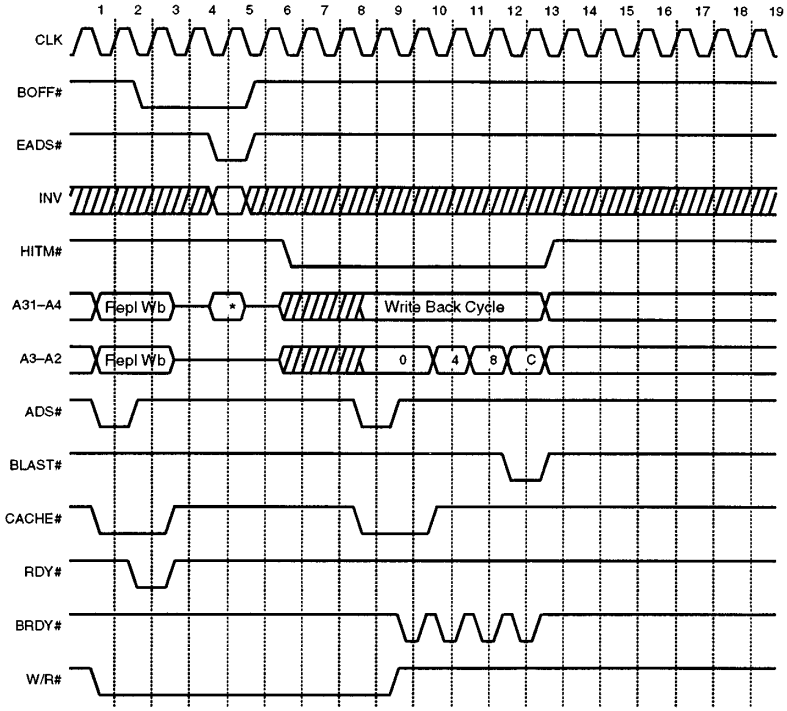


Figure 10-40. Snoop under BOFF# to the Line that is Being Replaced

10.3.3.4 Snoop under HOLD

HOLD can only fracture a non-cacheable, non-bursted code prefetch cycle. For all other cycles, the Write-Back Enhanced Intel486 processors will not assert HLDA until the entire current cycle is completed. If the system snoop hits a modified line under HLDA during a non-cacheable, non-burstable code prefetch, the snoop write-back cycle will be reordered ahead of the fractured cycle. The fractured non-cacheable, non-bursted code prefetch resumes with an ADS# and begins with the first uncompleted transfer. Snoops are permitted under HLDA, but write-back cycles will not occur until HOLD is de-asserted. Consequently, multiple snoop cycles are permitted under a continuously asserted HLDA only up to the first asserted HITM#.

Snoop under HOLD during Cache Line Fill

As shown in Figure 10-41, HOLD (asserted in clock two) does not fracture the bursted cache line-fill cycle until the line fill is completed (in clock five). Upon completing the line fill in clock five, the Write-Back Enhanced Intel486 processors assert HLDA and the system begins snooping by driving EADS# and INV in the following clock period. The assertion of HITM# in clock nine indicates that the snoop cycle has hit a modified line and the cache line is written back to memory. The assertion of HITM# in clock nine and CACHE# and ADS# in clock 11 identifies the beginning of the snoop write-back cycle. The snoop write-back cycle begins upon the de-assertion of HOLD, and HITM# is asserted throughout the duration of the snoop write-back cycle.

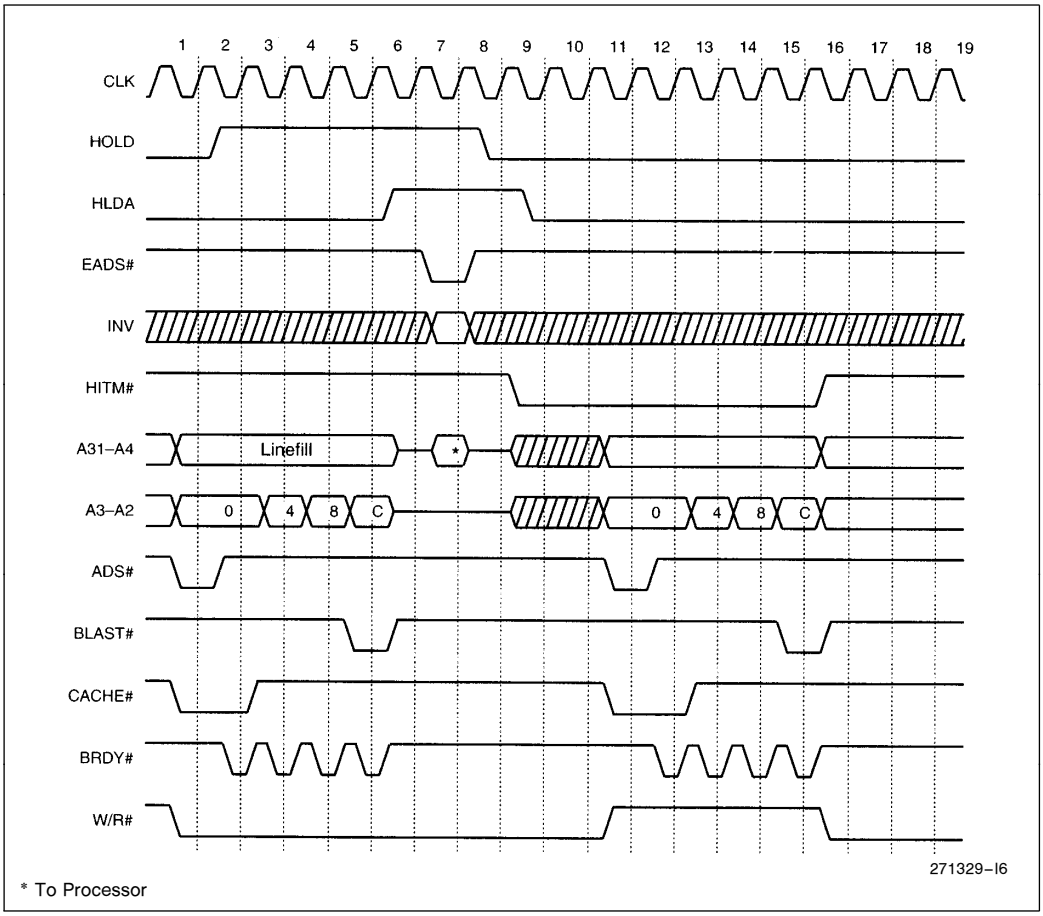


Figure 10-41. Snoop under HOLD during Line Fill

If HOLD is asserted during a non-cacheable, non-bursted code prefetch cycle, as shown in Figure 10-42, the Write-Back Enhanced Intel486 processors will issue HLDA in clock seven (which is the clock period in which the next RDY# is returned). If the system snoop hits a modified line, the snoop write-back cycle will begin after HOLD is released. After the snoop write-back cycle is completed, an ADS# is issued and the code prefetch cycle resumes.

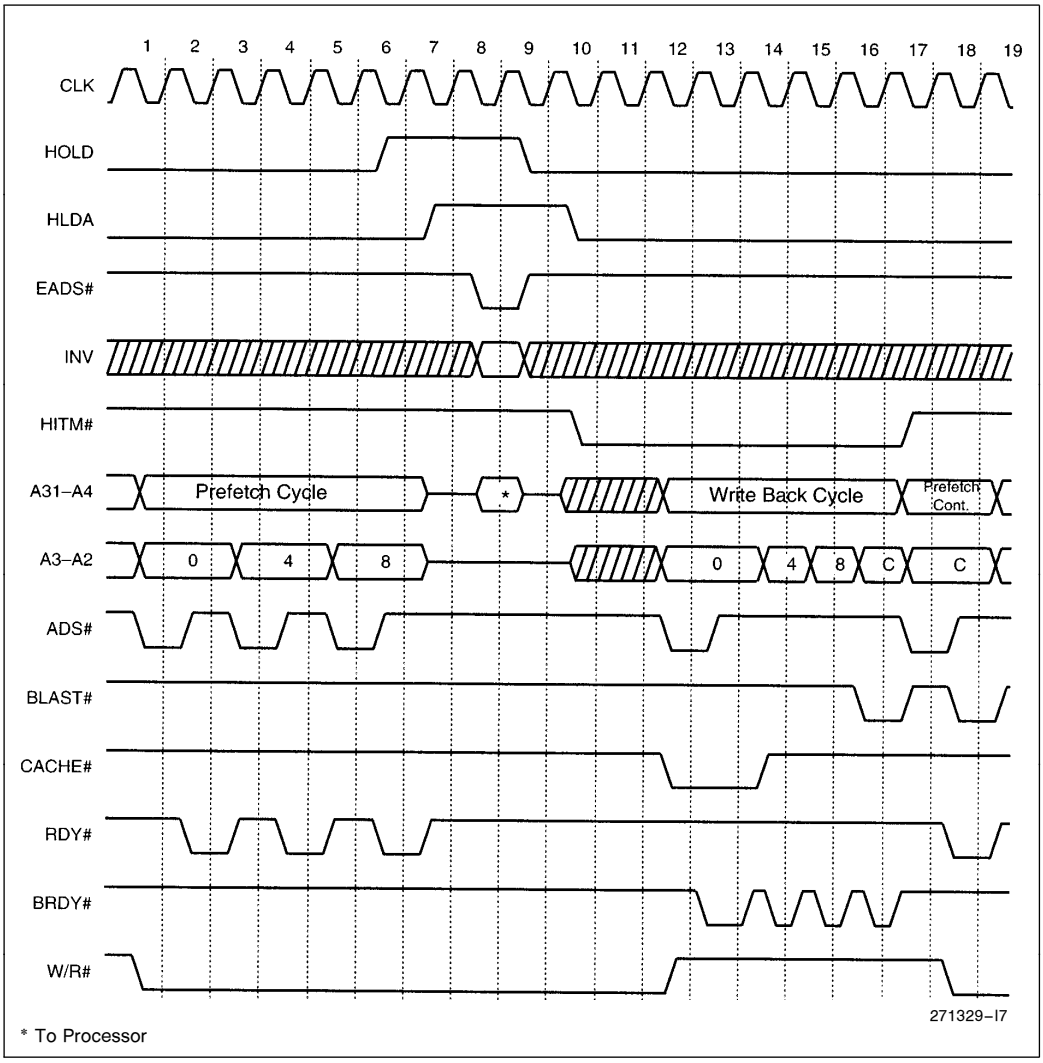


Figure 10-42. Snoop using HOLD during a Non-Cacheable, Non-Burstable Code Prefetch

Snoop under HOLD during Replacement Write-Back

Collision of snoop cycles under a HOLD during the replacement write-back cycle can never occur, because HLDA is asserted only after the replacement write-back cycle (bursted or non-bursted) is completed.

10.3.4 LOCKED CYCLES

In both Standard and Enhanced Bus modes, the Write-Back Enhanced Intel486 processors architecture supports atomic memory access. A programmer can modify the contents of a memory variable and be assured that the variable will not be accessed by another bus master between the read of the variable and the update of that variable. This function is provided for instructions that contain a LOCK prefix, and also for instructions that implicitly perform locked read modify write cycles. In hardware, the LOCK function is implemented through the LOCK# pin, which indicates to the system that the processor is performing this sequence of cycles, and that the processor should be allowed atomic access for the location accessed during the first locked cycle.

A locked operation is a combination of one or more read cycles followed by one or more write cycles with the LOCK# pin asserted. Before a locked read cycle is run, the processor first determines if the corresponding line is in the cache. If the line is present in the cache, and is in an E or S state, it is invalidated. If the line is in the M state, the processor does a write-back and then invalidates the line. A locked cycle to an M, S, or E state line is always forced out to the bus. If the operand is misaligned across cache lines, the processor could potentially run two write back cycles before starting the first locked read. In this case the sequence of bus cycles is: write back, write back, locked read, locked read, locked write and the final locked write. Note that although a total of six cycles are generated, the LOCK# pin will be active only during the last four cycles, as shown in Figure 10-43.

LOCK# will not be de-asserted if AHOLD is asserted in the middle of a locked cycle. LOCK# will remain asserted even if there is a snoop write-back during a locked cycle. LOCK# will be floated if BOFF# is asserted in the middle of a locked cycle. However, it will be driven LOW again when the cycle restarts after BOFF#. Locked read cycles are never transformed into line fills, even if KEN# is returned active. **If there are back to back locked cycles, the Write-Back Enhanced Intel486 processors do not insert a dead clock between these two cycles**. HOLD is recognized if there are two back to back locked cycles, and LOCK# will float when HLDA is asserted.

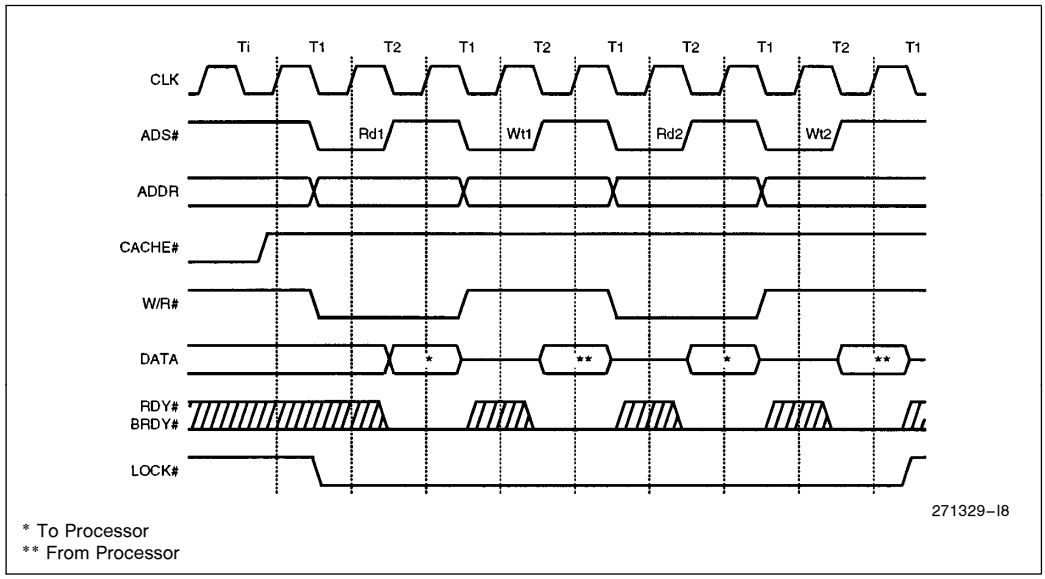


Figure 10-43. Locked Cycles (Back to Back)

10.3.4.1 Snoop/Lock Collision

If there is a snoop cycle overlaying a locked cycle, the snoop write-back cycle will fracture the locked cycle. As shown in Figure 10-44, after the read portion of the locked cycle is completed, the snoop write-back starts under HITM#. After the write-back is completed the locked cycle will continue. But during all this time (including the write-back cycle), the LOCK# signal remains asserted.

Because HOLD is not acknowledged if LOCK# is asserted, snoop-lock collisions are restricted to AHOLD and BOFF# snooping.

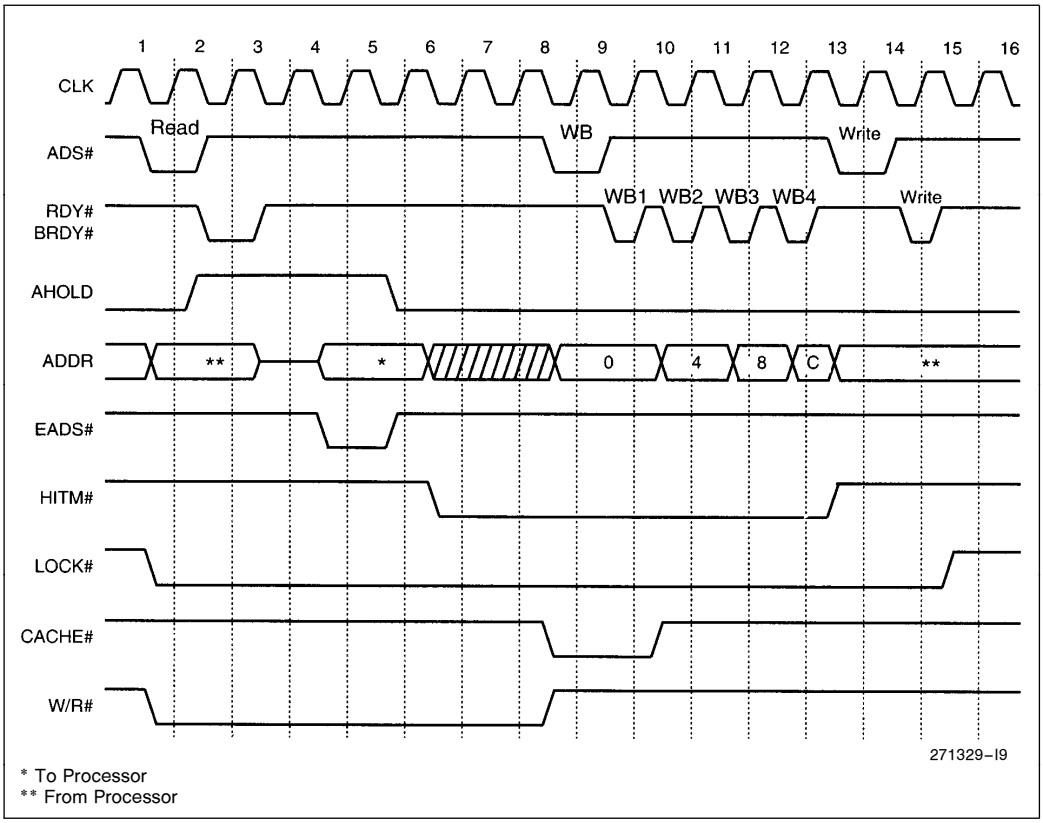


Figure 10-44. Snoop Cycle Overlaying a Locked Cycle

10.3.5 FLUSH OPERATION

The Write-Back Enhanced Intel486 processors executes a flush operation when the FLUSH# pin is active, and no outstanding bus cycles, such as a line fill or write back, are being processed. In the Enhanced Bus mode, the processor first writes back all the modified lines to external memory. After the write-back is completed, two special cycles are generated, indicating to the external system that the write-back is done. All lines in the internal cache are invalidated after all the write back cycles are done. Depending on the number of modified lines in the cache, the flush could take a minimum of 1280 bus clocks (2560 processor clocks) and up to a maximum of 5000+ bus clocks to scan the cache, perform the write backs, invalidate the cache, and run the flush acknowledge cycles. FLUSH# is implemented as an interrupt in the Enhanced Bus mode, and will be recognized only on an instruction boundary. Write-back system designs should look for the flush acknowledge cycles to recognize the end of the flush operation. Figure 10-45 shows the flush operation of the Write-Back Enhanced Intel486 processors, when configured in the Enhanced Bus mode.

If the processor is in Standard Bus mode, the processor will not issue special acknowledge cycles in response to the FLUSH# input, although the internal cache is invalidated. The invalidation of the cache in this case, takes only two bus clocks.

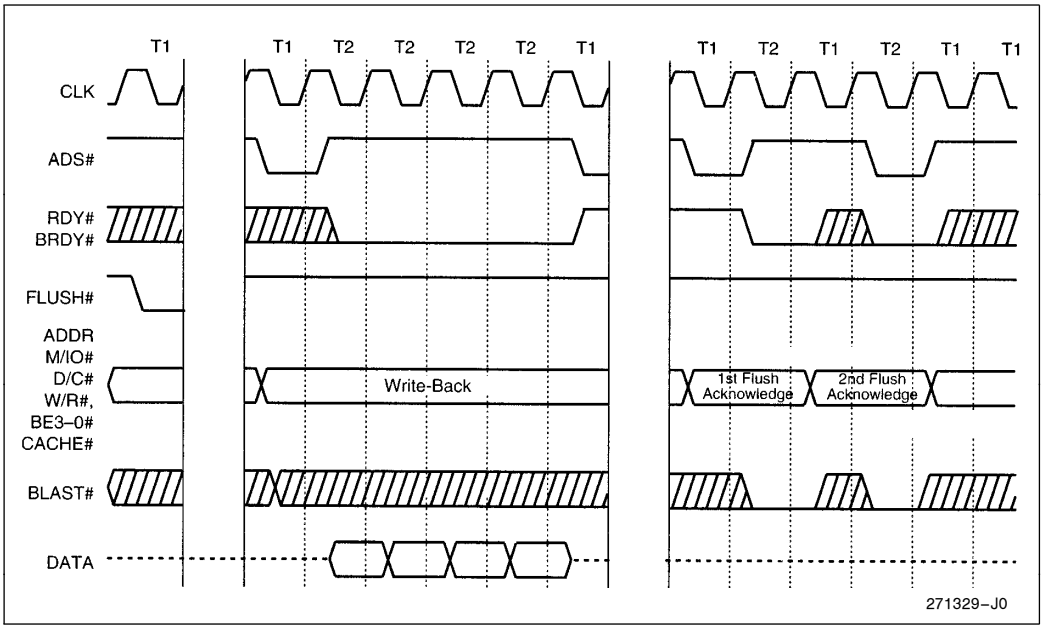


Figure 10-45. Flush Cycle

10.3.6 PSEUDO LOCKED CYCLES

In Enhanced Bus mode, PLOCK# is always driven inactive for both burst and non-burst cycles. Hence, it is possible for other bus masters to gain control of the bus during operand transfers that take more than one bus cycle. A 64-bit aligned operand can be read in one burst cycle or two non-burst cycles if BS8# and BS16# are not asserted. Figure 10-46 shows a 64-bit Floating-Point operand or Segment Descriptor read cycle, which is burst by the system returning BRDY#.

10.3.6.1 Snoop under AHOLD during Pseudo-Locked Cycles

AHOLD can fracture a 64-bit transfer if it is a non-burst cycle. If the 64-bit cycle is burst, as shown in Figure 10-46, the entire transfer goes to completion and only then does the snoop write-back cycle start.

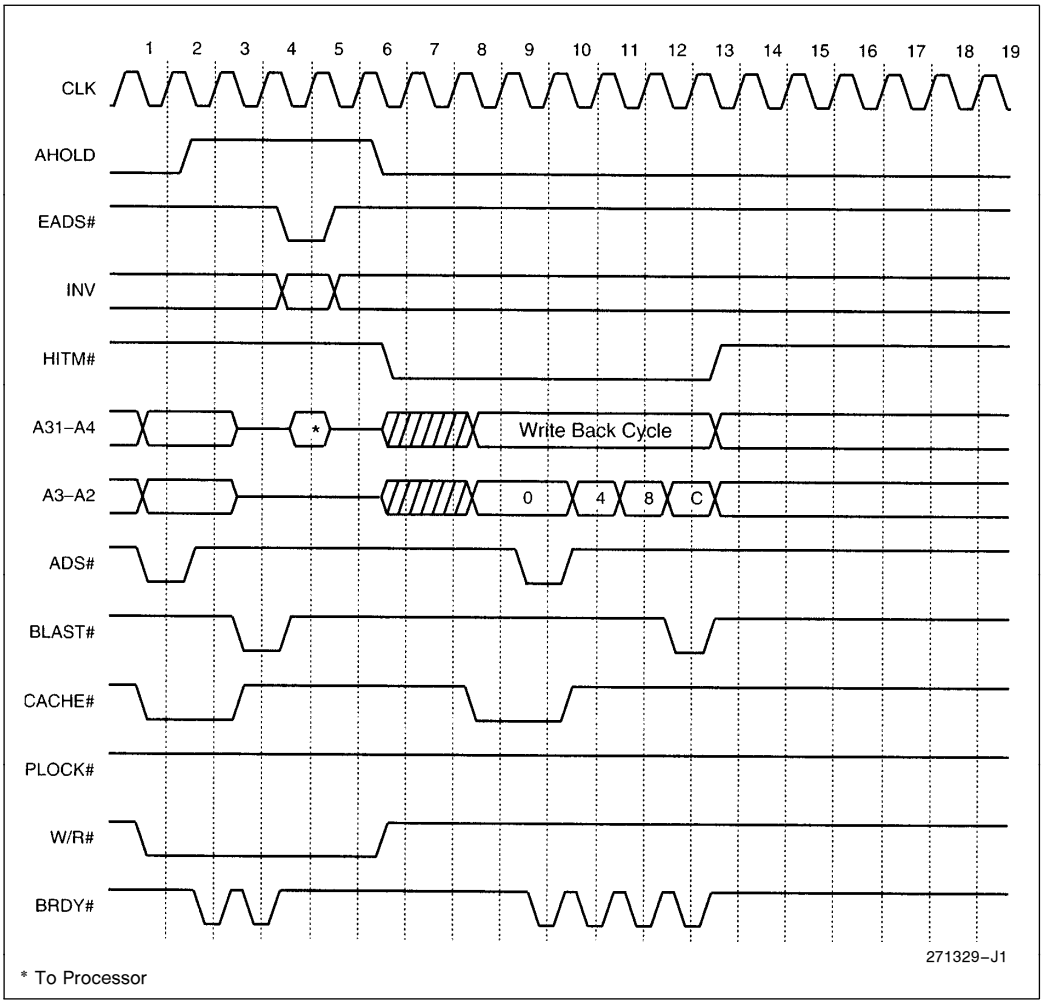


Figure 10-46. Snoop under AHOLD Overlaying Pseudo-Locked Cycle

10.3.6.2 Snoop under Hold during Pseudo-Locked Cycles

As shown in Figure 10-47, HOLD will not fracture the 64-bit burst transfer. The Write-Back Enhanced Intel486 processors will not issue HLDA until clock four. After the 64-bit transfer is completed, the Write-Back Enhanced Intel486 processors writes back the modified line to memory (if snoop hits to modified line). If the 64-bit transfer is non-bursted, the Write-Back Enhanced Intel486 processors can issue HLDA in between bus cycles for a 64-bit transfer.

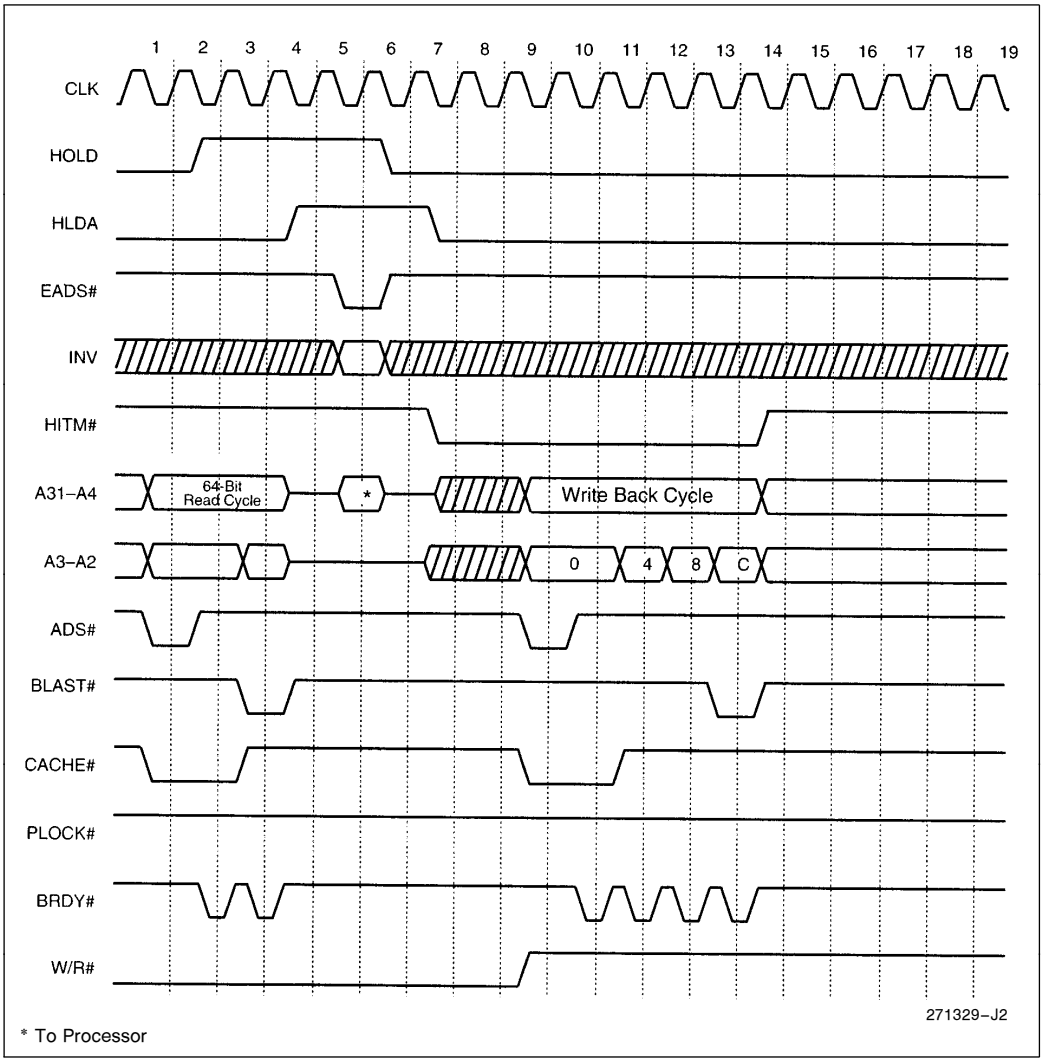


Figure 10-47. Snoop under HOLD Overlaying Pseudo-Locked Cycle

10.3.6.3 Snoop under BOFF# Overlaying a Pseudo-Locked Cycle

BOFF# is capable of fracturing any bus operation. As shown in Figure 10-48, BOFF# fractured a current 64-bit read cycle in clock four. If there is a snoop hit under BOFF#, the snoop write-back operation will begin after BOFF# is de-asserted. The 64-bit write cycle resumes after the snoop write-back operation completes.

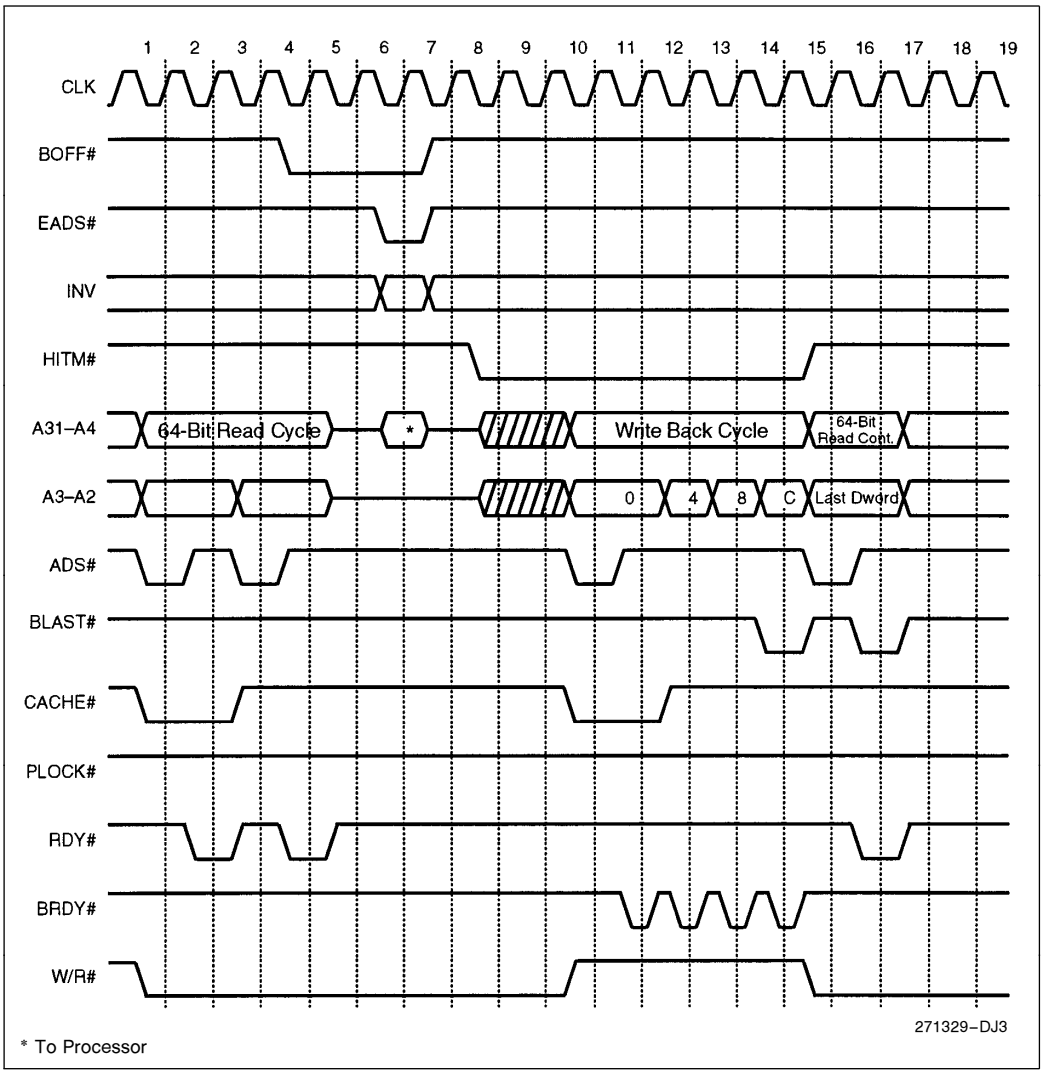


Figure 10-48. Snoop under BOFF# Overlaying a Pseudo-Locked Cycle

11.0 TESTABILITY

Testing in the Military Intel486 processor can be divided into two categories: Built-in Self Test (BIST) and external testing. The BIST tests the non-random logic, control ROM (CROM), translation lookaside buffer (TLB) and on-chip cache memory. External tests can be run on the TLB and the on-chip cache. The Military Intel486 processor also has a test mode in which all outputs are tri-stated.

11.1 Built-In Self Test (BIST)

The BIST is initiated by holding the AHOLD (address hold) HIGH for 1 CLK after RESET goes from HIGH to LOW, as shown in Figure 9.6. No bus cycles will be run by the Military Intel486 processor until the BIST is concluded. Note that for the Military Intel486 processor, the RESET must be active for 15 clocks with or without BIST enabled for warm resets. SRESET should not be driven active (i.e., high) when entering or during BIST. See Table 11-1 for approximate clocks and maximum completion times for different Military Intel486 processors.

The results of BIST is stored in the EAX register. The Military Intel486 processor has successfully passed the BIST if the contents of the EAX register are zero. If the results in EAX are not zero, then the BIST has detected a flaw in the Military Intel486 processor. The Military Intel486 processor performs reset and begins normal operation at the completion of the BIST.

The non-random logic, control ROM, on-chip cache and translation lookaside buffer (TLB) are tested during the BIST.

The cache portion of the BIST verifies that the cache is functional and that it is possible to read and write to the cache. The BIST manipulates test registers TR3, TR4 and TR5 while testing the cache. These test registers are described in section 11.2, ''On-Chip Cache Testing.''

The cache testing algorithm writes a value to each cache entry, reads the value back, and checks that the correct value was read back. The algorithm may be repeated more than once for each of the 512 cache entries using different constants. The IntelDX4 processor has 1024 cache entries. All other Military Intel486 processors have 512 cache entries.

The TLB portion of the BIST verifies that the TLB is functional and that it is possible to read and write to the TLB. The BIST manipulates test registers TR6 and TR7 while testing the TLB. TR6 and TR7 are described in section 11.3.2, ''TLB Test Registers TR6 and TR7.''

11.2 On-Chip Cache Testing

The on-chip cache testability hooks are designed to be accessible during the BIST and for assembly language testing of the cache.

The Military Intel486 processor contains a cache fill buffer and a cache read buffer. For testability writes, data must be written to the cache fill buffer before it can be written to a location in the cache. Data must be read from a cache location into the cache read buffer before the processor can access the data. The cache fill and cache read buffer are both 128 bits wide.

11.2.1 CACHE TESTING REGISTERS TR3, TR4 AND TR5

Figure 11-1 shows the three cache testing registers: the Cache Data Test Register (TR3), the Cache Status Test Register (TR4) and the Cache Control Test Register (TR5). External access to these registers is provided through MOV reg, TREG and MOV TREG, reg instructions.

Table 11-1. Maximum BIST Completion Time

Processor Type	Core Clock Freq.	Approximate Clocks	Approximate Time for Completions
Military Intel486 DX	33 MHz	1.05 million	32 milliseconds
IntelDX2™	50 MHz	0.6 million	24 milliseconds
IntelDX4™	75 MHz	1.6 million	22 milliseconds

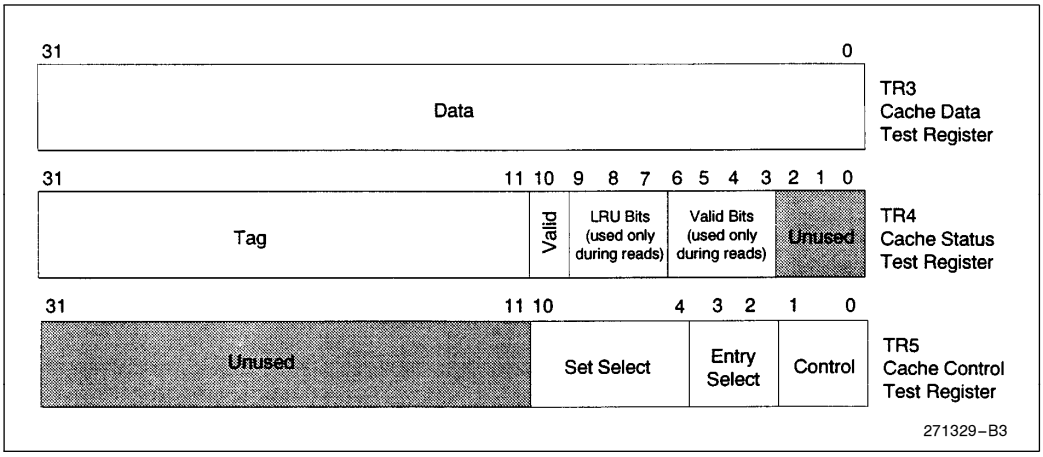


Figure 11-1. Cache Test Registers
(All Military Intel486™ Processors Except the IntelDX4™ Processor)

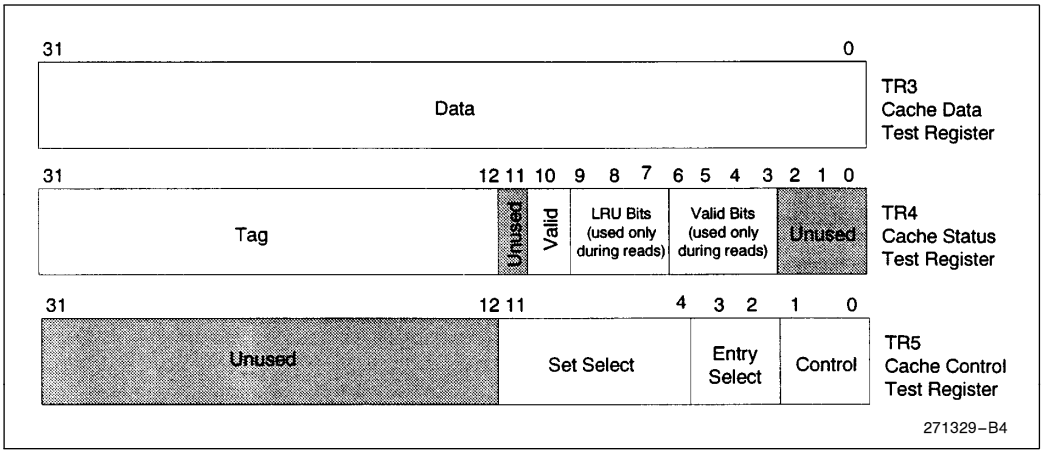


Figure 11-2. IntelDX4™ Processor Cache Test Registers

Cache Data Test Register: TR3

The cache fill buffer and the cache read buffer can only be accessed through TR3. Data to be written to the cache fill buffer must first be written to TR3. Data read from the cache read buffer must be loaded into TR3.

TR3 is 32 bits wide while the cache fill and read buffers are 128 bits wide. 32 bits of data must be written to TR3 four times to fill the cache fill buffer. 32 bits of data must be read from TR3 four times to empty the cache read buffer. The entry select bits in TR5 determine which 32 bits of data TR3 will access in the buffers.

Cache Status Test Register: TR4

TR4 handles tag, LRU and valid bit information during cache tests. TR4 must be loaded with a tag and a valid bit before a write to the cache. After a read from a cache entry, TR4 contains the tag and valid bit from that entry, and the LRU bits and four valid bits from the accessed set. Note that the IntelDX4 processor has one less bit in the TR4 TAG field. (See Figure 11-1.)

Cache Control Test Register: TR5

TR5 specifies which testability operation will be performed and the set and entry within the set which will be accessed. The set select field determines which will be accessed. Note that the IntelDX4 processor has an 8-bit set select field and 256 sets. All other Military Intel486 processors have a 7-bit set select field and 128 sets. (See Figure 11-1.)

The function of the two entry select bits depends on the state of the control bits. When the fill or read buffers are being accessed, the entry select bits point to the 32-bit location in the buffer being accessed. When a cache location is specified, the entry select bits point to one of the four entries in a set. (Refer to Table 11-2.)

Five testability functions can be performed on the cache. The two control bits in TR5 specify the operation to be executed. The five operations are:

1. Write cache fill buffer
2. Perform a cache testability write
3. Perform a cache testability read
4. Read the cache read buffer
5. Perform a cache flush

Table 11-2 shows the encoding of the two control bits in TR5 for the cache testability functions. Table 11-2 also shows the functionality of the entry and set select bits for each control operation.

The cache tests attempt to use as much of the normal operating circuitry as possible. Therefore, when cache tests are being performed, the cache must be disabled (the CD and NW bits in control register 0 (CR0) must be set to 1 to disable the cache. (See section 7.0, ‘‘On-Chip Cache.’’)

11.2.2 CACHE TESTING REGISTERS FOR THE INTELDX4 PROCESSOR

The cache testing registers for the IntelDX4 processor differ slightly from the other Military Intel486 processors. TR3 in the IntelDX4 processor is identical to other Military Intel486 processors. TR4 in the IntelDX4 processor uses bits 31 to 12 for the Tag field, and bit 11 is unused. TR5 uses bits 11 to 4 for the Set Select field. The Test Registers for the IntelDX4 processor are shown in Figure 11-2.

NOTE:

Software written for the Military Intel486 processor for testing the cache using the Test Register will produce failures due to the changes in the TAG bits and Set Select bits for the IntelDX4 processor.

Rewrite the code to take into account the 20 TAG bits and 8 Set Select bits to address the larger cache.

11.2.3 CACHE TESTABILITY WRITE

A testability write to the cache is a two step process. First the cache fill buffer must be loaded with 128 bits of data and TR4 loaded with the tag and valid bit. Next the contents of the fill buffer are written to a cache location.

Loading the fill buffer is accomplished by first writing to the entry select bits in TR5 and setting the control bits in TR5 to 00. The entry select bits identify one of four 32-bit locations in the cache fill buffer to put 32 bits of data. Following the write to TR5, TR3 is written with 32 bits of data which are immediately placed in the cache fill buffer. Writing to TR3 initiates the write to the cache fill buffer. The cache fill buffer is loaded with 128 bits of data by writing to TR5 and TR3 four times using a different entry select location each time.

TR4 must be loaded with the tag and valid bit (bit 10 in TR4) before the contents of the fill buffer are written to a cache location. **The IntelDX4 processor has a 20-bit tag in TR4. All other Military Intel486 processors use a 21-bit tag in TR4.**

The contents of the cache fill buffer are written to a cache location by writing TR5 with a control field of 01 along with the set select and entry select fields. The set select and entry select field indicate the location in the cache to be written. The normal cache LRU update circuitry updates the internal LRU bits for the selected set.

Table 11-2. Cache Control Bit Encoding and Effect of Control Bits on Entry Select and Set Select Functionality

Control Bits		Operation	Entry Select Bits Function	Set Select Bits
Bit 1	Bit 0			
0	0	Enable: Fill Buffer Write Read Buffer Read	Select 32-bit location in fill/read buffer	—
0	1	Perform Cache Write	Select an entry in set	Select a set to write to
1	0	Perform Cache Read	Select an entry in set	Select a set to read from
1	1	Perform Cache Flush	—	—

Note that a cache testability write can only be done when the cache is disabled for replaces (the CD bit is control register 0 is reset to 1). Care must be taken when directly writing to entries in the cache. If the entry is set to overlap an area of memory that is being used in external memory, that cache entry could inadvertently be used instead of the external memory. This is exactly the type of operation that one would desire if the cache were to be used as a high speed RAM. Also, a memory reference (or any external bus cycle) should not occur in between the move to TR4 and the move to TR5, in order to avoid having the value in TR4 change due to the memory reference.

11.2.4 CACHE TESTABILITY READ

A cache testability read is a two step process. First the contents of the cache location are read into the cache read buffer. Next the data is examined by reading it out of the read buffer.

Reading the contents of a cache location into the cache read buffer is initiated by writing TR5 with the control bits set to 10 and the desired set select and two-bit entry select. **The IntelDX4 processor has a seven-bit select field. All other Military Intel486 processors have an eight-bit select field.** In response to the write to TR5, TR4 is loaded with the 21-bit tag field and the single valid bit from the cache entry read. TR4 is also loaded with the three LRU bits and four valid bits corresponding to the cache set that was accessed. The cache read buffer is filled with the 128-bit value which was found in the data array at the specified location.

The contents of the read buffer are examined by performing four reads of TR3. Before reading TR3 the entry select bits in TR5 must loaded to indicate which of the four 32-bit words in the read buffer to transfer into TR3 and the control bits in TR5 must be loaded with 00. The register read of TR3 will initiate the transfer of the 32-bit value from the read buffer to the specified general purpose register.

Note that it is very important that the entire 128-bit quantity from the read buffer and also the information from TR4 be read before any memory references are allowed to occur. If memory operations are allowed to happen, the contents of the read buffer will be corrupted. This is because the testability operations use hardware that is used in normal memory accesses for the Military Intel486 processor whether the cache is enabled or not.

11.2.5 FLUSH CACHE

The control bits in TR5 must be written with 11 to flush the cache. None of the other bits in TR5 have any meaning when 11 is written to the control bits. Flushing the cache will reset the LRU bits and the valid bits to 0, but will not change the cache tag or data arrays.

When the cache is flushed by writing to TR5 the special bus cycle indicating a cache flush to the external system is not run. (See section 10.2.11, ‘‘Special Bus Cycles.’’) For normal operation, the cache should be flushed with the instruction INVD (Invalidate Data Cache) instruction or the WBINVD (Write-back and Invalidate Data Cache) instruction.

11.2.6 WRITE-BACK ENHANCED INTELDX4™ PROCESSOR

When in Enhanced Bus (Write-Back) mode, the Write-Back Enhanced IntelDX4 cache testing is a superset of the Standard Bus (Write-Through) mode. The additional cache testing features for the Write-Back Enhanced IntelDX4 processor are summarized below.

There are two state bits per cache line (VH and VL) instead of one (V). The assignment of VH and VL state bits is shown in Table 11-3.

Table 11-3. State Bit Assignments for the Write Back Enhanced IntelDX4™ Processor

State	VH, VL
M	1, 1
E	0, 1
S	1, 0
I	0, 0

The state assignments have been chosen so that VH is identical to the V-state of the IntelDX4 processor, when the Write-Back Enhanced IntelDX4 is in Standard Bus mode and where only S and I states are possible.

There are no changes to TR3 between the Standard Bus mode and the Enhanced Bus mode. The TR4 definition remains the same in Standard Bus mode as in Intel486 processors. The changes to TR4 in Enhanced Bus mode are shown in Figure 11-5.

In Enhanced Bus mode, the cache line state bits of all four lines of the set are no longer available, which eliminates the possibility of a conflicting definition of state bits for the selected entry. The entry's state bits are moved to positions 0 and 1.

TR5 is also the same in Standard Bus mode as in standard Intel486 processors. A minor change to TR5 in Enhanced Bus mode is illustrated in Figure 11-6.

In Enhanced Bus mode, control bit TR5.SLF (bit 13) is added to allow 1,1 of TR5.CTL (bits 1-0) to perform two different kinds of cache flushes. When SLF = 0, CTL = 1,1 performs a single clock invalidate of all lines in the cache, which will **NOT** write-back M-State lines. If SLF = 1, the specific line addressed will be written back (IF in M-State) and invalidated. The state of SLF is significant only when CTL = 1,1.

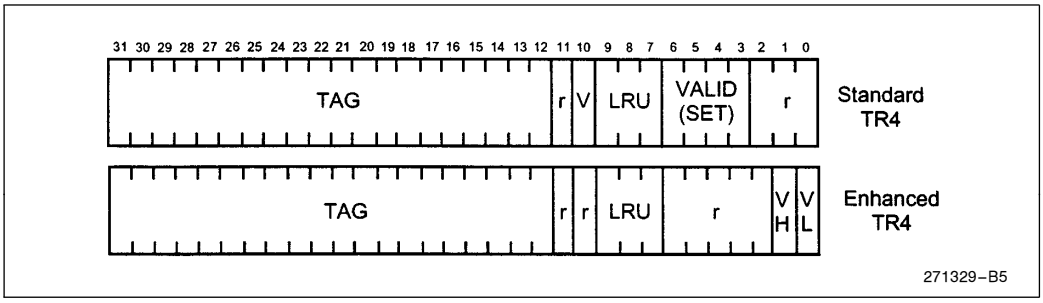


Figure 11-3. TR4 Definition for Standard and Enhanced Bus Modes for the Write-Back Enhanced IntelDX4™Processor

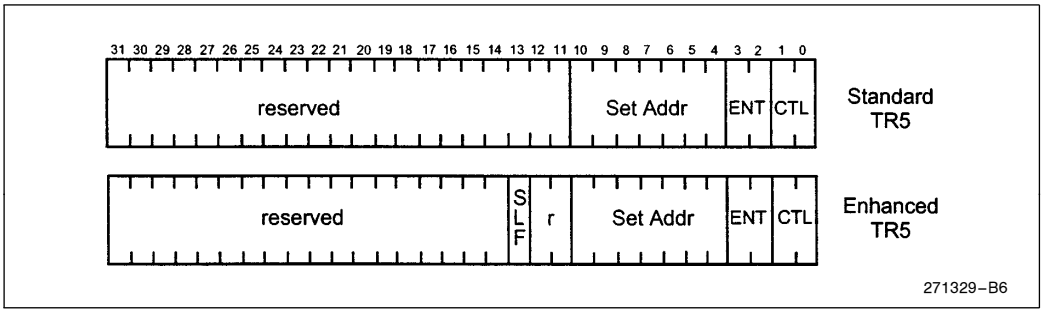


Figure 11-4. TR5 Definition for Standard and Enhanced Bus Modes for the Write-Back Enhanced IntelDX4™ Processor

11.3 Translation Lookaside Buffer (TLB) Testing

The Military Intel486 processor TLB testability hooks are similar to those in the Intel386 processor. The testability hooks have been enhanced to provide added test features and to include new features in the Military Intel486 processor. The TLB testability hooks are designed to be accessible during the BIST and for assembly language testing of the TLB.

11.3.1 TRANSLATION LOOKASIDE BUFFER ORGANIZATION

The Military Intel486 processor TLB is 4-way set associative and has space for 32 entries. The TLB is logically split into three blocks shown in Figure 11-5.

The data block is physically split into four arrays, each with space for eight entries. An entry in the data block is 22 bits wide containing a 20-bit physical address and two bits for the page attributes. The page attributes are the PCD (page cache disable) bit and the PWT (page write-through) bit. Refer to section 7.6, ‘‘Page Cacheability,’’ for a discussion of the PCD and PWT bits.

The tag block is also split into four arrays, one for each of the data arrays. A tag entry is 21 bits wide containing a 17-bit linear address and four protection bits. The protection bits are valid (V), user/supervisor (U/S), read/write (R/W) and dirty (D).

The third block contains eight three bit quantities used in the pseudo least recently used (LRU) replacement algorithm. These bits are called the LRU bits. Unlike the on-chip cache, the TLB will replace a valid line even when there is an invalid line in a set.

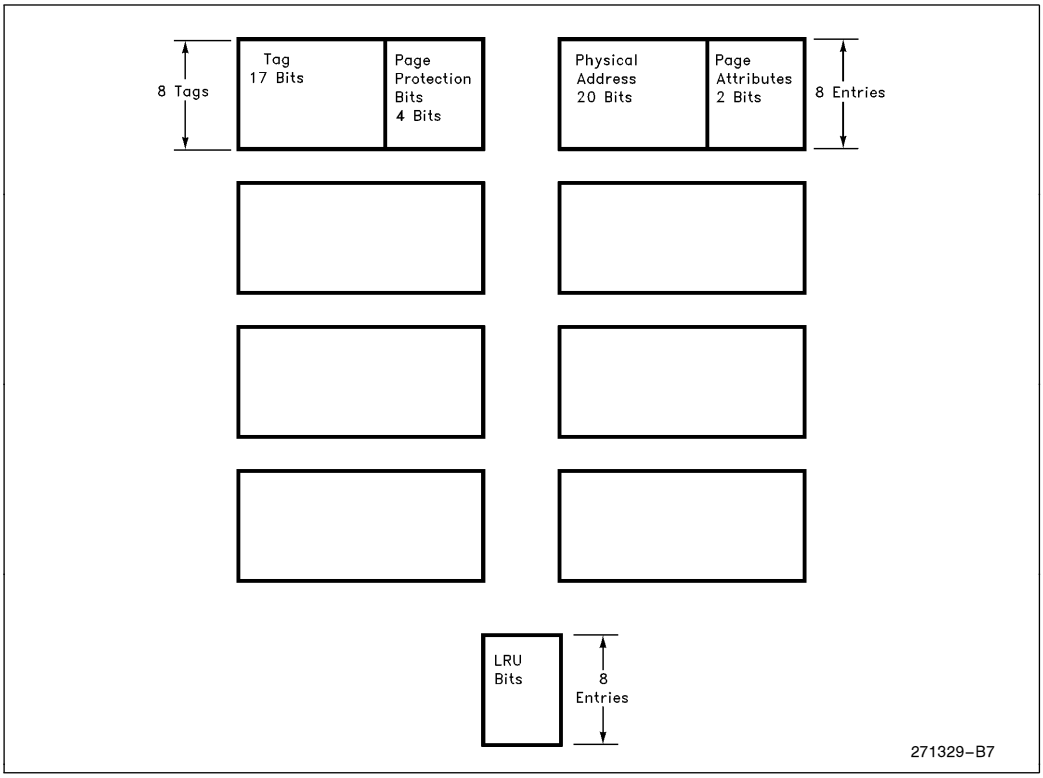


Figure 11-5. TLB Organization

11.3.2 TLB TEST REGISTERS TR6 AND TR7

The two TLB test registers are shown in Figure 11-6. TR6 is the command test register and TR7 is the data test register. External access to these registers is provided through MOV reg,TREG and MOV TREG,reg instructions.

Command Test Register: TR6

TR6 contains the tag information and control information used in a TLB test. Loading TR6 with tag and control information initiates a TLB write or lookup test.

TR6 contains three bit fields, a 20-bit linear address (bits 12–31), seven bits for the TLB tag protection bits (bits 5-11) and one bit (bit 0) to define the type of operation to be performed on the TLB.

The 20-bit linear address forms the tag information used in the TLB access. The lower three bits of the linear address select which of the eight sets are accessed. The upper 17 bits of the linear address form the tag stored in the tag array.

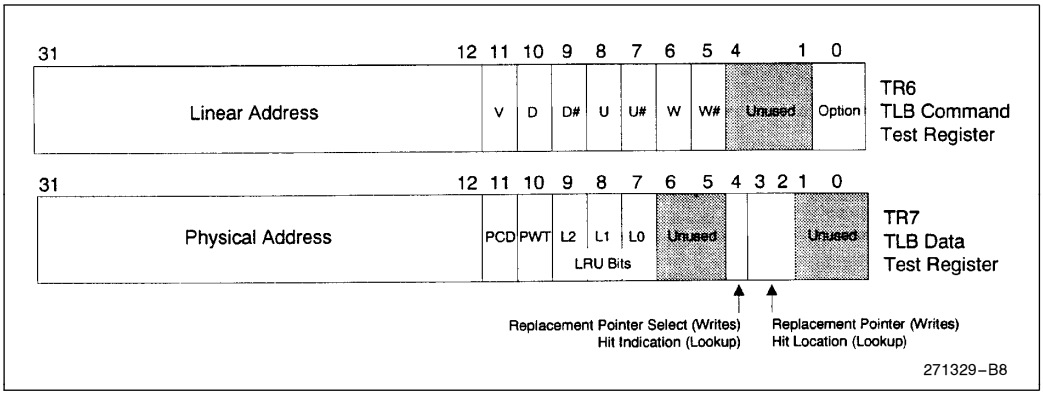


Figure 11-6. TLB Test Registers

The seven TLB tag protection bits are described below.

V: The valid bit for this TLB entry

D,D#: The dirty bit for/from the TLB entry

U,U#: The user/supervisor bit for/from the TLB entry

W,W#: The read/write bit for/from the TLB entry

Two bits are used to represent the D, U/S and R/W bits in the TLB tag to permit the option of a forced miss or hit during a TLB lookup operation. The forced miss or hit will occur regardless of the state of the actual bit in the TLB. The meaning of these pairs of bits is given in Table 11-4.

The operation bit in TR6 determines if the TLB test operation will be a write or a lookup. The function of the operation bit is given in Table 11-5.

Table 11-4. Meaning of a Pair of TR6 Protection Bits

TR6 Protection Bit (B)	TR6 Protection Bit# (B#)	Meaning on TLB Write Operation	Meaning on TLB Lookup Operation
0	0	Undefined	Miss any TLB TAG Bit B
0	1	Write 0 to TLB TAG Bit B	Match TLB TAG Bit B if 0
1	0	Write 1 to TLB TAG Bit B	Match TLB TAG Bit B if 1
1	1	Undefined	Match any TLB TAG Bit B

Table 11-5. TR6 Operation Bit Encoding

TR6 Bit 0	TLB Operation to Be Performed
0	TLB Write
1	TLB Lookup

Data Test Register: TR7

TR7 contains the information stored or read from the data block during a TLB test operation. Before a TLB test write, TR7 contains the physical address and the page attribute bits to be stored in the entry. After a TLB test lookup hit, TR7 contains the physical address, page attributes, LRU bits and entry location from the access.

TR7 contains a 20-bit physical address (bits 12–31), PLD bit (bit 11), PWT bit (bit 10), and three bits for the LRU bits (bits 7–9). The LRU bits in TR7 are only used during a TLB lookup test. The functionality of TR7 bit 4 differs for TLB writes and lookups. The encoding of bit 4 is defined in Table 11-6 and Table 11-7. Finally, TR7 contains two bits (bits 2–3) to specify a TLB replacement pointer or the location of a TLB hit.

Table 11-6. Encoding of Bit 4 of TR7 on Writes

TR7 Bit 4	Replacement Pointer Used on TLB Write
0	Pseudo-LRU Replacement Pointer
1	Data Test Register Bits 3:2

A replacement pointer is used during a TLB write. The pointer indicates which of the four entries in an accessed set is to be written. The replacement pointer can be specified to be the internal LRU bits or bits 2–3 in TR7. The source of the replacement pointer is specified by TR7 bit 4. The encoding of bit 4 during a write is given by Table 11-6.

Note that both testability writes and lookups affect the state of the internal LRU bits regardless of the replacement pointer used. All TLB write operations (testability or normal operation) cause the written entry to become the most recently used. For example, during a testability write with the replacement pointer specified by TR7 bits 2–3, the indicated entry is written and that entry becomes the most recently used as specified by the internal LRU bits.

There are two TLB testing operations: write entries into the TLB, and perform TLB lookups. One major enhancement over TLB testing in the Intel386 processor is that paging need not be disabled while executing testability writes or lookups.

Note that any time one TLB set contains the same linear address in more than one of its entries, looking up that linear address will give unpredictable results. Therefore a single linear address should not be written to one TLB set more than once.

Table 11-7. Encoding of Bit 4 of TR7 on Lookups

TR7 Bit 4	Meaning after TLB Lookup Operation
0	TLB Lookup Resulted in a Miss
1	TLB Lookup Resulted in a Hit

11.3.3 TLB WRITE TEST

To perform a TLB write TR7 must be loaded followed by a TR6 load. The register operations must be performed in this order because the TLB operation is triggered by the write to TR6.

TR7 is loaded with a 20-bit physical address and values for PCD and PWT to be written to the data portion of the TLB. In addition, bit 4 of TR7 must be loaded to indicate whether to use TR7 bits 3-2 or the internal LRU bits as the replacement pointer on the TLB write operation. Note that the LRU bits in TR7 are not used in a write test.

TR6 must be written to initiate the TLB write operation. Bit 0 in TR6 must be reset to zero to indicate a TLB write. The 20-bit linear address and the seven page protection bits must also be written in TR6 to specify the tag portion of the TLB entry. Note that the three least significant bits of the linear address specify which of the eight sets in the data block will be loaded with the physical address data. Thus only 17 of the linear address bits are stored in the tag array.

11.3.4 TLB LOOKUP TEST

To perform a TLB lookup it is only necessary to write the proper tags and control information into TR6. Bit 0 in TR6 must be set to 1 to indicate a TLB lookup. TR6 must be loaded with a 20-bit linear address and the seven protection bits. To force misses and matches of the individual protection bits on TLB lookups, set the seven protection bits as specified in Table 11-4.

A TLB lookup operation is initiated by the write to TR6. TR7 will indicate the result of the lookup operation following the write to TR6. The hit/miss indication can be found in TR7 bit 4 (see Table 11-7).

TR7 will contain the following information if bit 4 indicated that the lookup test resulted in a hit. Bits 2–3 will indicate in which set the match occurred. The 22 most significant bits in TR7 will contain the physical address and page attributes contained in the entry. Bits 9–7 will contain the LRU bits associated with the accessed set. The state of the LRU bits is previous to their being updated for the current lookup.

If bit 4 in TR7 indicated that the lookup test resulted in a miss the remaining bits in TR7 are undefined.

Again it should be noted that a TLB testability lookup operation affects the state of the LRU bits. The LRU bits will be updated if a hit occurred. The entry which was hit will become the most recently used.

11.4 Tri-State Output Test Mode

The Military Intel486 processor provides the ability to float all its outputs and bidirectional pins, except for the VOLDET pin in the IntelDX4 processor. This includes all pins floated during bus hold as well as pins which are never floated in normal operation of the chip (HLDA, BREQ, FERR# and PCHK#). When the Military Intel486 processor is in the tri-state output test mode external testing can be used to test board connections.

The tri-state test mode is invoked if FLUSH# is sampled active at the falling edge of RESET. FLUSH# is an asynchronous signal. When driven, FLUSH# should be asserted for 2 clocks before and 2 clocks after RESET is de-asserted. If FLUSH# is driven synchronously, the tri-state output test mode is initiated by driving FLUSH# so that it is sampled active in the clock prior to RESET going low and ensuring that specified setup and hold times are met. The outputs are guaranteed to tri-state no later than 10 clocks after RESET goes low (see Figure 9.6). The Military Intel486 processor remains in the tri-state test mode until the next RESET.

11.5 Military Intel486 Processor Boundary Scan (JTAG)

The Military Intel486 processor provides additional testability features compatible with the IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1). The test logic provided allows for testing to insure that components function correctly, that interconnections between various components are correct, and that various components interact correctly on the printed circuit board.

The boundary scan test logic consists of a boundary scan register and support logic that are accessed through a test access port (TAP). The TAP provides a simple serial interface that makes it possible to test all signal traces with only a few probes.

The TAP can be controlled via a bus master. The bus master can be either automatic test equipment or a component (PLD) that interfaces to the four-pin test bus.

11.5.1 BOUNDARY SCAN ARCHITECTURE

The boundary scan test logic contains the following elements:

- Test access port (TAP), consisting of input pins TMS, TCK, and TDI; and output pin TDO.
- TAP controller, which interprets the inputs on the test mode select (TMS) line and performs the corresponding operation. The operations performed by the TAP include controlling the instruction and data registers within the component.
- Instruction register (IR), which accepts instruction codes shifted into the test logic on the test data input (TDI) pin. The instruction codes are used to select the specific test operation to be performed or the test data register to be accessed.
- Test data registers: The Military Intel486 processor contains three test data registers: Bypass register (BPR), Device Identification register (DID), and Boundary Scan register (BSR).

The instruction and test data registers are separate shift-register paths connected in parallel and have a common serial data input and a common serial data output connected to the TAP signals, TDI and TDO, respectively.

11.5.2 DATA REGISTERS

The Military Intel486 processor contains the two required test data registers; bypass register and

boundary scan register. In addition, they also have a device identification register.

Each test data register is serially connected to TDI and TDO, with TDI connected to the most significant bit and TDO connected to the least significant bit of the test data register.

Data is shifted one stage (bit position within the register) on each rising edge of the test clock (TCK). In addition the Military Intel486 processor contains a runbist register to support the RUNBIST boundary scan instruction.

11.5.2.1 Bypass Register

The Bypass Register is a one-bit shift register that provides the minimal length path between TDI and TDO. This path can be selected when no test operation is being performed by the component to allow rapid movement of test data to and from other components on the board. While the bypass register is selected data is transferred from TDI to TDO without inversion.

11.5.2.2 Boundary Scan Register

The Boundary Scan Register is a single shift register path containing the boundary scan cells that are connected to all input and output pins of the Military Intel486 processor. Figure 11-7 shows the logical structure of the boundary scan register. While output cells determine the value of the signal driven on the corresponding pin, input cells only capture data; they do not affect the normal operation of the device. Data is transferred without inversion from TDI to TDO through the boundary scan register during scanning. The boundary scan register can be operated by the EXTEST and SAMPLE instructions. The boundary scan register order is described in section 11.5.5 ‘‘Boundary Scan Register Bits and Bit Orders.’’

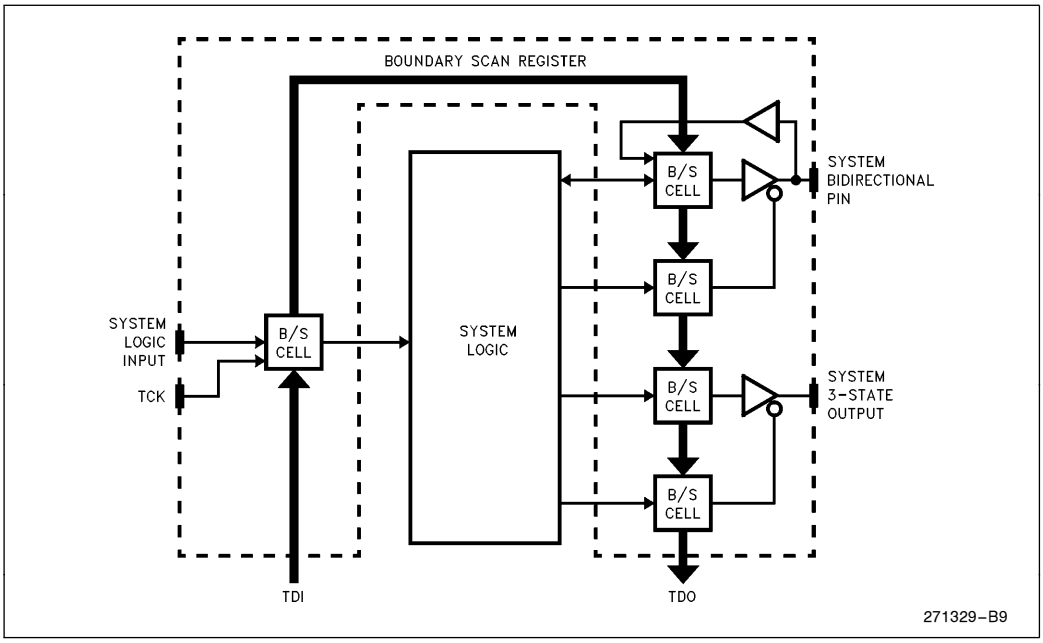


Figure 11-7. Logical Structure of Boundary Scan Register

11.5.2.3 Device Identification Register

The Device Identification Register contains the manufacturer's identification code, part number code, and version code. Table 11-8 lists the codes corresponding to the Military Intel486 processor.

11.5.2.4 Runbist Register

The Runbist Register is a one bit register used to report the results of the Military Intel486 processor BIST when it is initiated by the RUNBIST instruction. This register is loaded with a ''1'' prior to invoking the BIST and is loaded with ''0'' upon successful completion.

11.5.3 INSTRUCTION REGISTER

The Instruction Register (IR) allows instructions to be serially shifted into the device. The instruction selects the particular test to be performed, the test data register to be accessed, or both. The instruction register is four (4) bits wide. The most significant bit is connected to TDI and the least significant bit is connected to TDO. There are no parity bits associated with the Instruction register. Upon entering the Capture-IR TAP controller state, the Instruction register is loaded with the default instruction ''0001,'' SAMPLE/PRELOAD. Instructions are shifted into the instruction register on the rising edge of TCK while the TAP controller is in the SHIFT-IR state.

11.5.3.1 Boundary Scan Instruction Set

The Military Intel486 processor supports all three mandatory boundary scan instructions (BYPASS, SAMPLE/PRELOAD, and EXTEST) along with two optional instructions (IDCODE and RUNBIST). Table 11-9 lists the Military Intel486 processor boundary scan instruction codes. The instructions listed as PRIVATE cause TDO to become enabled in the Shift-DR state and cause ''0'' to be shifted out of TDO on the rising edge of TCK. Execution of the PRIVATE instructions will not cause hazardous operation of the Military Intel486 processor.

EXTEST The instruction code is ''0000.'' The EXTEST instruction allows testing of circuitry external to the component package, typically board interconnects. It does so by driving the values loaded into the Military Intel486 processor's boundary scan register out on the output pins corresponding to each boundary scan cell and capturing the values on Military Intel486 processor input pins to be loaded into their corresponding boundary scan register locations. I/O pins are selected as input or output, depending on the value loaded into their control setting locations in the boundary scan register. Values shifted into input latches in the boundary scan register are never used by the internal logic of the Military Intel486 processor.

Table 11-8. Boundary Scan Component Identification Codes

Processor Type	Version	V_{CC} 1 = 3.3V 0 = 5V	Intel Architecture Type	Family	Model	MFG ID Intel = 009H	1st Bit	Boundary Scan ID (Hex)
Military Intel486 DX processor (5V)	xxxx*	0	000001	0100	00001	00000001001	1	x0281013H
IntelDX2 processor (5V)	xxxx*	0	000001	0100	00101	00000001001	1	x0285013H
IntelDX4™ processor (3.3V)	xxxx*	1	000001	0100	01001	00000001001	1	x8289013H

NOTE:
*Contact Intel for details

Table 11-9. Boundary Scan Instruction Codes

Instruction Code	Instruction Name
0000	EXTEST
0001	SAMPLE
0010	IDCODE
0011	PRIVATE
0100	PRIVATE
0101	PRIVATE
0110	PRIVATE
0111	PRIVATE
1000	RUNBIST
1001	PRIVATE
1010	PRIVATE
1011	PRIVATE
1100	PRIVATE
1101	PRIVATE
1110	PRIVATE
1111	BYPASS

NOTE:
After using the EXTEST instruction, the Military Intel486 processor must be reset before normal (non-boundary scan) use.

SAMPLE/PRELOAD The instruction code is ''0001.'' The SAMPLE/PRELOAD has two functions that it performs. When the TAP controller is in the Capture-DR state, the SAMPLE/PRELOAD instruction allows a ''snap-shot'' of the normal operation of the component without interfering with that normal operation. The instruction causes boundary scan register cells associated with outputs to sample the value being driven by the Military Intel486 processor. It causes the cells associated with inputs to sample the value being driven into the Military Intel486 processor. On both outputs and inputs the sampling occurs on the rising edge of TCK. When the TAP controller is in the Update-DR state, the SAMPLE/PRELOAD instruction preloads data to the device pins to be driven to the board by executing the EXTEST instruction. Data is preloaded to the pins from the boundary scan register on the falling edge of TCK.

IDODE The instruction code is ''0010.'' The IDCODE instruction selects the device identification register to be connected to TDI and TDO, allowing the device identification code to be shifted out of the device on TDO. Note that the device identification register is not altered by data being shifted in on TDI.

BYPASS The instruction code is ''1111.'' The BYPASS instruction selects the bypass register to be connected to TDI and TDO, effectively bypassing the test logic on the Military Intel486 processor by reducing the shift length of the device to one bit. Note that an open circuit fault in the board level test data path will cause the bypass register to be selected following an instruction scan cycle due to the pull-up resistor on the TDI input. This has been done to prevent any unwanted interference with the proper operation of the system logic.

RUNBIST The instruction code is ''1000.'' The RUNBIST instruction selects the one (1) bit runbist register, loads a value of ''1'' into the runbist register, and connects it to TDO. It also initiates the built-in self test (BIST) feature of the Military Intel486 processor, which is able to detect approximately 60% of the stuck-at faults on the Military Intel486 processor. The Military Intel486 processor ac/dc specifications for V_{CC} and CLK must be met and RESET must have been asserted at least once prior to executing the RUNBIST boundary scan instruction. After loading the RUNBIST instruction code in the instruction register, the TAP controller must be placed in the Run-Test/Idle state. BIST begins on the first rising edge of TCK after entering the Run-Test/Idle state. The TAP controller must remain in the Run-Test/Idle state until BIST is completed. It requires 1.2 million clock (CLK) cycles to complete BIST and report the result to the runbist register. After completing the 1.2 million clock (CLK) cycles, the value in the runbist register should be shifted out on

TDO during the Shift-DR state. A value of ‘‘0’’ being shifted out on TDO indicates BIST successfully completed. A value of ‘‘1’’ indicates a failure occurred. After executing the RUNBIST instruction, the Military Intel486 processor must be reset prior to normal operation.

11.5.4 TEST ACCESS PORT (TAP) CONTROLLER

The TAP controller is a synchronous, finite state machine. It controls the sequence of operations of the test logic. The TAP controller changes state only in response to the following events:

1. a rising edge of TCK
2. power-up.

The value of the test mode state (TMS) input signal at a rising edge of TCK controls the sequence of the state changes. The state diagram for the TAP controller is shown in Figure 11-8. Test designers must consider the operation of the state machine in order to design the correct sequence of values to drive on TMS.

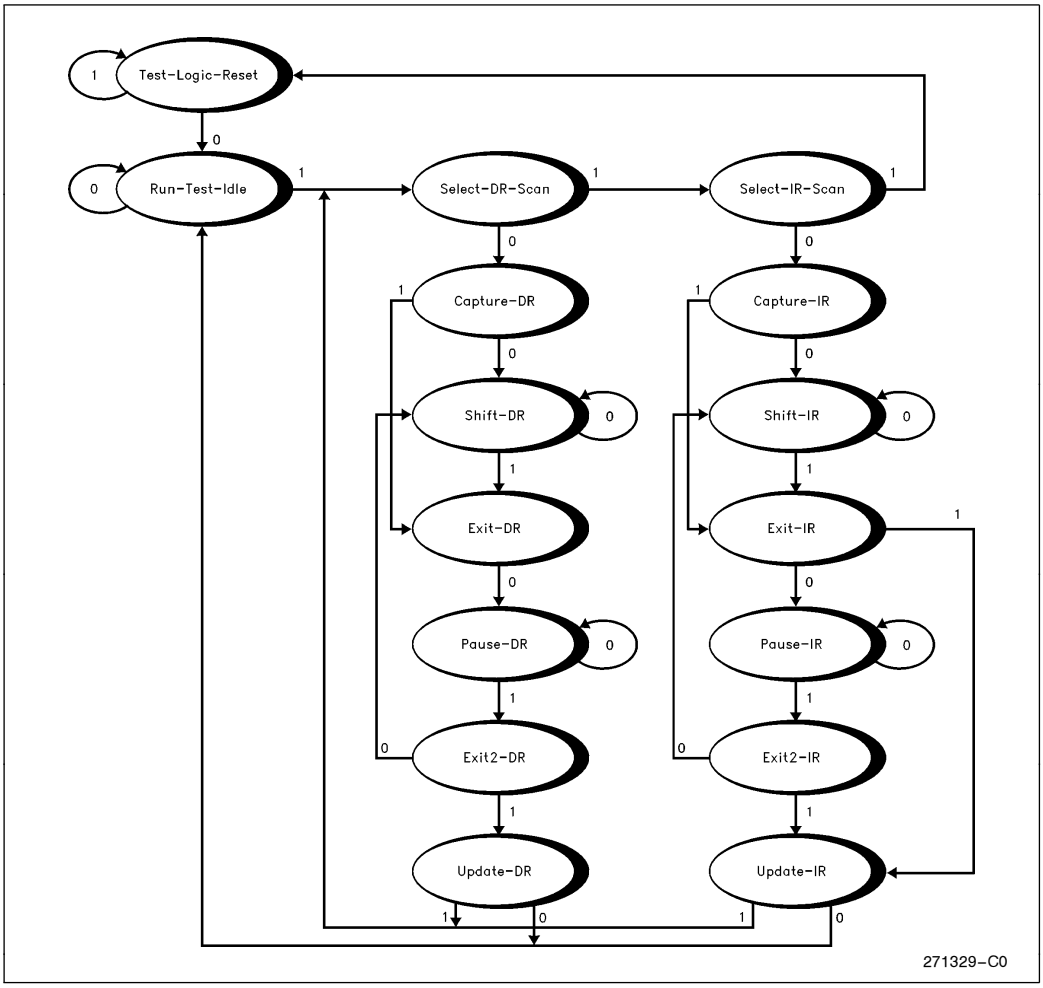


Figure 11-8. TAP Controller State Diagram

11.5.4.1 Test-Logic-Reset State

In this state, the test logic is disabled so that normal operation of the device can continue unhindered. This is achieved by initializing the instruction register such that the IDCODE instruction is loaded. No matter what the original state of the controller, the controller enters Test-Logic-Reset state when the TMS input is held high (1) for at least five rising edges of TCK. The controller remains in this state while TMS is high. The TAP controller is also forced to enter this state at power-up.

11.5.4.2 Run-Test/Idle State

A controller state between scan operations. Once in this state, the controller remains in this state as long as TMS is held low. In devices supporting the RUNBIST instruction, the BIST is performed during this state and the result is reported in the runbist register. For instruction not causing functions to execute during this state, no activity occurs in the test logic. The instruction register and all test data registers retain their previous state. When TMS is high and a rising edge is applied to TCK, the controller moves to the Select-DR state.

11.5.4.3 Select-DR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous state. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-DR state, and a scan sequence for the selected test data register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Select-IR-Scan state.

The instruction does not change in this state.

11.5.4.4 Capture-DR State

In this state, the boundary scan register captures input pin data if the current instruction is EXTEST or SAMPLE/PRELOAD. The other test data registers, which do not have parallel input, are not changed.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or the Shift-DR state if TMS is low.

11.5.4.5 Shift-DR State

In this controller state, the test data register connected between TDI and TDO as a result of the current instruction shifts data one stage toward its serial output on each rising edge of TCK.

The instruction does not change in this state.

When the TAP controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-DR state if TMS is high or remains in the Shift-DR state if TMS is low.

11.5.4.6 Exit1-DR State

This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-DR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

11.5.4.7 Pause-DR State

The pause state allows the test controller to temporarily halt the shifting of data through the test data register in the serial path between TDI and TDO. An example of using this state could be to allow a tester to reload its pin memory from disk during application of a long test sequence.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-DR state.

11.5.4.8 Exit2-DR State

This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-DR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-DR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

11.5.4.9 Update-DR State

The boundary scan register is provided with a latched parallel output to prevent changes at the parallel output while data is shifted in response to the EXTEST and SAMPLE/PRELOAD instructions. When the TAP controller is in this state and the boundary scan register is selected, data is latched onto the parallel output of this register from the shift-register path on the falling edge of TCK. The data held at the latched parallel output does not change other than in this state.

All test data registers selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

11.5.4.10 Select-IR-Scan State

This is a temporary controller state. The test data register selected by the current instruction retains its previous value. If TMS is held low and a rising edge is applied to TCK when in this state, the controller moves into the Capture-IR state, and a scan sequence for the instruction register is initiated. If TMS is held high and a rising edge is applied to TCK, the controller moves to the Test-Logic-Reset state.

The instruction does not change in this state.

11.5.4.11 Capture-IR State

In this controller state the shift register contained in the instruction register loads the fixed value ‘‘0001’’ on the rising edge of TCK.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state. When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or the Shift-IR state if TMS is held low.

11.5.4.12 Shift-IR State

In this state the shift register contained in the instruction register is connected between TDI and TDO and shifts data one stage towards its serial output on each rising edge of TCK.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

When the controller is in this state and a rising edge is applied to TCK, the controller enters the Exit1-IR state if TMS is held high, or remains in the Shift-IR state if TMS is held low.

11.5.4.13 Exit1-IR State

This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Pause-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

11.5.4.14 Pause-IR State

The pause state allows the test controller to temporarily halt the shifting of data through the instruction register.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

The controller remains in this state as long as TMS is low. When TMS goes high and a rising edge is applied to TCK, the controller moves to the Exit2-IR state.

11.5.4.15 Exit2-IR State

This is a temporary state. While in this state, if TMS is held high, a rising edge applied to TCK causes the controller to enter the Update-IR state, which terminates the scanning process. If TMS is held low and a rising edge is applied to TCK, the controller enters the Shift-IR state.

The test data register selected by the current instruction retains its previous value during this state. The instruction does not change in this state.

11.5.4.16 Update-IR State

The instruction shifted into the instruction register is latched onto the parallel output from the shift-register path on the falling edge of TCK. Once the new instruction has been latched, it becomes the current instruction.

Test data registers selected by the new current instruction retain the previous value.

11.5.5 BOUNDARY SCAN REGISTER BITS AND BIT ORDERS

The boundary scan register contains a cell for each pin, as well as cells for control of I/O and tri-state pins.

Military Intel486 DX and IntelDX2 Processor Boundary Scan Register Bits

The following is the bit order of the Military Intel486 DX and IntelDX2 processor boundary scan register (from left to right and top to bottom. See notes below):

TDO ← A2, A3, A4, A5, UP#, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, DP0, D0, D1, D2, D3, D4, D5, D6, D7, DP1, D8, D9, D10, D11, D12, D13, D14, D15, DP2, D16, D17, D18, D19, D20, D21, D22, D23, DP3, D24, D25, D26, D27, D28, D29, D30, D31, STPCLK#, IGNNE#, FERR#, SMI#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3#, BE2#, BE1#, BE0#, BREQ, W/R#, HLDA, CLK, Reserved, AHOLD, HOLD, KEN#, RDY#, BS8#, BS16#, BOFF#, BRDY#, PCHK#, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRTL ← TDI

Write-Back Enhanced IntelDX4™ Processors Boundary Scan Register Bits

The following is the bit order of the Write-Back Enhanced IntelDX4 processor boundary scan register (from left to right and top to bottom. See notes below):

TDO ← A2, A3, A4, A5, UP#, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19, A20, A21, A22, A23, A24, A25, A26, A27, A28, A29, A30, A31, DP0, D0, D1, D2, D3, D4, D5, D6, D7, DP1, D8, D9, D10, D11, D12, D13, D14, D15, DP2, D16, D17, D18, D19, D20, D21, D22, D23, DP3, D24, D25, D26, D27, D28, D29, D30, D31, STPCLK#, IGNNE#, INV, CACHE#, FERR#, SMI#, WB/WT#, HITM#, SMIACT#, SRESET, NMI, INTR, FLUSH#, RESET, A20M#, EADS#, PCD, PWT, D/C#, M/IO#, BE3, BE2, BE1, BE0, BREQ, W/R#, HLDA, CLK, AHOLD, HOLD, KEN#, RDY#, CLKMUL, BS8#, BS16#, BOFF#, BRDY#, PCHK#, LOCK#, PLOCK#, BLAST#, ADS#, MISCCTL, BUSCTL, ABUSCTL, WRCTL ← TDI

NOTES:

''Reserved'' corresponds to no connect ''NC'' or ''INC'' signals on the Military Intel486 processor.

All the *CTL cells are control cells that are used to select the direction of bidirectional pins or tri-state output pins. If '1' is loaded into the control cell (*CTL), the associated pin(s) are tri-stated or selected as input. The following lists the control cells and their corresponding pins.

1. WRCTL controls the D31–D0 and DP3–DP0 pins.
2. ABUSCTL controls the A31–A2 pins.
3. BUSCTL controls the ADS#, BLAST#, PLOCK#, LOCK#, WR#, BE0#, BE1#, BE2#, BE3#, MIO#, DC#, PWT, and PCD pins.
4. MISCCTL controls the PCHK#, HLDA, and BREQ pins.

11.5.6 TAP CONTROLLER INITIALIZATION

The TAP controller is automatically initialized when a device is powered up. In addition, the TAP controller can be initialized by applying a high signal level on the TMS input for five TCK periods.

11.5.7 BOUNDARY SCAN DESCRIPTION LANGUAGE (BSDL) FILES

See Appendix C for an example of a BSDL file for Military Intel486 processors.

12.0 DEBUGGING SUPPORT

The Military Intel486 processor provides several features that simplify the debugging process. The three categories of on-chip debugging aids are:

1. Code execution breakpoint opcode (0CCH),
2. Single-step capability provided by the TF bit in the flag register, and
3. Code and data breakpoint capability provided by the Debug Registers DR0–3, DR6, and DR7.

12.1 Breakpoint Instruction

A single-byte-opcode breakpoint instruction is available for use by software debuggers. The breakpoint opcode is 0CCH, and generates an exception 3 trap when executed. In typical use, a debugger program can ''plant'' the breakpoint instruction at all desired code execution breakpoints. The single-byte breakpoint opcode is an alias for the two-byte general software interrupt instruction, INT n, where n = 3. The only difference between INT 3 (0CCh) and INT n is that INT 3 is never IOPL-sensitive, while INT n is IOPL-sensitive in Protected Mode and Virtual 8086 Mode.

12.2 Single-Step Trap

If the single-step flag (TF, bit 8) in the EFLAG register is found to be set at the end of an instruction, a single-step exception occurs. The single-step exception is auto vectored to exception number 1. Precisely, exception 1 occurs as a trap after the instruction following the instruction which set TF. In typical practice, a debugger sets the TF bit of a flag register image on the debugger's stack. It then typically transfers control to the user program and loads the flag image with a signal instruction, the IRET instruction. The single-step trap occurs after executing one instruction of the user program.

Because exception 1 occurs as a trap (that is, it occurs after the instruction has already executed), the CS:EIP pushed onto the debugger's stack points to the next unexecuted instruction of the program being debugged. An exception 1 handler, merely by ending with an IRET instruction, can therefore efficiently support single-stepping through a user program.

12.3 Debug Registers

The Debug Registers are an advanced debugging feature of the Military Intel486 processor. They allow data access breakpoints as well as code execution breakpoints. Because the breakpoints are indicated by on-chip registers, an instruction execution breakpoint can be placed in ROM code or in code shared by several tasks, neither of which can be supported by the INT3 breakpoint opcode.

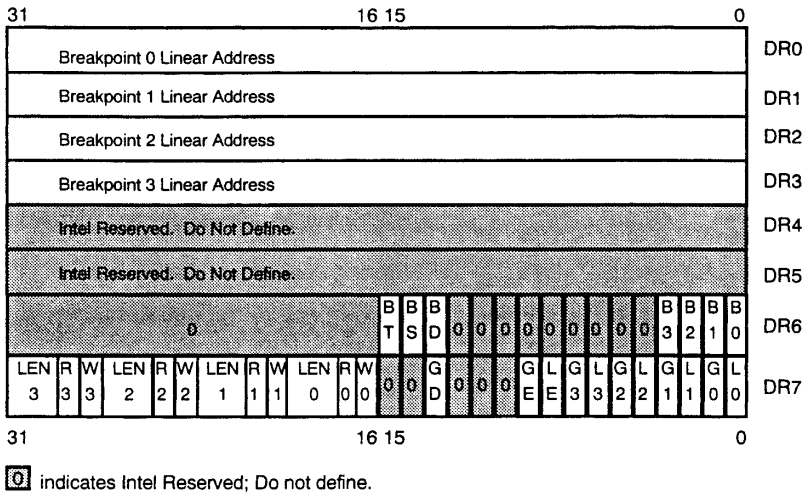
The Military Intel486 processor contains six Debug Registers, providing the ability to specify up to four distinct breakpoints addresses, breakpoint control options, and read breakpoint status. Initially after reset, breakpoints are in the disabled state. Therefore, no breakpoints will occur unless the debug registers are programmed. Breakpoints set up in the Debug Registers are auto vectored to exception number 1.

12.3.1 LINEAR ADDRESS BREAKPOINT REGISTERS (DR0–DR3)

Up to four breakpoint addresses can be specified by writing into Debug Registers DR0–DR3, shown in Figure 12-1. The breakpoint addresses specified are 32-bit linear addresses. Military Intel486 processor hardware continuously compares the linear breakpoint addresses in DR0–DR3 with the linear addresses generated by executing software (a linear address is the result of computing the effective address and adding the 32-bit segment base address). Note that if paging is not enabled the linear address equals the physical address. If paging is enabled, the linear address is translated to a physical 32-bit address by the on-chip paging unit. Regardless of whether paging is enabled or not, however, the breakpoint registers hold linear addresses.

12.3.2 DEBUG CONTROL REGISTER (DR7)

A Debug Control Register, DR7 shown in Figure 12-1, allows several debug control functions such as enabling the breakpoints and setting up other control options for the breakpoints. The fields within the Debug Control Register, DR7, are as follows:



NOTE:
See section 4.2.7

Figure 12-1. Debug Registers

LENi (breakpoint length specification bits)

A 2-bit LEN field exists for each of the four breakpoints. LEN specifies the length of the associated breakpoint field. The choices for data breakpoints are: 1 byte, 2 bytes, and 4 bytes. Instruction execution breakpoints must have a length of 1 (LENi = 00). Encoding of the LENi field is as described in Table 12-1.

The LENi field controls the size of breakpoint field i by controlling whether all low-order linear address bits in the breakpoint address register are used to detect the breakpoint event. Therefore, all breakpoint fields are aligned; 2-byte breakpoint fields begin on Word boundaries, and 4-byte breakpoint fields begin on Dword boundaries.

Figure 12-2 is an example of various size breakpoint fields. Assume the breakpoint linear address in DR2 is 00000005H. In that situation, the Figure 12-2 indicates the region of the breakpoint field for lengths of 1, 2, or 4 bytes.

RWi (memory access qualifier bits)

A 2-bit RW field exists for each of the four breakpoints. The 2-bit RW field specifies the type of usage which must occur in order to activate the associated breakpoint.

Table 12-1. LENi Encoding

LENi Encoding	Breakpoint Field Width	Usage of Least Significant Bits in Breakpoint Address Register i, (i = 0-3)
00	1 byte	All 32-bits used to specify a single-byte breakpoint field.
01	2 bytes	A1–A31 used to specify a two-byte, word-aligned breakpoint field. A0 in Breakpoint Address Register is not used.
10	Undefined—do not use this encoding	
11	4 bytes	A2–A31 used to specify a four-byte, dword-aligned breakpoint field. A0 and A1 in Breakpoint Address Register are not used.

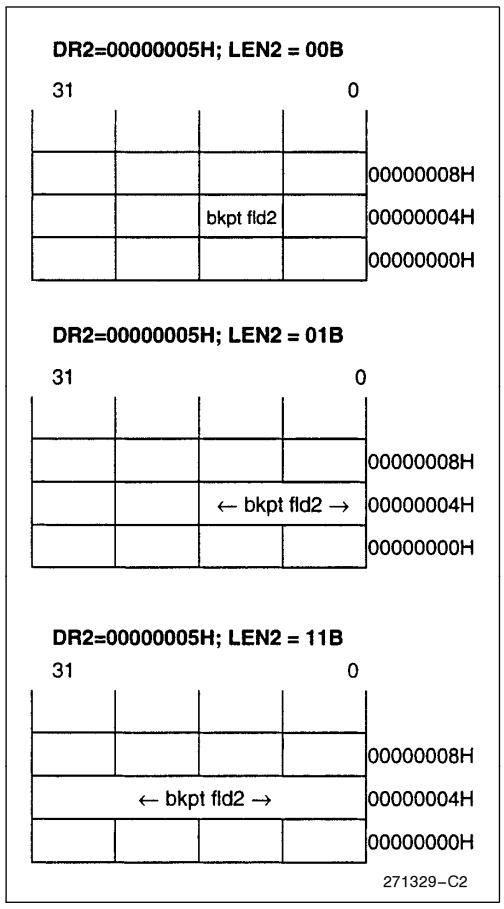


Figure 12-2. Size Breakpoint Fields

Table 12-2. RW Encoding

RW Encoding	Usage Causing Breakpoint
00	Instruction execution only
01	Data writes only
10	Undefined-do not use this encoding
11	Data reads and writes only

RW encoding 00 is used to set up an instruction execution breakpoint. RW encodings 01 or 11 are used to set up write-only or read/write data breakpoints.

Note that **instruction execution breakpoints are taken as faults** (i.e., before the instruction executes), but **data breakpoints are taken as traps** (i.e., after the data transfer takes place).

Using LENi and RWi to Set Data Breakpoint i

A data breakpoint can be set up by writing the linear address into DRi (i = 0–3). For data breakpoints, RWi can = 01 (write-only) or 11 (write/read). LEN can = 00, 01, or 11.

If a data access entirely or partly falls within the data breakpoint field, the data breakpoint condition has occurred, and if the breakpoint is enabled, an exception 1 trap will occur.

Using LENi and RWi to Set Instruction Execution Breakpoint i

An instruction execution breakpoint can be set up by writing address of the beginning of the instruction (including prefixes if any) into DRi (i = 0–3). RWi must = 00 and LEN must = 00 for instruction execution breakpoints.

If the instruction beginning at the breakpoint address is about to be executed, the instruction execution breakpoint condition has occurred, and if the breakpoint is enabled, an exception 1 fault will occur before the instruction is executed.

Note that an instruction execution breakpoint address must be equal to the **beginning** byte address of an instruction (including prefixes) in order for the instruction execution breakpoint to occur.

GD (Global Debug Register access detect)

The Debug Registers can only be accessed in Real Mode or at privilege level 0 in Protected Mode. The GD bit, when set, provides extra protection against **any** Debug Register access even in Real Mode or at privilege level 0 in Protected Mode. This additional protection feature is provided to guarantee that a software debugger can have full control over the Debug Register resources when required. The GD bit, when set, causes an exception 1 fault if an instruction attempts to read or write any Debug Register. The GD bit is then automatically cleared when the exception 1 handler is invoked, allowing the exception 1 handler free access to the debug registers.

GE and LE (Exact data breakpoint match, global and local)

The breakpoint mechanism of the Military Intel486 processor differs from that of the Intel386 processor. The Military Intel486 processor always does exact data breakpoint matching, regardless of GE/LE bit settings. Any data breakpoint trap will be reported exactly after completion of the instruction that caused the operand transfer. Exact reporting is provided by forcing the Military Intel486 processor execution unit to wait for completion of data operand transfers before beginning execution of the next instruction.

When the Military Intel486 processor performs a task switch, the LE bit is cleared. Thus, the LE bit supports fast task switching out of tasks, that have enabled the exact data breakpoint match for their task-local breakpoints. The LE bit is cleared by the Military Intel486 processor during a task switch, to avoid having exact data breakpoint match enabled in the new task. Note that exact data breakpoint match must be re-enabled under software control.

The Military Intel486 processor GE bit is unaffected during a task switch. The GE bit supports exact data breakpoint match that is to remain enabled during all tasks executing in the system.

Note that **instruction execution** breakpoints are always reported exactly.

Gi and Li (breakpoint enable, global and local)

If either Gi or Li is set then the associated breakpoint (as defined by the linear address in DRi, the length in LENi and the usage criteria in RWi) is enabled. If either Gi or Li is set, and the Military Intel486 processor detects the ith breakpoint condition, then the exception 1 handler is invoked.

When the Military Intel486 processor performs a task switch to a new Task State Segment (TSS), all Li bits are cleared. Thus, the Li bits support fast task switching out of tasks that use some task-local breakpoint registers. The Li bits are cleared by the Military Intel486 processor during a task switch, to avoid spurious exceptions in the new task. Note that the breakpoints must be re-enabled under software control.

All Military Intel486 processor Gi bits are unaffected during a task switch. The Gi bits support breakpoints that are active in all tasks executing in the system.

12.3.3 DEBUG STATUS REGISTER (DR6)

A Debug Status Register, DR6 shown in Figure 12-1, allows the exception 1 handler to easily determine why it was invoked. Note the exception 1 handler can be invoked as a result of one of several events:

1. DR0 Breakpoint fault/trap.
2. DR1 Breakpoint fault/trap.
3. XDR2 Breakpoint fault/trap.
4. XDR3 Breakpoint fault/trap.
5. XSingle-step (TF) trap.
6. XTask switch trap.
7. XFault due to attempted debug register access when GD = 1.

The Debug Status Register contains single-bit flags for each of the possible events invoking exception 1. Note below that some of these events are faults (exception taken before the instruction is executed), while other events are traps (exception taken after the debug events occurred).

The flags in DR6 are set by the hardware but never cleared by hardware. Exception 1 handler software should clear DR6 before returning to the user program to avoid future confusion in identifying the source of exception 1.

The fields within the Debug Status Register, DR6, are as follows:

Bi (debug fault/trap due to breakpoint 0–3)

Four breakpoint indicator flags, B0–B3, correspond one-to-one with the breakpoint registers in DR0–DR3. A flag Bi is set when the condition described by DRi, LENi, and RWi occurs.

If Gi or Li is set, and if the ith breakpoint is detected, the Military Intel486 processor will invoke the exception 1 handler. The exception is handled as a fault if an instruction execution breakpoint occurred, or as a trap if a data breakpoint occurred.

IMPORTANT NOTE:

A flag Bi is set whenever the hardware detects a match condition on **enabled** breakpoint i. Whenever a match is detected on at least one **enabled** breakpoint i, the hardware immediately sets all Bi bits corresponding to breakpoint conditions matching at that instant, whether enabled **or not.** Therefore, the exception 1 handler may see that multiple Bi bits are set, but only set Bi bits corresponding to **enabled** breakpoints (Li or Gi set) are **true** indications of why the exception 1 handler was invoked.

BD (debug fault due to attempted register access when GD bit set)

This bit is set if the exception 1 handler was invoked due to an instruction attempting to read or write to the debug registers when GD bit was set. If such an event occurs, then the GD bit is automatically cleared when the exception 1 handler is invoked, allowing handler access to the debug registers.

BS (debug trap due to single-step)

This bit is set if the exception 1 handler was invoked due to the TF bit in the flag register being set (for single-stepping).

BT (debug trap due to task switch)

This bit is set if the exception 1 handler was invoked due to a task switch occurring to a task having a Military Intel486 processor TSS with the T bit set. Note the task switch into the new task occurs normally, but before the first instruction of the task is executed, the exception 1 handler is invoked. With respect to the task switch operation, the operation is considered to be a trap.

12.3.4 USE OF RESUME FLAG (RF) IN FLAG REGISTER

The Resume Flag (RF) in the flag word can suppress an instruction execution breakpoint when the exception 1 handler returns to a user program at a user address which is also an instruction execution breakpoint.

13.0 INSTRUCTION SET SUMMARY

This section describes the Military Intel486 processor instruction set. Detailed information on the CPUID instruction can be found in Appendix A: Feature Determination. Further details of the instruction encoding are then provided in section 13.1, which describes the entire encoding structure and the definition of all fields occurring within the Military Intel486 processor instructions.

13.1 Instruction Encoding

13.1.1 OVERVIEW

All instruction encodings are subsets of the general instruction format shown in Figure 13-1. Instructions consist of one or two primary opcode bytes, possibly an address specifier consisting of the "mod r/m" byte and "scaled index" byte, a displacement if required, and an immediate data field if required.

Within the primary opcode or opcodes, smaller encoding fields may be defined. These fields vary according to the class of operation. The fields define such information as direction of the operation, size of the displacements, register encoding, or sign extension.

Almost all instructions referring to an operand in memory have an addressing mode byte following the primary opcode byte(s). This byte, the mod r/m byte, specifies the address mode to be used. Certain encodings of the mod r/m byte indicate a second addressing byte, the scale-index-base byte, follows the mod r/m byte to fully specify the addressing mode.

Addressing modes can include a displacement immediately following the mod r/m byte, or scaled index byte. If a displacement is present, the possible sizes are 8, 16 or 32 bits.

If the instruction specifies an immediate operand, the immediate operand follows any displacement bytes. The immediate operand, if specified, is always the last field of the instruction.

Figure 13-1 illustrates several of the fields that can appear in an instruction, such as the mod field and the r/m field, but the figure does not show all fields. Several smaller fields also appear in certain instructions, sometimes within the opcode bytes themselves. Table 13-1 is a complete list of all fields appearing in the Military Intel486 processor instruction set. Following Table 13-1 are detailed tables for each field.

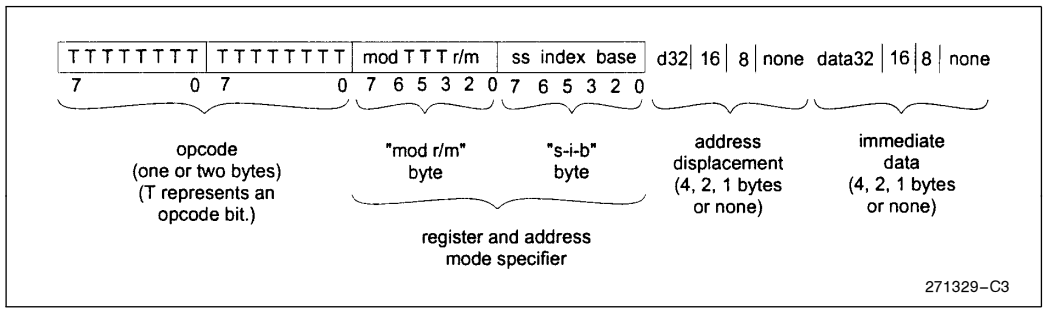


Figure 13-1. General Instruction Format

Table 13-1. Fields within Military Intel486™ Processor Instructions

Field Name	Description	Number of Bits
w	Specifies if Data is Byte or Full Size (Full Size is either 16 or 32 Bits)	1
d	Specifies Direction of Data Operation	1
s	Specifies if an Immediate Data Field Must be Sign-Extended	1
reg	General Register Specifier	3
mod r/m	Address Mode Specifier (Effective Address can be a General Register)	2 for mod; 3 for r/m
ss	Scale Factor for Scaled Index Address Mode	2
index	General Register to be used as Index Register	3
base	General Register to be used as Base Register	3
sreg2	Segment Register Specifier for CS, SS, DS, ES	2
sreg3	Segment Register Specifier for CS, SS, DS, ES, FS, GS	3
tttn	For Conditional Instructions, Specifies a Condition Asserted or a Condition Negated	4

NOTE:
Table 13-15 through Table 13-19 show encoding of individual instructions.

13.1.2 32-BIT EXTENSIONS OF THE INSTRUCTION SET

With the Military Intel486 processor, the 8086/80186/80286 instruction set is extended in two orthogonal directions: 32-bit forms of all 16-bit instructions are added to support the 32-bit data types, and 32-bit addressing modes are made available for all instructions referencing memory. This orthogonal instruction set extension is accomplished having a Default (D) bit in the code segment descriptor, and by having 2 prefixes to the instruction set.

Whether the instruction defaults to operations of 16 bits or 32 bits depends on the setting of the D bit in the code segment descriptor, which gives the default length (either 32 bits or 16 bits) for both operands and effective addresses when executing that code segment. In the Real Address Mode or Virtual 8086 Mode, no code segment descriptors are used, but a D value of 0 is assumed internally by the Military Intel486 processor when operating in those modes (for 16-bit default sizes compatible with the 8086/80186/80286).

Two prefixes, the Operand Size Prefix and the Effective Address Size Prefix, allow overriding individually the Default selection of operand size and effective address size. These prefixes may precede any opcode bytes and affect only the instruction they precede. If necessary, one or both of the prefixes may be placed before the opcode bytes. The presence of the Operand Size Prefix and the Effective Address Prefix will toggle the operand size or the effective address size, respectively, to the value ''opposite'' from the Default setting. For example, if the default operand size is for 32-bit data operations, then presence of the Operand Size Prefix toggles the instruction to 16-bit data operation. As another example, if the default effective address size is 16 bits, presence of the Effective Address Size prefix toggles the instruction to use 32-bit effective address computations.

These 32-bit extensions are available in all Military Intel486 processor modes, including the Real Address Mode or the Virtual 8086 Mode. In these modes the default is always 16 bits, so prefixes are needed to specify 32-bit operands or addresses. For instructions with more than one prefix, the order of prefixes is unimportant.

Unless specified otherwise, instructions with 8-bit and 16-bit operands do not affect the contents of the high-order bits of the extended registers.

13.1.3 ENCODING OF INTEGER INSTRUCTION FIELDS

Within the instruction are several fields indicating register selection, addressing mode and so on. The exact encodings of these fields are defined immediately ahead.

13.1.3.1 Encoding of Operand Length (w) Field

For any given instruction performing a data operation, the instruction is executing as a 32-bit operation or a 16-bit operation. Within the constraints of the operation size, the w field encodes the operand size as either one byte or the full operation size, as shown in the table below.

Table 13-2. Encoding of Operand Length (w) Field

w Field	Operand Size during 16-Bit Data Operations	Operand Size during 32-Bit Data Operations
0	8 Bits	8 Bits
1	16 Bits	32 Bits

13.1.3.2 Encoding of the General Register (reg) Field

The general register is specified by the reg field, which may appear in the primary opcode bytes, or as the reg field of the ''mod r/m'' byte, or as the r/m field of the ''mod r/m'' byte.

Table 13-3. Encoding of reg Field when the w Field Is Not Present in Instruction

reg Field	Register Selected during 16-Bit Data Operations	Register Selected during 32-Bit Data Operations
000	AX	EAX
001	CX	ECX
010	DX	EDX
011	BX	EBX
100	SP	ESP
101	BP	EBP
110	SI	ESI
111	DI	EDI

Table 13-4. Encoding of reg Field when the w Field Is Present in Instruction

Register Specified by reg Field during 16-Bit Data Operations:		
reg	Function of w Field	
	(when w = 0)	(when w = 1)
000	AL	AX
001	CL	CX
010	DL	DX
011	BL	BX
100	AH	SP
101	CH	BP
110	DH	SI
111	BH	DI
Register Specified by reg Field during 32-Bit Data Operations		
reg	Function of w Field	
	(when w = 0)	(when w = 1)
000	AL	EAX
001	CL	ECX
010	DL	EDX
011	BL	EBX
100	AH	ESP
101	CH	EBP
110	DH	ESI
111	BH	EDI

13.1.3.3 Encoding of the Segment Register (sreg) Field

The sreg field in certain instructions is a 2-bit field allowing one of the four 80286 segment registers to be specified. The sreg field in other instructions is a 3-bit field, allowing the Military Intel486 processor FS and GS segment registers to be specified.

Table 13-5. 2-Bit sreg2 Field

2-bit sreg2 Field	Segment Register Selected
00	ES
01	CS
10	SS
11	DS

Table 13-6. 3-Bit sreg3 Field

3-bit sreg3 Field	Segment Register Selected
000	ES
001	CS
010	SS
011	DS
100	FS
101	GS
110	do not use
111	do not use

13.1.3.4 Encoding of Address Mode

Except for special instructions, such as PUSH or POP, where the addressing mode is pre-determined, the addressing mode for the current instruction is specified by addressing bytes following the primary opcode. The primary addressing byte is the ''mod r/m'' byte, and a second byte of addressing information, the ''s-i-b'' (scale-index-base) byte, can be specified.

The s-i-b byte (scale-index-base byte) is specified when using 32-bit addressing mode and the ''mod r/m'' byte has r/m = 100 and mod = 00, 01 or 10. When the sib byte is present, the 32-bit addressing mode is a function of the mod, ss, index, and base fields.

The primary addressing byte, the ''mod r/m'' byte, also contains three bits (shown as TTT in Figure 13-1) sometimes used as an extension of the primary opcode. The three bits, however, may also be used as a register field (reg).

When calculating an effective address, either 16-bit addressing or 32-bit addressing is used. 16-bit addressing uses 16-bit address components to calculate the effective address while 32-bit addressing uses 32-bit address components to calculate the effective address. When 16-bit addressing is used, the ''mod r/m'' byte is interpreted as a 16-bit addressing mode specifier. When 32-bit addressing is used, the ''mod r/m'' byte is interpreted as a 32-bit addressing mode specifier.

Tables 13-7, 13-8, and 13-9 define all encodings of all 16-bit addressing modes and 32-bit addressing modes.

Table 13-7. Encoding of 16-Bit Address Mode with "mod r/m" Byte

mod r/m	Effective Address
00 000	DS:[BX + SI]
00 001	DS:[BX + DI]
00 010	SS:[BP + SI]
00 011	SS:[BP + DI]
00 100	DS:[SI]
00 101	DS:[DI]
00 110	DS:d16
00 111	DS:[BX]
01 000	DS:[BX + SI + d8]
01 001	DS:[BX + DI + d8]
01 010	SS:[BP + SI + d8]
01 011	SS:[BP + DI + d8]
01 100	DS:[SI + d8]
01 101	DS:[DI + d8]
01 110	SS:[BP + d8]
01 111	DS:[BX + d8]

mod r/m	Effective Address
10 000	DS:[BX + SI + d16]
10 001	DS:[BX + DI + d16]
10 010	SS:[BP + SI + d16]
10 011	SS:[BP + DI + d16]
10 100	DS:[SI + d16]
10 101	DS:[DI + d16]
10 110	SS:[BP + d16]
10 111	DS:[BX + d16]
11 000	register—see below
11 001	register—see below
11 010	register—see below
11 011	register—see below
11 100	register—see below
11 101	register—see below
11 110	register—see below
11 111	register—see below

Register Specified by r/m during 16-Bit Data Operations

mod r/m	Function of w Field	
	(when w = 0)	(when w = 1)
11 000	AL	AX
11 001	CL	CX
11 010	DL	DX
11 011	BL	BX
11 100	AH	SP
11 101	CH	BP
11 110	DH	SI
11 111	BH	DI

Register Specified by r/m during 32-Bit Data Operations

mod r/m	Function of w Field	
	(when w = 0)	(when w = 1)
11 000	AL	EAX
11 001	CL	ECX
11 010	DL	EDX
11 011	BL	EBX
11 100	AH	ESP
11 101	CH	EBP
11 110	DH	ESI
11 111	BH	EDI

Table 13-8. Encoding of 32-Bit Address Mode with "mod r/m" Byte (No "s-i-b" Byte Present)

mod r/m	Effective Address
00 000	DS:[EAX]
00 001	DS:[ECX]
00 010	DS:[EDX]
00 011	DS:[EBX]
00 100	s-i-b is present
00 101	DS:d32
00 110	DS:[ESI]
00 111	DS:[EDI]
01 000	DS:[EAX + d8]
01 001	DS:[ECX + d8]
01 010	DS:[EDX + d8]
01 011	DS:[EBX + d8]
01 100	s-i-b is present
01 101	SS:[EBP + d8]
01 110	DS:[ESI + d8]
01 111	DS:[EDI + d8]

mod r/m	Effective Address
10 000	DS:[EAX + d32]
10 001	DS:[ECX + d32]
10 010	DS:[EDX + d32]
10 011	DS:[EBX + d32]
10 100	s-i-b is present
10 101	SS:[EBP + d32]
10 110	DS:[ESI + d32]
10 111	DS:[EDI + d32]
11 000	register—see below
11 001	register—see below
11 010	register—see below
11 011	register—see below
11 100	register—see below
11 101	register—see below
11 110	register—see below
11 111	register—see below

Register Specified by reg or r/m during 16-Bit Data Operations:

mod r/m	Function of w Field	
	(when w = 0)	(when w = 1)
11 000	AL	AX
11 001	CL	CX
11 010	DL	DX
11 011	BL	BX
11 100	AH	SP
11 101	CH	BP
11 110	DH	SI
11 111	BH	DI

Register Specified by reg or r/m during 32-Bit Data Operations:

mod r/m	Function of w Field	
	(when w = 0)	(when w = 1)
11 000	AL	EAX
11 001	CL	ECX
11 010	DL	EDX
11 011	BL	EBX
11 100	AH	ESP
11 101	CH	EBP
11 110	DH	ESI
11 111	BH	EDI

Table 13-9. Encoding of 32-Bit Address Mode (“mod r/m” Byte and “s-i-b” Byte Present)

mod base	Effective Address
00 000	DS:[EAX + (scaled index)]
00 001	DS:[ECX + (scaled index)]
00 010	DS:[EDX + (scaled index)]
00 011	DS:[EBX + (scaled index)]
00 100	SS:[ESP + (scaled index)]
00 101	DS:[d32 + (scaled index)]
00 110	DS:[ESI + (scaled index)]
00 111	DS:[EDI + (scaled index)]
01 000	DS:[EAX + (scaled index) + d8]
01 001	DS:[ECX + (scaled index) + d8]
01 010	DS:[EDX + (scaled index) + d8]
01 011	DS:[EBX + (scaled index) + d8]
01 100	SS:[ESP + (scaled index) + d8]
01 101	SS:[EBP + (scaled index) + d8]
01 110	DS:[ESI + (scaled index) + d8]
01 111	DS:[EDI + (scaled index) + d8]
10 000	DS:[EAX + (scaled index) + d32]
10 001	DS:[ECX + (scaled index) + d32]
10 010	DS:[EDX + (scaled index) + d32]
10 011	DS:[EBX + (scaled index) + d32]
10 100	SS:[ESP + (scaled index) + d32]
10 101	SS:[EBP + (scaled index) + d32]
10 110	DS:[ESI + (scaled index) + d32]
10 111	DS:[EDI + (scaled index) + d32]

NOTE:
Mod field in “mod r/m” byte; ss, index, base fields in “s-i-b” byte.

ss	Scale Factor
00	x1
01	x2
10	x4
11	x8
Index	**Index Register**
000	EAX
001	ECX
010	EDX
011	EBX
100	no index reg**
101	EBP
110	ESI
111	EDI

****IMPORTANT NOTE:**
When index field is 100, indicating “no index register,” then ss field MUST equal 00. If index is 100 and ss does not equal 00, the effective address is undefined.

13.1.3.5 Encoding of Operation Direction (d) Field

In many two-operand instructions the d field is present to indicate which operand is considered the source and which is the destination.

Table 13-10. Encoding of Operation Direction (d) Field

d	Direction of Operation
0	Register/Memory ← Register ''reg'' Field Indicates Source Operand; ''mod r/m'' or ''mod ss index base'' Indicates Destination Operand
1	Register ← Register/Memory ''reg'' Field Indicates Destination Operand; ''mod r/m'' or ''mod ss index base'' Indicates Source Operand

13.1.3.6 Encoding of Sign-Extend (s) Field

The s field occurs primarily to instructions with immediate data fields. The s field has an effect only if the size of the immediate data is 8 bits and is being placed in a 16-bit or 32-bit destination.

Table 13-11. Encoding of Sign-Extend (s) Field

S	Effect on Immediate Data 8	Effect on Immediate Data 16|32
0	None	None
1	Sign-Extend Data 8 to Fill 16-bit or 32-bit Destination	None

13.1.3.7 Encoding of Conditional Test (tttn) Field

For the conditional instructions (conditional jumps and set on condition), tttn is encoded with n indicating to use the condition (n = 0) or its negation (n = 1), and ttt giving the condition to test.

Table 13-12. Encoding of Conditional Test (tttn) Field

Mnemonic	Condition	tttn
O	Overflow	0000
NO	No Overflow	0001
B/NAE	Below/Not Above or Equal	0010
NB/AE	Not Below/Above or Equal	0011
E/Z	Equal/Zero	0100
NE/NZ	Not Equal/Not Zero	0101
BE/NA	Below or Equal/Not Above	0110
NBE/A	Not Below or Equal/Above	0111
S	Sign	1000
NS	Not Sign	1001
P/PE	Parity/Parity Even	1010
NP/PO	Not Parity/Parity Odd	1011
L/NGE	Less Than/Not Greater or Equal	1100
NL/GE	Not Less Than/Greater or Equal	1101
LE/NG	Less Than or Equal/Greater Than	1110
NLE/G	Not Less or Equal/Greater Than	1111

13.1.3.8 Encoding of Control or Debug or Test Register (eee) Field

For the loading and storing of the Control, Debug and Test registers.

Table 13-13. Encoding of Control or Debug or Test Register (eee) Field

eee Code	Reg Name
When Interpreted as Control Register Field:	
000	CR0
010	CR2
011	CR3
When Interpreted as Debug Register Field:	
000	DR0
001	DR1
010	DR2
011	DR3
110	DR6
111	DR7
When Interpreted as Test Register Field:	
011	TR3
100	TR4
101	TR5
110	TR6
111	TR7

Do not use any other encoding

Table 13-14. Encoding of Floating-Point Instruction Fields

	Instruction								Optional	
	First Byte				Second Byte				Fields	
1	11011	OPA		1	mod		1 OPB	r/m	s-i-b	disp
2	11011	MF		OPA	mod		OPB	r/m	s-i-b	disp
3	11011	d	P	OPA	1	1	OPB	ST(i)		
4	11011	0	0	1	1	1	1	OP		
5	11011	0	1	1	1	1	1	OP		
	15–11	10	9	8	7	6	5	4 3 2 1 0		

13.1.4 ENCODING OF FLOATING POINT INSTRUCTION FIELDS

Instructions for the FPU assume one of the five forms shown in the following table. In all cases, instructions are at least two bytes long and begin with the bit pattern 11011B.

OP = Instruction opcode, possible split into two fields OPA and OPB

MF = Memory Format
00–32-bit real
01–32-bit integer
10–64-bit real
11–16-bit integer

P = Pop
0–Do not pop stack
1–Pop stack after operation

d = Destination
0–Destination is ST(0)
1–Destination is ST(i)

R XOR d = 0–Destination (op) Source

R XOR d = 1–Source (op) Destination

ST(i) = Register stack element *i*
000 = Stack top
001 = Second stack element
111 = Eighth stack element

mod (Mode field) and r/m (Register/Memory specifier) have the same interpretation as the corresponding fields of the integer instructions.

s-i-b (Scale Index Base) byte and disp (displacement) are optionally present in instructions that have mod and r/m fields. Their presence depends on the values of mod and r/m, as for integer instructions.

13.2 Clock Count Summary

To calculate elapsed time for an instruction, multiply the instruction clock count, as listed in Table 13-15 through Table 13-19 by the processor core clock period (e.g., 10 ns for a 100-MHz IntelDX4 processor).

13.2.1 INSTRUCTION CLOCK COUNT ASSUMPTIONS

The Military Intel486 processor instruction core clock count tables give clock counts assuming data and instruction accesses hit in the cache. The combined instruction and data cache hit rate is over 90%.

A cache miss will force the Military Intel486 processor to run an external bus cycle. The Military Intel486 processor 32-bit burst bus is defined as r-b-w.

Where:

r = The number of bus clocks in the first cycle of a burst read or the number of clocks per data cycle in a non-burst read.

b = The number of bus clocks for the second and subsequent cycles in a burst read.

w = The number of bus clocks for a write.

The clock counts in the cache miss penalty column assume a 2-1-2 bus. For slower buses add r-2 clocks to the cache miss penalty for the first dword accessed. Other factors also affect instruction clock counts.

Instruction Clock Count Assumptions

1. The external bus is available for reads or writes at all times. Else add bus clocks to reads until the bus is available.
2. Accesses are aligned. Add three core clocks to each misaligned access.
3. Cache fills complete before subsequent accesses to the same line. If a read misses the cache during a cache fill due to a previous read or prefetch, the read must wait for the cache fill to complete. If a read or write accesses a cache line still being filled, it must wait for the fill to complete.
4. If an effective address is calculated, the base register is not the destination register of the preceding instruction. If the base register is the destination register of the preceding instruction add 1 to the core clock counts shown. Back-to-back PUSH and POP instructions are not affected by this rule.
5. An effective address calculation uses one base register and does not use an index register. However, if the effective address calculation uses an index register, 1 core clock **may** be added to the clock count shown.
6. The target of a jump is in the cache. If not, add r clocks for accessing the destination instruction of a jump. If the destination instruction is not completely contained in the first dword read, add a maximum of 3b bus clocks. If the destination instruction is not completely contained in the first 16 byte burst, add a maximum of another r + 3b bus clocks.
7. If no write buffer delay, w bus clocks are added only in the case in which all write buffers are full.
8. Displacement and immediate not used together. If displacement and immediate used together, 1 core clock **may** be added to the core clock count shown.
9. No invalidate cycles. Add a delay of 1 bus clock for each invalidate cycle if the invalidate cycle contends for the internal cache/external bus when the Military Intel486 processor needs to use it.
10. Page translation hits in TLB. A TLB miss will add 13, 21 or 28 bus clocks + 1 possible core clock to the instruction depending on whether the Accessed and/or Dirty bit in neither, one or both of the page entries needs to be set in memory. This assumes that neither page entry is in the data cache and a page fault does not occur on the address translation.
11. No exceptions are detected during instruction execution. Refer to Interrupt core Clock Counts Table for extra clocks if an interrupt is detected.
12. Instructions that read multiple consecutive data items (i.e. task switch, POPA, etc.) and miss the cache are assumed to start the first access on a 16-byte boundary. If not, an extra cache line fill may be necessary which may add up to (r + 3b) bus clocks to the cache miss penalty.

Table 13-15. Clock Count Summary

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS				
MOV = Move:				
reg1 to reg2	1000 100w : 11 reg1 reg2	1		
reg2 to reg1	1000 101w : 11 reg1 reg2	1		
memory to reg	1000 100w : mod reg r/m	1	2	
Immediate to reg	1100 011w : 11000 reg : immediate data	1		
or	1011W reg : immediate data	1		
Immediate to Memory	1100 01w : mod 000 r/m : displacement immediate	1		
Memory to Accumulator	1010 000w : full displacement	1	2	
Accumulator to Memory	1010 001w : full displacement	1		
MOVSX/MOVZX = Move with Sign/Zero Extension				
reg2 to reg1	0000 1111 : 1011 z11w : 11 reg1 reg2	3		
memory to reg	0000 1111 : 1011 z11w : mod reg r/m	3	2	
z instruction 0 MOVZX 1 MOVSX				
PUSH = Push				
reg	1111 1111 : 11 110 reg	4		
or	01010 reg	1		
memory	1111 1111 : mod 110 r/m	4	1	1
immediate	0110 10s0 : immediate data	1		
PUSHA = Push All	0110 0000	11		
POP = Pop				
reg	1000 1111 : 11 000 reg	4	1	
or	01011 reg	1	2	
memory	1000 1111 : mod 000 r/m	5	2	1
POPA = Pop All	0110 0001	9	7/15	16/32
XCHG = Exchange				
reg1 with reg2	1000 011w : 11 reg1 reg2	3		2
Accumulator with reg	10010 reg	3		2
Memory with reg	1000 011w : mod reg r/m	5		2

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
NOP = No Operation	1001 0000	1		
LEA = Load EA to Register	1000 1101 : mod reg r/m			
no index register		1		
with index register		2		
Instruction	TTT			
ADD = Add	000			
ADC = Add with Carry	010			
AND = Logical AND	100			
OR = Logical OR	001			
SUB = Subtract	101			
SBB = Subtract with Borrow	011			
XOR = Logical Exclusive OR	110			
reg1 to reg2	00TT T00w : 11 reg1 reg2	1		
reg2 to reg1	00TT T01w : 11 reg1 reg2	1		
memory to register	00TT T01w : mod reg r/m	2	2	
register to memory	00TT T00w : mod reg r/m	3	6/2	U/L
immediate to register	1000 00sw : 11 TTT reg : immediate register	1		
immediate to Accumulator	00TT T10w : immediate data	1		
immediate to memory	1000 00sw : mod TTT r/m : immediate data	3	6/2	U/L
Instruction	TTT			
INC = Increment	000			
DEC = Decrement	001			
reg	1111 111w : 11 TTT reg	1		
or	01TTT reg	1		
memory	1111 111w : mod TTT r/m	3	6/2	U/L
Instruction	TTT			
NOT = Logical Complement	010			
NEG = Negate	011			
reg	1111 011w : 11 TTT reg	1		
memory	1111 011w : mod TTT r/m	3	6/2	U/L

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
CMP = Compare				
reg1 with reg2	0011 100w : 11 reg1 reg2	1		
reg2 with reg1	0011 101w : 11 reg1 reg2	1		
memory with register	0011 100w : mod reg r/m	2	2	
register with memory	0011 101w : mod reg r/m	2	2	
immediate with register	1000 00sw : 11 111 reg : immediate data	1		
immediate with acc.	0011 110w : immediate data	1		
immediate with memory	1000 00sw : mod 111 r/m : immediate data	2	2	
TEST = Logical Compare				
reg1 and reg2	1000 010w : 11 reg1 reg2	1		
memory and register	1000 010w : mod reg r/m	2	2	
immediate and register	1111 011w : 11 000 reg : immediate data	1		
immediate and acc.	1010100w : immediate data	1		
immediate and memory	1111 011w : mod 000 r/m : immediate data	2	2	
MUL = Multiply (unsigned)				
acc. with register	1111 011w : 11 100 reg			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3
acc. with memory	1111 011w : mod 100 r/m			
Multiplier-Byte		13/18	1	MN/MX,3
Word		13/26	1	MN/MX,3
Dword		13/42	1	MN/MX,3
IMUL = Integer Multiply (unsigned)				
acc. with register	1111 011w : 11 101 reg			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3
acc. with memory	1111 011w : mod 101 r/m			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3
reg1 with reg2	0000 1111 : 10101111 : 11 reg1 reg2			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
IMUL = Integer Multiply (unsigned), (Continued)				
register with memory	0000 1111 : 10101111 : mod reg r/m			
Multiplier-Byte		13/18	1	MN/MX,3
Word		13/26	1	MN/MX,3
Dword		13/42	1	MN/MX,3
reg1 with imm. to reg2	0110 10s1 : 11 reg1 reg2 : immediate data			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3
mem. with imm. to reg.	0110 10s1 : mod reg r/m : immediate data			
Multiplier-Byte		13/18		MN/MX,3
Word		13/26		MN/MX,3
Dword		13/42		MN/MX,3
For the IntelDX4™ Processor Only: **IMUL = Integer Multiply (signed)**				
acc. with register	1111 011w : 11101 reg			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,3
acc. with memory	1111 011w : mod 101 r/m			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,3
reg1 with reg2	0000 1111 : 1010 1111 : 11 reg1 reg2			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,
register with memory	0000 1111 : 1010 1111 : mod reg r/m			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,
reg1 with imm. to reg2	0110 10s1 : 11 reg1 reg2 : immediate data			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,
mem. with imm. to reg.	0110 10s1 : mod reg r/m : immediate data			
Multiplier-Byte		5/5		MN/MX,3
Word		5/6		MN/MX,3
Dword		6/12		MN/MX,3

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
DIV = Divide (unsigned)				
acc. by register	1111 011w : 11110 reg			
Divisor-Byte		16		
Word		24		
Dword		40		
acc. by memory	1111 011w : mod 110 r/m			
Divisor-Byte		16		
Word		24		
Dword		40		
IDIV = Integer Divide (signed)				
acc. by register	1111 011w : 11111 reg			
Divisor-Byte		19		
Word		27		
Dword		43		
acc. by memory	1111 011w : mod 111 r/m			
Divisor-Byte		20		
Word		28		
Dword		44		
CBW = Convert Byte to Word	1001 1000	3		
CWD = Convert Word to Dword	1001 1001	3		
Instruction	TTT			
ROL = Rotate Left	000			
ROR = Rotate Right	001			
RCL = Rotate Through Carry Left	010			
RDR = Rotate Through Carry Right	011			
SHL/SAL = Shift Logical/ Arithmetic Left	100			
SHR = Shift Logical Right	101			
SAR = Shift Arithmetic Right	111			
Not Through Carry (ROL, ROR, SAR, SHL, and SHR)				
reg by 1	1101 000w : 11 TTT reg	3		
memory by 1	1101 000w : mod TTT r/m	4	6	
reg by CL	1101 001w : 11 TTT reg	3		
memory by CL	1101 001w : mod TTT r/m	4	6	
reg by immediate count	1100 000w : 11 TTT reg : imm. 8-bit data	2		
mem by immediate count	1100 000w : mod TTT r/m : imm. 8-bit data	4	6	

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTEGER OPERATIONS (Continued)				
Through Carry (RCL and RCR)				
reg by 1	1101 000w : 11 TTT reg	3		
memory by 1	1101 000w : mod TTT r/m	4	6	
reg by CL	1101 001w : 11 TTT reg	8/30		MN/MX,4
memory by CL	1101 001w : mod TTT r/m	9/31		MN/MX,5
reg by immediate count	1100 000w : 11 TTT reg : imm. 8-bit data	8/30		MN/MX,4
mem by immediate count	1100 000w : mod TTT r/m : imm. 8-bit data	9/31		MN/MX,5
Instruction SHLD = Shift Left Double SHRD = Shift Right Double	TTT 100 101			
register with immediate	0000 1111 : 10TT T100 : 11 reg2 reg1 : imm. 8-bit data	2		
memory with immediate	0000 1111 : 10TT T100 : mod reg r/m : imm. 8-bit data	3	6	
register by CL	0000 1111 : 10TT T101 : 11 reg2 reg1	3		
memory by CL	0000 1111 : 10TT T101 : mod reg r/m	4	5	
BSWAP = Byte Swap	0000 1111 : 11001 reg	1		
XADD = Exchange and Add				
reg1, reg2	0000 1111 : 1100 000w : 11 reg2 reg1	3		
memory, reg	0000 1111 : 1100 000w : mod reg r/m	4	6/2	U/L
CMPXCHG = Compare and Exchange				
reg1, reg2	0000 1111 : 1011 000w : 11 reg2 reg1	6		
memory, reg	0000 1111 : 1011 000w : mod reg r/m	7/10	2	6
CONTROL TRANSFER (within segment)				
Note: Times are jump taken/not taken **J_{CCCC} = Jump on cccc**				
8-bit displacement	0111 tttn : 8-bit disp.	3/1		T/NT,23
full displacement	0000 1111 : 1000 tttn : full displacement	3/1		T/NT,23
Note: Times are jump taken/not taken **SET_{CCCC} = Set Byte on cccc (Times are cccc true/false)**				
reg	0000 1111 : 1001 tttn : 11 000 reg	4/3		
memory	0000 1111 : 1001 tttn : mod 0000 r/m	3/4		

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
CONTROL TRANSFER (within segment) (Continued)				
Mnemonic cccc / Condition / tttn				
O — Overflow — 0000				
NO — No Overflow — 0001				
B/NAE — Below/Not Above or Equal — 0010				
NB/AE — Not Below/Above or Equal — 0011				
E/Z — Equal Zero — 0100				
NE/NZ — Not Equal/Not Zero — 0101				
BE/NA — Below or Equal/Not Above — 0110				
NBE/A — Not Below or Equal/Above — 0111				
S — Sign — 1000				
NS — Not Sign — 1001				
P/PE — Parity/Parity Even — 1010				
NP/PO — Not Parity/Parity Odd — 1011				
L/NGE — Less Than/Not Greater or Equal — 1100				
NL/GE — Not Less Than/Greater or Equal — 1101				
LE/NG — Less Than or Equal/Greater Than — 1110				
NLE/G — Not Less Than or Equal/Greater Than — 1111				
LOOP = LOOP CX Times	1110 0010 : 8-bit disp.	7/6		L/NL,23
LOOPZ/LOOPE = Loop with Zero/Equal	1110 0001 : 8-bit disp.	9/6		L/NL,23
LOOPNZ/LOOPNE = Loop While Not Zero	1110 0000 : 8-bit disp.	9/6		L/NL,23
JCXZ = Jump on CX Zero	1110 0011 : 8-bit disp.	8/5		T/NT,23
JECXZ = Jump on ECX Zero (Address Size Prefix Differentiates JCXZ for JECXZ)	1110 0011 : 8-bit disp.	8/5		T/NT,23
JMP = Unconditional Jump (within segment)				
Short	1110 1011 : 8-bit disp.	3		7,23
Direct	1110 1001 : full displacement	3		7,23
Register Indirect	1111 1111 : 11 100 reg	5		7,23
Memory Indirect	1111 1111 : mod 100 r/m	5	5	7
CALL = Call (within segment)				
Direct	1110 1000 : full displacement	3		7,23
Register Indirect	1111 1111 : 11 010 reg	5		7,23
Memory Indirect	1111 1111 : mod 010 reg	5	5	7
RET = Return from CALL (within segment)	1100 0011	5	5	
Adding Immediate to SP	1100 0010 : 16-bit disp.	5	5	
ENTER = Enter Procedure	1100 1000 : 16-bit disp., 8-bit level			
Level = 0		14		
Level = 1		17		
Level (L) > 1		17+3L		8
LEAVE = Leave Procedure	1100 1001	5	1	

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
MULTIPLE-SEGMENT INSTRUCTIONS				
MOV = Move				
reg. to segment reg.	1000 1110 : 11 sreg3 reg	3/9	0/3	RV/P,9
memory to segment reg.	1000 1110 : mod sreg3 r/m	3/9	2/5	RV/P,9
segment reg. to reg.	1000 1100 : 11 sreg3 reg	3		
segment reg. to memory	1000 1100 : mod sreg3 r/m	3		
PUSH = Push				
segment reg. (ES, CS, SS, or DS)	000sreg 2110	3		
segment reg. (FS or GS)	0000 1111 : 10 sreg3001	3		
POP = Pop				
segment reg. (ES, CS, SS, or DS)	000sreg 2111	3/0	2/5	RV/P,9
segment reg. (FS or GS)	0000 1111 : 10 sreg3001	3/9	2/5	RV/P,9
LDS = Load Pointer to DS	1100 0101 : mod reg r/m	6/12	7/10	RV/P,9
LES = Load Pointer to ES	1100 0100 : mod reg r/m	6/12	7/10	RV/P,9
LFS = Load Pointer to FS	0000 1111 : 1011 0100 : mod reg r/m	6/12	7/10	RV/P,9
LGS = Load Pointer to GS	0000 1111 : 1011 0101 : mod reg r/m	6/12	7/10	RV/P,9
LSS = Load Pointer to SS	0000 1111 : 1011 0010 : mod reg r/m	6/12	7/10	RV/P,9
CALL = Call				
Direct intersegment	1001 1010 : unsigned full offset, selector	18	2	R,7,22
to same level		20	3	P,9
thru Gate to same level		35	6	P,9
to inner level, no parameters		69	17	P,9
to inner level, x parameters (d) words		77+4X	17+n	P,11,9
to TSS		37+TS	3	P,10,9
thru Task Gate		38+TS	3	P,10,9
Indirect intersegment	1111 1111 : mod 011 r/m	17	8	R,7
to same level		20	10	P,9
thru Gate to same level		35	13	P,9
to inner level, no parameters		69	24	P,9
to inner level, x parameters (d) words		77+4X	24+n	P,11,9
to TSS		37+TS	10	P,10,9
thru Task Gate		38+TS	10	P,10,9
RET = Return from CALL				
intersegment	1100 1010	13	8	R,7
to same level		17	9	P,9
to outet lever		35	12	P,9
intersegment adding imm. to SP	1100 1010 : 16-bit disp.	14	8	R,7
to same level		18	9	P,9
to outer level		36	12	P,9

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
MULTIPLE-SEGMENT INSTRUCTIONS (Continued)				
JMP = Unconditional Jump				
Direct intersegment	1110 1010 : unsigned full offset, selector	17	2	R,7,22
to same level		19	3	P,9
thru Call Gate to same level		32	6	P,9
thru TSS		42+TS	3	P,10,9
thru Task Gate		43+TS	3	P,10,9
Indirect intersegment	1111 1111 : mod 011 r/m	13	9	R,7,9
to same level		18	10	P,9
thru Call Gate to same level		31	13	P,9
thru TSS		41+TS	10	P,10,9
thru Task Gate		42+TS	10	P,10,9
BIT MANIPULATION				
BT = Test Bit				
register, immediate	0000 1111 : 1011 1010 : 11 100 reg : imm. 8-bit data	3		
memory, immediate	0000 1111 : 1011 1010 : mod 100 r/m : imm. 8-bit data	3	1	
reg1, reg2	0000 1111 : 1010 0011 : 11 reg2 reg1	3		
memory, reg	0000 1111 : 1010 0011 : mod reg r/m	8	2	
Instruction	TTT			
BTS = Test Bit and Set	101			
BTR = Test Bit and Reset	110			
BTC = Test Bit and Compliment	111			
register, immediate	0000 1111 : 1011 1010 : 11 TTT reg imm. 8-bit data	6		
memory, immediate	0000 1111 : 1011 1010 : mod TTT r/m imm. 8-bit data	8		U/L
reg1, reg2	0000 1111 : 10TT T011 : 1 1 reg2 reg1	6		
memory, reg	0000 1111 : 10TT T011 : mod reg r/m	13		U/L
BSF = Scan Bit Forward				
reg1, reg2	0000 1111 : 1011 1100 : 11 reg2 reg1	6/42		MN/MX, 12
memory, reg	0000 1111 : 1011 1100 : mod reg r/m	7/43	2	MN/MX, 15
BSR = Scan Bit Reverse				
reg1, reg2	0000 1111 : 1011 1101 : 11 reg2 reg1	6/103		MN/MX, 14
memory, reg	0000 1111 : 1011 1101 : mod reg r/m	7/104	1	MN/MX, 15

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
STRING INSTRUCTIONS				
CMPS = **Compare Byte Word**	1010 011w	8	6	16
LODS = **Load Byte/Word** to AL/AX/EAX	1010 111w	5	2	
MOVS = **Move Byte/Word**	1010 010w	7	2	16
SCAS = **Scan Byte/Word**	1010 111w	6	2	
STOS = **Store Byte/Word** from AL/AX/EX	1010 101w	5		
XLAT = **Translate String**	1101 0111	4	2	
REPEATED STRING INSTRUCTIONS Repeated by Count in CX or ECX (C = Count in CX or ECX)				
REPE CMPS = **Compare String** (Find Non-match)	1111 0011 : 1010 011w			
C = 0		5		16, 17
C > 0		7+7c		
REPNE CMPS = **Compare String** (Find Match)	1111 0010 : 1010 011w			
C = 0		5		16, 17
C > 0		7+7c		
REP LODS = **Load String**	1111 0010 : 1010 110w			
C = 0		5		16, 18
C > 0		7+4c		
REP MOVS = **Move String**	1111 0010 : 1010 010w			
C = 0		5	1	16
C = 1		13		16, 19
C > 1		12+3c		
REPE SCAS = **Scan String** (Find Non-AL/AX/EAX)	1111 0011 : 1010 111w			
C = 0		5		
C > 0		7+5c		20
REPNE SCAS = **Scan String** (Find AL/AX/EAX)	1111 0010 : 1010 111w			
C = 0		5		
C > 0		7+5c		20
REP STOS = **Store String**	1111 0010 : 1010 101w			
C = 0		5		
C > 0		7+4c		

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
FLAG CONTROL				
CLC = Clear Carry Flag	1111 1000	2		
STC = Set Carry Flag	1111 1001	2		
CMC = Complement Carry Flag	1111 0101	2		
CLD = Clear Direction Flag	1111 1100	2		
STD = Set Direction Flag	1111 1101	2		
CLI = Clear Interrupt Enable Flag	1111 1010	5		
STI = Set Interrupt Enable Flag	1111 1011	5		
LAHF = Load AH into Flag	1001 1111	3		
SAHF = Store AH into Flag	1001 1110	2		
PUSHF = Push Flags	1001 1100	4/3		RV/P
POFF = Pop Flags	1001 1101	9/6		RV/P
DECIMAL ARITHMETIC				
AAA = ASCII Adjust to Add	0011 0111	3		
AAS = ASCII Adjust for Subtract	0011 1111	3		
AAM = ASCII Adjust for Multiply	1101 0100 : 0000 1010	15		
AAD = ASCII Adjust for Divide	1101 0101 : 0000 1010	14		
DAA = Decimal Adjust for Add	0010 0111	2		
DAS = Decimal Adjust for Subtract	0010 1111	2		
PROCESSOR CONTROL INSTRUCTIONS				
HLT = Halt	1111 0100	4		
MOV = Move To and From Control/Debug/Test Registers				
CR0 from register	0000 1111 : 0010 0010 : 11 000 reg	17	2	
CR2/CR3 from register	0000 1111 : 0010 0010 : 11 eee reg	4		
Reg from CR0-3	0000 1111 : 0010 0000 : 11 eee reg	4		
DR0-3 from register	0000 1111 : 0010 0011 : 11 eee reg	10		
DR6-7 from register	0000 1111 : 0010 0011 : 11 eee reg	10		
Register from DR6-7	0000 1111 : 0010 0001 : 11 eee reg	9		
Register from DR0-3	0000 1111 : 0010 0001 : 11 eee reg	9		
TR3 from register	0000 1111 : 0010 0110 : 11 011 reg	4		
TR4-7 from register	0000 1111 : 0010 0110 : 11 eee reg	4		
Register from TR3	0000 1111 : 0010 0100 : 11 011 reg	3		
Register from TR4-7	0000 1111 : 0010 0100 : 11 eee reg	4		

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
PROCESSOR CONTROL INSTRUCTIONS (Continued)				
CPUID = CPU Identification	0000 1111 : 1010 0010			
EAX = 1		14		
EAX = 0, >1		9		
CLTS = Clear Task Switched Flag	0000 1111 : 0000 0110	7	2	
INVD = Invalidate Data Cache	0000 1111 : 0000 1000	4		
WBINVD = Write-Back and Invalidate Data Cache	0000 1111 : 0000 1001	5		
INVLPG = Invalidate TLB Entry				
INVLPG memory	0000 1111 : 0000 0001 : mod 111 r/m	12/11		H/NH
PREFIX BYTES				
Address Size Prefix	0110 0111	1		
LOCK = Bus Lock Prefix	1111 0000	1		
Operand Size Prefix	0110 0110	1		
Segment Override Prefix				
CS:	0010 1110	1		
DS:	0011 1110	1		
ES:	0010 0110	1		
FS:	0110 0100	1		
GS:	0110 0101	1		
SS:	0011 0110	1		
PROTECTION CONTROL				
ARPL = Adjust Requested Privilege Level				
From register	0110 0011 : 11 reg1 reg2	9		
From memory	0110 0011 : mod reg r/m	9		
LAR = Load Access Rights				
From register	0000 1111 : 0000 0010 : 11 reg1 reg2	11	3	
From memory	0000 1111 : 0000 0010 : mod reg r/m	11	5	
LGDT = Load Global Descriptor				
Table register	0000 1111 : 0000 0001 : mod 010 r/m	12	5	
LIDT = Load Interrupt Descriptor				
Table register	0000 1111 : 0000 0001 : mod 011 r/m	12	5	
LLDT = Load Local Descriptor				
Table register from reg.	0000 1111 : 0000 0000 : 11 010 reg	11	3	
Table register from mem.	0000 1111 : 0000 0000 : mod 010 r/m	11	6	

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
PROTECTION CONTROL (Continued)				
LMSW = Load Machine Status Word				
From register	0000 1111 : 0000 0001 : 11 110 reg	13		
From memory	0000 1111 : 0000 0001 : mod 110 r/m	13	1	
LSL = Load Segment Limit				
From register	0000 1111 : 0000 0011 : 11 reg1 reg2	10	3	
From memory	0000 1111 : 0000 0011 : mod reg r/m	10	6	
LTR = Load Task Register				
From register	0000 1111 : 0000 0000 : 11 011 reg	20		
From memory	0000 1111 : 0000 0000 : mod 011 r/m	20		
SGDT = Store Global Descriptor Table	0000 1111 : 0000 0001 : mod 000 r/m	10		
SIDT = Store Interrupt Descriptor Table	0000 1111 : 0000 0001 : mod 001 r/m	2		
SLDT = Store Local Descriptor Table				
To register	0000 1111 : 0000 0000 : 11 000 reg	2		
To memory	0000 1111 : 0000 0001 : mod 000 r/m	3		
SMSW = Store Machine Status Word				
To register	0000 1111 : 0000 0001 : 11 000 reg	2		
To memory	0000 1111 : 0000 0001 : mod 100 r/m	3		
STR = Store Task Register				
To register	0000 1111 : 0000 0000 : 11 001 r/m	2		
To memory	0000 1111 : 0000 0000 : mod 001 r/m	3		
VERR = Verify Read Access				
Register	0000 1111 : 0000 0000 : 11 100 r/m	11	3	
Memory	0000 1111 : 0000 0000 : mod 100 r/m	11	7	
VERW = Verify Write Access				
To register	0000 1111 : 0000 0000 : 11 101 r/m	11	3	
To memory	0000 1111 : 0000 0000 : mod 101 r/m	11	7	
INTERRUPT INSTRUCTIONS				
INTn = Interrupt Type n	1100 1101 : type	INT + 4/0		RV/P, 21
INT3 = Interrupt Type 3	1100 1100	INT + 0		21

Table 13-15. Clock Count Summary (Continued)

Instruction	Format	Cache Hit	Penalty if Cache Miss	Notes
INTERRUPT INSTRUCTIONS (Continued)				
INTO = Interrupt 4 if Overflow Flag Set	1100 1110			
Taken		INT+2		21
Not Taken		3		21
BOUND = Interrupt 5 if Detect Value Out Range	0110 0010 : mod reg r/m			
If in range		7	7	21
If out of range		INT+ 24	7	21
IRET = Interrupt Return	1100 1111			
Real Mode/Virtual Mode		15		
Protected Mode				
To same level		20	11	9
To outer level		36	19	9
To nested task		TS+32	4	9,10
(EFLAGS.NT=1)				
RSM = Exit System Management Mode	0000 1111 : 1010 1010			
SMBASE Relocation		452		
Auto HALT Restart		456		
I/O Trap Restart		465		
External Interrupt		INT+ 11		21
NMI = Non-Maskable Interrupt		INT+3		21
Page Fault		INT+ 24		21
VM86 Exceptions				
CLI		INT+8		21
STI		INT+8		21
INTn		INT+9		
PUSHF		INT+9		21
POPF		INT+8		21
IRET		INT+9		
IN				
Fixed Port		INT+50		21
Variable Port		INT+51		21
OUT				
Fixed Port		INT+50		21
Variable Port		INT+51		21
INS		INT+50		21
OUTS		INT+50		21
REP INS		INT+51		21
REP OUTS		INT+51		21

Table 13-16. Task Switch Clock Counts

Method	Value for TS	
	Cache Hit	Miss Penalty
VM/Military Intel486 Processor/286 TSS to Military Intel486 Processor TSS	162	55
VM/Military Intel486 Processor/286 TSS to 286 TSS	144	31
VM/Military Intel486 Processor/286 TSS to VM TSS	140	37

Table 13-17. Interrupt Clock Counts

Method	Value for INT		
	Cache Hit	Miss Penalty	Notes
Real Mode	26	2	
Protected Mode			
Interrupt/Trap gate, same level	44	6	9
Interrupt/Trap gate, different level	71	17	9
Task Gate	37 + TS	3	9, 10
Virtual Mode			
Interrupt/Trap gate, different level	82	17	
Task Gate	37 + TS	3	10

Abbreviations	Definition
16/32	16/32 bit modes
U/L	unlocked/locked
MN/MX	minimum/maximum
L/NL	loop/no loop
RV/P	real and virtual mode/protected mode
R	real mode
P	protected mode
T/NT	taken/not taken
H/NH	hit/no hit

NOTES (for Tables 13-17 through 13-19):

1. Assuming that the operand address and stack address fall in different cache sets.
2. Always locked, no cache hit case.
3. Clocks = 10 + max($\log_2$(|m|),n)
4. Clocks = {qoutient(couint/operand length)}*7+9
   = 8 if count ≤ operand length (8/16/32)
5. Clocks = {qoutient(couint/operand length)}*7+9
   = 9 if count ≤ operand length (8/16/32)
6. Equal/not equal cases (penalty is the same regardless of lock)
7. Assuming that addresses for memory read (for indirection), stack puch/pop and branch fall in different cache sets.
8. Penalty for cache miss: add 6 clocks for every 16 bytes copied to new stack frame.
9. Add 11 clocks for each unaccessed descriptor load.
10. Refer to task switch clock counts table for value of TS.
11. Add 4 extra clocks to the cache miss penalty for each 16 bytes.

For notes 12-13: (b = 0-3, non-zero byte number);
(i = 0-1, non-zero nibble number);
(n = 0-3, non-bit number in nibble);
12. Clocks = 8 + 4 (b + 1) + 3(i + 1) + 3(n + 1)
= 6 if second operand = 0
13. Clocks = 9 + 4 (b + 1) + 3(i + 1) + 3(n + 1)
= 7 if second operand = 0
For notes 14-15: (n = bit position 0-31)
14. Clocks = 7 + 3(32-n)
= 6 if second operand = 0
15. Clocks = 8 + 3(32-n)
= 7 if second operand = 0
16. Assuming that the two string addresses fall in different cache sets.
17. Cache miss penalty: add 6 clocks for every 16 bytes compared. Entire penalty on first compare.
18. Cache miss penalty: add 2 clocks for every 16 bytes of data. Entire penalty on first load.
19. Cache miss penalty: add 4 clocks for every 16 bytes moved. (1 clock for the first operation and 3 for the second)
20. Cache miss penalty: add 4 clocks for every 16 bytes scanned. (2 clocks each for first and second operations)
21. Refer to interrupt clock counts table for value of INT.
22. Clock count includes one clock for using both displacement and immediate.
23. Refer to assumption 6 in the case of a cache miss.
24. Virtual Mode Extensions are disabled.
25. Protected Virtual Interrupts are disabled.

Table 13-18. I/O Instructions Clock Count Summary

Instruction	Format	Real Mode	Protected Mode (CPL ≤ IOPL)	Protected Mode (CPL > IOPL)	Virtual 86 Mode	Notes
IN = Input from:						
Fixed Port	1110 010w : port number	14	9	29	27	
Variable Port	1110 110w	14	8	28	27	
OUT = Output to:						
Fixed Port	1110 011w : port number	16	11	31	29	
Variable Port	1110 110w	16	10	30	29	
INS = Input Byte/Word from DX Port	0110 110w	17	10	32	30	
OUTS = Output Byte/Word to DX Port	0110 111w	17	10	32	30	1
REP INS = Input String	1111 0010 : 0110 110w	16 + 8c	10 + 8c	30 + 8c	29 + 8c	2
REP OUTS = Output String	1111 0010 : 0110 111w	17 + 5c	11 + 5c	31 + 5c	30 + 5c	3

NOTES:
1. Two clock cache miss penalty in all cases.
2. c = count in CX or ECX.
3. Cache miss penalty in all modes: Add 2 clocks for every 16 bytes. Entire penalty on second operation.

Table 13-19. Floating Point Clock Count Summary

Instruction	Format	Cache Hit: Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution: Avg (Lower Range . . . Upper Range)	Notes
DATA TRANSFER					
FLD = Real Load to ST(0)					
32-bit memory	11011 001 : mod 000 r/m : s-i-b/disp.	3	2		
64-bit memory	11011 101 : mod 000 r/m : s-i-b/disp.	3	3		
80-bit memory	11011 011 : mod 101 r/m : s-i-b/disp.	6	4		
ST(i)	11011 001 : 11000 ST(i)	4			
FILD = Integer Load to ST(0)					
16-bit memory	11011 111 : mod 000 r/m : s-i-b/disp.	14.5(13-16)	2	4	
32-bit memory	11011 011 : mod 000 r/m : s-i-b/disp.	11.5(9-12)	2	4(2-4)	
64-bit memory	11011 111 : mod 101 r/m : s-i-b/disp.	16.8(10-18)	3	7.8(2-8)	
FBLD = BCD Load to ST(0)					
	11011 111 : mod 100 r/m : s-i-b/disp.	75(70-103)	4	7.7(2-8)	
FST = Store Real from ST(0)					
32-bit memory	11011 011 : mod 010 r/m : s-i-b/disp.	7			1
64-bit memory	11011 101 : mod 010 r/m : s-i-b/disp.	8			2
ST(i)	11011 101 : 11001 ST(i)	3			
FSTP = Store Real from ST(0) and Pop					
32-bit memory	11011 011 : mod 011 r/m : s-i-b/disp.	7			1
64-bit memory	11011 101 : mod 011 r/m : s-i-b/disp.	8			2
80-bit memory	11011 011 : mod 111 r/m : s-i-b/disp.	6			
ST(i)	11011 101 : 11001 ST(i)	3			
FIST = Store Integer from ST(0)					
16-bit memory	11011 111 : mod 010 r/m : s-i-b/disp.	33.4(29-34)			
32-bit memory	11011 011 : mod 010 r/m : s-i-b/disp.	32.4(28-34)			
FISTP = Store Integer from ST(0) and Pop					
16-bit memory	11011 111 : mod 011 r/m : s-i-b/disp.	33.4(29-34)			
32-bit memory	11011 011 : mod 011 r/m : s-i-b/disp.	33.4(29-34)			
64-bit memory	11011 111 : mod 111 r/m : s-i-b/disp.	33.4(29-34)			
FBSTP = Store BCD from ST(0) and Pop					
	11011 111 : mod 110 r/m : s-i-b/disp.	175(172-176)			
FXCH = Exchange ST(0) and ST(i)					
	11011 001 : 11001 ST(i)	4			

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction	Format	Cache Hit: Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution: Avg (Lower Range . . . Upper Range)	Notes
COMPARISON INSTRUCTIONS					
FCOM = Compare ST(0) with Real					
32-bit memory	11011 000 : mod 010 r/m : s-i-b/disp.	4	2	1	
64-bit memory	11011 100 : mod 010 r/m : s-i-b/disp.	4	3	1	
ST(i)	11011 000 : 11010 ST(i)	4			
FCOMP = Compare ST(0) with Real and Pop					
32-bit memory	11011 000 : mod 011 r/m : s-i-b/disp.	4	2	1	
64-bit memory	11011 100 : mod 011 r/m : s-i-b/disp.	4	3	1	
ST(i)	11011 000 : 11011 ST(i)	4		1	
FCOMPP = Compare ST(0) with ST(1) and Pop Twice					
	11011 110 : 1101 1001	5		1	
FICOM = Compare ST(0) with Integer					
16-bit memory	11011 110 : mod 010 r/m : s-i-b/disp.	18(16-20)	2	1	
32-bit memory	11011 010 : mod 010 r/m : s-i-b/disp.	16.5(15-17)	2	1	
FICOMP = Compare ST(0) with Integer					
16-bit memory	11011 110 : mod 011 r/m : s-i-b/disp.	18(16-20)	2	1	
32-bit memory	11011 010 : mod 011 r/m : s-i-b/disp.	16.5(15-17)	2	1	
FTST = Compare ST(0) with 0.0					
	11011 011 : 1110 0100	4		1	
FUCOM = Unordered compare ST(0) with ST(i)					
	11011 101 : 11100 ST(i)	4		1	
FUCOMP = Unordered compare ST(0) with ST(i) and Pop					
	11011 101 : 11101 ST(i)	4		1	
FUCOMPP = Unordered compare ST(0) with ST(1) and Pop Twice					
	11011 101 : 11101 1001	5		1	
FXAM = Examine ST(0)					
	11011 001 : 1110 0101	8			

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit: Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution: Avg (Lower Range . . . Upper Range)	Notes
CONSTANTS				
FLDZ = Load +0.0 Into ST(0) 11011 001 : 1110 1110 :	4			
FLD1 = Load +1.0 Into ST(0) 11011 001 : 1110 1000 :	4			
FLDP1 = Load π Into ST(0) 11011 001 : 1110 1011 :	8		2	
FLDL2T = Load $\log_2(10)$ Into ST(0) 11011 001 : 1110 1001 :	8		2	
FLDL2E = Load $\log_2(e)$ Into ST(0) 11011 001 : 1110 1010 :	8		2	
FLDLG2 = Load $\log_{10}(2)$ Into ST(0) 11011 001 : 1110 1100 :	8		2	
FLDLN2 = Load $\log_e(2)$ Into ST(0) 11011 001 : 1110 1101 :	8		2	
ARITHMETIC				
FADD = Add Real with ST(0)				
ST(0) ← ST(0) + 32-bit memory 11011 000 : mod 000 r/m : s-i-b/disp.	10(8-20)	2	7(5-17)	
ST(0) ← ST(0) + 64-bit memory 11011 100 : mod 000 r/m : s-i-b/disp.	10(8-20)	3	7(5-17)	
ST(d) ← ST(0) + ST(i) 11011 d00 : 11000 ST(i)	10(8-20)		7(5-17)	
FADDP = Add real with ST(0) and Pop (ST(i) ← ST(0) +ST(i)) 11011 110 : 11000 ST(i) :	10(8-20)		7(5-17)	

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution Avg (Lower Range . . . Upper Range)	Notes
ARITHMETIC (Continued)				
FSUB = Subtract Real from ST(0)				
ST(0) ← ST(0) − 32-bit memory				
11011 000 : mod 100 r/m : s-i-b/disp.	10(8-20)	2	7(5-17)	
ST(0) ← ST(0) − 64-bit memory				
11011 100 : mod 100 r/m : s-i-b/disp.	10(8-20)	3	7(5-17)	
ST(d) ← ST(0) − ST(i)				
11011 d00 : 11001 ST(i)	10(8-20)		7(5-17)	
FSUBP = Subtract real from ST(0) and Pop (ST(i) ← ST(0) − ST(i))				
11011 110 : 11001 ST(i)	10(8-20)		7(5-17)	
FSUBR = Subtract Real reversed (Subtract ST(0) from Real)				
ST(0) ← 32-bit memory − ST(0)				
11011 000 : mod 101 r/m : s-i-b/disp.	10(8-20)	2	7(5-17)	
ST(0) ← 64-bit memory − ST(0)				
11011 100 : mod 101 r/m : s-i-b/disp.	10(8-20)	3	7(5-17)	
ST(d) ← ST(i) − ST(0)				
11011 d00 : 11001 ST(i)	10(8-20)		7(5-17)	
FSUBRP = Subtract Real reversed and Pop (ST(i) ← ST(i) − ST(0))				
11011 110 : 11100 ST(i)	10(8-20)		7(5-17)	
FMUL = Multiply Real with ST(0)				
ST(0) ← ST(0) X 32-bit memory				
11011 000 : mod 001 r/m : s-i-b/disp.	11	2	8	
ST(0) ← ST(0) X 64-bit memory				
11011 100 : mod 001 r/m : s-i-b/disp.	14	3	11	
ST(d) ← ST(0) X ST(i)				
11011 d00 : 11001 ST(i)	16		13	
FMULP = Multiply ST(0) with ST(i) and Pop (ST(i) ← ST(0) XST(i))				
11011 110 : 11001 ST(i)	16		13	
FDIV = Divide ST(0) by Real				
ST(0) ← ST(0)/ 32-bit memory				
11011 000 : mod 110 r/m : s-i-b/disp.	73	2	70	3
ST(0) ← ST(0)/ 64-bit memory				
11011 100 : mod 110 r/m : s-i-b/disp.	73	3	70	3
ST(d) ← ST(0)/ ST(i)				
11011 d00 : 11111 ST(i)	73		70	3
FDIVP = Divide ST(0) by ST(i) and Pop (ST(i) ← ST(0)/ ST(i))				
11011 110 : 11111 ST(i)	73		70	3

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit: Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution: Avg (Lower Range . . . Upper Range)	Notes
ARITHMETIC (Continued)				
FDIVR = Divide real reversed (Real/ST(0))				
ST(0) ← 32-bit memory/ ST(0)				
11011 000 : mod 111 r/m : s-i-b/disp.	73	2	70	3
ST(0) ← 64-bit memory/ ST(0)				
ST(d) ← ST(i)/ ST(0) 11011 100 : mod 111 r/m : s-i-b/disp.	73	3	70	3
11011 d00 : 11110 ST(i)	73		70	3
FDIVRP = Divide real reversed and Pop (ST(i) ← ST(i)/ ST(0))				
11011 110 : 11110 ST(i)	73		70	3
FIADD = Add Integer to ST(0)				
ST(0) ← ST(0) + 16-bit memory				
11011 110 : mod 000 r/m : s-i-b/disp.	24(20-35)	2	7(5-17)	
ST(0) ← ST(0) + 32-bit memory				
11011 010 : mod 000 r/m : s-i-b/disp.	22.5(19-32)	2	7(5-17)	
FISUB = Subtract Integer from ST(0)				
ST(0) ← ST(0) − 16-bit memory				
11011 110 : mod 100 r/m : s-i-b/disp.	24(20-35)	2	7(5-17)	
ST(0) ← ST(0) − 32-bit memory				
11011 010 : mod 100 r/m : s-i-b/disp.	22.5(19-32)	2	7(5-17)	
FISUBR = Integer Subtract Reversed				
ST(0) ← 16-bit memory − ST(0)				
11011 110 : mod 101 r/m : s-i-b/disp.	24(20-35)	2	7(5-17)	
ST(0) ← 32-bit memory − ST(0)				
11011 010 : mod 101 r/m : s-i-b/disp.	22.5(19-32)	2	7(5-17)	
FIMUL = Multiply Integer with ST(0)				
ST(0) ← ST(0) X 16-bit memory				
11011 110 : mod 101 r/m : s-i-b/disp.	25(23-27)	2	8	
ST(0) ← ST(0) X 32-bit memory				
11011 010 : mod 001 r/m : s-i-b/disp.	23.5(19-32)	2	8	

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution Avg (Lower Range . . . Upper Range)	Notes
ARITHMETIC (Continued)				
FIDIV = Integer Divide				
ST(0) ← ST(0)/ 16-bit memory				
11011 110 : mod 110 r/m : s-i-b/disp.	87(85-89)	2	70	3
ST(0) ← ST(0)/ 32-bit memory				
11011 010 : mod 110 r/m : s-i-b/disp.	85.5(84-86)	2	70	3
FIDVR = Integer Divide Reversed				
ST(0) ← 16-bit memory/ST(0)				
11011 110 : mod 111 r/m : s-i-b/disp.	87(85-89)	2	70	3
ST(0) ← 32-bit memory/ST(0)				
11011 010 : mod 111 r/m : s-i-b/disp.	85.5(84-86)	2	70	3
FSQRT = Square Root				
11011 001 : 1111 1010	85.5(83-87)		70	
FSCALE = Scale ST(0) by ST(1)				
11011 001 : 1111 1101	31(30-32)		2	
FXTRACT = Extract Components of ST(0)				
11011 001 : 1111 0100	19(16-20)		4(2-4)	
FPREM = Partial Reminder				
11011 001 : 1111 1000	84(70-138)		2(2-8)	
FPREM1 = Partial Reminder (IEEE)				
11011 001 : 1111 0101	94.5(72-167)		5.5(2-18)	
FRNDINT = Round ST(0) to Integer				
11011 001 : 1111 1100	29.1(21-30)		7.4(2-8)	
FABS = Absolute value of ST(0)				
11011 001 : 1110 0001	3			
FCHS = Change Sign of ST(0)				
11011 001 : 1110 0000	6			
TRANSCENDENTAL				
FCOS = Cosine of ST(0)				
11011 001 : 1111 1111	241(193-279)		2	6,7
FPTAN = Partial Tangent of ST(0)				
11011 001 : 1111 0010	244(200-273)		70	6,7
FPATAN = Partial Arctangent				
11011 001 : 1111 0011	289(218-303)		5(2-17)	6

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit: Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution: Avg (Lower Range . . . Upper Range)	Notes
TRANSCENDENTAL (Continued)				
FSIN = Sine of ST(0) 11011 001 : 1111 1110	241(193-279)		2	6,7
FSINCOS = Sine and Cosine of ST(0) 11011 001 : 1111 1011	291(243-329)		2	6,7
F2XM1 = $2^{ST(0)}-1$ 11011 001 : 1111 0000	242(140-279)		2	6
FYL2X = ST(1) x $\log_2$(ST(0)) 11011 001 : 1111 0001	311(196-329)		13	6
FYL2XP1 = ST(1) x $\log_2$(ST(0) + 1.0) 11011 001 : 1111 1001	313(171-326)		13	6
PROCESSOR CONTROL				
FINIT = Initialize FPU 11011 001 : 1110 0011	17			4
FSTSW AX = Store status word into AX 11011 111 : 1110 0000	3			5
FSTSW = Store status word into memory 11011 101 : mod 111 r/m : s-i-b/disp.	3			5
FLDCW = Load control word 11011 001 : mod 101 r/m : s-i-b/disp.	4	2		
FSTCW = Store control word 11011 001 : mod 111 r/m : s-i-b/disp.	3			5
FCLEX = Clear exceptions 11011 011 : 1110 0010	7			4
FSTENV = Store environment 11011 011 : mod 110 r/m : s-i-b/disp.				
Real and Virtual Modes 16-bit address	67			4
Real and Virtual Modes 32-bit address	67			4
Protected Mode 16-bit address	56			4
Protected Mode 32-bit address	56			4
FLDENV = Load Environment 11011 011 : mod 100 r/m : s-i-b/disp.				
Real and Virtual Modes 16-bit address	44	2		
Real and Virtual Modes 32-bit address	44	2		
Protected Mode 16-bit address	34	2		
Protected Mode 32-bit address	34	2		

Table 13-19. Floating Point Clock Count Summary (Continued)

Instruction Format	Cache Hit Avg (Lower Range . . . Upper Range)	Penalty if Cache Miss	Concurrent Execution Avg (Lower Range . . . Upper Range)	Notes
PROCESSOR CONTROL (Continued)				
FSAVE = Save State				
11011 101 : mod 110 r/m : s-i-b/disp.				
Real and Virtual Modes 16-bit address	154			4
Real and Virtual Modes 32-bit address	154			4
Protected Mode 16-bit address	143			4
Protected Mode 32-bit address	143			4
FRSTOR = Restore State				
11011 101 : mod 100 r/m : s-i-b/				
Real and Virtual Modes 16-bit address	131	23		
Real and Virtual Modes 32-bit address	131	27		
Protected Mode 16-bit address	120	23		
Protected Mode 32-bit address	120	27		
FINCSTP = Increment Stack Pointer				
11011 001 : 1111 0111	3			
FDECSTP = Decrement Stack Pointer				
11011 001 : 1111 0110	3			
FFREE = Free ST(i)				
11011 101 : 11000 ST(i)	3			
FNOP = No Operations				
11011 101 : 1101 0000	3			
WAIT = Wait until FPU ready (min/max)				
10011011	1⁄3			

NOTES:
1. If operand is 0 clock counts = 27.
2. If operand is 0 clock counts = 28.
3. If CW.PC indicates 24-bit precision then subtract 38 clocks.
   If CW.PC indicates 53-bit precision then subtract 11 clocks.
4. If there is a numeric error pending from a previous instruction add 17 clocks.
5. If there is a numeric error pending from a previous instruction add 18 clocks.
6. The INT pin is polled several times while this function is executing to assure short interrupt latency.
7. If ABS(operand) is greater than $\pi/4$ then add n clocks, where n = (operand/($\pi/4$)).

14.0 DIFFERENCES BETWEEN MILITARY INTEL486 PROCESSORS AND INTEL386 PROCESSORS

The differences between Military Intel486 processors and Intel386 processors are due to performance enhancements. The differences are listed below.

1. Instruction clock counts have been reduced to achieve higher performance. (See section 13.0, ''Instruction Set Summary.'')
2. The Military Intel486 processor bus is significantly faster than the Intel386 processor bus. Differences include a 1X clock, parity support, burst cycles, cacheable cycles, cache invalidate cycles and 8-bit bus support. The Hardware Interface and Bus Operation sections (sections 9.0 and 10.0) of the data sheet should be carefully read to understand the Military Intel486 processor bus functionality.
3. To support the on-chip cache bits have been added to control register 0 (CD and NW) (see section 4.2.3.1, ''Control Registers''), new pins have been added to the bus (see section 9.0, ''Hardware Interface'') and new bus cycle types have been added (see section 10.0, ''Bus Operation''). The on-chip cache needs to be enabled after reset by clearing the CD and NW bit in CR0.
4. Eight new instructions have been added:
   - Byte Swap (BSWAP)
   - Exchange-and-Add (XADD)
   - Compare and Exchange (CMPXCHG)
   - Invalidate Data Cache (INVD)
   - Write-back and Invalidate Data Cache (WBINVD)
   - Invalidate TLB Entry (INVLPG)
   - Processor Identification (CPUID)
   - Resume (RSM)
5. Two bits defined in control register 3, the page table entries and page directory entries (PCD and PWT). (See section 6.4.2.5, ''Page Directory/Table Entries.'')
6. A page protection feature has been added. This feature required a new bit in control register 0 (WP) (See sections 4.2.3.1 ''Control Registers'' and 6.4.3 ''Page Level Protection.'')
7. An Alignment Check feature has been added. This feature required a bit in the flags register (AC) (section 4.2.2.3 ''Flags Register'') and a bit in control register 0 (AM) (section 4.2.3.1 ''Control Registers'').
8. The replacement algorithm for the translation lookaside buffer has been changed from a random algorithm to a pseudo least recently used algorithm like that used by the on-chip cache. (See section 7.5 ''Cache Replacement'' for a description of the algorithm.)
9. Three testability registers, TR3, TR4 and TR5, have been added for testing the on-chip cache. TLB testability has been enhanced. (See section 11.0, ''Testability.'')
10. The prefetch queue has been increased from 16 bytes to 32 bytes. A jump always needs to execute after modifying code to guarantee correct execution of the new instruction.
11. After reset, the ID in the upper byte of the DX register is 04.

14.1 Differences between the Intel386 Processor with an Intel387™ Math CoProcessor and Military Intel486 DX, IntelDX2 and IntelDX4 Processors

In addition to the previously mentioned enhancements, the Military Intel486 DX, IntelDX2 and IntelDX4 processors offer the following features:

1. The complete Intel387 math coprocessor instruction set and register set have been added. No I/O cycles are performed during Floating Point instructions. The instruction and data pointers are set to 0 after FINIT/FSAVE. Interrupt 9 can no longer occur, interrupt 13 occurs instead.
2. Support for floating point error reporting modes to guarantee DOS compatibility. These modes require a bit in control register 0 (NE) (see section 4.2.3.1, ''Control Registers'') and pins (FERR# and IGNNE#). (See sections 9.2.15, ''Numeric Error Reporting'' and 10.2.14 ''Floating Point Error Handling.'')
3. In some cases FERR# is asserted when the next floating point instruction is encountered and in other cases it is asserted before the next floating point instruction is encountered, depending upon the execution state the instruction causing exception. (See sections 9.2.15, ''Numeric Error Reporting'' and 10.2.14, ''Floating Point Error Handling.'') For both of these cases, the Intel387 math coprocessor asserts ERROR# when the error occurs and does not wait for the next floating point instruction to be encountered.
4. The contents of the base registers ***including the floating point registers*** may be different after reset.

15.0 ELECTRICAL DATA

The following sections describe recommended electrical connections and electrical specifications for the Military Intel486 processor.

15.1 Power and Grounding

15.1.1 POWER CONNECTIONS

The Military Intel486 processor is implemented in CHMOS technology and has modest power requirements. However, the high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, multiple V_{CC} and V_{SS} pins feed the Military Intel486 processor.

Power and ground connections must be made to all external V_{CC} and GND pins of the Military Intel486 processor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must be likewise connected on a GND plane.

15.1.2 MILITARY INTEL486 PROCESSOR POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Military Intel486 processor. The Military Intel486 processor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors (i.e., surface-mount capacitors) and interconnects are recommended for the best high-frequency electrical performance. Inductance can be reduced by connecting capacitors directly to the V_{CC} and V_{SS} planes, with minimal trace length between the component pads and vias to the plane. These capacitors should be evenly distributed around each component on the V_{CC} power plane.

Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

The recommendation for the Military Intel486 processor is 9 x 0.01 μF and 9 x 0.1 μF capacitors.

The power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the Military Intel486 processor to enter the Auto HALT Power Down state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the Military Intel486 processor. Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 microfarad range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel. These capacitors should be placed near the Military Intel486 processor (on the processor power plane) to ensure that the supply voltage stays within specified limits during changes in the supply current while in operation.

15.1.3 V_{CC5} AND V_{CC} POWER SUPPLY REQUIREMENTS FOR THE INTELDX4 PROCESSOR

In mixed voltage systems that will be driving IntelDX4 processor inputs in excess of 3.3V, the V_{CC5} pin must be connected to the system 5V supply. In order to limit current flow into the V_{CC5} pin, there is a limit to the voltage differential between the V_{CC5} pin and the other V_{CC} pins. The voltage differential between the V_{CC5} pin of the IntelDX4 processor and its 3.3V V_{CC} pins should never exceed 2.25V. The 2.25V limit applies to power up, power down and steady state operation. Table 15-1 outlines this requirement.

Table 15-1. Dual Power Supply Requirements for the IntelDX4™ Processor

Symbol	Parameter	Min	Max	Unit	Notes
VDIFF	$V_{CC5}-V_{CC}$ Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25V during power-up, power-down or during operation.

Meeting this requirement ensures proper operation of the IntelDX4 processor and guarantees that the current draw into the V_{CC5} pin will not exceed the I_{CC5} specification (see section 15.3, ''DC Specifications''). If the voltage difference requirement cannot be met due to system design limitations, then an alternate solution may be employed. A minimum of a 100Ω series resistor may be used to limit the current into the V_{CC5} pin. This resistor will ensure that current drawn by the V_{CC5} pin will not exceed the maximum rating of 55 mA for this pin (see section 15.2, ''Maximum Ratings'').

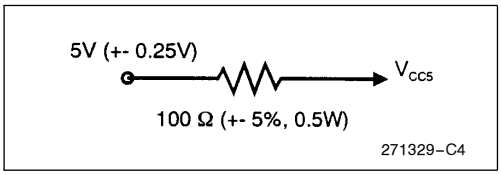


Figure 15-1. IntelDX4™ Processor V_{CC5} Current Limiting Resistor

Note that this resistor is not necessary if the system can guarantee that the voltage difference between V_{CC5} and V_{CC} is always limited to 2.25V, even during power up and power down.

In 3.3V-only systems and systems that will be driving all IntelDX4 processor inputs and I/Os from 3.3V logic, the V_{CC5} pin should be connected directly to the 3.3V V_{CC} plane. This will guarantee the voltage difference specification is met and will eliminate the current draw into the V_{CC5} pin. In a 3.3V-only system, the V_{CC5} may be connected to the 5V supply as described previously, as long as the voltage differential in Table 15-1 is met, and assuming the current drawn by the V_{CC5} pin is of little consequence to the system design.

15.1.4 SYSTEM CLOCK RECOMMENDATIONS

It is recommended that the CLK input to the Military Intel486 processor should not be driven until V_{CC} has reached its normal operating level (either 3.3V or 5V). The CLK input may be grounded or allowed to ramp with V_{CC} during this period. Once V_{CC} has reached its normal operating level, the Military Intel486 processor can handle the clock frequency for which it is specified and the oscillator/clock driver should have locked onto its desired frequency.

15.1.5 OTHER CONNECTION RECOMMENDATIONS

NC pins should always remain unconnected. Connection of NC pins to V_{CC} or V_{SS} or to any other signal can result in component malfunction or incompatibility with other steppings of the Military Intel486 processor family.

For reliable operation, always connect unused inputs to an appropriate signal level. Active LOW inputs should be connected to V_{CC} through a pull-up resistor. Pull-ups in the range of 20 KΩ are recommended. Active HIGH inputs should be connected to GND.

15.2 Maximum Ratings

Table 15-2 is a stress rating only. Functional operation at the maximums is not guaranteed. Function operating conditions are given in Table 15-3 for 3.3V processor DC Specifications, Table 15-5 for 5V DC Specifications, Tables 15-8 and 15-9 for 3.3V processor AC specifications, and Table 15-11 for 5V processor AC specifications.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Military Intel486 processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 15-2. Absolute Maximum Ratings

Case Temperature under Bias	−65°C to +125°C
Storage Temperature	−65°C to +150°C
DC Voltage on Any Pin with Respect to Ground	−0.5 to V_{CC} + 0.5V −0.5 to V_{CC5} + 0.5V(1)
Supply Voltage with Respect to V_{SS}	V_{CC} −0.5V to +6.5V(2) V_{CC} −0.5V to +4.6V(1) V_{CC5}(1) −0.5V to +6.5V(1)
Transient Voltage on Any Input	−1.6V to V_{CC5} +1.6V(1,3)
Maximum Allowable Current Sink on V_{CC5}(1)	55 mA

NOTES:
1. For IntelDX4™ processor only.
2. All Military Intel486™ processors except IntelDX4 processor.
3. Maximum voltage on any pin with respect to ground is the lesser of Vcc5 + 1.6V or 6.5V for the IntelDX4 processor.

15.3 DC Specifications

15.3.1 3.3V DC CHARACTERISTICS

Table 15-3 is for IntelDX4 processors.

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**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 15-3. 3.3V DC Specifications

Functional operating range: V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 7); T_{CASE} = −55°C to +125°C

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input LOW Voltage	−0.3		+0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC5}+0.3	V	
V_{IHC}	Input HIGH Voltage of CLK	V_{CC}−0.6		V_{CC}+0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 μA			 0.40 0.20	 V V	
				0.45	V	
V_{OH}	Output HIGH Voltage I_{OH} = −2.0 mA	 2.4			 V	
I_{CC5}	V_{CC5} Leakage Current		15	300	μA	
I_{LI}	Input Leakage Current			±15	μA	
I_{IH}	Input Leakage Current			200	μA	
I_{IL}	Input Leakage Current			−400	μA	
I_{LO}	Output Leakage Current			±15	μA	
C_{IN}	Input Capacitance			10	pF	
C_{OUT}	Output or I/O Capacitance			14	pF	6
C_{CLK}	CLK Capacitance			12	pF	

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Table 15-4. 3.3V I_{CC} Values for IntelDX4™ Processor

Functional Operating Range: $V_{CC} = 3.3V \pm 5\%$; $V_{CC5} = 5V \pm 0.25V$ (Note 7); $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	100 MHz 75 MHz		1450 mA 1100 mA	1
I_{CC} Active (Thermal Design)	100 MHz 75 MHz	1200 mA 900 mA	1300 mA 975 mA	2, 3, 4
I_{CC} Stop Grant	100 MHz 75 MHz	50 mA 20 mA	100 mA 75 mA	5
I_{CC} Stop Clock	0 MHz	600 μA	1 mA	6

NOTES:
1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at $V_{CC} = 3.465V$.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at $V_{CC} = 3.3V$.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at $V_{CC} = 3.3V$, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.
7. V_{CC5} should be connected to $3.3V \pm 5\%$ in 3.3V-only systems.

15.3.2 5V DC CHARACTERISTICS

Table 15-5 is for Military Intel486™ DX and IntelDX2 Processors.

Table 15-5. 5V DC Specifications

Functional operating range: $V_{CC} = 5V \pm 0.25V$; $T_{CASE} = -55°C$ to $+125°C$

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input LOW Voltage	−0.3		+0.8	V	7
V_{IH}	Input HIGH Voltage	2.0		V_{CC}+0.3	V	8
V_{OL}	Output LOW Voltage			0.45	V	1
V_{OH}	Output HIGH Voltage	2.4			V	2
I_{LI}	Input Leakage Current			±15	μA	3
I_{IH}	Input Leakage Current			200	μA	4
I_{IL}	Input Leakage Current			−400	μA	5
I_{LO}	Output Leakage Current			±15	μA	
C_{IN}	Input Capacitance PGA			20	pF	6
C_{OUT}	Output or I/O Capacitance PGA			20	pF	6
C_{CLK}	CLK Capacitance PGA			20	pF	6

NOTES:
1. This parameter is measured at: Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at: Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
3. This parameter is for inputs without pull-ups or pull-downs and $0V \leq V_{IN} \leq V_{CC}$.
4. This parameter is for inputs with pull-downs and $V_{IH} = 2.4V$.
5. This parameter is for inputs with pull-ups and $V_{IL} = 0.45V$.
6. F_C=1 MHz; Not 100% tested.
7. Minimum value guaranteed by design characterization but not tested.
8. Maximum value guaranteed by design characterization but not tested.

Table 15-6. 5V I_{CC} Values for Military Intel486™ DX Processor

Functional Operating Range: $V_{CC} = 5V \pm 0.25V$; $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	33 MHz 25 MHz		900 mA 700 mA	1
I_{CC} Active (Thermal Supply)	33 MHz 25 MHz	700 mA 550 mA	857 mA 666 mA	2, 3, 4
I_{CC} Stop Grant	33 MHz 25 MHz	40 mA 40 mA	80 mA 80 mA	5
I_{CC} Stop Clock	0 MHz	200 μA	2 mA	6

Table 15-7. 5V I_{CC} Values for IntelDX2™ Processor

Functional Operating Range: $V_{CC} = 5V \pm 0.25V$; $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	50 MHz 66 MHz		950 mA 1200 mA	1
I_{CC} Active (Thermal Supply)	50 MHz 66 MHz	775 mA 975 mA	906 mA 1145 mA	2, 3, 4
I_{CC} Stop Grant	50 MHz 66 MHz	35 mA 45 mA	70 mA 90 mA	5
I_{CC} Stop Clock	0 MHz	200 μA	2 mA	6

NOTES:

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at $V_{CC} = 5.25V$.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at $V_{CC} = 5V$.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at $V_{CC} = 5V$, running Microsoft Windows 3.1 at an idle condition at room temperature. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.

15.4 AC Specifications

The AC specifications given in the tables in this section consist of output delays, input setup requirements and input hold requirements. All AC specifications are relative to the rising edge of the input system clock (CLK) unless otherwise specified.

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15.4.1 3.3V AC CHARACTERISTICS

Table 15-8. 3.3V AC Characteristics for the 75/25-MHz IntelDX4™ Processor

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	25	MHz		2
t_1	CLK Period	40	125	ns	15-2	
t_2	CLK High Time	14		ns	15-2	at 2V
t_3	CLK Low Time	14		ns	15-2	at 0.8V
t_4	CLK Fall Time		4	ns	15-2	2V to 0.8V
t_5	CLK Rise Time		4	ns	15-2	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, CACHE#, HITM# Valid Delay	2	19	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, CACHE# Float Delay		28	ns	15-7	3
t_8	PCHK# Valid Delay	2	24	ns	15-5	
t_{8a}	BLAST#, PLOCK# SMIACT# Valid Delay	2	24	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		28	ns	15-7	3
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	2	20	ns	15-6	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	15-7	3
t_{12}	EADS#, INV Setup Time	8		ns	15-3	
t_{13}	EADS#, INV Hold Time	3		ns	15-3	
t_{14}	KEN#, BS16#, BS8#, WB/WT# Setup Time	8		ns	15-3	
t_{15}	KEN#, BS16#, BS8#, WB/WT# Hold Time	3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	8		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	8		ns	15-3	
t_{18a}	BOFF# Setup Time	8		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Setup Time	8		ns	15-3	5
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	15-3, 15-4	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	15-3, 15-4	

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
3. Not 100% tested. Guaranteed by design characterization.
4. All timing specifications assume C_L = 50 pF. See capacitive derating charts for additional timing delays due to loading.
5. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

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Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	33	MHz		2
t_1	CLK Period	30	125	ns	15-2	
t_2	CLK High Time	11		ns	15-2	at 2V
t_3	CLK Low Time	11		ns	15-2	at 0.8V
t_4	CLK Fall Time		3	ns	15-2	2V to 0.8V
t_5	CLK Rise Time		3	ns	15-2	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, CACHE#, HITM# Valid Delay	2	14	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, CACHE# Float Delay		20	ns	15-7	3
t_8	PCHK# Valid Delay	2	14	ns	15-5	
t_{8a}	BLAST#, PLOCK#, SMIACT# Valid Delay	2	14	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		20	ns	15-7	3
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	2	14	ns	15-6	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		20	ns	15-7	3
t_{12}	EADS#, INV Setup Time	5		ns	15-3	
t_{13}	EADS#, INV Hold Time	3		ns	15-3	
t_{14}	KEN#, BS16#, BS8#, WB/WT# Setup Time	5		ns	15-3	
t_{15}	KEN#, BS16#, BS8#, WB/WT# Hold Time	3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	5		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	6		ns	15-3	
t_{18a}	BOFF# Setup Time	7		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	

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Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors (Continued)

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Setup Time	5		ns	15-3	5
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	15-3, 15-4	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	15-3, 15-4	

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
3. Not 100% tested. Guaranteed by design characterization.
4. All timing specifications assume C_L = 50 pF. See capacitive derating charts for additional timing delays due to loading.
5. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 15-10. 3.3V IntelDX4™ Processor AC Specifications for the Test Access Port (All IntelDX4 Processor Frequencies)

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure
t_{24}	TCK Frequency		25	MHz	
t_{25}	TCK Period	40		ns	
t_{26}	TCK High Time	10		ns	
t_{27}	TCK Low Time	10		ns	
t_{28}	TCK Rise Time		4	ns	
t_{29}	TCK Fall Time		4	ns	
t_{30}	TDI, TMS Setup Time	8		ns	15-8
t_{31}	TDI, TMS Hold Time	7		ns	15-8
t_{32}	TDO Valid Delay	3	25	ns	15-8
t_{33}	TDO Float Delay		30	ns	
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	15-8
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	15-8
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	15-8
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	15-8

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. All inputs and outputs are TTL Level.
3. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
4. TCK period ≤ CLK period.
5. Parameters t_{30}–t_{37} are measured from TCK.

15.4.2 5V AC CHARACTERISTICS

Table 15-11 is for 25- and 33-MHz Military Intel486 DX, 50-MHz IntelDX2™ (25-MHz Max.) and 66-MHz IntelDX2 (33-MHz Max.) processors.

Table 15-11. 5V AC Characteristics

Functional operating range: V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF unless otherwise specified. (See also Table 15-12).

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
	Frequency	8	**25**	8	**33**	MHz		1
t_1	CLK Period	40	125	30	125	ns	15-2	
t_{1a}	CLK Period Stability		±250		±250	ps	15-2	Adjacent clocks(2)
t_2	CLK High Time	14		11		ns	15-2	at 2V
t_3	CLK Low Time	14		11		ns	15-2	at 0.8V(2)
t_4	CLK Fall Time		4		3	ns	15-2	2V to 0.8V(2)
t_5	CLK Rise Time		4		3	ns	15-2	0.8V to 2V(2)
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT#, FERR# Valid Delay	2	19	2	14	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA Float Delay		28		20	ns	15-7	2
t_8	PCHK# Valid Delay	2	24	2	14	ns	15-5	
t_{8a}	BLAST#, PLOCK# Valid Delay	2	24	2	14	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		28		20	ns	15-7	2
t_{10}	D0–D31, DP0–DP3 Write Data Valid Delay	2	20	2	14	ns	15-6	
t_{11}	D0–D31, DP0–DP3 Write Data Float Delay		28		20	ns	15-7	2
t_{12}	EADS# Setup Time	8		5		ns	15-3	
t_{13}	EADS# Hold Time	3		3		ns	15-3	
t_{14}	KEN#, BS16#, BS8# Setup Time	8		5		ns	15-3	

Table 15-11. 5V AC Characteristics (Continued)
Functional operating range: V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF unless otherwise specified.

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
t_{15}	KEN#, BS16#, BS8# Hold Time	3		3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	8		5		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	8		6		ns	15-3	
t_{18a}	BOFF# Setup Time	8		7		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	15-3	
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Setup Time	8		5		ns	15-3	
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Hold Time	3		3		ns	15-3	
t_{22}	D0–D31, DP0–DP3, A4–A31 Read Setup Time	5		5		ns	15-3 15-4	
t_{23}	D0–D31, DP0–DP3, A4–A31 Read Hold Time	3		3		ns	15-3 15-4	

NOTES:
1. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
2. Not 100% tested, guaranteed by design characterization.

Table 15-12. 5V Military Intel486 Processor AC Specifications for the Test Access Port (All Processors and Frequencies)

V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Notes
t_{24}	TCK Frequency		8	MHz	1
t_{25}	TCK Period	125		ns	
t_{26}	TCK High Time	40		ns	@ 2.0V
t_{27}	TCK Low Time	40		ns	@ 0.8V
t_{28}	TCK Rise Time		8	ns	2
t_{29}	TCK Fall Time		8	ns	2
t_{30}	TDI, TMS Setup Time	8		ns	3
t_{31}	TDI, TMS Hold Time	10		ns	3
t_{32}	TDO Valid Delay	2	30	ns	3
t_{33}	TDO Float Delay		36	ns	3
t_{34}	All Outputs (Non-Test) Valid Delay	2	30	ns	3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	3
t_{37}	All Inputs (Non-Test) Hold Time	10		ns	3

NOTES:
1. TCK period ≤ CLK period.
2. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
3. Parameters t_{30}–t_{37} are measured from TCK.
4. Refer to Figure 15-18 for signal waveforms.

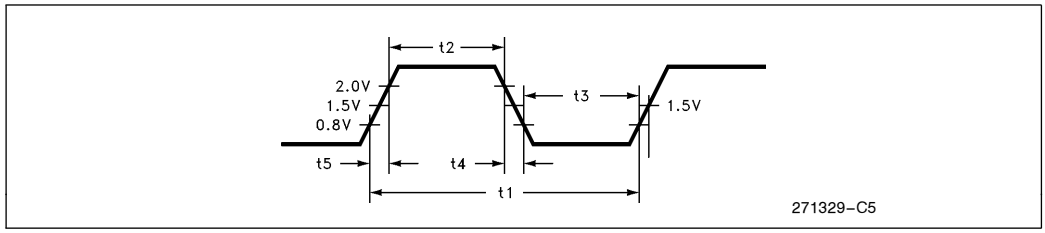


Figure 15-2. CLK Waveforms

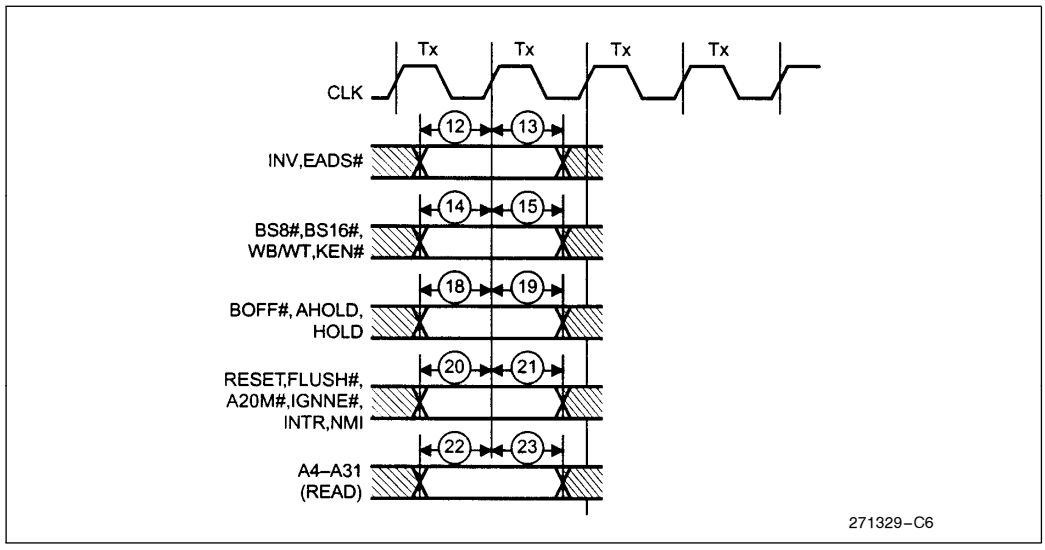


Figure 15-3. Input Setup and Hold Timing

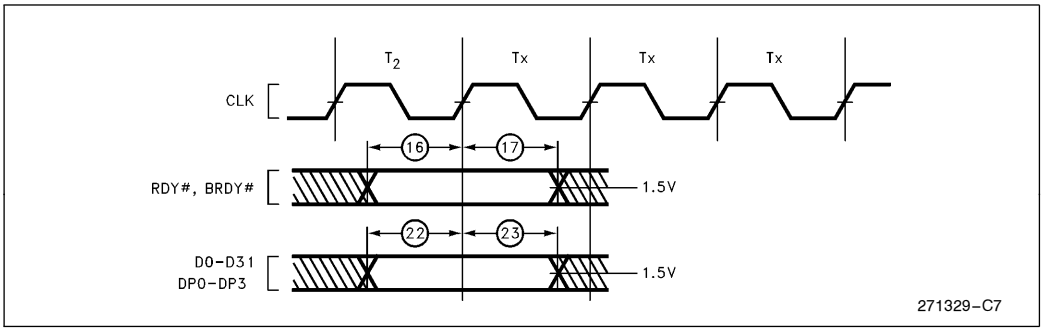


Figure 15-4. Input Setup and Hold Timing

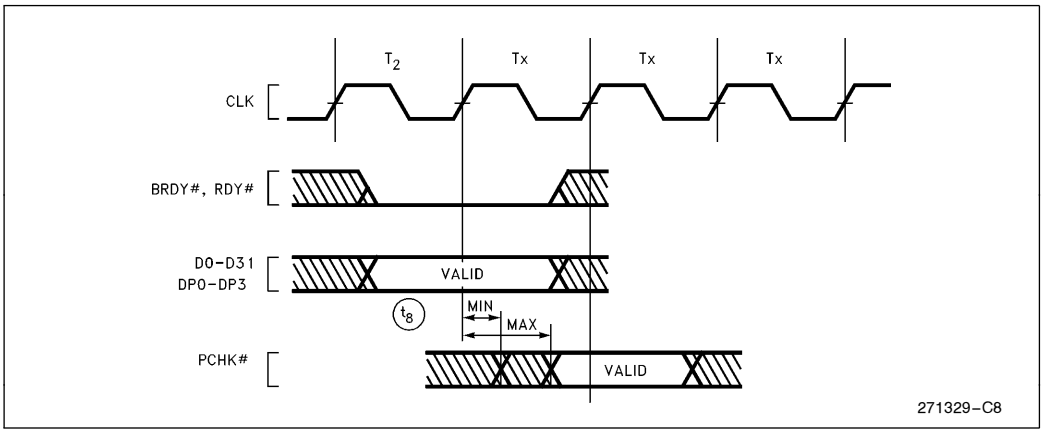


Figure 15-5. PCHK# Valid Delay Timing

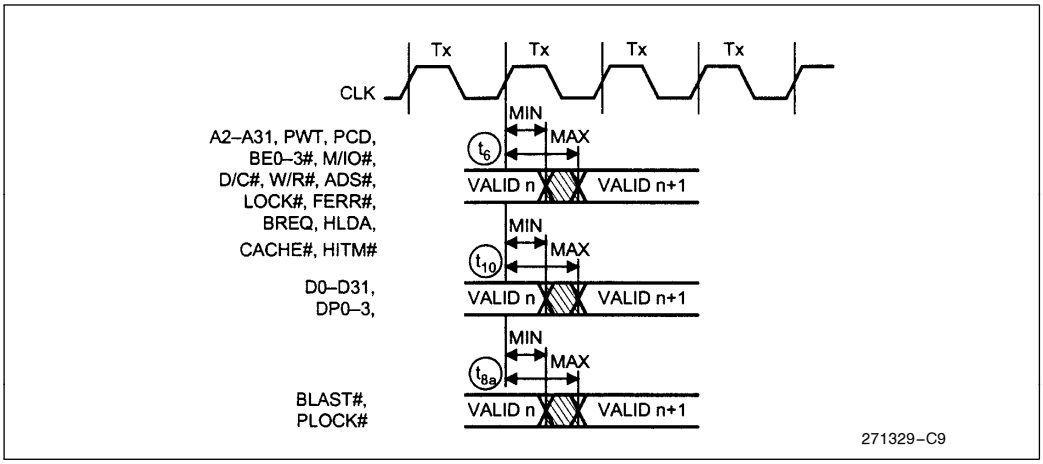


Figure 15-6. Output Valid Delay Timing

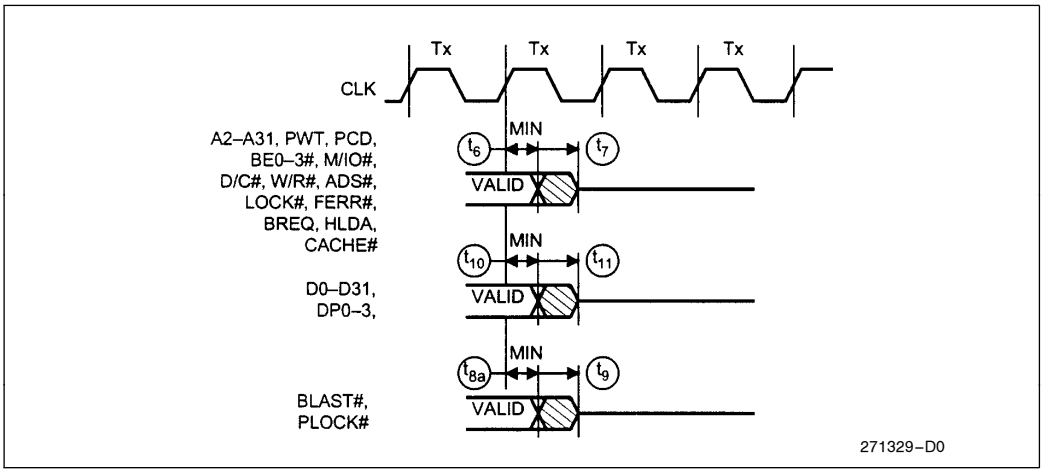


Figure 15-7. Maximum Float Delay Timing

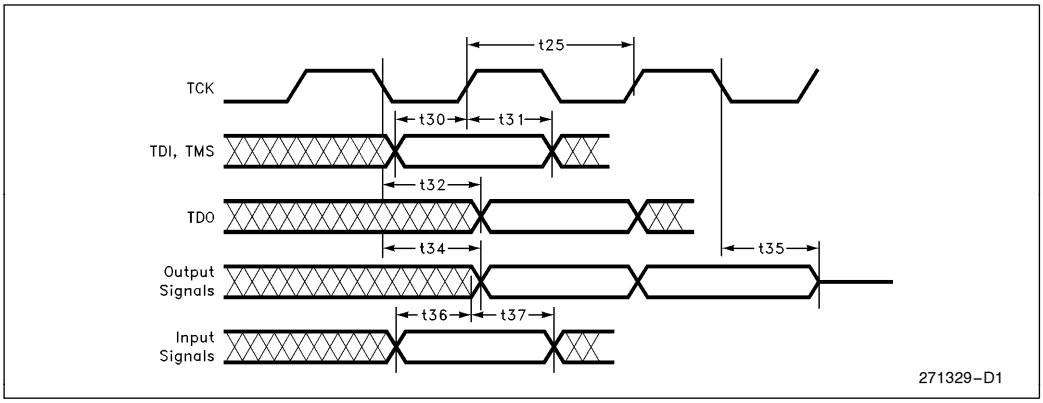
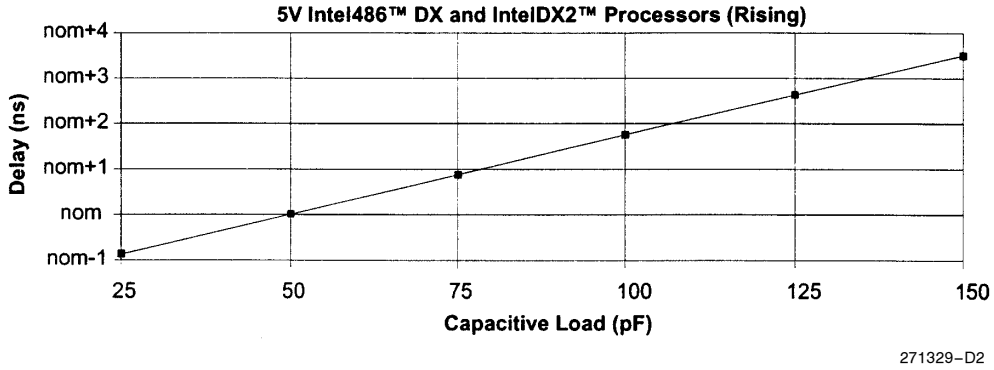


Figure 15-8. Test Signal Timing Diagram

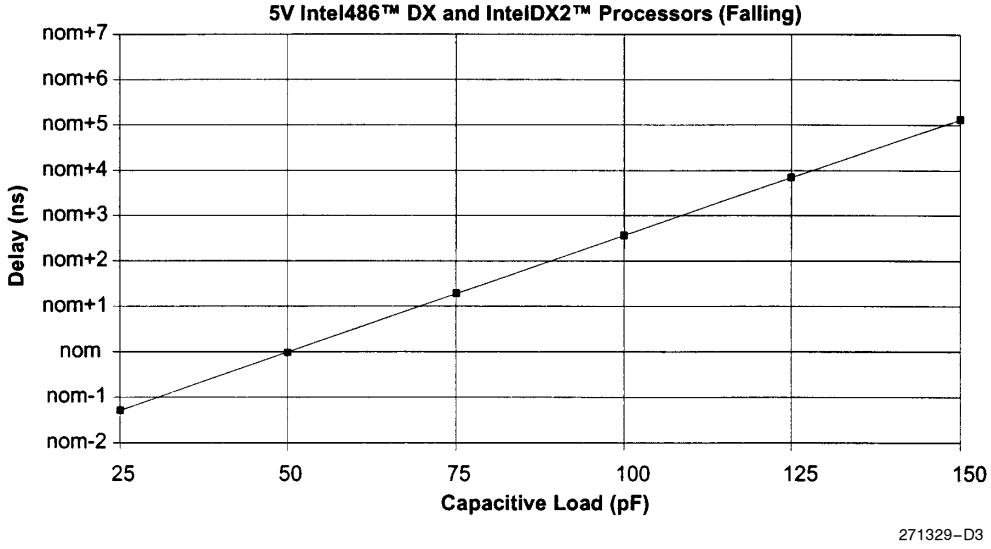
15.5 Capacitive Derating Curves

The capacitive derating curves illustrate output delay versus capacitive load for 5V Military Intel486 processors. The derating curves show the delays for the rising and falling edges under worst-case conditions. Figure 15-9 and Figure 15-10 apply to 5V Military Intel486 DX and IntelDX2 processors. Figures 15-11, 15-12 and 15-13 apply to the IntelDX4 processor. The figures apply to all frequencies specified for each corresponding product. Refer to Appendix B for bus frequencies above 33 MHz for Military Intel486 processors.



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 15-9. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 15-10. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition

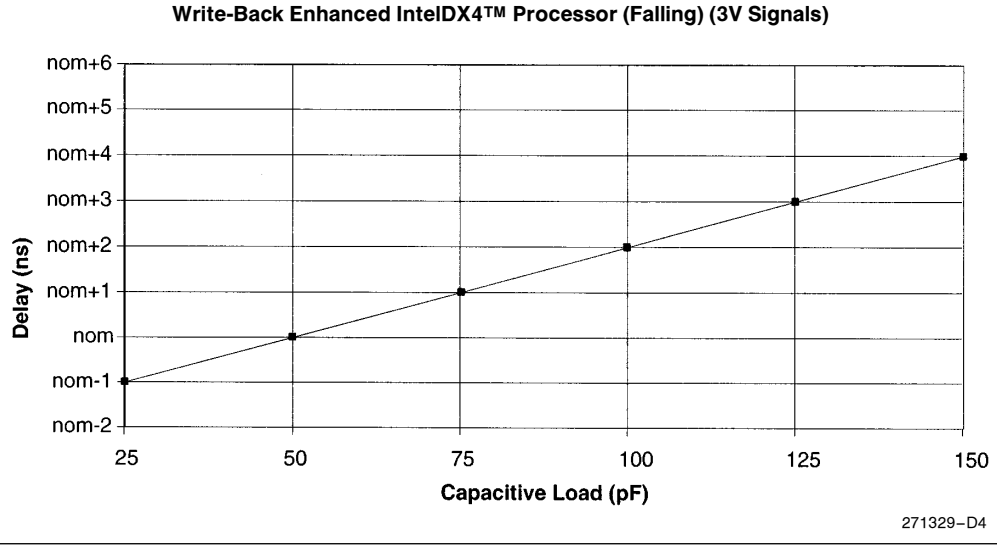


Figure 15-11. Write-Back Enhanced IntelDX4™ Processor (Falling) (3V Signals)

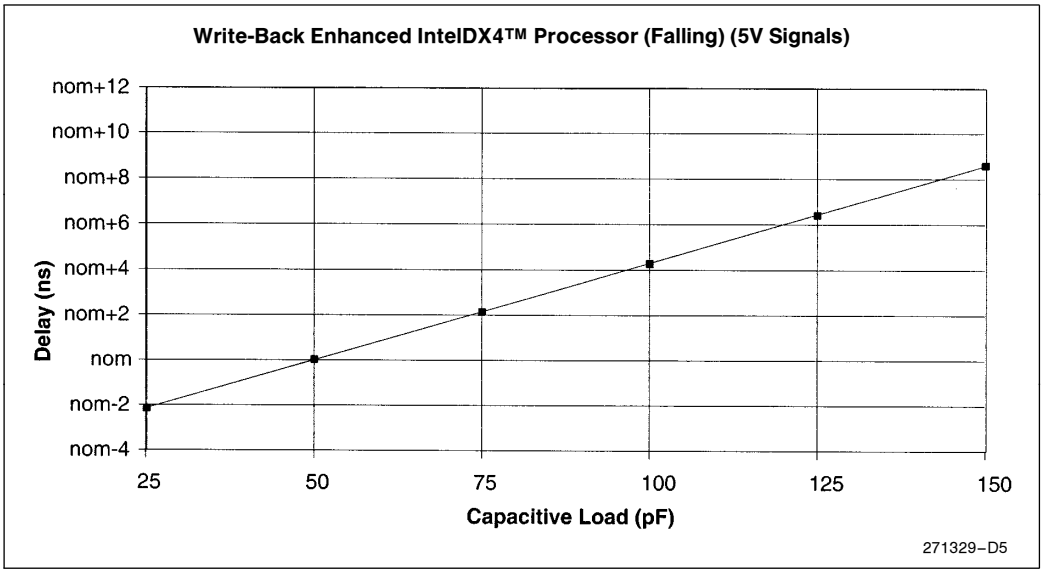


Figure 15-12. Write-Back Enhanced IntelDX4™ Processor (Falling) (5V Signals)

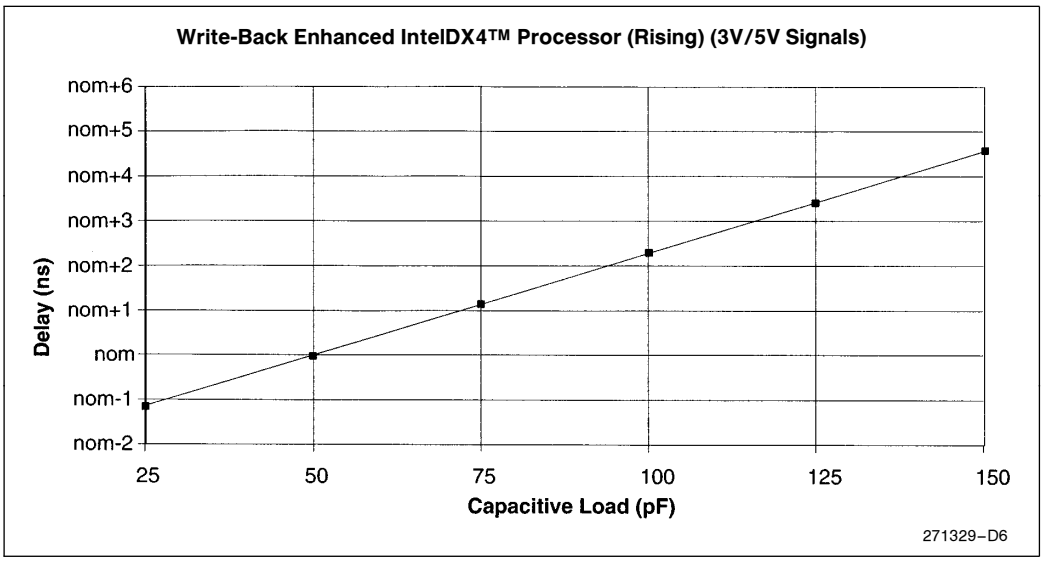


Figure 15-13. Write-Back Enhanced IntelDX4™ Processor (Rising) (3V/5V Signals)

16.0 MECHANICAL DATA

This section describes the package dimensions and thermal specifications for all processors in the Military Intel486 processor family.

NOTE:
For further details about thermal and mechanical package specifications and methodologies, refer to the 1994 Packaging Handbook (order number 240800).

16.1 Military Intel486 Processor Package Dimensions

The processor dimensions are listed in the following order:

- 168-pin PGA package;
- 196-lead PQFP package.

16.1.1 168-PIN PGA PACKAGE

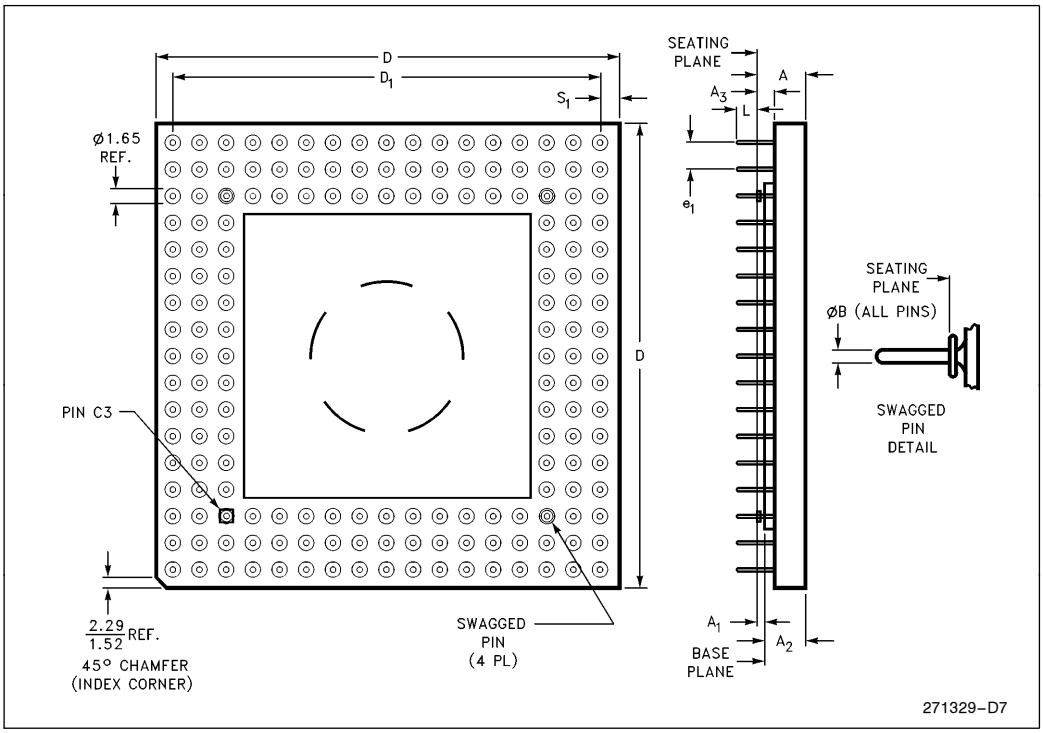


Figure 16-1. 168-Pin Ceramic PGA Package Dimensions

Table 16-1. 168-Pin Ceramic PGA Package Dimensions

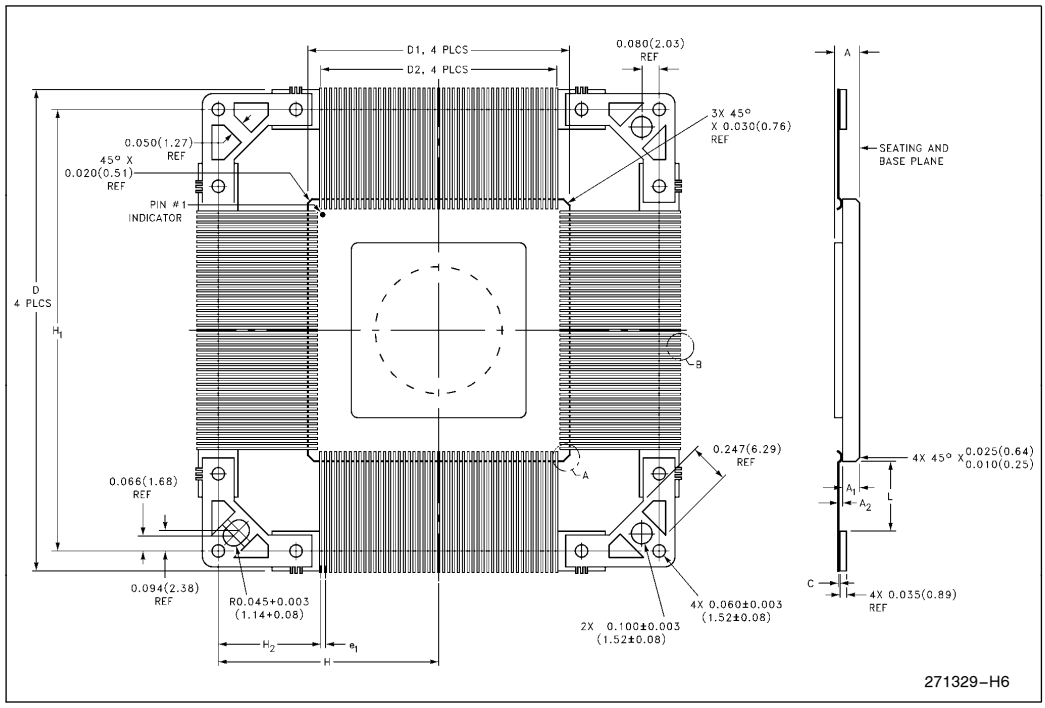
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	SOLID LID	0.025	0.045	SOLID LID
A_2	2.8	3.5	SOLID LID	0.110	0.140	SOLID LID
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168			168		
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS REV X 7/15/88					

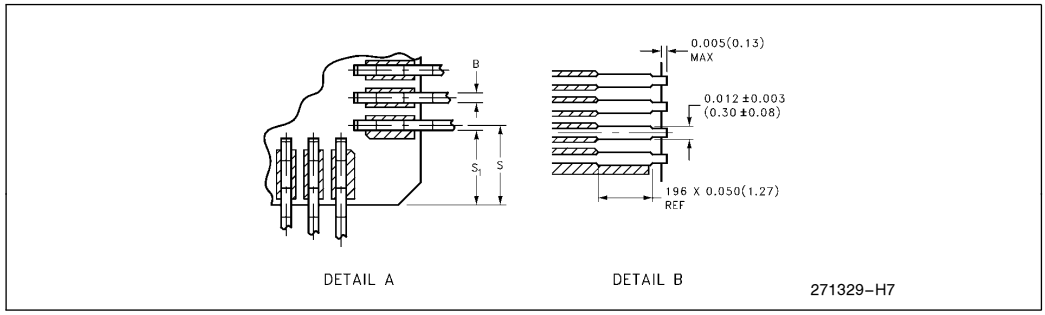
Table 16-2. Ceramic PGA Package Dimension Symbols

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane (lid)
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension ''e_1'' (''e'') is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions ''B'', ''B_1'' and ''C'' are nominal.
5. Details of Pin 1 identifier are optional.

196L CERAMIC QUADPACK PACKAGE INTEL TYPE Q CAVITY UP, WITH N/C TIE BAR





196L CERAMIC QUADPACK PACKAGE INTEL TYPE Q CAVITY UP, WITH N/C TIE BAR (Continued)

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A_1	1.96	2.39		0.077	0.094	
A_2	0.15	0.30		0.006	0.012	
B	0.20	0.25		0.008	0.010	
C	0.10	0.20		0.004	0.008	
D	62.99	64.01		2.480	2.520	
D_1	33.65	34.16		1.325	1.345	
D_2	30.48 Basic			1.200 Basic		
e_1	0.58	0.69		0.023	0.027	
H	29.21 Basic			1.150 Basic		
H_1	58.42 Basic			2.30 Basic		
H_2	13.97 Basic			0.550 Basic		
L	9.27	10.03		0.365	0.395	
N	196			196		
S	1.27	2.03	Reference	0.050	0.080	Reference
S_1	1.14	1.93	Reference	0.045	0.076	Reference
ISSUE	IWS 7/90					

16.2 Package Thermal Specifications

The Military Intel486 processors are specified for operation when T_C (the case temperature) is within the range of −55°C to +125°C. T_C may be measured in any environment to determine whether the Military Intel486 processor is within the specified operating range. The case temperature, with and without heat sink should be measured using a 0.005″ diameter (AWG#36) thermocouple with a 90° angle adhesive bond at the center of the package top surface, opposite the pins. Figure 16-2 and Figure 16-3 illustrate this methodology.

The ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} from the following equations.

$$T_J = T_C + P * \theta_{JC}$$
$$T_A = T_J - P * \theta_{JA}$$
$$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$$

Where:

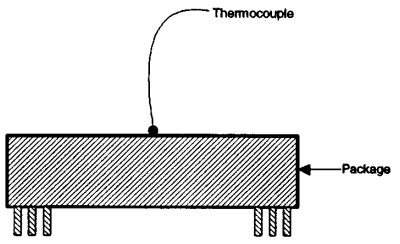
T_J, T_A, T_C = Junction, Ambient and Case Temperature, respectively.

θ_{JC}, θ_{JA} = Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively.

P = Maximum Power Consumption

The values for θ_{JA} and θ_{JC} are given below for the packaging and operating frequencies.

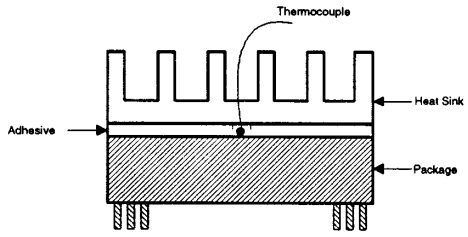
Note that T_A is greatly improved by attaching ''fins'' or a ''heat sink'' to the package. P (the maximum power consumption) is calculated by using the maximum I_{CC} at nominal V_{CC} (either 3.3V or 5V) as tabulated in the DC Charisteristics in section 15.



271329–D8

0.005″ diam. thermocouple on the center of the package top surface with a 90° angle adhesive bond

Figure 16-2. Case Temperature Measurement without Heat Sink

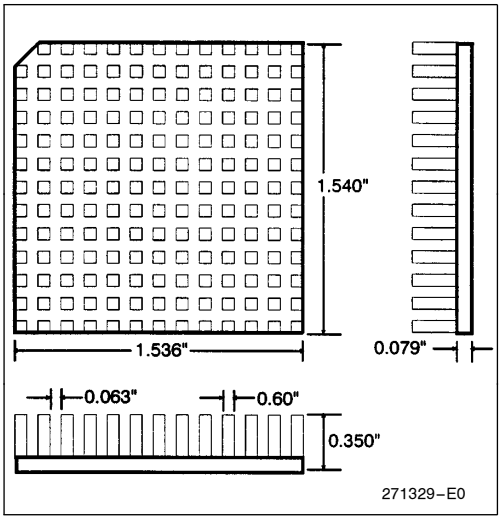


271329–D9

0.005″ diam. thermocouple on the center of the package top surface with a 90° angle adhesive bond through a hole drilled at the heat sink base

Figure 16-3. Case Temperature Measurement with Heat Sink

16.2.1 168-PIN PGA PACKAGE THERMAL CHARACTERISTICS FOR 3.3V IntelDX4 PROCESSOR



271329–E0

Figure 16-4. Sample IntelDX4™ Processor PGA Heat Sink

Table 16-3. PGA Package Thermal Resistance (°C/W)–θ_{JC} and θ_{JA} for IntelDX4™ Processor

		θ_{JA} vs Airflow—ft/min (m/sec)					
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
With Heat Sink*	2	13.5	8.5	6.5	5.5	4.5	4.25
Without Heat Sink	2	17.5	15	13	11.5	10.0	9.5

*0.350″ high omnidirectional heat sink.

Table 16-4. PGA Package Maximum Ambient Temperature for IntelDX4™ Processor

		Airflow—ft/min (m/sec)			
	Freq. (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
$T_{ambient}$ °C with Heat Sink*	100	35.5	57	65.5	70
$T_{ambient}$ °C without Heat Sink	100	18.5	29	37.5	44

*0.350″ high omnidirectional heat sink.

16.2.2 168-Pin PGA Package Thermal Characteristics for 5V Military Intel486 Processors

Table 16-5. Thermal Resistance (°C/W) θ_{JC} and θ_{JA} for the 168-Pin PGA Package of the Military Intel486™ Processor

		θ_{JA} vs. Airflow—ft/min. (m/sec)					
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
With Heat Sink*	1.5	13	8.0	6.0	5.0	4.5	4.25
Without Heat Sink	1.5	17	14.5	12.5	11.0	10.0	9.5

*0.350″ high omnidirectional heat sink.

16.2.3 Thermal Specifications for 196-Lead CQFP Package

Table 16-6. Thermal Resistance (°C/W) °JC and °JA

		θ_{JA} vs Airflow—ft/min (m/sec)			
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
With Heat Sink*	2.5	17.0	10.5	8.5	8.0
Without Heat Sink	2.5	20.5	16.5	14.0	12.5

*0.350″ high omnidirectional heat sink.

APPENDIX A
FEATURE DETERMINATION

CPUID Instruction

The Military Intel486 processor implements the CPUID instruction that makes information available to the system software about the family, model, and stepping of the processor on which it is executing. Support of this instruction is indicated by the ability of system software to write and read the bit in position EFLAGS.21, referred to as the EFLAGS.ID bit. The actual state of the EFLAGS.ID bit is irrelevant and provides no significance to the hardware. This bit is reset to zero upon device reset (RESET and SRESET) for compatibility with older Military Intel486 processor designs.

Operation

The CPUID instruction requires the software developer to pass an input parameter to the processor in the EAX register. The processor response is returned in registers EAX, EBX, ECX, and EDX.

1. When the parameter passed to EAX is zero, the register values returned upon instruction execution are:

   EAX[31:0] ← 1

   EBX[31:0] ← 756E6547—''Genu'', with ''G'' in the low nibble of BL

   EDX[31:0] ← 49656E69—''inel'', with ''i' in the low nibble of DL

   ECX[31:0] ← 6C65746E—''ntel'', with ''n'' in the low nibble of CL

   The values in EBX, ECX, and EDX indicate an Intel processor. When taken in the proper order, they decode to the string ''GenuineIntel.''

2. When the parameter passed to EAX is one, the register values returned upon instruction execution are:

   EAX[3:0] ← xxxx—Stepping ID

   EAX[7:4] ← xxxx—Model

   EAX[11:8] ← 0100—Family

   EAX[15:12] ← 0000

   EAX[31:16] ← Intel Reserved

   EBX[31:0] ← 00000000

   ECX[31:0] ← 00000000

   EDX[0:0] ← 1—FPU on-chip

   EDX[3:1] ← 1

   EDX[31:4] ← Intel Reserved

   The value returned in EAX after CPUID instruction execution is identical to the value loaded into EDX upon device reset. Software must avoid any dependency upon the state of reserved processor bits.

3. When the parameter in EAX is greater than one, the register values returned upon instruction execution are:

   EAX[31:0] ← 00000000

   EBX[31:0] ← 00000000

   EDX[31:0] ← 00000000

   ECX[31:0] ← 00000000

Flags Affected

No flags are affected.

Exceptions

None.

For More Information

Refer to the Intel application note AP-485, *Intel Processor Identification with the CPUID Instruction* for more details.

Table A-1. CPUID Instruction Description

OPCODE	Instruction	Processor Core Clocks	EAX Input Value	Description
0F A2	CPUID	14 9	1 0 or greater than 1	Processor Identification Intel String/Null Registers

APPENDIX B
I/O BUFFER MODELS

For processor bus speeds above 33 MHz (e.g., 50 MHz), the capacitive derating curves are not guaranteed. For bus speeds of 50 MHz, I/O buffer modeling techniques should be used to accurately simulate (and predict) the behavior of processor signals in a particular environment.

This appendix presents a sample I/O buffer model parameters for the IntelDX4 processor. The first section presents an overview of signal buffer type catagorization. The second section presents a graphical representation of IBIS (I/O Buffer Information Sheet) data for each of the input, input/output, and output buffers types on the processor. The third section provides a text listing of the data presented in the IBIS format.

I/O buffer model information is available for all Military Intel486 processors described in this datasheet. Contact your Intel representative for the latest I/O buffer models for the IntelDX4 and other members of the Military Intel486 processor family.

I/O Buffer Models for IntelDX4 Processor

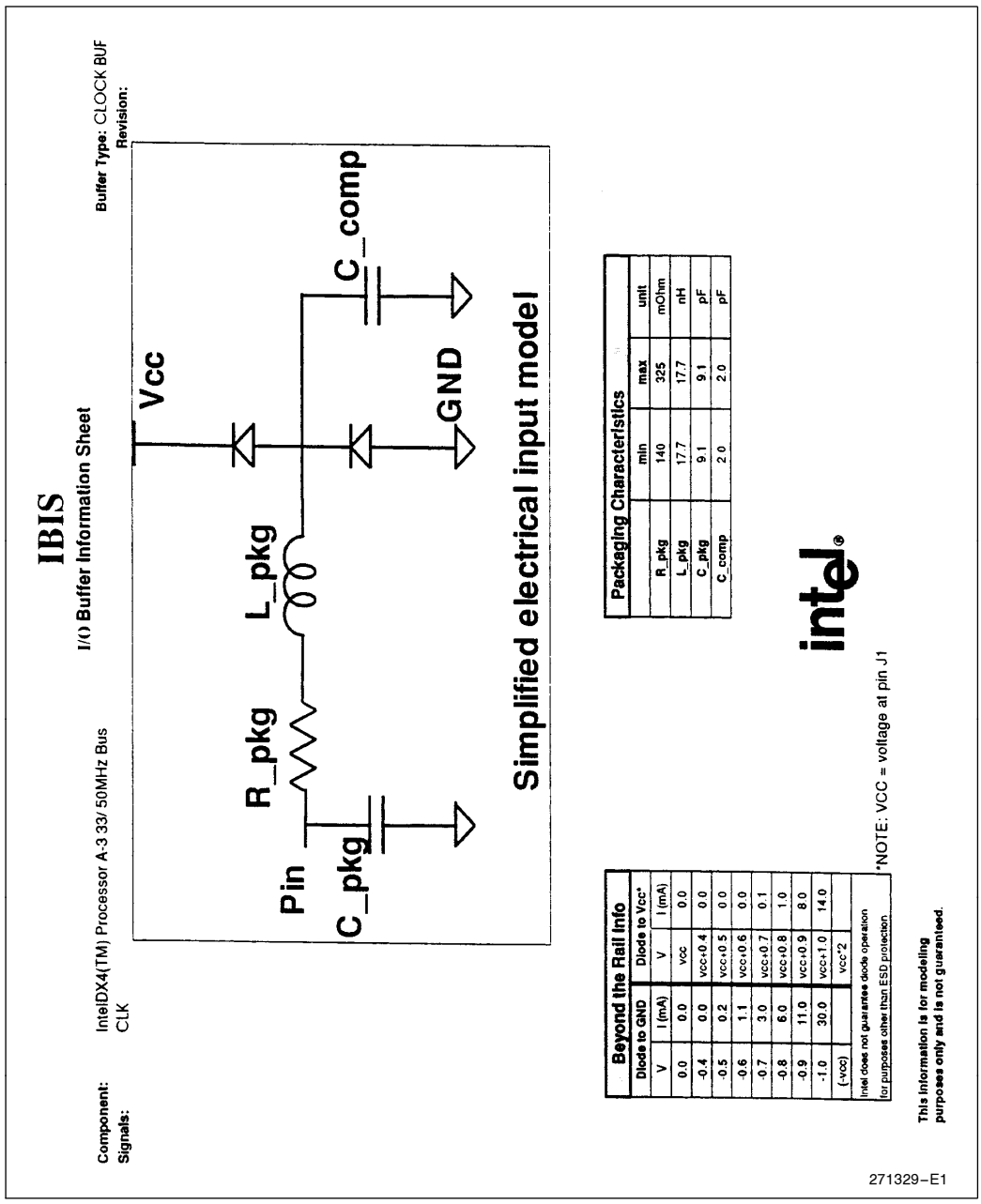
Each valid delay for the 50-MHz bus is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal delays due to loading. Table B-1 lists the buffer type to be used for each signal in the external interface.

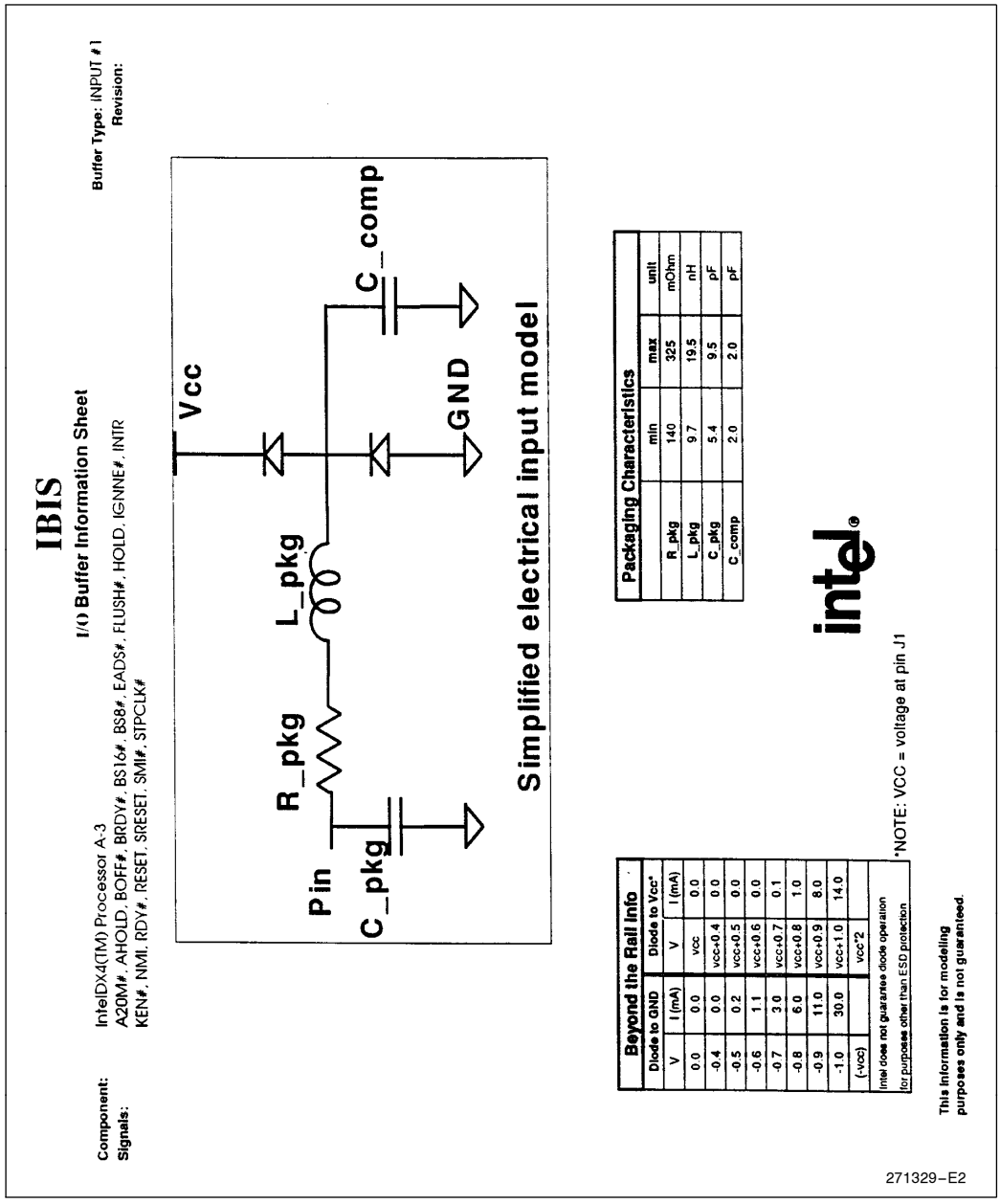
Table B-1. External Interface Signal Buffer Assignment

Device	Signals	Type	Drive Buffer TYPE	Receiver Buffer Type
IntelDX4™ Processor	A20M#, AHOLD, BOFF#, BRDY#, BS8# BS16#, FLUSH#, HOLD, IGNNE#, INTR, KEN#, NMI, RDY#, RESET#, EADS#, SMI#, STPCLK#, SRESET, CLKMUL	I	N/A	IN1
	CLK	I	N/A	CLK
	D16–D0, DP2–DP0	I/O	I/O1	IN1
	D31–D17, DP3	I/O	I/O2	IN1
	A31–A4	I/O	I/O3	IN1
	ADS#, BLAST#, LOCK#, PLOCK#, SMIACT#, A3–A2, FERR#, HLDA	O	O1	N/A
	BE3#–BE0#, BREQ#, D/C#, M/IO#, PCD, PWT, PCHK#, W/R#	O	O2	N/A

Sample IBIS Files for IntelDX4 Processor

The following pages present sample IBIS file outputs for the IntelDX4 processor.


IBIS
I/O Buffer Information Sheet
Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: CLK
Buffer Type: CLOCK BUF
Revision:
Vcc
R_pkg
L_pkg
C_comp
Pin
C_pkg
GND
Simplified electrical input model
Beyond the Rail Info
Diode to GND
Diode to Vcc*
V
I (mA)
V
I (mA)
0.0 0.0 vcc 0.0
-0.4 0.0 vcc+0.4 0.0
-0.5 0.2 vcc+0.5 0.0
-0.6 1.1 vcc+0.6 0.0
-0.7 3.0 vcc+0.7 0.1
-0.8 6.0 vcc+0.8 1.0
-0.9 11.0 vcc+0.9 8.0
-1.0 30.0 vcc+1.0 14.0
(-vcc) vcc*2
Intel does not guarantee diode operation for purposes other than ESD protection
*NOTE: VCC = voltage at pin J1
Packaging Characteristics
min max unit
R_pkg 140 325 mOhm
L_pkg 17.7 17.7 nH
C_pkg 9.1 9.1 pF
C_comp 2.0 2.0 pF
This information is for modeling purposes only and is not guaranteed.
271329–E1

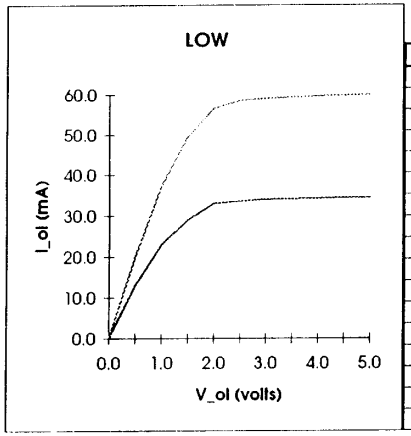

IBIS
I/O Buffer Information Sheet
Component: IntelDX4(TM) Processor A-3
Signals: A20M#, AHOLD, BOFF#, BRDY#, BS16#, BS8#, EADS#, FLUSH#, HOLD, IGNNE#, INTR
KEN#, NMI, RDY#, RESET, SRESET, SMI#, STPCLK#
Buffer Type: INPUT #1
Revision:
Vcc
R_pkg
L_pkg
C_comp
Pin
C_pkg
GND
Simplified electrical input model
Beyond the Rail Info
Diode to GND
V
I (mA)
0.0
0.0
-0.4
0.0
-0.5
0.2
-0.6
1.1
-0.7
3.0
-0.8
6.0
-0.9
11.0
-1.0
30.0
(-vcc)
Diode to Vcc*
V
I (mA)
vcc
0.0
vcc+0.4
0.0
vcc+0.5
0.0
vcc+0.6
0.0
vcc+0.7
0.1
vcc+0.8
1.0
vcc+0.9
8.0
vcc+1.0
14.0
vcc*2
Intel does not guarantee diode operation for purposes other than ESD protection
*NOTE: VCC = voltage at pin J1
Packaging Characteristics
min
max
unit
R_pkg
140
325
mOhm
L_pkg
9.7
19.5
nH
C_pkg
5.4
9.5
pF
C_comp
2.0
2.0
pF
This information is for modeling purposes only and is not guaranteed.
271329-E2

IBIS

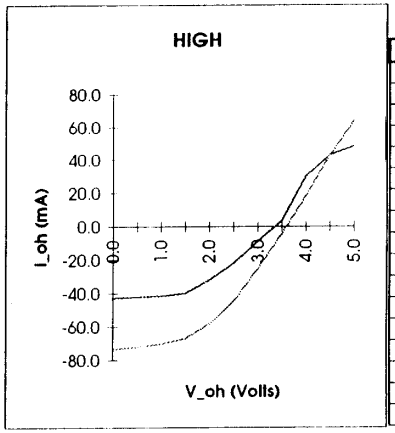
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/50MHz Bus
Signals: ADS#, BLAST#, SMIACT#, A<3:2>, FERR#, HLDA, PLOCK#, LOCK#

Buffer Type: OUT GROUP #1
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	-472.0	-370.0
-1.0	-46.7	-57.1	-51.0
-0.5	-8.9	20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
-5.0	-1050.0	-1880.0	-1410.0
-1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	9.5	15.1	nH
C_pkg	5.6	9.7	pF
C_comp	2.9	3.2	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

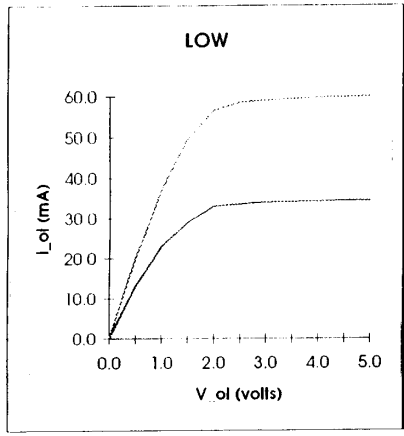
271329-E3

IBIS

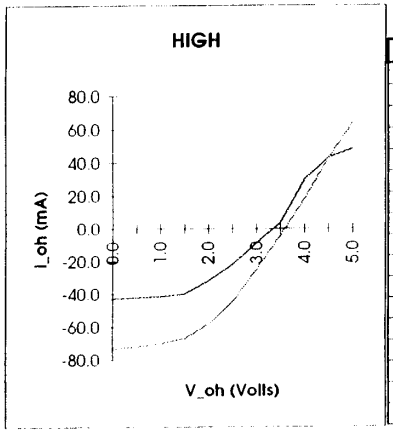
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: BE<3:0>#, BREQ, D/C#, M/IO#, PWT, PCD, PCHK#, W/R#

Buffer Type: OUT GROUP #2
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	472.0	-370.0
-1.0	-46.7	57.1	-51.0
-0.5	-8.9	20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
-5.0	-1050.0	-1880.0	-1410.0
-1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

Packaging Characteristics

	min	max	unit
R_pkg	140	325	mOhm
L_pkg	8.5	20.4	nH
C_pkg	5.2	11.0	pF
C_comp	2.7	2.7	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

*NOTE: VCC = voltage at pin J1

271329-E4

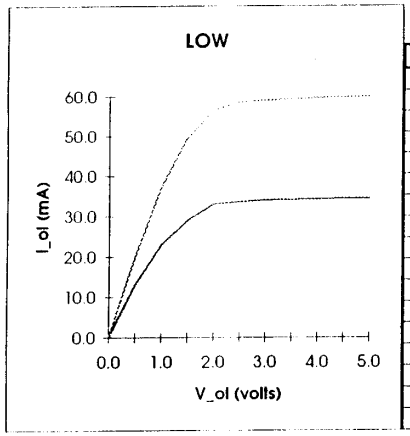
This information is for modeling purposes only and is not guaranteed.

IBIS

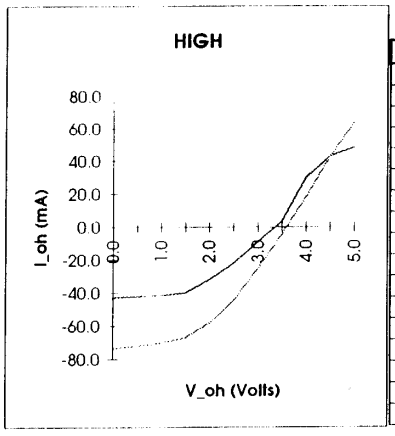
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 step 33/50MHz
Signals: DBUS<16:0>, DP<2:0>

Buffer Type: I/O GROUP #1
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	279.0	472.0	370.0
-1.0	-46.7	57.1	51.0
0.5	-8.9	20.7	13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
-5.0	-1050.0	-1880.0	-1410.0
-1.0	66.7	95.2	79.8
0.0	43.0	73.5	47.1
0.5	42.0	72.1	46.1
1.0	41.5	70.2	44.8
1.5	40.0	67.1	42.1
2.0	32.0	58.5	35.1
2.5	22.0	44.9	24.1
3.0	-9.0	25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-vcc)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	9.1	15.0	nH
C_pkg	4.8	6.5	pF
C_comp	2.7	2.7	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

*NOTE: VCC = voltage at pin J1

This information is for modeling purposes only and is not guaranteed.

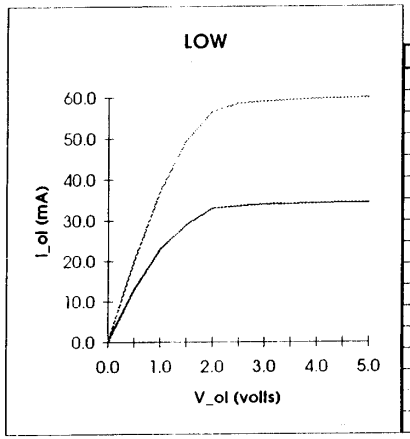
271329-E5

IBIS

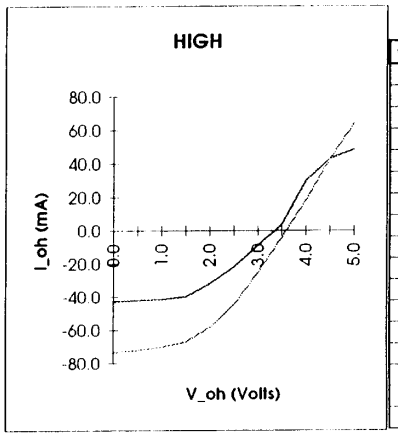
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: DBUS<31:17>, DP<3>

Buffer Type: I/O GROUP #1
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
-5.0	-1000	-1830	-1380
-2.0	-279.0	-472.0	-370.0
-1.0	-46.7	-57.1	-51.0
0.5	-8.9	-20.7	-13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
5.0	-1050.0	-1880.0	-1410.0
1.0	-66.7	-95.2	-79.8
0.0	-43.0	-73.5	-47.1
0.5	-42.0	-72.1	-46.1
1.0	-41.5	-70.2	-44.8
1.5	-40.0	-67.1	-42.1
2.0	-32.0	-58.5	-35.1
2.5	-22.0	-44.9	-24.1
3.0	-9.0	-25.2	-9.5
3.5	3.4	-4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
-0.4	0.0	vcc+0.4	0.0
-0.5	0.2	vcc+0.5	0.0
-0.6	1.1	vcc+0.6	0.0
-0.7	3.0	vcc+0.7	0.1
-0.8	6.0	vcc+0.8	1.0
-0.9	11.0	vcc+0.9	8.0
-1.0	30.0	vcc+1.0	14.0
(-VCC)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

*NOTE: VCC = voltage at pin J1

Packaging Characteristics

	min	max	unit
R_pkg	140.0	325.0	mOhm
L_pkg	8.5	13.7	nH
C_pkg	4.0	6.3	pF
C_comp	2.9	3.2	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

271329-E6

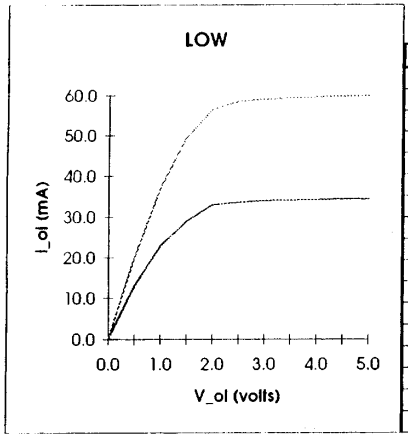
This information is for modeling purposes only and is not guaranteed.

IBIS

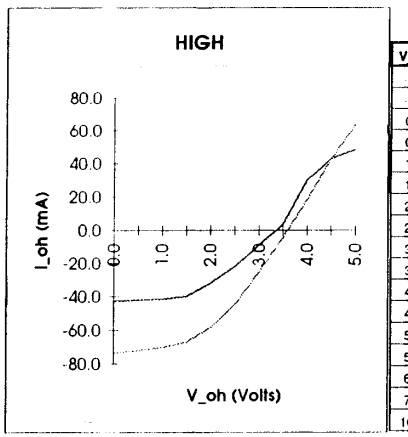
I/O Buffer Information Sheet

Component: IntelDX4(TM) Processor A-3 33/ 50MHz Bus
Signals: ABUS<31:4>

Buffer Type: I/O GROUP #3
Revision:



V_ol	I_ol min	I_ol max	I_ol typ
.5.0	-1000	-1830	-1380
2.0	279.0	472.0	370.0
1.0	46.7	57.1	51.0
0.5	8.9	20.7	13.5
0.0	0.0	0.0	0.0
0.5	13.0	20.1	12.9
1.0	23.0	37.2	23.7
1.5	29.0	49.7	31.5
2.0	33.0	56.6	35.4
2.5	33.5	58.6	36.3
3.0	34.0	59.0	36.6
3.5	34.1	59.4	36.9
4.0	34.2	59.7	37.0
4.5	34.4	59.8	37.1
5.0	34.4	60.0	37.2
6.0	34.4	60.0	37.2
10.0	34.4	60.0	37.2



V_oh	I_oh min	I_oh max	I_oh typ
5.0	-1050.0	1880.0	-1410.0
1.0	66.7	95.2	79.8
0.0	43.0	73.5	47.1
0.5	42.0	72.1	46.1
1.0	41.5	70.2	44.8
1.5	40.0	67.1	42.1
2.0	32.0	58.5	35.1
2.5	22.0	44.9	24.1
3.0	9.0	25.2	9.5
3.5	3.4	4.6	6.5
4.0	30.0	18.1	24.3
4.5	43.0	43.0	41.7
5.0	48.5	64.0	56.4
5.5	55.4	80.9	67.3
6.0	59.3	93.4	74.6
7.0	62.2	104.0	79.8
10.0	63.7	109.0	82.4

Beyond The Rail Info

Diode to GND		Diode to Vcc*	
V	I (mA)	V	I (mA)
0.0	0.0	vcc	0.0
0.4	0.0	vcc+0.4	0.0
0.5	0.2	vcc+0.5	0.0
0.6	1.1	vcc+0.6	0.0
0.7	3.0	vcc+0.7	0.1
0.8	6.0	vcc+0.8	1.0
0.9	11.0	vcc+0.9	8.0
1.0	30.0	vcc+1.0	14.0
(-VCC)		vcc*2	

Intel does not guarantee diode operation for purposes other than ESD protection

*NOTE: VCC = voltage at pin J1

Packaging Characteristics

	min	max	unit
R_pkg	140	325	mOhm
L_pkg	7.9	14.7	nH
C_pkg	4.4	7.4	pF
C_comp	2.9	2.9	pF

Ramp Rate (into 0pF, no pkg)

	min	max	typ	unit
Rise	1.51	1.91	1.7	volts/ns
Fall	1.72	2.43	2.07	volts/ns

Simplified Output Resistance

	min	max	unit
Low	27.4	113.6	ohms
High	25.2	63.1	ohms

Simplified Output Resistance calculated using a 50 ohm load line

271329-E7

This information is for modeling purposes only and is not guaranteed.

Sample Text Listing of IBIS Files for IntelDX4 Processor

```
|**************************************************************************
|
[IBIS Ver]     1.1
[File name]    inteldx4pg.ibs
[File Rev]     2.0
[Date]         3/23/94
[Source]       File originated at Intel Corporation
[Notes]        The following information corresponds to the INTELDX4(TM)
|              processor and has been correlated with silicon.  This file
               is for the PGA package only.IntelDX4 processor
[Disclaimer]   This information is for modeling purposes only, and is not
|              guaranteed.
|
|**************************************************************************
|
|
[Component]      INTELDX4 PROCESSOR
[Manufacturer]   Intel
[Package]
|
|     typ   min         max
R_pkg       2329m 728m  3930m
L_pkg       17.79nH     8.56nH      27.01nH
C_pkg       6.03pF      1.89pF      10.16pF
|
|
|**************************************************************************
|
[Pin]    signal_name      model_name   R_pin    L_pin    C_pin
 A01     D20                 I/O2         1866m    15.54n    3.88p
 A02     D22                 I/O2         1808m    13.70n    5.60p
 A04     D23                 I/O2         1468m    13.33n    3.14p
 A05     DP3                 I/O2         1406m    11.59n    4.50p
 A06     D24                 I/O2         1412m    13.02n    3.04p
 A08     D29                 I/O2         1274m    10.90n    4.14p
 A15     IGNNE#              Input1       1858m    13.96n    5.74p
 A16     INTR                Input1       1956m    14.47n    6.00p
 A17     AHOLD               Input1       3414m    22.11n    9.99p
 B01     D19                 I/O2         1762m    13.46n    5.47p
 B02     D21                 I/O2         1636m    14.27n    3.45p
 B06     D25                 I/O2         1178m    11.72n    2.61p
 B08     D31                 I/O2         1050m     9.73n    3.52p
 B10     SMI#                Input1       948m     10.45n    2.19p
 B15     NMI                 Input1       1430m    13.12n    3.07p
 B17     EADS#               Input1       1728m    14.78n    3.62p
 C01     D11                 I/O1         2440m    18.73n    4.93p
 C02     D18                 I/O2         1446m    13.21n    3.10p
 C03     CLK                 Clockbuffer  2486m    18.99n    5.02p
 C06     D27                 I/O2         964m     10.54n    2.21p
 C07     D26                 I/O2         892m     8.90n     3.09p
 C08     D28                 I/O2         752m     9.36n     1.82p
 C09     D30                 I/O2         728m     9.22n     1.78p
 C10     SRESET              Input1       784m     9.54n     1.88p
 C12     SMIACT#             Output1      1270m    12.23n    2.78p
```

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C14	FERR#	Output1	1904m	15.76n	3.95p
C15	FLUSH#	Input1	1342m	11.26n	4.32p
C16	RESET	Input1	1480m	11.98n	4.70p
C17	BS16#	Input1	2756m	20.49n	5.52p
D01	D9	I/O1	2718m	18.47n	8.09p
D02	D13	I/O1	2100m	16.84n	4.31p
D03	D17	I/O2	1156m	11.60n	2.57p
D15	A20M#	Input1	1148m	11.56n	2.55p
D16	BS8#	Input1	3474m	22.43n	10.16p
D17	BOFF#	Input1	3452m	22.31n	10.10p
E03	D10	I/O1	2356m	16.57n	7.10p
E15	HOLD	Input1	1920m	15.85n	3.98p
F01	DP1	I/O1	2394m	16.77n	7.20p
F02	D8	I/O1	1864m	15.53n	3.87p
F03	D15	I/O1	858m	9.95n	2.02p
F15	KEN#	Input1	2404m	16.82n	7.23p
F16	RDY#	Input1	1804m	15.20n	3.76p
F17	BE3#	Output2	3336m	23.71n	6.58p
G03	D12	I/O1	1912m	14.24n	5.88p
G15	STPCLK#	Input1	3930m	27.01n	7.68p
H02	D3	I/O1	1708m	14.67n	3.59p
H03	DP2	I/O1	928m	9.09n	3.19p
H15	BRDY#	Input1	2134m	17.03n	4.37p
J02	D5	I/O1	1528m	13.67n	3.25p
J03	D16	I/O1	1614m	14.14n	3.41p
J15	BE2#	Output2	848m	8.67n	2.97p
J16	BE1#	Output2	1002m	10.75n	2.28p
J17	PCD	Output2	2266m	17.77n	4.61p
K03	D14	I/O1	1160m	10.30n	3.83p
K15	BE0#	Output2	954m	9.22n	3.26p
L02	D6	I/O1	1432m	11.73n	4.57p
L03	D7	I/O1	1048m	11.00n	2.37p
L15	PWT	Output2	1548m	12.34n	4.89p
M03	D4	I/O1	1000m	9.47n	3.39p
M15	D/C#	Output2	1442m	13.19n	3.10p
N01	D2	I/O1	1448m	11.81n	4.61p
N02	D1	I/O1	1198m	11.84n	2.65p
N03	DP0	I/O1	1038m	10.95n	2.35p
N15	LOCK#	Output1	1118m	10.09n	3.71p
N16	M/IO#	Output2	1744m	14.87n	3.65p
N17	W/R#	Output2	1676m	13.01n	5.24p
P01	D0	I/O1	1532m	12.25n	4.84p
P02	A29	I/O3	1292m	12.36n	2.82p
P03	A30	I/O3	1194m	10.48n	3.92p
P15	HLDA	Output1	1568m	13.89n	3.33p
Q01	A31	I/O3	1608m	14.11n	3.40p
Q03	A17	I/O3	2016m	16.38n	4.15p
Q04	A19	I/O3	1584m	12.53n	4.99p
Q05	A21	I/O3	956m	10.49n	2.20p
Q06	A24	I/O3	920m	9.05n	3.17p
Q07	A22	I/O3	894m	8.91n	3.10p
Q08	A20	I/O3	788m	9.56n	1.89p
Q09	A16	I/O3	850m	8.68n	2.98p
Q10	A13	I/O3	836m	9.82n	1.98p
Q11	A9	I/O3	914m	9.02n	3.15p
Q12	A5	I/O3	966m	9.29n	3.29p

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```
 Q13    A7                  I/O3         1084m   11.20n   2.44p
 Q14    A2                  Output1      1134m   11.48n   2.53p
 Q15    BREQ                Output2      1872m   15.58n   3.89p
 Q16    PLOCK#              Output1      1630m   14.23n   3.44p
 Q17    PCHK#               Output2      1616m   12.69n   5.07p
 R01    A28                 I/O3         1708m   14.67n   3.59p
 R02    A25                 I/O3         1604m   12.63n   5.04p
 R05    A18                 I/O3         1498m   13.50n   3.20p
 R07    A15                 I/O3         1148m   11.56n   2.55p
 R12    A11                 I/O3         1274m   10.90n   4.14p
 R13    A8                  I/O3         1252m   12.13n   2.75p
 R15    A3                  Output1      1504m   12.11n   4.77p
 R16    BLAST#              Output1      1698m   14.61n   3.57p
 S01    A27                 I/O3         1900m   14.18n   5.85p
 S02    A26                 I/O3         1800m   15.18n   3.75p
 S03    A23                 I/O3         1756m   14.93n   3.67p
 S05    A14                 I/O3         1842m   13.88n   5.69p
 S07    A12                 I/O3         1530m   12.24n   4.84p
 S13    A10                 I/O3         1444m   13.20n   3.10p
 S15    A6                  I/O3         1722m   13.25n   5.36p
 S16    A4                  I/O3         1792m   15.13n   3.74p
 S17    ADS#                Output1      1888m   14.12n   5.82p
|
|*******************************************************************************
|
[Model]  Output1
Model_type Output
Polarity Non-Inverting
Enable  Active-Low
|signals ADS#,BLAST#,SMIACT#,A<3:2>,FERR#,HLDA,PLOCK#,LOCK#
|
|          typ   min   max
C_comp     3.05pF  2.9pF   3.2pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*******************************************************************************
|
[Pulldown]
| voltage  I(typ)    I(min)    I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
```

271329-F0

```
|
|*************************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*************************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*************************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*************************************************************************
|
[POWER_clamp]
```

271329-F1

```
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*****************************************************************************
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*****************************************************************************
|
[Model]  Output2
Model_type Output
Polarity Non-Inverting
Enable  Active-Low
|signal  BE<3:0>#,BREQ,D/C#,M/IO#,PWT,PCD,PCHK#,W/R#
|
|          typ   min   max
C_comp     2.7pF      2.7pF      2.7pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*****************************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
```

271329-F2

```
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| Voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
```

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```
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O1
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|signal  DBUS<16:0>,DP<2:0>
|
|          typ   min   max
C_comp     2.7pF      2.7pF      2.7pF
[Voltage range] 3.3V  3.0V  3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
```

271329-F4

```
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
```

271329-F5

```
 -2.0V  100mA  NA  NA
|
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O2
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 3.3v
Vinh = 6.0v
|siganl  DBUS<31:17>,DP<3>
|
|  typ  min  max
C_comp  3.05pF  2.9pF  3.2pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
```

271329-F6

```
 3.3V   -47.1mA  -40.80mA -72.66mA
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*********************************************************************
|
```

271329-F7

```
[Ramp]
|  typ  min  max
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  I/O3
Model_type I/O
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|
|signal  ABUS<31:4>
|
|  typ min max
C_comp  2.9pF 2.9pF 2.9pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[Pulldown]
| voltage  I(typ)  I(min)  I(max)
 -5.0V   -960.0mA  -580.0mA  -1410mA
 -2.0V   -190.0mA  -99.0mA  -292.0mA
 -1.0V   -21.0mA  -16.7mA  -27.1mA
 -0.5V   -13.30mA  -8.7mA   -20.5mA
 0.0V   0.0   0.0   0.0
 0.5V   12.9mA   8.3mA   20.1mA
 1.0V   23.7mA   15.1mA   37.2mA
 1.5V   31.5mA   19.7mA   49.7mA
 2.0V   35.4mA   21.6mA   56.6mA
 2.5V   36.3mA   22.0mA   58.6mA
 3.0V   36.6mA   22.2mA   59.0mA
 3.5V   36.9mA   22.3mA   59.4mA
 4.0V   37.0mA   22.4mA   59.7mA
 4.5V   37.1mA   22.5mA   59.8mA
 5.0V   37.2mA   22.5mA   60.0mA
 6.0V   37.2mA   22.5mA   60.0mA
 10.0V   37.2mA   22.5mA   60.0mA
|
|*****************************************************************
| Note that the pullup voltage in the data table is derived from
| the equation:
|  Vtable = Vcc - Voutput
| For the 8.3V in the table, it is actually 8.3V below Vcc and -5V
| with respected to Ground.
|*****************************************************************
|
[Pullup]
| voltage  I(typ)  I(min)  I(max)
|
 8.3V   -1410mA  -976.25mA -1992.8mA
 4.3V  -79.8mA  -55.6mA  -229.06mA
 3.3V   -47.1mA  -40.80mA -72.66mA
```

271329-F8

```
 2.8V   -46.1mA  -29.42mA -70.96mA
 2.3V   -44.8mA  -28.64mA -68.34mA
 1.8V   -42.1mA  -27.14mA -61.94mA
 1.3V   -35.1mA  -23.34mA -50.34mA
 0.8V  -24.1mA  -16.08mA -33.08mA
 0.3V   -9.5mA   -6.3mA  -12.86mA
 -0.2V   6.5mA   4.76mA  9.02mA
 -0.7V   24.3mA   17.3mA  33.04mA
 -1.2V   41.7mA   30.48mA  55.6mA
 -1.7V   56.4mA   42.26mA  74.14mA
 -2.2V   67.3mA   51.26mA  88.4mA
 -2.7V   74.6mA   56.96mA  96.58mA
 -3.7V   79.8mA   61.33mA  104.5mA
 -6.7V   82.4mA   63.55mA  109.5mA
|
[GND_clamp]
|
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*********************************************************************
[Ramp]
|  typ  min  max
```

271329-F9

```
dV/dt_r  1.13/0.749n 0.93/0.868n 1.35/0.642n
dV/dt_f  0.99/0.447n 0.75/0.543n 1.27/0.387n
|
|*********************************************************************
|
[Model]  Input1
Model_type Input
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8v
Vinh = 2.0v
|signal  A20M#,AHOLD,BOFF#,BRDY#,BS16#,BS8#,FLUSH#,
|  HOLD,IGNNE#,INTR,KEN#,NMI,RDY#,RESET,SRESET,SMI#,STPCLK#
|  typ  min  max
C_comp  2.0pF  2.0pF  2.0pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*********************************************************************
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
|
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*********************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*********************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
```

271329-G0

```
|
|*****************************************************************************
|
[Model]  Clockbuffer
Model_type Input
Polarity Non-Inverting
Enable  Active-Low
Vinl = 0.8V
Vinh = 2.0V
|signal  CLK
|  typ  min  max
C_comp  2.0pF  2.0pF  2.0pF
[Voltage range]  3.3V 3.0V 3.6V
|
|*****************************************************************************
|
[GND_clamp]
| Voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  -0.2mA  NA  NA
 -0.6V  -1.1mA  NA  NA
 -0.7V  -3.0mA  NA  NA
 -0.8V  -6.0mA  NA  NA
 -0.9V  -11.0mA  NA  NA
 -1.0V  -30.0mA  NA  NA
 -1.2V  -120.0mA NA  NA
 -2.0V  -180.0mA NA  NA
 -5.0V  -420.0mA NA  NA
|
|*****************************************************************************
|  The data in the following POWER_clamp table is listed
| as "Vcc-relative", meaning that the voltage values are
| referenced to the Vcc pin.  The voltages in the data tables
|  are derived from the equation:
|   Vtable = Vcc - Voutput
| In this case, assuming that Vcc  is referenced to 3.3V.
| 0V in the table actually means 3.3V with respected to
| Ground and 0V above Vcc.
|*****************************************************************************
|
[POWER_clamp]
| voltage  I(typ)  I(min)  I(max)
 0.0V  0mA  NA  NA
 -0.4V  0mA  NA  NA
 -0.5V  0mA  NA  NA
 -0.6V  0mA  NA  NA
 -0.7V  0.1mA  NA  NA
 -0.8V  1.0mA  NA  NA
 -0.9V  8.0mA  NA  NA
 -1.0V  14.0mA  NA  NA
 -2.0V  100mA  NA  NA
|
|*****************************************************************************
|
[End]
```

271329-G1

APPENDIX C
BSDL LISTINGS

Below is a listing of a boundary scan description language (BSDL) file for the IntelDX4 processor.

This file is provided as an example. Contact Intel for design information for this and other Military Intel486 processors. See section 11.5, "Military Intel486 Processor Boundary Scan," for a complete description of BSDL instructions and usage.

IntelDX4 Processor Listing

```
-- Copyright Intel Corporation 1993
--*************************************************************************
-- Intel Corporation makes no warranty for the use of its products
-- and assumes no responsibility for any errors which may appear in
-- this document nor does it make a commitment to update the information
-- contained herein.
--*************************************************************************
-- Boundary-Scan Description Language (BSDL Version 0.0) is a de-facto
-- standard means of describing essential features of ANSI/IEEE 1149.1-1990
-- compliant devices.  This language is under consideration by the IEEE for
-- formal inclusion within a supplement to the 1149.1-1990 standard.  The
-- generation of the supplement entails an extensive IEEE review and a formal
-- acceptance balloting procedure which may change the resultant form of the
-- language.  Be aware that this process may extend well into 1993, and at
-- this time the IEEE does not endorse or hold an opinion on the language.
--*************************************************************************
--
-- IntelDX4(tm) processor BSDL description
-- This file has been electrically verified.
-- ---------------------------------------------------------
-- Rev: 1.2 09/27/93  =


entity IntelDX4 is

   generic (PHYSICAL_PIN_MAP : string := "PGA_17x17");

   port (A20M            :  in    bit;
         ABUS2           :  out   bit;
         ABUS3           :  out   bit;
         ABUS            :  inout bit_vector (4 to 31);  -- Address bus (words)
         ADS             :  out   bit;
         AHOLD           :  in    bit;
         BE              :  out   bit_vector (0 to 3);
         BLAST           :  out   bit;
         BOFF            :  in    bit;
         BRDY            :  in    bit;
         BREQ            :  out   bit;
         BS8             :  in    bit;
         BS16            :  in    bit;
         CLK             :  in    bit;
```

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```
        CLKMUL          :  in    bit;
        DBUS            :  inout bit_vector (0 to 31);  -- Data bus
        DC              :  out   bit;
        DP              :  inout bit_vector (0 to 3);
        EADS            :  in    bit;
        FERR            :  out   bit;
        FLUSH           :  in    bit;
        HLDA            :  out   bit;
        HOLD            :  in    bit;
        IGNNE           :  in    bit;
        INC_PGA         :  linkage bit_vector (1 to 5);  -- Internal NC PGA
        INTR            :  in    bit;
        KEN             :  in    bit;
        LOCK            :  out   bit;
        MIO             :  out   bit;
        NC_PGA          :  linkage bit;  -- No Connect for PGA
        NC_SQFP         :  linkage bit_vector (1 to 7);  -- NC SQFP
        NMI             :  in    bit;
        PCD             :  out   bit;
        PCHK            :  out   bit;
        PLOCK           :  out   bit;
        PWT             :  out   bit;
        RDY             :  in    bit;
        RESET           :  in    bit;
        SMI             :  in    bit;
        SMIACT          :  out   bit;
        SRESET          :  in    bit;
        STPCLK          :  in    bit;
        TCK, TMS, TDI   :  in    bit;    -- Scan Port inputs
        TDO             :  out   bit;    -- Scan Port output
        UP              :  in    bit;
        VCC_PGA         :  linkage bit_vector (1 to 23);  -- VCC
        VCC_SQFP        :  linkage bit_vector (1 to 53);  -- VCC
        VCC5            :  linkage bit;  -- Reference Voltage
        VOLDET          :  linkage bit;  -- Voltage Detect Pin, PGA only
        VSS_PGA         :  linkage bit_vector (1 to 28);  -- VSS
        VSS_SQFP        :  linkage bit_vector (1 to 38);  -- VSS
        WR              :  out   bit);

use STD_1149_1_1990.all;

attribute PIN_MAP of IntelDX4 : entity is PHYSICAL_PIN_MAP;

constant PGA_17x17 : PIN_MAP_STRING :=            -- Define Pin Out of PGA

     "A20M     : D15, "&
     "ABUS2    : Q14, "&
     "ABUS3    : R15, "&
     "ABUS     : (S16,Q12,S15,Q13,R13,Q11,S13,R12,"&
     "             S07,Q10,S05,R07,Q09,Q03,R05,Q04,Q08,Q05,"&
     "             Q07,S03,Q06,R02,S02,S01,R01,P02,P03,Q01),"&
     "ADS      : S17, "&
     "AHOLD    : A17, "&
     "BE       : (K15,J16,J15,F17),"&
     "BLAST    : R16, "&
     "BOFF     : D17, "&
```

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```
      "BRDY     : H15, "&
      "BREQ     : Q15, "&
      "BS8      : D16, "&
      "BS16     : C17, "&
      "CLK      : C03, "&
      "CLKMUL   : R17, "&
      "DBUS     : (P01,N02,N01,H02,M03,J02,L02,L03,F02,D01,E03,"&
      "             C01,G03,D02,K03,F03,J03,D03,C02,B01,A01,B02,"&
      "             A02,A04,A06,B06,C07,C06,C08,A08,C09,B08)," &
      "DC       : M15, "&
      "DP       : (N03,F01,H03,A05),"&
      "EADS     : B17, "&
      "FERR     : C14, "&
      "FLUSH    : C15, "&
      "HLDA     : P15, "&
      "HOLD     : E15, "&
      "IGNNE    : A15, "&
      "INC_PGA  : (A10,A12,A13,B12,B13),"&
      "INTR     : A16, "&
      "KEN      : F15, "&
      "LOCK     : N15, "&
      "MIO      : N16, "&
      "NC_PGA   : C13, "&
      "NMI      : B15, "&
      "PCD      : J17, "&
      "PCHK     : Q17, "&
      "PLOCK    : Q16, "&
      "PWT      : L15, "&
      "RDY      : F16, "&
      "RESET    : C16, "&
      "SMI      : B10, "&
      "SMIACT   : C12, "&
      "SRESET   : C10, "&
      "STPCLK   : G15, "&
      "TCK      : A03, "&
      "TDI      : A14, "&
      "TDO      : B16, "&
      "TMS      : B14, "&
      "UP       : C11, "&
      "VCC_PGA  : (B07,B09,B11,C04,C05,E2,E16,G02,G16,H16,K02,"&
      "             K16,L16,M02,M16,P16,R03,R06,R08,R09,R10,R11,"&
      "             R14),"&
      "VCC5     : J01, "&
      "VOLDET   : S04, "&
      "VSS_PGA  : (A07,A09,A11,B03,B04,B05,E01,E17,G01,G17,H01,H17,"&
      "             K01,K17,L01,L17,M01,M17,P17,Q02,R04,S06,S08,S09,"&
      "             S10,S11,S12,S14),"&
      "WR       : N17  ";


constant SQFP_208 : PIN_MAP_STRING :=          -- Define Pin Out of SQFP

      "A20M     : 47,  "&
      "ABUS2    : 202, "&
      "ABUS3    : 197, "&
```

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```
"ABUS     : (196,195,193,192,190,187,186,182,180,178,"&
"            177,174,173,171,166,165,164,161,160,159,"&
"            158,154,153,152,151,149,148,147),"  &
"ADS      : 203, "&
"AHOLD    : 17,  "&
"BE       : (31,32,33,34),"&
"BLAST    : 204, "&
"BOFF     : 6,   "&
"BRDY     : 5,   "&
"BREQ     : 30,  "&
"BS8      : 8,   "&
"BS16     : 7,   "&
"CLK      : 24,  "&
"CLKMUL   : 11,  "&
"DBUS     : (144,143,142,141,140,130,129,126,124,123,119,"&
"            118,117,116,113,112,108,103,101,100,99,93,"&
"            92,91,87,85,84,83,79,78,75,74),"&
"DC       : 39,  "&
"DP       : (145,125,109,90),"&
"EADS     : 46,  "&
"FERR     : 66,  "&
"FLUSH    : 49,  "&
"HLDA     : 26,  "&
"HOLD     : 16,  "&
"IGNNE    : 72,  "&
"INTR     : 50,  "&
"KEN      : 13,  "&
"LOCK     : 207, "&
"MIO      : 37,  "&
"NC_SQFP  : (63,64,67,70,71,96,127),"&
"NMI      : 51,  "&
"PCD      : 41,  "&
"PCHK     : 4,   "&
"PLOCK    : 206, "&
"PWT      : 40,  "&
"RDY      : 12,  "&
"RESET    : 48,  "&
"SMI      : 65,  "&
"SMIACT   : 59,  "&
"SRESET   : 58,  "&
"STPCLK   : 73,  "&
"TCK      : 18,  "&
"TDI      : 168, "&
"TDO      : 68,  "&
"TMS      : 167, "&
"UP       : 194, "&
"VCC_SQFP : (2,9,14,19,20,22,23,25,29,35,38,42,44,45,54,"&
"            56,60,62,69,77,80,82,86,89,95,98,102,106,111,"&
"            114,121,128,131,133,134,136,137,139,150,155,"&
"            162,163,169,172,176,179,183,185,188,191,198,"&
"            200,205),"&
"VCC5     : 3,   "&
"VSS_SQFP : (1,10,15,21,28,36,43,52,53,55,57,61,76,81,88,94,"&
"            97,104,105,107,110,115,120,122,132,135,138,146,"&
"            156,157,170,175,181,184,189,199,201,208),"&
"WR       : 27 ";
```

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```
   attribute Tap_Scan_In of    TDI : signal is true;
   attribute Tap_Scan_Out of   TDO : signal is true;
   attribute Tap_Scan_Mode of  TMS : signal is true;

   attribute Tap_Scan_Clock of TCK : signal is (25.0e6, BOTH);

   attribute Instruction_Length of IntelDX4 : entity is 4;

   attribute Instruction_Opcode of IntelDX4 : entity is

      "BYPASS   (1111)," &
      "EXTEST   (0000)," &
      "SAMPLE   (0001)," &
      "IDCODE   (0010)," &
      "RUNBIST  (1000)," &
      "PRIVATE  (0011,0100,0101,0110,0111,1001,1010,1011,1100,1101,1110)";

   attribute Instruction_Capture of IntelDX4 : entity is "0001";

   -- there is no Instruction_Disable attribute for IntelDX4

   attribute Instruction_Private of IntelDX4 : entity is "private";

   attribute Idcode_Register of IntelDX4: entity is
-- ******************************************
      "0000"                    &  --version
      "1000001010001000"&  --new part number
      "00000001001"     &  --manufacturers identity
      "1";                          --required by the standard

   attribute Instruction_Usage of IntelDX4 : entity is
      "RUNBIST (registers BIST; "&
      "result 0;"          &
      "clock CLK in Run_Test_Idle;"&
      "length 1600000)";

   attribute Register_Access of IntelDX4 : entity is
      "BIST[1] (RUNBIST)";

--{*********************************************************************}
--{  The first cell is closest to TDO                                    }
--{*********************************************************************}

   attribute Boundary_Length of IntelDX4 : entity is 109;
   attribute Boundary_Cells of IntelDX4 : entity is "BC_2, BC_1, BC_6";

   attribute Boundary_Register of IntelDX4 : entity is
      "0        (BC_2,  ABUS2,          output3,        X,  107,  1,  Z),"&
      "1        (BC_2,  ABUS3,          output3,        X,  107,  1,  Z),"&
      "2        (BC_6,  ABUS(4),        bidir,          X,  107,  1,  Z),"&
      "3        (BC_6,  ABUS(5),        bidir,          X,  107,  1,  Z),"&
      "4        (BC_1,  UP,             input,          X),"         &
      "5        (BC_6,  ABUS(6),        bidir,          X,  107,  1,  Z),"&
      "6        (BC_6,  ABUS(7),        bidir,          X,  107,  1,  Z),"&
      "7        (BC_6,  ABUS(8),        bidir,          X,  107,  1,  Z),"&
```

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```
"8        (BC_6,  ABUS(9),        bidir,          X,  107,  1,  Z),"&
"9        (BC_6,  ABUS(10),       bidir,          X,  107,  1,  Z),"&
"10       (BC_6,  ABUS(11),       bidir,          X,  107,  1,  Z),"&
"11       (BC_6,  ABUS(12),       bidir,          X,  107,  1,  Z),"&
"12       (BC_6,  ABUS(13),       bidir,          X,  107,  1,  Z),"&
"13       (BC_6,  ABUS(14),       bidir,          X,  107,  1,  Z),"&
"14       (BC_6,  ABUS(15),       bidir,          X,  107,  1,  Z),"&
"15       (BC_6,  ABUS(16),       bidir,          X,  107,  1,  Z),"&
"16       (BC_6,  ABUS(17),       bidir,          X,  107,  1,  Z),"&
"17       (BC_6,  ABUS(18),       bidir,          X,  107,  1,  Z),"&
"18       (BC_6,  ABUS(19),       bidir,          X,  107,  1,  Z),"&
"19       (BC_6,  ABUS(20),       bidir,          X,  107,  1,  Z),"&
"20       (BC_6,  ABUS(21),       bidir,          X,  107,  1,  Z),"&
"21       (BC_6,  ABUS(22),       bidir,          X,  107,  1,  Z),"&
"22       (BC_6,  ABUS(23),       bidir,          X,  107,  1,  Z),"&
"23       (BC_6,  ABUS(24),       bidir,          X,  107,  1,  Z),"&
"24       (BC_6,  ABUS(25),       bidir,          X,  107,  1,  Z),"&
"25       (BC_6,  ABUS(26),       bidir,          X,  107,  1,  Z),"&
"26       (BC_6,  ABUS(27),       bidir,          X,  107,  1,  Z),"&
"27       (BC_6,  ABUS(28),       bidir,          X,  107,  1,  Z),"&
"28       (BC_6,  ABUS(29),       bidir,          X,  107,  1,  Z),"&
"29       (BC_6,  ABUS(30),       bidir,          X,  107,  1,  Z),"&
"30       (BC_6,  ABUS(31),       bidir,          X,  107,  1,  Z),"&
"31       (BC_6,  DP(0),          bidir,          X,  108,  1,  Z),"&
"32       (BC_6,  DBUS(0),        bidir,          X,  108,  1,  Z),"&
"33       (BC_6,  DBUS(1),        bidir,          X,  108,  1,  Z),"&
"34       (BC_6,  DBUS(2),        bidir,          X,  108,  1,  Z),"&
"35       (BC_6,  DBUS(3),        bidir,          X,  108,  1,  Z),"&
"36       (BC_6,  DBUS(4),        bidir,          X,  108,  1,  Z),"&
"37       (BC_6,  DBUS(5),        bidir,          X,  108,  1,  Z),"&
"38       (BC_6,  DBUS(6),        bidir,          X,  108,  1,  Z),"&
"39       (BC_6,  DBUS(7),        bidir,          X,  108,  1,  Z),"&
"40       (BC_6,  DP(1),          bidir,          X,  108,  1,  Z),"&
"41       (BC_6,  DBUS(8),        bidir,          X,  108,  1,  Z),"&
"42       (BC_6,  DBUS(9),        bidir,          X,  108,  1,  Z),"&
"43       (BC_6,  DBUS(10),       bidir,          X,  108,  1,  Z),"&
"44       (BC_6,  DBUS(11),       bidir,          X,  108,  1,  Z),"&
"45       (BC_6,  DBUS(12),       bidir,          X,  108,  1,  Z),"&
"46       (BC_6,  DBUS(13),       bidir,          X,  108,  1,  Z),"&
"47       (BC_6,  DBUS(14),       bidir,          X,  108,  1,  Z),"&
"48       (BC_6,  DBUS(15),       bidir,          X,  108,  1,  Z),"&
"49       (BC_6,  DP(2),          bidir,          X,  108,  1,  Z),"&
"50       (BC_6,  DBUS(16),       bidir,          X,  108,  1,  Z),"&
"51       (BC_6,  DBUS(17),       bidir,          X,  108,  1,  Z),"&
"52       (BC_6,  DBUS(18),       bidir,          X,  108,  1,  Z),"&
"53       (BC_6,  DBUS(19),       bidir,          X,  108,  1,  Z),"&
"54       (BC_6,  DBUS(20),       bidir,          X,  108,  1,  Z),"&
"55       (BC_6,  DBUS(21),       bidir,          X,  108,  1,  Z),"&
"56       (BC_6,  DBUS(22),       bidir,          X,  108,  1,  Z),"&
"57       (BC_6,  DBUS(23),       bidir,          X,  108,  1,  Z),"&
"58       (BC_6,  DP(3),          bidir,          X,  108,  1,  Z),"&
"59       (BC_6,  DBUS(24),       bidir,          X,  108,  1,  Z),"&
"60       (BC_6,  DBUS(25),       bidir,          X,  108,  1,  Z),"&
"61       (BC_6,  DBUS(26),       bidir,          X,  108,  1,  Z),"&
"62       (BC_6,  DBUS(27),       bidir,          X,  108,  1,  Z),"&
"63       (BC_6,  DBUS(28),       bidir,          X,  108,  1,  Z),"&
```

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```
      "64       (BC_6,  DBUS(29),       bidir,          X,  108,  1,  Z),"&
      "65       (BC_6,  DBUS(30),       bidir,          X,  108,  1,  Z),"&
      "66       (BC_6,  DBUS(31),       bidir,          X,  108,  1,  Z),"&
      "67       (BC_2,  STPCLK,         input,          X),"&
      "68       (BC_1,  IGNNE,          input,          X),"&
      "69       (BC_2,  FERR,           output3,        X,  105,  1,  Z),"&
      "70       (BC_1,  SMI,            input,          X),"&
      "71       (BC_2,  SMIACT,         output3,        X,  106,  1,  Z),"&
      "72       (BC_1,  SRESET,         input,          X),"&
      "73       (BC_1,  NMI,            input,          X),"&
      "74       (BC_1,  INTR,           input,          X),"&
      "75       (BC_1,  FLUSH,          input,          X),"&
      "76       (BC_1,  RESET,          input,          X),"&
      "77       (BC_1,  A20M,           input,          X),"&
      "78       (BC_1,  EADS,           input,          X),"&
      "79       (BC_2,  PCD,            output3,        X,  106,  1,  Z),"&
      "80       (BC_2,  PWT,            output3,        X,  106,  1,  Z),"&
      "81       (BC_2,  DC,             output3,        X,  106,  1,  Z),"&
      "82       (BC_2,  MIO,            output3,        X,  106,  1,  Z),"&
      "83       (BC_2,  BE(3),          output3,        X,  106,  1,  Z),"&
      "84       (BC_2,  BE(2),          output3,        X,  106,  1,  Z),"&
      "85       (BC_2,  BE(1),          output3,        X,  106,  1,  Z),"&
      "86       (BC_2,  BE(0),          output3,        X,  106,  1,  Z),"&
      "87       (BC_2,  BREQ,           output3,        X,  105,  1,  Z),"&
      "88       (BC_2,  WR,             output3,        X,  106,  1,  Z),"&
      "89       (BC_2,  HLDA,           output3,        X,  105,  1,  Z),"&
      "90       (BC_1,  CLK,            input,          X),"&
      "91       (BC_1,  AHOLD,          input,          X),"&
      "92       (BC_1,  HOLD,           input,          X),"&
      "93       (BC_1,  KEN,            input,          X),"&
      "94       (BC_1,  RDY,            input,          X),"&
      "95       (BC_1,  CLKMUL,         input,          X),"&
      "96       (BC_1,  BS8,            input,          X),"&
      "97       (BC_1,  BS16,           input,          X),"&
      "98       (BC_1,  BOFF,           input,          X),"&
      "99       (BC_1,  BRDY,           input,          X),"&
      "100      (BC_2,  PCHK,           output3,        X,  105,  1,  Z),"&
      "101      (BC_2,  LOCK,           output3,        X,  106,  1,  Z),"&
      "102      (BC_2,  PLOCK,          output3,        X,  106,  1,  Z),"&
      "103      (BC_2,  BLAST,          output3,        X,  106,  1,  Z),"&
      "104      (BC_2,  ADS,            output3,        X,  106,  1,  Z),"&
      "105      (BC_2,  *,      control, 1),"&              -- DISMISC
      "106      (BC_2,  *,      control, 1),"&              -- DISBUS
      "107      (BC_2,  *,      control, 1),"&              -- DISABUS
      "108      (BC_2,  *,      control, 1)";               -- DISWR

end IntelDX4;
```

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APPENDIX D
SYSTEM DESIGN NOTES

SMM Environment Initialization

When the Military Intel486 processors are operating in Real Mode, the physical address at which instructions and data are fetched is determined by the segment register and an offset (i.e., CS and IP for instructions). When a new value is loaded into a segment register, the new value is shifted to the left by four bits and stored in a segment base register that corresponds to that particular segment (CSBASE, DSBASE, ESBASE, etc.). It is the value stored in the segment base register that is actually used to generate a physical address. For example, the linear address to be used for fetching instructions is determined by adding the value contained in the CS segment base register with the value in the IP register.

When the processor is in Protected Mode, the segment registers are used as selectors to a descriptor table. Each descriptor in a descriptor table contains information about the segment in use, including the segments BASE address (i.e., CSBASE), the limit (or size of the segment), as well as protection level, privileges, operand sizes, and the segment type. In Protected Mode, the linear address is determined by adding the base portion of the descriptor to the appropriate offset.

When in System Management Mode, the processor operates in a pseudo-Real Mode, with address calculation performed in the Real Mode manner. However, the processor adds the value in the segment base register with the value in the EIP register, rather than the IP register, so there are no limits as to the segment size. The physical address of an instruction is obtained by adding the value in CSBASE to the value in EIP.

When entering SMM, it may be necessary to initialize the segment registers to point to SMRAM (see section 8.4.2, ‘‘Processor Environment,’’ for their value on SMM entry). If SMBASE has not been relocated, then the necessary segment registers can be initialized to point to SMRAM by using the value in the CS register, 3000H, which points to the SMRAM address space.

When an SMI# occurs after SMBASE has been modified, CSBASE is loaded with the new value of SMBASE. **However, the CS selector register still contains the value 3000H, not the value corresponding to the new SMBASE**.

To initialize segment registers to point to the new SMRAM area, read the SMBASE value from the SMM state that was saved in memory. Because the data segment registers are initialized to 0, do not use them to access the SMM state save area. Instead, perform a read relative to the CS register by using a CS override prefix to a normal memory read. Although CS still contains 3000H, CSBASE contains the value of SMBASE, and CSBASE is used for the address generation.

Once the value of SMBASE is obtained, it must be shifted to the right by four bits to get the appropriate value to be placed in the segment registers. The CS register itself can be initialized by executing a far jump instruction to an address within SMBASE, which causes CS to be reloaded with a value corresponding to SMBASE.

Example D-1 describes one method of initializing the segment registers when SMBASE has been relocated. This method works if SMBASE is less than 1 Megabyte.

Example D-1. Initialization of Segment Registers within SMM

```
;read the value of SMBASE from the state save area
      mov   si,FEF8H     ;SMBASE slot in SMM state save area
      mov   eax,cs:[si]  ;copy SMBASE from SMBASE:FEF8H to eax

;scale the SMBASE value to a 16-bit quantity
      mov   cl,4
      ror   eax,cl       ;scaled value of SMBASE now in ax

;to load cs, execute a far jump to an address that has been stored
;at memory location PTR_ADDR

;store the SMBASE value and an offset to a memory location that can be used as
;an indirect jump address

      mov   di,PTR_ADDR  ;PTR_ADDR is the location used to
                         ;store the jump address
      mov   bx,OFFSET    ;OFFSET is the address where
                         ;execution continues after the
                         ;far jump

      mov   cs:[di],bx   ;store the offset for the far jump
      inc   di
      inc   di
      mov   cs:[di],ax   ;store the segment address for the
                         ;far jump, which is SMBASE
      mov   bx,PTR_ADDR  ;bx now contains the address of the
                         ;location holding the jump address

;initialize DS and ES with the correct address of SMBASE
      mov   ds,ax
      mov   es,ax

;execute a far jump instruction to load the CS register
      jmp   far [bx]     ;jump to address stored at memory
                         ;location pointed to by bx

;CS now contains the correct value of SMBASE, and execution continues from the
;address SMBASE:OFFSET
```

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Accessing SMRAM

LOADING SMRAM WITH AN INITIAL SMI HANDLER

Under normal conditions, the SMRAM address space should only be accessible by the processor while it is in SMM mode. However, some provision must be made for providing the initial SMM interrupt handler routine.

Because System Management Mode must be transparent to all operating systems, the initial SMM handler must be loaded by the system BIOS. At some time during the power on sequence, the system BIOS will need to move the SMM handler routine from the BIOS ROM to the SMRAM. The system designer must provide a hardware mechanism that allows access to SMRAM while SMIACT# from the processor is inactive. One method would be to provide an I/O port in the memory controller that forces

memory cycles at a given address to be relocated to the SMRAM. Once the initial SMM handler has been loaded to SMRAM, the I/O port would be disabled to protect against accidental accesses to SMRAM.

The system BIOS must provide an SMM handler at the address 38000H. If the system designer has chosen to take advantage of the SMRAM relocation feature of the processor, this handler must change the SMBASE register in the SMM state save. Next, the BIOS must move the full featured SMM handler to the new address. An SMI# must be generated in order to change the SMBASE register before the BIOS passes control to the operating system.

SMRAM HIDDEN FROM DMA AND BUS MASTERS

In a system that allows DMA or other devices to take control of the system bus, care must be taken to ensure that only the master processor can access SMRAM. If an external bus master requests use of the system bus (by asserting HOLD or BOFF#) while the processor is executing an SMM handler routine, the processor would respond by passing control of the bus to the requesting device. The system memory controller must redirect any memory accesses that are not generated by the processor to normal system memory as if SMIACT# was inactive. DMA accesses to the SMRAM area must be redirected to the correct address space when the initialization routine is loading SMRAM, as well as when the processor is in SMM.

It is not recommended to block bus control requests when in SMM, because the increased bus access latency could cause compatibility issues with some software or expansion hardware.

ACCESSING SYSTEM MEMORY FROM WITHIN SMM

In order to enter a suspend state where power is removed from some or all of system memory, it is necessary for the processor to have access to the entire system address space from within SMM. Access to system memory from within SMM requires that the memory controller decode both SMIACT# and the processor address to determine accesses to SMRAM. Only those memory addresses that are defined as being SMRAM space would be directed to SMRAM. If SMRAM is located at an address that overlays normal system memory address space (see section 8.6.1, ''SMRAM Interface,''.), the processor must have a method of accessing both SMRAM (for code reads) and system memory simultaneously.

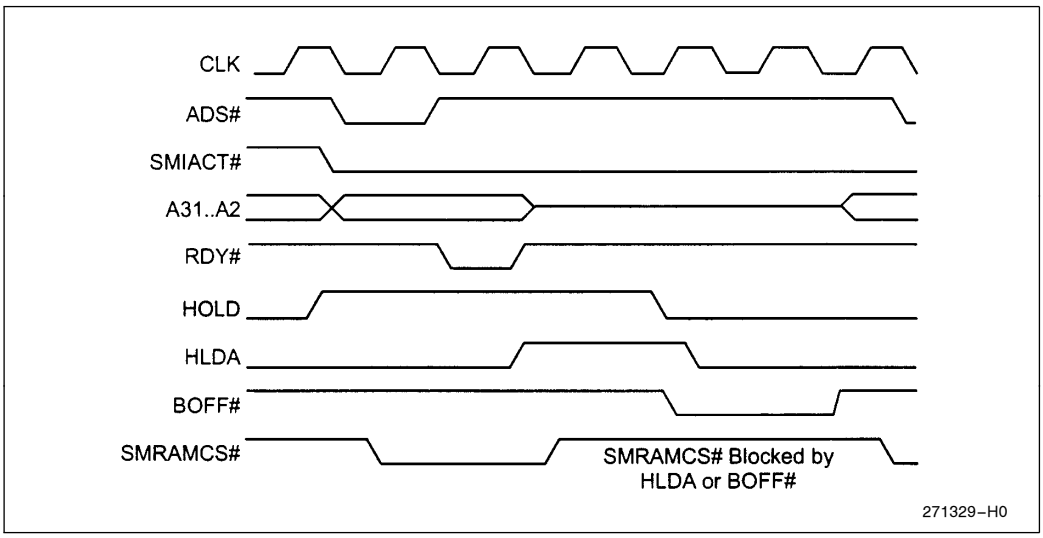

Figure D-1. Blocking Other Bus Masters from Accessing SMRAM

Ideally, a method of accessing system memory that is mapped underneath SMRAM would be provided by the system memory controller. The memory controller would provide a register that allows system memory at a given address to be remapped to a different address, which is not overlaid by SMRAM. When the SMM handler implements a suspend, it would first move all of system memory that is not underneath SMRAM to a non-volatile medium (such as a hard disk drive). Next, the SMRAM image would be transferred to the non-volatile medium. Finally, the memory underneath SMRAM would be accessed and copied to the non-volatile medium with a processor read to the remap address space, which is redirected to the overlaid system memory (see Figure D-2).

If the memory controller does not provide a method of accessing overlaid system memory, it is possible to implement a software procedure to accomplish the same goal. However, the software method is quite complex, and a hardware method is preferred. A description of the software method follows.

The ability to access the system memory that is located in the address space under SMRAM requires a method of resuming from SMM to a predetermined address space. This can be accomplished with the following procedure.

When resuming from SMM, the processor continues execution at the address contained in the CS and EIP slots within the SMM state save. However, the resume address cannot be changed by simply modifying the CS and EIP slots, because the processor will use the CS descriptor to determine the actual resume address. The descriptor registers are stored in reserved slots in the SMM state save, and they cannot be directly modified.

By replacing the suspend state save with a previously obtained image of a state save that returns to a known location, the SMM suspend handler can force a return to a given address:

1. During initial system power up, execute an SMI# from a predetermined address (the address immediately preceding the address to which you later wish to resume). This can be accomplished by generating an SMI# in response to an I/O instruction or executing a halt instruction and using an SMI# to exit the halt state.
2. Save the state save from this SMM to a safe location (SMRAM).
3. When the system needs to resume to a given address from some other SMI#, the stored state save can be substituted for the state save generated from that particular SMM.

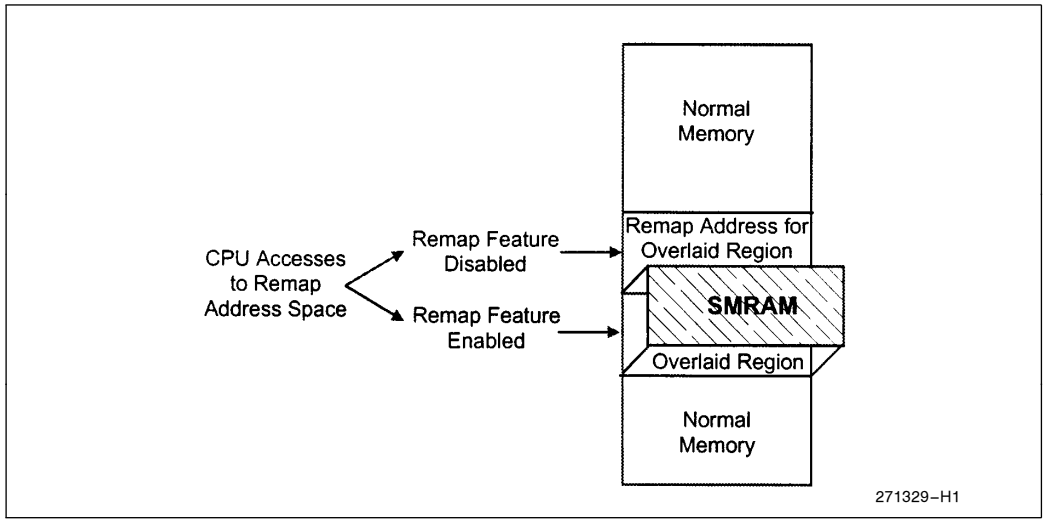

Figure D-2. Remapping Memory That Is Overlaid by SMRAM

Now that SMM can be resumed at a predetermined address, access the entire system memory space from within SMM before executing a suspend:

1. During a suspend SMM, save all system memory except that which is located underneath SMRAM to a specified (and reserved) section of the hard disk. The ability to access system memory requires the memory controller to decode both SMIACT# and the processor address, and direct a limited section (maybe 64 or 128K) of the processor address space to SMRAM. All other processor memory accesses should go to normal system memory.
2. Save the contents of the SMM state save to the hard disk.
3. Modify the SMM state save so that the RSM instruction will return to a predefined address, which is not in the application that was interrupted. The code at this address must contain the remainder of the suspend SMM handler. The predefined address can be anywhere in the processor address space, because the contents of system memory have already been saved to disk.
4. Execute an RSM instruction, which exits SMM and returns control to a predetermined address (which must contain the rest of the SMM suspend handler).
5. Save the rest of system memory (that which is located underneath SMRAM) to the hard disk. This address space can now be accessed with normal move instructions, because we are no longer in SMM.
6. Save a flag (in CMOS memory) indicating that the next reset should cause a resume from suspend.
7. Powerdown the memory (and possibly the processor).
8. When power is restored, the processor is reset and begins execution of the POST in BIOS. Early in the POST, the system should check the status of the suspend flag.
9. Load a preliminary SMM handler to location 38000H and generate an SMI#. The SMM handler should read the SMBASE slot from the SMM state save that was stored to hard disk. SMBASE is then modified to point to the final SMRAM location and the system resumes from SMM back to the system BIOS.
10. Restore the contents of system memory located underneath SMRAM from the hard disk.
11. Generate a second SMI#, which executes an SMM handler at the original value of SMBASE (before the suspend SMM). The SMM handler restores the contents of the rest of system memory from the hard disk, and then restores the original SMM state save to the SMM state save area in SMRAM, discarding the most recent SMM state save.
12. Execute an RSM instruction, which returns execution to the application that was interrupted by the suspend request.

Interrupts and Exceptions During SMM Handler Routines

To ensure transparency to existing system software, the SMM handler should not depend on interrupt or exception handlers provided by the operating system. However, in some cases it may be necessary to service interrupts or exceptions while in System Management Mode. In these cases, SMM compliant interrupt and exception handlers, as well as an SMM compliant interrupt vector table, should be provided.

SMM COMPLIANT VECTOR TABLES

An SMI# interrupt request can be generated while code is running under any of the other three processor operating modes (Real, Virtual-86, or Protected). When entering the SMM handler, the processor enters a pseudo-real mode, and the beginning of the interrupt vector table must be located at the address 00000000H. Before allowing any interrupts or exceptions to occur, the SMM handler routine must provide a valid interrupt vector table. Any code that is executed before setting up an SMM compliant interrupt vector table must be written carefully to ensure that no exceptions are generated.

The system memory controller could relocate accesses to the SMM interrupt vector table to a location within SMRAM. In this case, when SMIACT# is active, all accesses to the lowest 1 Kbyte of the processor address space would be redirected to SMRAM, which would contain an SMM compliant vector table that has already been initialized.

If the system memory controller does not redirect interrupt vector table reads to an address within SMRAM, there are three steps required to provide an SMM compliant interrupt vector table:

1. Save the contents of memory at address 00000000H to SMRAM

2. Provide vectors for any possible interrupts or exceptions at the appropriate location in the vector table
3. Restore the original memory contents from SMRAM before exiting the SMM handler routine

INTERRUPTS AND SUBROUTINES WITH SMRAM RELOCATION

There is an additional issue that must be considered if interrupts or exceptions are to be executed within SMM and SMRAM has been relocated. Interrupt or subroutine calls from within SMM operate in a manner similar to Real Mode. When a subroutine is called or an interrupt is recognized, the 16-bit CS and IP registers are pushed onto the stack to provide a return address.

When SMRAM is relocated to an address space above 1M and an interrupt or subroutine call occurs, only 16 bits of the EIP register are pushed onto the stack. When returning from the subroutine or interrupt, the processor will vector to a location where the upper 16 bits of EIP are zero. This can be avoided for subroutines by using an address size override before calling the subroutine. However, the issue remains for interrupts.

Military Intel486 DX, IntelDX2, and IntelDX4 Processor Floating Point Operation and SMM

THE NEED TO SAVE THE FPU ENVIRONMENT

When the processor enters System Management Mode, the context information for the interrupted application is automatically saved to a specific state save address. When the SMM handler returns control to the interrupted application by executing the RSM instruction, the context information from the interrupted application is restored to the processor by reading from the state save location. This mechanism allows the SMM handler routine to modify most of the processor registers without the need to explicitly save them to memory. However, the registers in the processor's Floating Point Unit (FPU) are not automatically saved when the processor enters SMM. If the SMM handler needs to modify any of the registers in the FPU, or if the register data will be lost due to entering a power down state, the SMM handler must first explicitly save the FPU state as it existed in the interrupted application.

There are two instances in which an SMM handler routine must be aware of the Floating Point Unit (FPU):

1. When removing power from the processor / FPU for the purpose of executing a suspend sequence.
2. When the SMM handler uses FPU instructions.

In both of these cases, the SMM handler must save the state of the FPU as it was left by the interrupted application.

The information stored by the FPU state save instructions (FSAVE, FNSAVE, FSTENV, and FNSTENV) is dependent on the operating mode of the processor. The FPU state save instructions store the FPU state information in one of four formats: 16-bit Real Mode, 32-bit Real Mode, 16-bit Protected Mode, or 32-bit Protected Mode, depending on the processor operating mode. The content of the information saved also varies slightly, depending on the processor operating mode in which the save instruction was executed. For example, the 32-bit Protected Mode FNSAVE instruction saves the address of the last executed FPU instruction and its operands in the form of a segment selector and a 32-bit offset. In contrast, the 16-bit Real Mode FNSAVE instruction saves the address information in the form of a 20 bit physical address. Because the format with which the FPU state restore instructions (FRSTOR and FLDENV) recall the information is also dependent on the operating mode of the processor, the save and restore instructions must be executed from the same processor operating mode.

SAVING THE STATE OF THE FLOATING POINT UNIT

When an SMM handler routine needs to save the state of the Floating Point Unit, it must save all FPU state information necessary for the interrupted application to continue processing. This state information includes the contents of the Floating Point Unit stack, which requires use of the FNSAVE or FSAVE instruction (FSTENV does not save the contents of the FPU stack). If the last executed non-control Floating Point instruction caused an error (such as a divide by 0), the saved information must also include the address of the failing instruction and the addresses of any operands for that instruction. Without these addresses, it would be impossible for the FPU exception handler of the interrupted application to correct the error and restart the instruction.

The FNSAVE and FSAVE instructions differ in that FNSAVE does not wait for the FPU to check for an existing error condition before storing the FPU environment information. If there is an unmasked FPU exception condition pending, execution of the FSAVE instruction will force the processor to wait until the error condition is cleared by the software exception handler. Because the processor is in System Management Mode, the appropriate exception handler will not be available, and the FPU error would not be corrected in the manner expected by the interrupted application program. For this reason, the FNSAVE instruction should be used when saving the environment of the FPU within SMM.

Because the SMM handler does not know the processor mode in which the interrupted application was executing (16 or 32 bit, Real or Protected), the SMM handler must execute the FNSAVE instruction in a mode in which all FPU state information is stored. The 32-bit Protected Mode format of the FNSAVE instruction is a super set of all other formats of the FNSAVE instruction. Therefore, executing the 32-bit Protected Mode FNSAVE instruction ensures that all FPU state information will be saved.

Executing the FNSAVE instruction in 32-bit Protected Mode requires that the processor be temporarily placed in Protected Mode. Rather than perform all of the setup details and overhead necessary to place the processor into Protected Mode, including the initialization of all descriptors and descriptor tables, it is possible to temporarily place the processor into Protected Mode for the purpose of executing only a few carefully written instructions. This can be accomplished by setting the PE bit in the CR0 register, and then executing a short jump to clear the instruction pipelines.

It is important to note that any instruction that modifies a segment register will cause the processor to attempt to load a new descriptor from the descriptor table. (The occurrence of an interrupt or an exception would cause the processor to load a new descriptor, so interrupts must be disabled during this sequence.) Because neither the descriptors nor the descriptor table have been initialized, this would cause the system to crash. Therefore, all segment registers that are to be used in the FPU state save instructions must be initialized before entering Protected Mode.

Example D-2 gives an example of the code that can be used to place the processor in Protected Mode and save the FPU state.

Note that the no wait form (FNSAVE) of the save instruction must be used. In the event that the previous FPU instruction caused a floating point error, we do not want to wait for this error to be serviced before executing the save instruction. Additionally, if the FSAVE instruction were used, the operand size override prefix would be incorrectly applied to the implicit WAIT instruction which precedes FSAVE, rather than to the save instruction itself.

Before exiting the SMM handler and returning to the interrupted application, the register contents of the Floating Point Unit must be returned to their previous values. This can be accomplished by executing the 32-bit Protected Mode format of the FRSTOR instruction. Example D-3 gives an example code segment that can be used to restore the FPU to the state in which it was interrupted by the SMI request.

Note that the no wait form (FNRSTOR) of the restore instruction must be used. If the FRSTOR instruction were used, the operand size override prefix would be incorrectly applied to the implicit WAIT instruction which precedes FRSTOR, rather than to the save instruction itself.

Support for Power Managed Peripherals

SHADOW REGISTERS

Before power is removed from any device, the state of that device must be saved in a protected memory space so that the device can be reinitialized to its previous state. If a peripheral contains a write only register, the value in that register can be recovered by providing shadow registers that are both readable and writeable.

These shadow registers should be updated every time the peripheral registers are written, but they have no function other than tracking the data written to a particular register.

Example D-2. Saving the FPU State in 32-Bit Protected Mode

```
;first initialize the registers used to store the state save information
      mov   dx,SEGMENT          ;SEGMENT is the segment to be used by
                                ;the save instruction,
      mov   ds,dx               ; normally it should point to SMRAM
      mov   si,OFFSET           ;OFFSET is the offset used in the save
                                ;instruction

;set the PE bit in CR0
      mov   eax,cr0             ;read the old value of CR0
      or    eax,00000001H       ;set the PE bit
      mov   cr0, eax

;enter protected mode by executing a short jump to clear the prefetch queue
      jmp   protect
protect:

;we can now save the state of the FPU in the protected mode format

      db    66H                 ;use an operand size override prefix
                                ;to set 32-bit format
      fnsave[si]                ;FPU state saved to SEGMENT:OFFSET

;now return to real mode to continue with the SMM handler (no jump is
;required)

      mov   eax,cr0             ;clear the PE bit in CR0
      and   eax,0FFFFFFFEH
      mov   cr0,eax
```

271329–H2

In addition to the write only registers in a system, there are several other registers that must be shadowed. Any device that requires registers to be programmed in a particular sequence must also have its registers shadowed. Examples in a typical personal computer include the programmable interrupt controller, the DMA controller, and the programmable timer/counter.

It is also possible to perform shadowing of some write only registers using SMM. Any time a write cycle is generated to a write only register, the system can generate an SMI#. The SMM handler can use the processor state information saved in the SMM state save to save the data from the interrupted I/O cycle to a predetermined location in the SMRAM space.

Example D-3. Restoring the FPU State from a 32-Bit Protected Mode Save

```
;first initialize the registers used to recall the state save information

      mov   dx,SEGMENT          ;SEGMENT is the segment to be used by
                                ;the restore instruction,
      mov   ds,dx               ;normally it should point to SMRAM
      mov   si,OFFSET           ;OFFSET is the offset used in the
                                ;restore instruction

;set the PE bit in CR0

      mov   eax,cr0             ;read the old value of CR0
      or    eax,00000001H       ;set the PE bit
      mov   cr0, eax

;enter protected mode by executing a short jump to clear the prefetch queue

      jmp   protect
protect:

;we can now recall the state of the FPU from the previous FNSAVE instruction
;(in the protected mode format)

      db    66H                 ;use an operand size override prefix
                                ;to set 32-bit format
      fnrstor     [si]          ;FPU state restored from
                                ;SEGMENT:OFFSET

;now return to real mode to continue with the SMM handler (no jump is
;required)

      mov   eax,cr0      ;clear the PE bit in CR0
      and   eax,FFFFFFFEH
      mov   cr0,eax
```

271329–H3

The information contained in the SMM state save can be used (with the knowledge that the SMI# was in response to an I/O write instruction) to determine both the address and the data of the interrupted write instruction. The SMM handler can examine the OPCODEs of previous instructions by decrementing the IP (or EIP) register. Once the correct OPCODE is determined, it can be used with the values in the EAX and DX slots of the SMM state save to update the information in the memory used to shadow the I/O register. I/O write instructions occur in one of three forms: 1) a write to an address that is specified in the OPCODE; 2) a write to an address contained in the DX register; or 3) a string write to an address contained in the DX register.

The I/O write instructions have the following OPCODEs:

Table D-1. I/O Write Instruction OPCODEs

Instruction	OPCODE	Notes
OUT x,al	E6x	x is the address of the I/O port
OUT x,ax	E7x	x is the address of the I/O port
OUT x,eax	E7x	x is the address of the I/O port
OUT dx,al	EE	
OUT dx,ax	EF	
OUT dx,eax	EF	
OUTSB	6E	
OUTSW	6F	
OUTSD	6F	

The SMM handler must know whether a particular I/O port is 16 or 32 bits in order to distinguish between 16 and 32 bit I/O write cycles.

The SMM handler can decrement the value of IP contained in the state save, and then examine the memory contents at that address. If the SMM handler knows that the last instruction was an I/O write instruction, and writes to I/O addresses 6EH, 6FH, 0EEH, and 0EFH will not cause an SMI#, it can use the SMM state save data for EAX and EDX to reconstruct the last instruction.

HANDLING INTERRUPTED I/O WRITE SEQUENCES

In a typical personal computer, there are several hardware devices that require the control registers for that device to be programmed in a particular order. For example, the interrupt controller, the DMA controller, the programmable timer/counter, the keyboard controller, and the real time clock all require a series of accesses to properly initialize the registers in that particular device. Some of these devices may require successive accesses to registers located at different addresses, while others may require several control registers to be programmed through write cycles to the same address.

If an SMI request interrupts an application that is in the process of initializing the registers in one of these devices, special care must be taken to ensure that the peripheral is returned to its original state when control is returned to the interrupted program. For some SMM handler events, it may be necessary to power down the device or change the state of a register within the device. In these cases, the SMM handler must return control to the interrupted application in such a way that the application can continue with the correct sequential access in the interrupted sequence.

To accomplish this, the SMM handler must restore the original values of all registers in the device, and restart the interrupted sequence so that the application may continue where it left off. This requires system hardware to shadow all registers that need to be accessed in the sequence, keep an index indicating which position in the sequence the register occupies, and keep a pointer so that SMM software knows to which register the last access was directed. This pointer would indicate the last register of each sequence that was programmed in the particular peripheral.

For example, programming the master interrupt controller requires a write to I/O port 20H (ICW1) followed by four write cycles to I/O port 21H (ICW2, ICW3, ICW4, and OCW1). If this sequence is interrupted by an SMI request, and the resulting SMM handler either modifies or powers down the interrupt controller, the SMM handler must return control to the interrupted application such that the following access to the interrupt controller would access the correct register in the sequence. System hardware must save the contents of each of the registers, as well as a pointer indicating which register was last written.

Before returning control to the interrupted application, the SMM handler must initialize ICW1–ICW4 and OCW1 to their previous values. It would then rewrite the appropriate registers so that the first access by the application program would be to the location in the sequence following the last location it programmed before it was interrupted by the SMI request.

A similar procedure must be followed for each of the peripherals that require control registers to be initialized in a particular order.