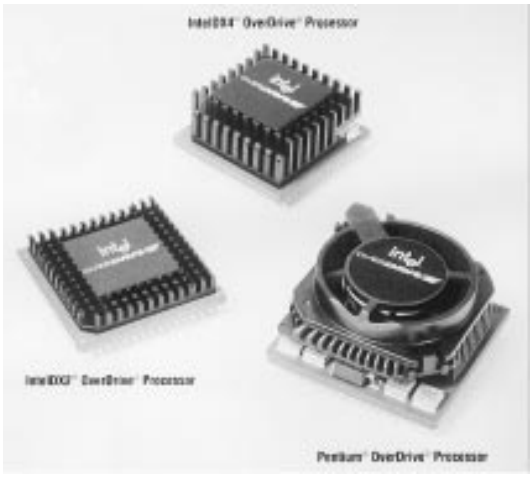
PRELIMINARY

INTEL OverDrive® PROCESSORS

- **Powerful Processor Upgrades for most Intel486™ Microprocessor-Based Systems**
  - **— Significantly Accelerates All Software Applications**
- **Intel OverDrive® Processor Family Includes:**
  - **— Pentium® OverDrive Processor**
  - **— IntelDX4™ OverDrive Processor**
  - **— IntelDX2™ OverDrive Processor**
- **Designed to Upgrade Systems Based on:**
  - **— Intel486™ SX Processors**
  - **— Intel486™ DX Processors**
  - **— IntelSX2™ Processors**
  - **— IntelDX2™ Processors**
- **Large Installed Base of Thousands of Applications**
- **Incorporates SMM Power Saving Features**



290436–61

The Pentium® OverDrive® processor upgrades most Intel486 processor-based systems to Pentium processor technology. It is the recommended upgrade option for IntelSX2™ and IntelDX2™ CPU-based systems, and the superior upgrade option for Intel486 SX and DX CPU-based systems. It features a true Pentium processor core (superscalar architecture, branch prediction and faster floating point unit), silicon enhancements (separate code and data caches, 16 KB each and 32-bit bus interface), and package innovations (on-package voltage regulation and fan heat sink).

The IntelDX4™ OverDrive processor is an upgrade for most Intel486 SX and DX CPU-based systems. It features Intel's speed-tripling technology, enhanced 16 KB on-chip cache memory and a math coprocessor.

The IntelDX2 OverDrive processor is an entry-level upgrade for most Intel486 SX and DX CPU-based systems. It features Intel's speed-doubling technology, on-chip math coprocessor and 8 KB on-chip cache memory.

*Other brands and names are the property of their respective owners.

December 1995 **Order Number: 290436-006**

Intel OverDrive® Processors

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1.0 INTRODUCTION

This data sheet describes the Intel OverDrive processors, a family of CPU upgrades for Intel486 processor-based systems. This family includes the IntelDX2 OverDrive processor, the IntelDX4 OverDrive processor and the Pentium OverDrive processor. These processor upgrades significantly accelerate all software applications, thereby increasing overall PC performance.

It is important to note that this data sheet is intended to be used in conjunction with the Intel486 Microprocessor Family Datasheet—which describes the Intel Family Architecture and functionality (Order # 242202-003). All enhancements or differences between the OverDrive processor and the original processor (i.e., IntelDX2 or IntelDX4 OverDrive vs. Intel486 DX processor, Pentium vs. Pentium OverDrive processors) are described in this data sheet.

Intel486 SX, Intel486 DX, IntelSX2, or IntelDX2 processor-based systems that are compatible to the Intel OverDrive processor(s) must be designed to both the original processor specifications and the Intel OverDrive processor(s) specifications.

1.1 Product Overview

The following sections provide an overview of each of the OverDrive processors. Refer to the specific product section(s) for more detailed information.

Figure 1-1 lists some of the key features of each OverDrive processor. Figure 1-2 describes the upgrade choices available for an existing Intel486 SX or DX system.

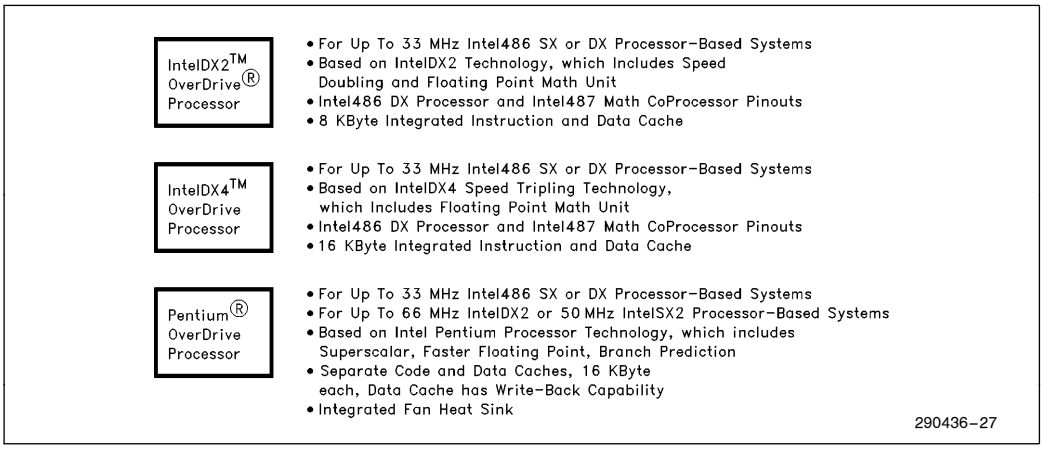


Figure 1-1. Key Features

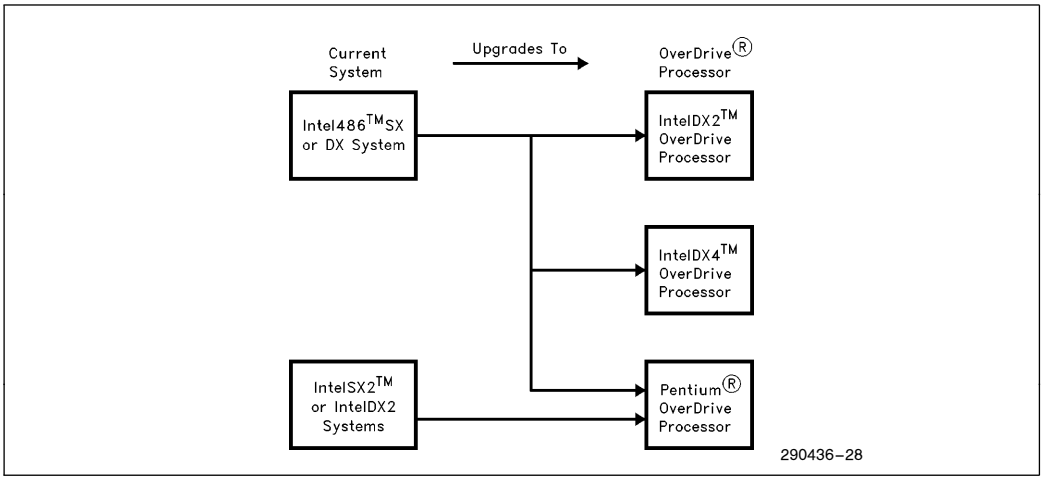


Figure 1-2. Upgrade Choices

1.1.1 IntelDX2™ OverDrive® PROCESSOR

The IntelDX2 OverDrive processor is the entry-level processor upgrade designed for most Intel486 SX and Intel486 DX processor-based systems. Based on the IntelDX2 processor, it features the Intel speed doubling technology. This accelerates both integer and floating point software, to deliver performance equivalent to a similarly configured IntelDX2 processor-based system.

The IntelDX2 OverDrive processor integrates an integer unit, a floating point math coprocessor unit, a memory management unit and an 8 KByte cache on a single chip. The speed doubling technology allows the processor to operate internally at twice the speed of the system bus; up to a maximum of 66 MHz for a 33 MHz system.

The IntelDX2 OverDrive processor comes in two package offerings; 168-lead Pin Grid Array (PGA) and 169-lead PGA. It is designed to be installed into the OverDrive processor socket of Intel486 SX and DX processor-based systems. It can also replace the existing processor in single-socket systems.

1.1.2 IntelDX4™ OverDrive® PROCESSOR

The IntelDX4 OverDrive processor is an upgrade designed for most Intel486 SX and Intel486 DX processor-based systems. Utilizing the Intel speed tripling technology, the IntelDX4 OverDrive processor accelerates both integer and floating point software, achieving performance comparable to a similarly configured IntelDX4 processor-based system.

The IntelDX4 OverDrive processor integrates an integer unit, a floating point math coprocessor unit, a memory management unit and a 16-KByte cache on a single chip. The speed tripling technology allows the processor to operate internally at three times the speed of the system bus; up to a maximum of 100 MHz for a 33 MHz system.

The IntelDX4 OverDrive processor comes in two package offerings; 168-lead Pin Grid Array (PGA) and 169-lead PGA. It is designed to be installed into the OverDrive processor socket of Intel486 SX and DX processor-based systems. It can also replace the existing processor in most single-socket systems.

1.1.3 Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor is the highest performance CPU upgrade available for systems based on the Intel486 family of CPUs, bringing Pentium processor technology (including Superscalar Architecture, Branch Prediction, faster floating-point unit, and separate data and code caches) to most Intel486 processor-based systems. It is the recommended upgrade option for most IntelSX2 and IntelDX2 processor-based systems, and the superior upgrade option for most Intel486 SX and DX processor-based systems.

Inclusion of the Pentium OverDrive processor socket in systems based on the Intel486 family of microprocessors provides the end user with an easy and cost-effective way to increase system performance for most Intel486 processor-based systems. The majority of upgrade installations which take advantage of the Pentium OverDrive processor socket will be performed by end users and resellers. Therefore, it is important that the design be ''end user easy'', and that the amount of training and technical expertise required to install the OverDrive processors be minimized. Upgrade installation instructions should be clearly described in the system user's manual. In addition, by making installation simple and foolproof, PC manufacturers can reduce the risk of system damage, warranty claims and service calls. Feedback from Intel's upgrade customers highlight three main characteristics of end user easy designs: accessible socket location, clear indication of upgrade component orientation, and minimization of insertion force. Recommendations regarding designing for easy upgradability appear in Appendix C.

1.2 Pinouts

1.2.1 168/169 PIN SOCKET

Refer to Figures 1-3 and 1-4 for an illustration of each of the two PGA packages. Figure 1-3 shows the 169-lead PGA package, while Figure 1-4 illustrates the 168-lead PGA package.

Table 1-1 cross-references the pin number to pin function for the 169-lead PGA package. Table 1-2 is a cross-reference for the 168-lead package.

Table 5-1 in Section 5 gives a brief description of the function of each pin.

Refer to each specific OverDrive processor section for a description of any differences from the pinouts described in this section.

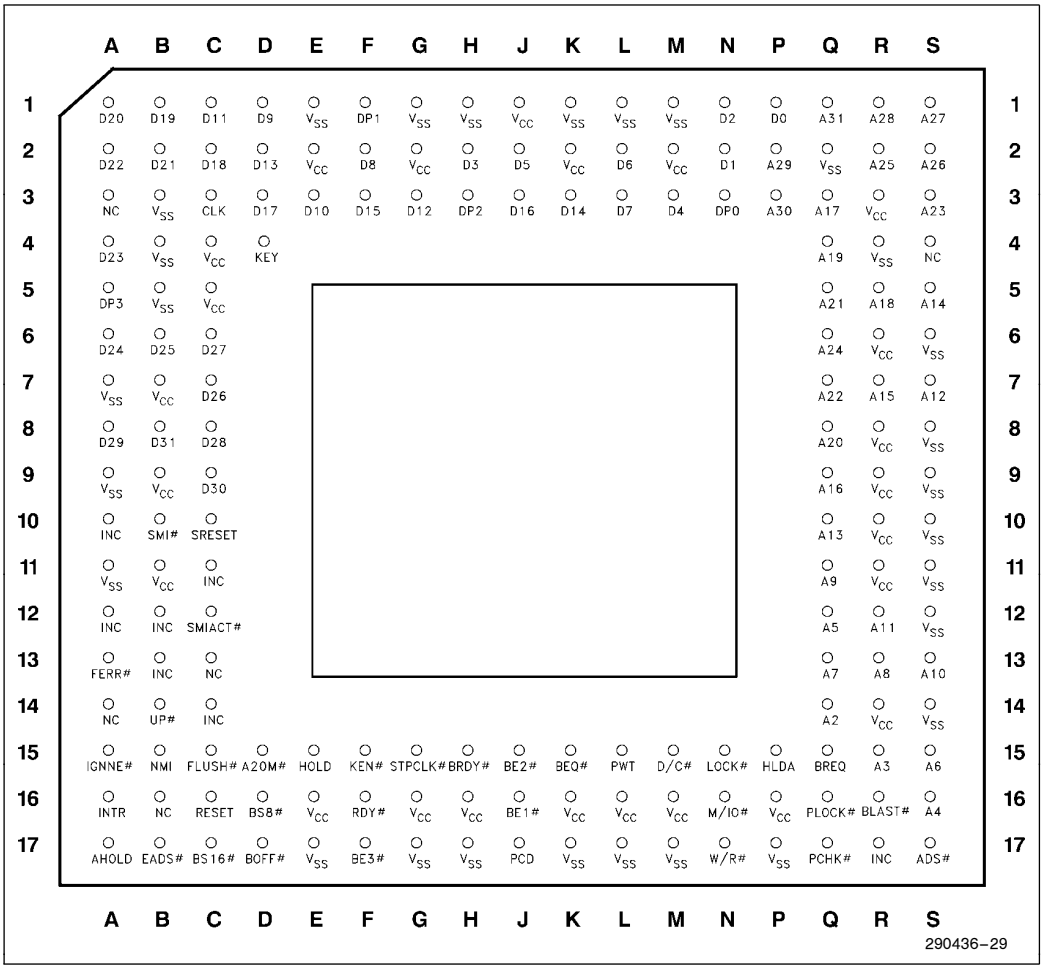


Figure 1-3. 169-Lead PGA Bottom View Pinout (ODP)

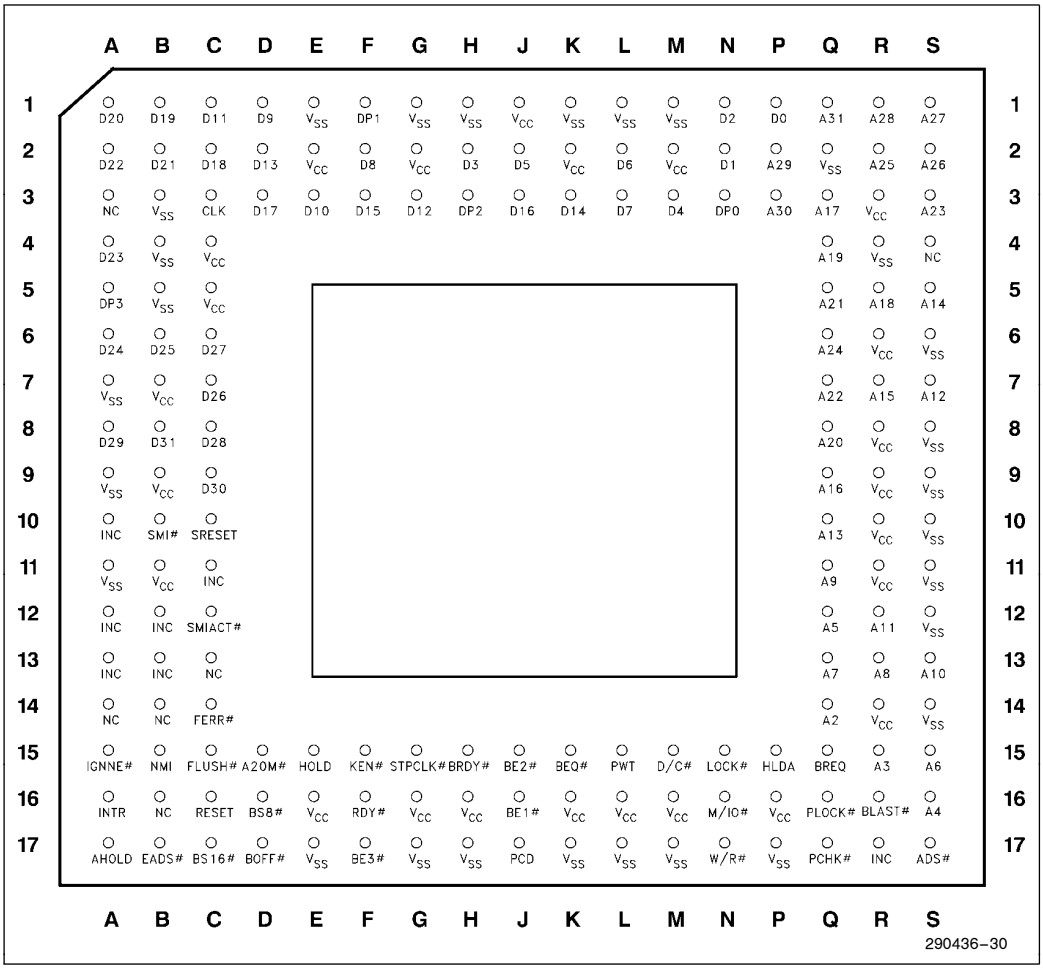


Figure 1-4. 168-Lead PGA Bottom View Pinout (ODPR)

Table 1-1. 169-Lead PGA Pin Cross Reference by Pin Name (ODP)

Address		Data		Control		Control		NC	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	PLOCK#	Q16	A3	B7	A7
A_3	R15	D_1	N2	ADS#	S17	PWT	L15	A14	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	RDY#	F16	B16	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	RESET	C16	C13	C4	B3
A_6	S15	D_4	M3	BE1#	J16	SMI#	B10		C5	B4
A_7	Q13	D_5	J2	BE2#	J15	SMIACT#	C12		E2	B5
A_8	R13	D_6	L2	BE3#	F17	SRESET	C10		E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	STPCLK#	G15		G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	UP#	B14		G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	W/R#	N17		H16	G17
A_{12}	S7	D_{10}	E3	BREQ#	Q15				J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16				K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17				K16	K1
A_{15}	R7	D_{13}	D2	CLK	C3				L16	K17
A_{16}	Q9	D_{14}	K3	D/C#	M15	**Position**			M2	L1
A_{17}	Q3	D_{15}	F3	DP0	N3	KEY	D4		M16	L17
A_{18}	R5	D_{16}	J3	DP1	F1	PLUG	D5		P16	M1
A_{19}	Q4	D_{17}	D3	DP2	H3	PLUG	D13		R3	M17
A_{20}	Q8	D_{18}	C2	DP3	A5	PLUG	D14		R6	P17
A_{21}	Q5	D_{19}	B1	EADS#	B17	PLUG	E4	**INC**	R8	Q2
A_{22}	Q7	D_{20}	A1	FERR#	A13	PLUG	E14		R9	R4
A_{23}	S3	D_{21}	B2	FLUSH#	C15	PLUG	N4	A10	R10	S6
A_{24}	Q6	D_{22}	A2	HLDA	P15	PLUG	N14	A12	R11	S8
A_{25}	R2	D_{23}	A4	HOLD	E15	PLUG	P4	B12	R14	S9
A_{26}	S2	D_{24}	A6	IGNNE#	A15	PLUG	P5	B13		S10
A_{27}	S1	D_{25}	B6	INTR	A16	PLUG	P13	C11		S11
A_{28}	R1	D_{26}	C7	KEN#	F15	PLUG	P14	C14		S12
A_{29}	P2	D_{27}	C6	LOCK#	N15			R17		S14
A_{30}	P3	D_{28}	C8	M/IO#	N16			S4		
A_{31}	Q1	D_{29}	A8	NMI	B15					
		D_{30}	C9	PCD	J17					
		D_{31}	B8	PCHK#	Q17					

NOTES:
1. All NC pins must remain unconnected.
2. Refer to each specific OverDrive section for differences in pin functions.
3. NC = No Connection.
4. INC = Internal No Connect.

Table 1-2. 168-Lead PGA Pin Cross Reference by Pin Name (ODPR)

Address		Data		Control		Control		N/C	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	PLOCK#	Q16	A3	B7	A7
A_3	R15	D_1	N2	ADS#	S17	PWT	L15	A14	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	RDY#	F16	B14	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	RESET	C16	B16	C4	B3
A_6	S15	D_4	M3	BE1#	J16	SMI#	B10	C13	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	SMIACT#	C12		E2	B5
A_8	R13	D_6	L2	BE3#	F17	SRESET	C10		E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	STPCLK#	G15		G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	UP#	C11		G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	W/R#	N17		H16	G17
A_{12}	S7	D_{10}	E3	BREQ#	Q15				J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16				K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17				K16	K1
A_{15}	R7	D_{13}	D2	CLK	C3				L16	K17
A_{16}	Q9	D_{14}	K3	D/C#	M15				M2	L1
A_{17}	Q3	D_{15}	F3	DP0	N3				M16	L17
A_{18}	R5	D_{16}	J3	DP1	F1				P16	M1
A_{19}	Q4	D_{17}	D3	DP2	H3				R3	M17
A_{20}	Q8	D_{18}	C2	DP3	A5			**INC**	R6	P17
A_{21}	Q5	D_{19}	B1	EADS#	B17				R8	Q2
A_{22}	Q7	D_{20}	A1	FERR#	C14			A10	R9	R4
A_{23}	S3	D_{21}	B2	FLUSH#	C15			A12	R10	S6
A_{24}	Q6	D_{22}	A2	HLDA	P15			A13	R11	S8
A_{25}	R2	D_{23}	A4	HOLD	E15			B12	R14	S9
A_{26}	S2	D_{24}	A6	IGNNE#	A15			B13		S10
A_{27}	S1	D_{25}	B6	INTR	A16			R17		S11
A_{28}	R1	D_{26}	C7	KEN#	F15			S4		S12
A_{29}	P2	D_{27}	C6	LOCK#	N15					S14
A_{30}	P3	D_{28}	C8	M/IO#	N16					
A_{31}	Q1	D_{29}	A8	NMI	B15					
		D_{30}	C9	PCD	J17					
		D_{31}	B8	PCHK#	Q17					

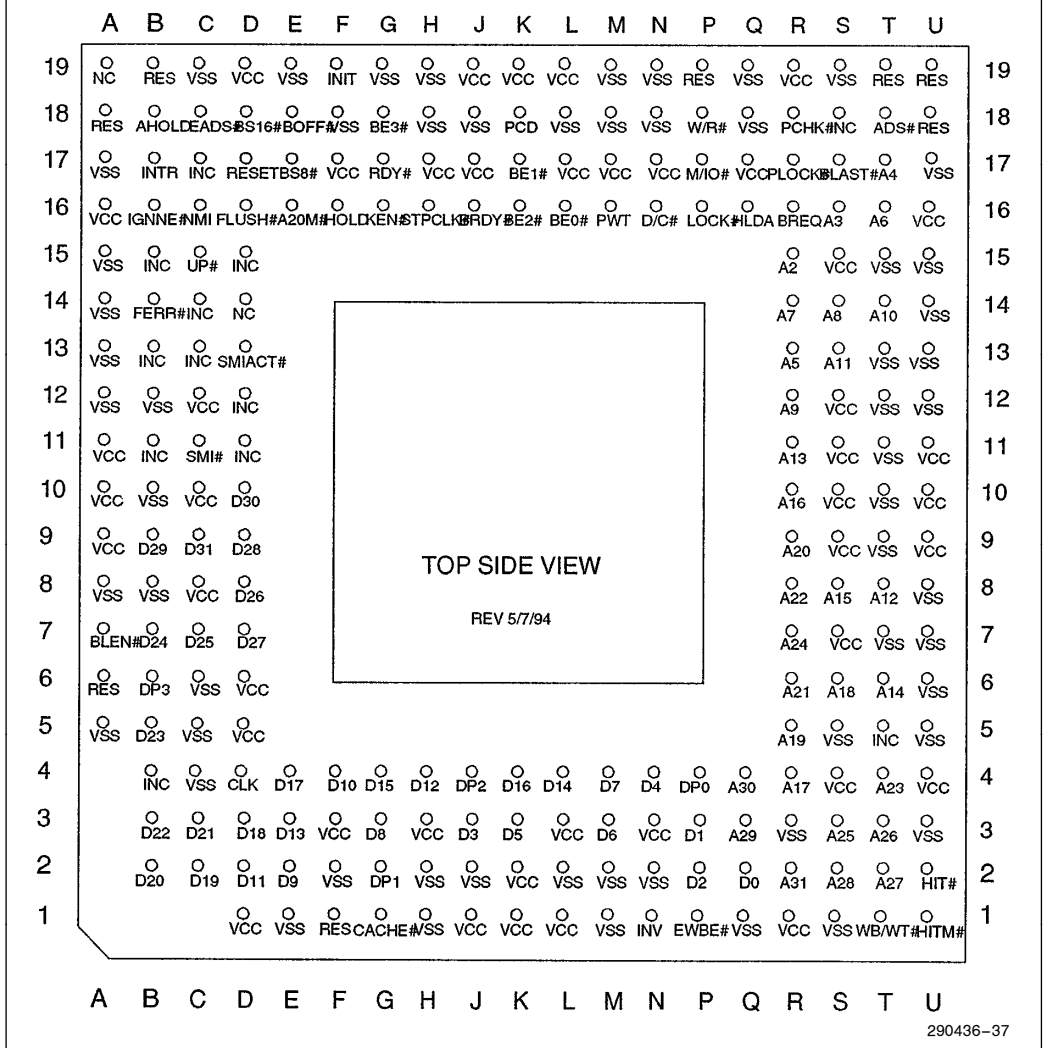
NOTES:
1. All NC pins must remain unconnected.
2. Refer to each specific OverDrive section for differences in pin functions.
3. NC = No Connection.
4. INC = Internal No Connect.

1.2.2 Pentium® OverDrive® PROCESSOR SPECIFICATIONS

The Intel Pentium OverDrive processor socket specifies 237 contacts. The 237 contacts correspond to a standard 240 pin socket with one inside ''KEY'' contact, one outer ''KEY'' contact and four 'orientation' contacts plugged on the outside corner. The inside ''KEY'' contact provides backward compatibility for the IntelDX2 and IntelDX4 OverDrive processors for Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems. The Pentium OverDrive processor itself (not the socket) **does not have** any ''KEY'' pins. The five contacts plugged on the outside corner ensure proper orientation for the Pentium OverDrive processor. The Pentium OverDrive processor pinout is shown in Figures 1-5 and 1-6.

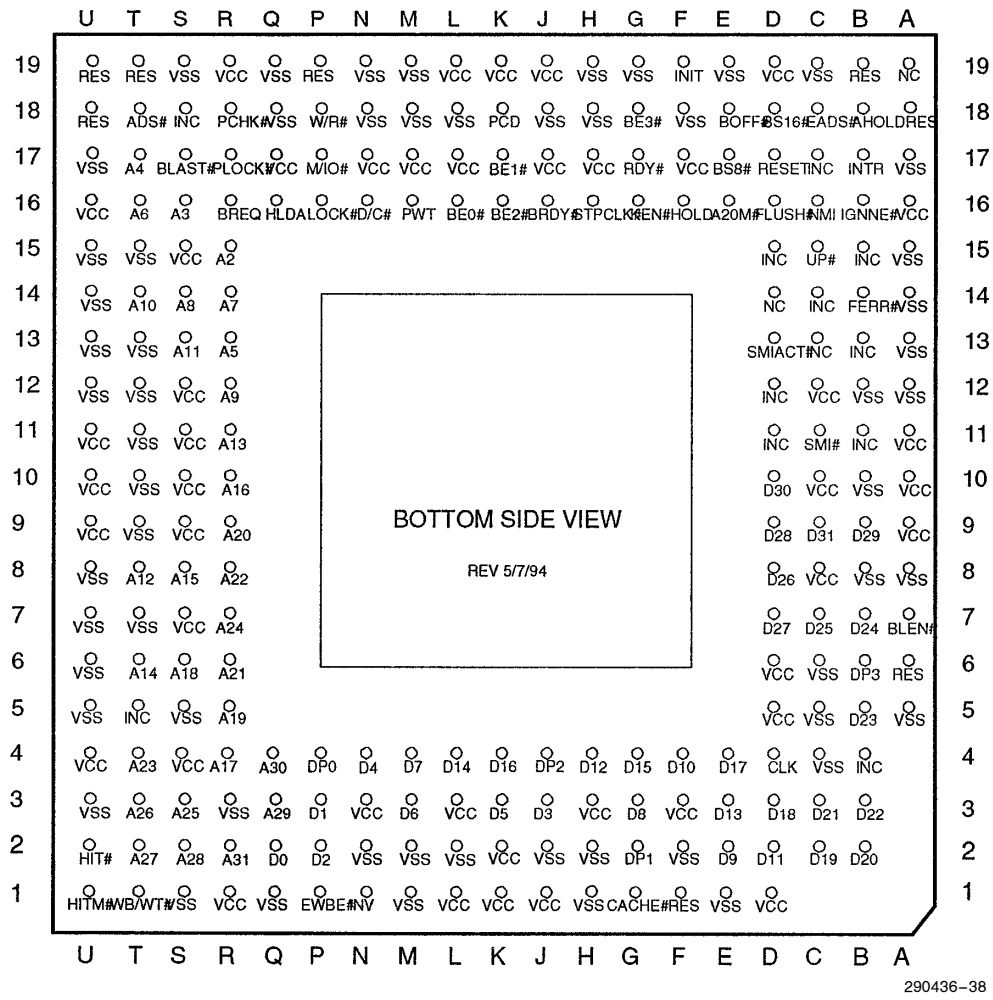
Please note that the boundary scan pins (**TCK, TDO,TDI,** and **TMS**), and all testability pins have been removed from the production version of the Pentium OverDrive processor. An engineering sample will be available that will allow the use of boundary scan and testability functions. For more information on boundary scan and testability pins, please contact Intel.

1.2.2.1 Pentium® OverDrive® Processor Pinout



***NOTE:**
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 1-5. Pentium® OverDrive® Processor Pinout (Top Side View)



*__NOTE:__
Pin A1 is located in the lower left corner to make the labels on the top plate of Intel processors orient right side up. All "RES" and "NC" pins should be left unconnected to insure proper operation.

Figure 1-6. Pentium® OverDrive® Processor Pinout (Bottom Side View)

1.2.2.2 Pin Cross Reference

Table 1-3. Pentium® OverDrive® Processor Pin Cross Reference

Address		Data		Control				N/C	V_{CC}		V_{SS}	
A2	R15	D0	Q2	A20M#	E16	INV	N1	A19	A9	L1	A5	M18
A3	S16	D1	P3	ADS#	T18	KEN#	G16	D14	A10	L3	A8	M19
A4	T17	D2	P2	AHOLD	B18	LOCK#	P16		A11	L17	A12	N2
A5	R13	D3	J3	BE0#	L16	M/IO#	P17	**INC**	A16	L19	A13	N18
A6	T16	D4	N4	BE1#	K17	NMI	C16		C8	M17	A14	N19
A7	R14	D5	K3	BE2#	K16	PCD	K18	B11	C10	N3	A15	Q1
A8	S14	D6	M3	BE3#	G18	PCHK#	R18	B13	C12	N17	A17	Q18
A9	R12	D7	M4	BLAST#	S17	PLOCK#	R17	B4	D1	Q17	B8	Q19
A10	T14	D8	G3	BLEN#	A7	PWT	M16	B15	D5	R1	B10	R3
A11	S13	D9	E2	BOFF#	E18	RDY#	G17	C17	D6	R19	B12	S1
A12	T8	D10	F4	BRDY#	J16	RESET	D17	C13	D19	S4	C4	S5
A13	R11	D11	D2	BREQ	R16	SMI#	C11	C14	F3	S7	C5	S19
A14	T6	D12	H4	BS8#	E17	SMIACT#	D13	D11	F17	S9	C6	T7
A15	S8	D13	E3	BS16#	D18	STPCLK#	H16	D12	H3	S10	C19	T9
A16	R10	D14	L4	CACHE#	G1	UP#	C15	D15	H17	S11	E1	T10
A17	R4	D15	G4	CLK	D4	W/R#	P18	S18	J1	S12	E19	T11
A18	S6	D16	K4	D/C#	N16	WB/WT#	T1	T5	J17	S15	F2	T12
A19	R5	D17	E4	DP0	P4				J19	U4	F18	T13
A20	R9	D18	D3	DP1	G2				K1	U9	G19	T15
A21	R6	D19	C2	DP2	J4				K2*	U10	H1	U3
A22	R8	D20	B2	DP3	B6			**RES**	K19	U11	H2	U5
A23	T4	D21	C3	EADS#	C18			A6		U16	H18	U6
A24	R7	D22	B3	EWBE#	P1			A18			H19	U7
A25	S3	D23	B5	FERR#	B14			B19			J2	U8
A26	T3	D24	B7	FLUSH#	D16			F1			J18	U12
A27	T2	D25	C7	HIT#	U2			P19			L2	U13
A28	S2	D26	D8	HITM#	U1			T19			L18	U14
A29	Q3	D27	D7	HLDA	Q16			U18			M1	U15
A30	Q4	D28	D9	HOLD	F16			U19			M2	U17
A31	R2	D29	B9	IGNNE#	B16							
		D30	D10	INIT	F19							
		D31	C9	INTR	B17							

*If designing for single socket compatibility with future Pentium OverDrive processors, pin K2 may be connected to V_{CC} via a circuit to limit the current through the pin. Please contact Intel for more information about compatibility with future Pentium OverDrive processors.

NOTE:
The Pentium OverDrive processor socket provides orientation guides for IntelDX2 OverDrive processors one ''KEY'' pin in location E5. The Pentium OverDrive processor does not employ this inside ''KEY'' pin, which is left for backwards compatibility, but relies on the keying mechanism in the A1 corner to ensure proper orientation.

2.0 IntelDX2™ OverDrive® PROCESSOR FOR Intel486™ SX AND DX MICROPROCESSOR-BASED SYSTEMS

- **Processor Upgrade for most Intel486™ SX and DX Processor-Based Systems**
  - **— Single-Chip Upgrade**
  - **— Increases Both Integer and Floating Point Performance**
- **Two Package Variations to Support Systems with and without an OverDrive® Processor Socket**
- **169-Lead Pin Grid Array Package**
  - **— Pin Compatible with Intel487™ SX Math CoProcessor**
  - **— 169th Alignment Pin Ensures Proper Chip Orientation**
- **168-Lead Pin Grid Array Package**
  - **— Pin Compatible with Intel486™ DX Processor**
- **Utilizes IntelDX2 Speed-Doubling Technology**
  - **— Processor Core Runs at Twice the Frequency of the System Bus**
  - **— Compatible with 33, 25, 20 and 16 MHz Systems**
- **Floating Point Math Unit Included On-Chip**
- **High Integration Enables On-Chip**
  - **— 8 KByte Code and Data Cache**
  - **— Paged, Virtual Memory Management**
- **Binary Compatible with Large Installed Software Base**
  - **— MS-DOS, OS/2™, Windows**
  - **— UNIX System V/386**
  - **— IRMX, IRMK™ Kernals**
- **High Performance Design**
  - **— Core Clock Speed up to 66 MHz**
  - **— 106 Mbyte/sec Burst Bus**
  - **— CHMOS V Process Technology**
- **Complete 32-Bit Architecture**
  - **— Address and Data Busses**
  - **— Registers**
  - **— 8-, 16-, 32-Bit Data Types**
- **Compatible with Intel SL Enhanced Features**

The IntelDX2 OverDrive processor is the entry-level processor upgrade option offering excellent price/performance for cost-conscious users of most Intel486 SX and DX processor-based systems. Based on Intel's IntelDX2 technology, the IntelDX2 OverDrive processor integrates an integer unit, a floating point unit, a memory management unit, SL Enhanced features and an 8 KByte cache on a single chip.

Using the IntelDX2 processor's speed doubling technology, the IntelDX2 OverDrive processor operates internally at twice the speed of the system bus. This allows users of Intel486 SX and DX microprocessor-based systems to double the frequency of their computer's processor by adding a single chip, without upgrading any other system components. For example, adding an IntelDX2 OverDrive processor to an Intel486 DX 33 MHz system will double the processor's internal operating speed to 66 MHz.

The IntelDX2 OverDrive processor is based on the IntelDX2 microprocessor technology. This technology doubles the clock speed of the internal processor core, while interfacing with the system at the same external clock speed. When installed in a 33 MHz Intel486 SX or DX microprocessor-based system, the internal processor core, integer unit, floating point unit and cache operate at 66 MHz, while the speed of the external bus remains at 33 MHz. This provides increased processor performance while maintaining compatibility with the existing system design.

The IntelDX2 OverDrive processor is currently available in four product versions, which consist of two speed options (50 MHz and 66 MHz) and two package options (168-lead Pin Grid Array (PGA) and 169-lead PGA).

The 50 MHz IntelDX2 OverDrive processor is designed to upgrade 25 MHz Intel486 DX microprocessor-based systems and 16 MHz, 20 MHz and 25 MHz Intel486 SX microprocessor-based systems. The 66 MHz IntelDX2 OverDrive processor is designed to upgrade 33 MHz Intel486 SX and DX microprocessor-based systems. Table 2-1 illustrates the speed and pinout configurations for each system type.

These products come with a (0.25″ high) heat sink attached to the standard 169-lead PGA or 168-lead PGA package to aid in heat dissipation. All IntelDX2 OverDrive processors are binary compatible with a large base of software based on DOS, OS/2, Windows and Unix operating systems.

For more detailed information about the operation of the IntelDX2 OverDrive processor, refer to the IntelDX2 microprocessor data book (Order #241731-001).

Table 2-1. IntelDX2 OverDrive Processor to System Reference Table

OverDrive® Processor Part Number	OverDrive Processor Pinout	Systems Upgraded
DX2ODP50	169	Intel486™ SX -16 MHz -20 MHz -25 MHz
DX2ODP66	169	Intel486 SX -33 MHz
DX2ODPR50	168	Intel486 DX -25 MHz
DX2ODPR66	168	Intel 486 DX -33 MHz

2.1 Socket Configurations

Both single-socket and two-socket system configurations can be upgraded with the IntelDX2 OverDrive processor. In a single-socket Intel486 microprocessor-based system, this is done by replacing the original processor with the OverDrive processor. In a two-socket system, the IntelDX2 OverDrive processor can simply be placed into the empty OverDrive processor socket.

2.2 169-Lead PGA Device (DX2ODP)

The 169-lead version of the IntelDX2 OverDrive processor is currently available in two speeds; 50 MHz (DX2ODP50) and 66 MHz (DX2ODP66). The 169-lead versions are designed to be used in most Intel486 SX processor-based system and contain a key pin to assure proper orientation of the device (refer to Table 2-1). The OverDrive processor is simply inserted into the OverDrive processor socket, while the original processor remains in its socket.

Figure 1-3 shows the bottom-view (pin-side) pinout diagram of the 169-lead Pin Grid Array (PGA) package. Table 1-1 cross references the device's pin numbers to the pin names.

2.3 168-Lead PGA Device (DX2ODPR)

The 168-lead version of the IntelDX2 OverDrive processor is currently available in two speeds; 50 MHz (DX2ODPR50) and 66 MHz (DX2ODPR66). The 168-lead versions are designed to be used in most Intel486 DX processor-based system (refer to Table 2-1). The existing processor is removed and the upgrade processor is simply inserted into the same socket.

Figure 1-4 shows the bottom-view (pin-side) pinout diagram of the 168-lead Pin Grid Array (PGA) package. Table 1-2 cross references the device's pin numbers to the pin names.

3.0 IntelDX4™ OverDrive® PROCESSOR FOR Intel486™ SX AND DX MICROPROCESSOR-BASED SYSTEMS

- **Processor Upgrade for most Intel486™ SX and DX Processor-Based Systems**
  - **— Single-Chip Upgrade**
  - **— Increases Both Integer and Floating Point Performance**
- **Two Package Variations to Support Systems with and without an OverDrive® Processor Socket**
- **169-Lead Pin Grid Array Package**
  - **— Pin Compatible with Intel487™ SX Math CoProcessor**
  - **— 169th Alignment Pin Ensures Proper Chip Orientation**
- **168-Lead Pin Grid Array Package**
  - **— Pin Compatible with Intel486™ DX Processor**
- **High Integration Enables On-Chip**
  - **— 16 KByte Code and Data Cache**
  - **— Paged, Virtual Memory Management**
- **Floating Point Math Unit Included On-Chip**
- **Utilizes IntelDX4 Speed-Tripling Technology**
  - **— Processor Core Runs at Three Times the Frequency of the System Bus**
  - **— Compatible with 33, 25, 20 and 16 MHz Systems**
- **Binary Compatible with Large Installed Software and Operating System Base**
  - **— MS-DOS, OS/2™, Windows**
  - **— UNIX System V/386**
  - **— IRMX, IRMK™ Kernals**
- **High Performance Design**
  - **— Core Clock Speed up to 100 MHz**
  - **— CHMOS V Process Technology**
- **Complete 32-Bit Architecture**
  - **— Address and Data Busses**
  - **— Registers**
  - **— 8-, 16-, 32-Bit Data Types**
- **SL Enhanced Intel486™ Microprocessor Features Included On-Chip**

The IntelDX4 OverDrive processor is an upgrade for most Intel486 SX and DX microprocessor-based systems. It operates at a maximum internal core frequency of 100 MHz and is available in two package versions. When installed in a system, the IntelDX4 OverDrive processor significantly increases both the integer and floating point performance.

The IntelDX4 OverDrive processor offers several new features not found in the IntelDX2 OverDrive processors. It has 16 KByte on-chip cache and the internal core operates at 3x (speed tripled) the external clock frequency. The underlying technology behind the IntelDX4 OverDrive processor is the IntelDX4 microprocessor core with on-package voltage regulation. This allows the OverDrive processor to plug directly into existing 5V systems. Like the IntelDX2 OverDrive processor the IntelDX4 OverDrive processor supports System Management Mode (SMM) and Stop Clock Mode. The SMM and Stop Clock Mode, identical to those implemented in SL Enhanced Intel486 SX and DX microprocessors, make the IntelDX4 OverDrive processor compatible with the advanced power management, system security and device emulation features of SL Enhanced systems.

The IntelDX4 OverDrive processor is based on the IntelDX4 microprocessor technology. This technology triples the clock speed of the internal processor core, while interfacing with the system at the same external clock speed. When installed in a 33 MHz Intel486 SX or DX microprocessor-based system, the internal processor core, integer unit, floating point unit and cache operate at 100 MHz, while the speed of the external bus remains at 33 MHz. This provides increased processor performance while maintaining compatibility with the existing system design. In addition, the internal cache has been doubled to 16 KBytes.

The IntelDX4 OverDrive processor is currently available in four product versions, which consist of two speed options (75 MHz and 100 MHz) and two package options (168-lead Pin Grid Array (PGA) and 169-lead PGA).

The 100 MHz OverDrive processors are designed to upgrade most 33 MHz Intel486 SX and DX microprocessor-based systems. The 75 MHz OverDrive processors are designed to upgrade most 25 MHz Intel486 DX microprocessor-based systems and 16 MHz, 20 MHz and 25 MHz Intel486 SX microprocessor-based systems. Table 3-1 illustrates this. The speed tripling technology will triple the internal speed of the processor to three times the bus speed of the existing system.

These products come with a (0.6″ high) heat sink attached to the standard 169-lead PGA or 168-lead PGA package to aid in heat dissipation. Refer to Sections 14.0 and 15.0 for clearance and thermal requirements. All IntelDX4 OverDrive processors are binary compatible with a large base of software based on DOS, OS/2, Windows and Unix operating systems.

For more detailed information about the operation of the IntelDX4 OverDrive processor, refer to the IntelDX4 microprocessor data book (Order #241944-001).

Table 3-1. IntelDX4 OverDrive Processor to System Reference Table

OverDrive® Processor Part Number	OverDrive Processor Pinout	Systems Upgraded
DX4ODP75	169	Intel486™ SX -16 MHz -20 MHz -25 MHz
DX4ODP100	169	Intel486 SX -33 MHz
DX4ODPR75	168	Intel486 DX -25 MHz
DX4ODPR100	168	Intel 486 DX -33 MHz

3.1 Socket Configurations

Both single-socket and two-socket system configurations can be upgraded with the IntelDX4 OverDrive processor. In a single-socket Intel486 microprocessor-based system, this is done by replacing the original processor with the OverDrive processor. In a two-socket system, the IntelDX4 OverDrive processor can simply be placed into the empty OverDrive processor socket.

3.2 169-Lead PGA Device (DX4ODP)

The 169-lead version of the IntelDX4 OverDrive processor is currently available in two speeds; 75 MHz (DX4ODP75) and 100 MHz (DX4ODP100). The 169-lead versions are designed to be used in most Intel486 SX processor-based system and contain a key pin to assure proper orientation of the device (refer to Table 3-1). The processor is simply inserted into the OverDrive processor socket, while the original processor remains in its socket.

Figure 1-3 shows the bottom-view (pin-side) pinout diagram of the 169-lead Pin Grid Array (PGA) package. Table 1-1 cross references the device's pin numbers to the pin names.

3.3 168-Lead PGA Device (DX4ODPR)

The 168-lead version of the IntelDX4 OverDrive processor is currently available in two speeds; 75 MHz (DX4ODPR75) and 100 MHz (DX4ODPR100). The 168-lead versions are designed to be used in most Intel486 DX processor-based system (refer to Table 3-1). The existing processor is removed and the upgrade processor is simply inserted into the same socket.

Figure 1-4 shows the bottom-view (pin-side) pinout diagram of the 168-lead Pin Grid Array (PGA) package. Table 1-2 cross references the device's pin numbers to the pin names.

4.0 INTEL Pentium® OverDrive® PROCESSOR

- **Powerful CPU Upgrade for most Intel486™ CPU-Based Systems**
  - **— Makes Intel Procesor-Based Systems Run Faster**
  - **— Significantly Accelerates All Software Applications**
- **Designed for Systems Based on:**
  - **— Intel486 SX Processors**
  - **— Intel486 DX Processors**
  - **— IntelSX2™ Processors**
  - **— IntelDX2™ Processors**
- **Compatible with Installed Base of Thousands of Applications**
- **Based on Intel Pentium® Processor Technology**
  - **— Superscalar Architecture**
  - **— Branch Prediction**
  - **— Faster Floating Point Unit**
- **Enhancements to Core Pentium Processor Silicon**
  - **— Separate Code and Data Caches**
  - **— 16 KB Code Cache**
  - **— 16 KB Write-Back Data Cache**
  - **— 32-Bit Bus Interface**
- **Package Innovations**
  - **— On-Package Voltage Regulation**
  - **— Integrated Fan Heat Sink**
- **Incorporates SMM Power Saving Features**

The Pentium OverDrive processor is Intel's highest performance CPU upgrade for systems based on the Intel486 family of CPUs. It is the recommended upgrade option for most IntelSX2 and IntelDX2 CPU-based systems and the superior upgrade option for most Intel486 SX and DX CPU-based systems. The Pentium processor's superscalar architecture (which allows more than one instruction per clock cycle to be executed), the 32 KB enhanced on-chip cache memory and faster floating point unit provide a significant performance boost across a wide range of applications. The specially-designed bus interface unit enables the Pentium OverDrive processor to operate internally at 64 bits while working seamlessly with the 32-bit Intel486 architecture.

The Pentium OverDrive processor may contain certain design defects or errors known as errata. Current characterized errata are available on request.

4.1 Product Description

The Pentium OverDrive processor is designed to upgrade most systems based on Intel486 SX, Intel486 DX, IntelSX2, and IntelDX2 processor-based systems and is based on Intel's Pentium processor technology. It is 100% binary compatible with the 8086/88, 80286, Intel386 DX, Intel386 SX, Intel486 DX, Intel486 SX, IntelSX2, and the IntelDX2 processor family.

The Pentium OverDrive processor provides significant improvements over the Intel486 CPU including:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Separate 16K Code and 16K Data Caches
- Improved Instruction Execution Times
- Write back MESI Protocol implemented in Data Cache
- System Management Mode

The Pentium OverDrive processor significantly increases the integer performance, and can attain up to 2x floating-point performance relative to an equivalent frequency IntelDX2 processor. The bus frequencies for the Pentium OverDrive processor are 25 MHz and 33 MHz.

The Pentium OverDrive processor has two pipelines and a floating-point unit that are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, 2 floating point instructions) in one clock.

The floating-point unit has been completely redesigned over the IntelDX2 processor. Faster algorithms provide at least 3X internal speed-up for common floating point operations including ADD, MUL, and LOAD. With instruction scheduling and overlapped (pipelined) execution, these three performance enhancements can allow many math intensive applications to achieve a 2X performance boost.

The Pentium OverDrive processor implements 32-bit address and data busses.

The Pentium OverDrive processor has separate code and data caches, both are 16 KBytes each. The data cache has write-back capabilities.

The Pentium OverDrive also has an integrated fan heat sink. The heat sink contains logic circuitry which senses if the speed of the fan is insufficient to cool the processor and will reduce the internal frequency of the processor to that of the internal bus. This will allow the processor to run indefinitely without damage.

NOTE:

1. Refer to the *Pentium Processor Data Book* for more information on instruction execution timing and pairing.

5.0 PIN DESCRIPTIONS

5.1 Pins Common to All OverDrive® Processors

Tables 5-1 through 5-4 list pin descriptions of the signals present on the Intel DX2, IntelDX4 OverDrive processors, and are not unique on the Pentium OverDrive processor.

Table 5-1. Pin Descriptions

Symbol	Type	Name and Function
CLK	I	*Clock* provides the fundamental timing for the bus interface unit and is multiplied by two (2x) for the IntelDX2 OverDrive Processors or three (3x) for the IntelDX4 OverDrive Processor to provide the internal frequency for the Intel OverDrive processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31–A4 A2–A3	I/O O	A31–A2 are the *address lines* of the processor. A31–A2, together with the byte enables BE0#–BE3#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the processor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE0–3#	O	The *byte enable* signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24–D31, BE2# applies to D16–D23, BE1# applies to D8–D15 and BE0# applies to D0–D7. BE0#–BE3# are active LOW and are not driven during bus hold.
DATA BUS		
D31–D0	I/O	These are the *data lines* for the Intel OverDrive processor. Lines D0–D7 define the least significant byte of the data bus while lines D24–D31 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP0–DP3	I/O	There is one *data parity* pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the Intel OverDrive processor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the Intel OverDrive processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP0–DP3 should be connected to V_{CC} through a pullup resistor in systems which do not use parity. DP0–DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles.

Table 5-1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
DATA PARITY (Continued)		
PCHK#	O	*Parity Status* is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the microprocessor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.
BUS CYCLE DEFINITION		
M/IO# D/C# W/R#	O O O	The *memory/input-output, data/control* and *write/read* lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted.
		M/IO# D/C# W/R# Bus Cycle Initiated 0 0 0 Interrupt Acknowledge 0 0 1 Halt/Special Cycle 0 1 0 I/O Read 0 1 1 I/O Write 1 0 0 Code Read 1 0 1 Reserved 1 1 0 Memory Read 1 1 1 Memory Write
		The bus definition signals are not driven during bus hold and follow the timing of the address bus. Refer to Section 7.2.11 for a description of the special bus cycles.
LOCK#	O	The *bus lock* pin indicates that the current bus cycle is locked. The Intel OverDrive processor will not allow a bus hold when LOCK# is asserted (but address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when RDY# is returned. LOCK# is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active.
PLOCK#	O	The *pseudo-lock* pin indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating point long reads and writes (64 bits), segment table descriptor reads (64 bits), in addition to cache line fills (128 bits). The Intel OverDrive processor will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. However during the first bus cycle of a 64-bit floating point write, both PLOCK# and BLAST# will be asserted. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock RDY# is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	The *address status* output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock as the addresses are driven. ADS# is active LOW and is not driven during bus hold.

Table 5-1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
BUS CONTROL (Continued)		
RDY#	I	The *non-burst ready* input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the Intel OverDrive processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the processor while AHOLD is active. RDY# is active LOW, and is not provided with an internal pullup resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.
BURST CONTROL		
BRDY#	I	The *burst ready input* performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely interrupted BRDY# is active LOW and is provided with a small pullup resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	The *burst last* signal indicates that the next time BRDY# is returned the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	The **RESET** input forces the processor to begin execution at a known state. Reset is asynchronous, but must meet setup and hold times t20 and t21 for recognition in any specific clock. The processor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper AC and DC specifications. However, for soft resets, RESET should remain active for at least 15 CLK periods. The RESET pin should remain active during this time to ensure proper processor operation. RESET is active HIGH. RESET sets the SMBASE descriptor to a default address of 30000H. If the system uses SMBASE relocation, then the SRESET pin should be used for soft resets.
SRESET	I	The SRESET pin duplicates all the functionality of the RESET pin with the following two exceptions: 1. The SMBASE register will retain its previous value. 2. If UP# (I) is asserted, SRESET will not have an effect on the host microprocessor. For soft resets, SRESET should remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

Table 5-1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
INTERRUPTS (Continued)		
SMI#	I	The **System Management Interrupt** input is used to invoke the System Management Mode (SMM). SMI# is a falling edge triggered signal which forces the processor into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The processor will latch the falling edge of one pending SMI# signal while the processor is executing an existing SMI. The nested SMI will not be recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	The **System Management Interrupt ACTive** is an active low output, indicating that the processor is operating in SMM. It is asserted when the processor begins to execute the SMI state save sequence and will remain active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	The **SToP CLocK request** input signal indicates a request has been made to turn off the CLK input. When the processor recognizes a STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, empty all internal pipelines and the write buffers and generate a Stop Grant acknowledge bus cycle. STPCLK# is active LOW and is provided with an internal pull-up resistor. STPCLK# is asynchronous but setup and hold times t_{20} and t_{21} must be met to ensure recognition in any specific clock.
INTR	I	The *maskable interrupt* indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The Intel OverDrive processor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pulldown resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	The *non-maskable interrupt* request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pulldown resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
BUS ARBITRATION		
BREQ	O	The *internal cycle pending* signal indicates that the Intel OverDrive processor has internally generated a bus request. BREQ is generated whether or not the Intel OverDrive processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	The *bus hold request* allows another bus master complete control of the Intel OverDrive processor bus. In response to HOLD going active the Intel OverDrive processor will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The Intel OverDrive processor will remain in this state until HOLD is deasserted. HOLD is active high and is not provided with an internal pulldown resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

Table 5-1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
BUS ARBITRATION (Continued)		
HLDA	O	*Hold acknowledge* goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Intel OverDrive processor has given the bus to another local bus master. HLDA is driven active in the same clock that the Intel OverDrive processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.
BOFF#	I	The *backoff* input forces the Intel OverDrive processor to float its bus in the next clock. The microprocessor will float all pins normally floated during bus hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The microprocessor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	The *address hold* request allows another bus master access to the Intel OverDrive processor's address bus for a cache invalidation cycle. The Intel OverDrive processor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pulldown resistor. For proper operation AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	This signal indicates that a *valid external address* has been driven onto the Intel OverDrive processor address pins. This address will be used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pullup resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	The *cache enable* pin is used to determine whether the current cycle is cacheable. When the Intel OverDrive processor generates a cycle that can be cached and KEN# is active, the cycle will become a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pullup resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	The *cache flush* input forces the Intel OverDrive processor to flush its entire internal cache. FLUSH# is active low and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. FLUSH# being sampled low in the clock before the falling edge of RESET causes the Intel OverDrive processor to enter the tri-state test mode.
PAGE CACHEABILITY		
PWT PCD	O O	The *page write-through* and *page cache disable* pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for cycles that are not paged, PWT and PCD reflect the state of the PWT and PCD bits in control register 3. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C# and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.

Table 5-1. Pin Descriptions (Continued)

Symbol	Type	Name and Function
NUMERIC ERROR REPORTING		
FERR#	O	The *floating point error* pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# will not go active if FP errors are masked in FPU register. FERR# is active LOW, and is not floated during bus hold.
IGNNE#	I	When the *ignore numeric error* pin is asserted the Intel OverDrive processor will ignore a numeric error and continue executing non-control floating point instructions, but FERR# will still be activated by the Intel OverDrive processor. When IGNNE# is deasserted the Intel OverDrive processor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
BUS SIZE CONTROL		
BS16# BS8#	I I	The *bus size 16* and *bus size 8* pins (bus sizing pins) cause the Intel OverDrive processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Intel OverDrive processor to determine the bus size. These signals are active LOW and are provided with internal pullup resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	When the *address bit 20 mask* pin is asserted, the Intel OverDrive processor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte which occurs on the 8086. A20M# is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled high at the falling edge of RESET.
i486 DX AND i486 SX PROCESSOR INTERFACE		
UP#(1,2)	O	The *upgrade present* pin is used to signal the Intel486 Microprocessor to float its outputs and get off the bus. It is active low and is never floated. UP# is driven low at power-up and remains active for the entire duration of the Upgrade Processor operation.
KEY PIN		
KEY(2)		The KEY pin is an electrically non-functional pin which is used to ensure correct Upgrade Processor orientation in a 169-pin socket.

NOTE:
1. The UP# pin was previously named the MP# pin in the i486 SX Microprocessor/i487 SX Math CoProcessor data book. The functionality is the same, only the name has changed.
2. The UP# input pin and KEY pin are not defined on the OverDrive processor for replacement of PGA Intel486 DX Microprocessor (ODPR).

Table 5-2. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE0#–BE3#	LOW	Bus Hold
PWT, PCD	HIGH	Bus Hold
W/R#, D/C#, M/IO#	HIGH	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR#	LOW	
SMIACT#	LOW	
UP#	LOW	
A2–A3	HIGH	Bus, Address Hold

Table 5-3. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK		
RESET	HIGH	Asynchronous
HOLD	HIGH	Synchronous
AHOLD	HIGH	Synchronous
EADS#	LOW	Synchronous
BOFF#	LOW	Synchronous
FLUSH#	LOW	Asynchronous
A20M#	LOW	Asynchronous
BS16#, BS8#	LOW	Synchronous
KEN#	LOW	Synchronous
RDY#	LOW	Synchronous
BRDY#	LOW	Synchronous
INTR	HIGH	Asynchronous
NMI	HIGH	Asynchronous
SRESET	HIGH	Asynchronous
SMI#	LOW	Asynchronous
STPCLK#	LOW	Asynchronous
IGNNE#	LOW	Asynchronous

Table 5-4. Input/Output Pins

Name	Active Level	When Floated
D0–D31	HIGH	Bus Hold
DP0–DP3	HIGH	Bus Hold
A4–A31	HIGH	Bus, Address Hold

5.2 Pentium® OverDrive® Processor Pin Descriptions

This section provides a summary of the Pentium OverDrive processor pins and how they function. For more information on the pinout differences between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor, please see Appendix B.

5.2.1 SIGNAL DESCRIPTIONS

Table 5-5 provides a brief pin description.

Table 5-5. Signal Description

Symbol	Type	Name and Function
INTERRUPTS		
INIT	I	The **INIT** pin is the Pentium OverDrive processor initialization pin. Since the SL-enhanced Intel486 processors implement this functionality on the **SRESET** pin, the corresponding pin (D11) on the Pentium OverDrive Processor is defined as an **INC** pin so that pin F19 and pin D11 may be tied together on the motherboard. **INIT** will force the Pentium OverDrive Processor to begin execution in a known state. The processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and the SMM base register retain whatever values they had prior to **INIT. INIT** may NOT be used in lieu of **RESET** after power-up. **INIT** can not be used to cause the processor to enter BIST or Tri-State Test Mode. INIT is an edge triggered interrupt and is processed at instruction boundaries. Since **INIT** is an interrupt, **ADS**# may be driven even if **INIT** is active. Recognition of **INIT** is guaranteed in a specific clock if it is asserted synchronously and meets setup and hold times. To guarantee recognition if **INIT** is asserted asynchronously, it must have been deasserted for a minimum of two clocks before being returned active to the processor and remain asserted for a minimum pulse width of two clocks. **INIT** must remain active for three clocks prior to the **BRDY**# or **RDY**# of I/O write cycle to guarantee the processor recognizes and performs **INIT** right after I/O write instruction. **INIT** is asynchronous but must meet setup and hold times t_{20} and t_{21} to be recognized on any one clock. **INIT** is supplied with an internal pull-down.
CACHE CONTROL		
WB/WT#	I	This pin allows a cache line to be defined as *write back or write through* on a line by line basis. As a result, it controls the MESI state that the line is saved in. This pin is sampled in the clock in which the first **BRDY**# or **RDY**# is returned for a read cycle or a write through cycle. However, it must the meet setup and hold times at every clock. Cache lines are not allocated on write through cycles. This pin is also used as a configuration pin at the falling edge of **RESET** only. If **WB/WT**# is driven low, or left unconnected, the processor will operate in a **standard bus (write through only)** mode. This means that the Pentium OverDrive processor will run in an IntelDX2 processor compatible write through cache mode. If **WB/WT**# is driven high, the processor will operate in enhanced bus **(write back)** mode. **INIT** can not be used to change the mode of the processor with **WB/WT**#**.** During **RESET, WB/WT**# should be held at its desired value for two clocks before and after the falling edge of **RESET. WB/WT**# is ignored when the processor is in **standard bus** mode. Please see Appendix A for a detailed description of the two modes of operation. **WB/WT**# has an internal pull down resistor to force the processor into the **standard bus** mode if left unconnected. The pin timings must meet setup and hold times t_{38} and t_{39} on every clock edge.

Table 5-5. Signal Description (Continued)

Symbol	Type	Name and Function
CACHE INQUIRE		
EWBE#	I	The *External Write Buffer Empty* pin, when inactive (HIGH), indicates that a write through cycle is pending in the external system. When the processor generates a non-write back cycle, and **EWBE#** is sampled inactive, the processor will hold off all subsequent writes to all E- or M- state lines until all write-through cycles have completed, as indicated by **EWBE#** going active. This ensures that writes are visible from outside the processor in the same order as they were generated by software. When the Pentium OverDrive processor serializes instruction execution through the use of a serializing instruction, it waits for **EWBE#** to go active before fetching and executing the next instruction. **EWBE#** is sampled with each **BRDY#** or **RDY#** of a write through cycle. If sampled inactive, the processor will repeatedly sample **EWBE#** in each clock until it is found active. Once sampled active, it will ignore **EWBE#** until the next **BRDY#** or **RDY#** of a write cycle. **EWBE#** is not sampled and has no effect on processor operation while the processor is in standard bus mode. If unused, **EWBE#** should be tied LOW or left unconnected. **EWBE#** is active low and must meet setup and hold times t_{38} and t_{39} and is supplied with an internal pull-down.
HIT#	O	This pin participates in an inquire cycle. If an inquire cycle hits a valid line in the processor, this pin is asserted two clocks after **EADS#** has been driven to the processor. If the inquire cycle misses in the processor cache, this pin is negated two clocks after **EADS#.** This pin changes its value only as a result of inquire cycle as described above and retains its value between any two inquire cycles.
HITM#	O	**HITM#** is asserted when an inquire cycle hits a modified line in the Pentium OverDrive processor. It can be used to inhibit another bus master from accessing the data until the line is completely written back. **HITM#** is asserted two clocks after an **EADS#** assertion hits a modified line in the processor cache and deasserts after the last **BRDY#** or **RDY#** of the corresponding write back is returned. **HITM#** is guaranteed to be deasserted before the next **ADS#** following a write back cycle. If an INVD instruction occurs at the same time as an external snoop, **HITM#** may be asserted and deasserted without a corresponding **ADS#** for a write back cycle.
CACHE BURST CONTROL		
BLEN#	I	**BLEN#** controls if write back cycles will be attempted to run as burst cycles. When **BLEN#** is HIGH, the processor will write out a dirty line as four separate writes, each with its own **ADS#** and **BLAST#.** When **BLEN#** is LOW, a write back is done as a 16 byte burst. **BLEN#** is a constant input, meaning that it will have to be tied HIGH or LOW. As a result, it does not have setup and hold time specifications. **BLEN#** is has no effect and is not sampled when the processor is in **standard bus** mode. **BLEN#** is supplied with an internal pull-up resistor.
CACHE#	O	The **CACHE#** pin is used to indicate a cache operation. **CACHE#** will be active along with the first **ADS#** until the first **RDY#/BRDY#** and is undefined during any other time period. On cacheable read accesses, **CACHE#** will be asserted when **PCD** is low, except on locked cycles. **CACHE#** will always be asserted in the beginning of cacheable reads (line fills and code prefetches) and can be used as an indication that the processor intends to perform a linefill. For write cycles, **CACHE#** is active for write backs only. The beginning of a replacement write back can be uniquely identified by the presence of **ADS#, W/R#** and **CACHE#** together. The beginning of a snoop write back is marked by **ADS#, W/R#, CACHE#** and **HITM#** being active together.

Table 5-5. Signal Description (Continued)

Symbol	Type	Name and Function
INC PINS		
INC		The **INC** pin is defined to be an *internal no-connect*. This means that the pin is not connected internally, and may be used for the routing of external signals. It will never be used for any other function, and is guaranteed to remain an **INC** pin. Any voltage level applied to an **INC** pin must remain within the processor V_{CC} specifications. Most **INC** pins have a specified use in creating a design that supports multiple processors in one socket. For more information, please see Section 9.

5.2.2 OUTPUT PINS

Table 5-6 lists all the output pins, indicating their active level, and when they are floated.

Table 5-6. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE3#–BE0#	LOW	Bus Hold, Backoff
PWT, PCD	HIGH	Bus Hold, Backoff
W/R#, D/C#, M/IO#	LOW	Bus Hold, Backoff
LOCK#	LOW	Bus Hold, Backoff
PLOCK#	LOW	Bus Hold, Backoff
ADS#	LOW	Bus Hold, Backoff
BLAST#	LOW	Bus Hold, Backoff
PCHK#	LOW	
FERR#	LOW	
SMIACT#	LOW	
A3–A2	HIGH	Bus Hold, Address Hold and Backoff
HIT#, HITM#	LOW	
CACHE#	LOW	Bus Hold, Backoff
UP#	LOW	

5.2.3 INPUT PINS

Table 5-7 lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Table 5-7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
CLK				
RESET	HIGH	Asynchronous		
HOLD	HIGH	Synchronous		
AHOLD	HIGH	Synchronous	PULLDOWN	
EADS#	LOW	Synchronous	PULLUP	
BOFF#	LOW	Synchronous	PULLUP	
FLUSH#	LOW	Asynchronous	PULLUP	
A20M#	LOW	Asynchronous	PULLUP	
BS16#, BS8#	LOW	Synchronous	PULLUP	
KEN#	LOW	Synchronous	PULLUP	
RDY#	LOW	Synchronous		
BRDY#	LOW	Synchronous	PULLUP	
INTR	HIGH	Asynchronous		
NMI	HIGH	Asynchronous		
IGNNE#	LOW	Asynchronous	PULLUP	
BLEN#	LOW	Tie High or Low	PULLUP	
EWBE#	LOW	Synchronous	PULLDOWN	BRDY#/RDY#
INIT	HIGH	Asynchronous	PULLDOWN	
INV	HIGH	Synchronous	PULLUP	EADS#
STPCLK#	LOW	Asynchronous	PULLUP	
SMI#	LOW	Asynchronous	PULLUP	
WB/WT#	BOTH	Synchronous	PULLDOWN	FIRST RDY#/RDY#

5.2.4 INPUT/OUTPUT PINS

Table 5-8 lists all the input/output pins, indicating their active level, and when they are floated.

Table 5-8. Input/Output Pins

Name	Active Level	When Floated
D31–D0	HIGH	Bus Hold, Backoff
DP3–DP0	HIGH	Bus Hold, Backoff
A31–A4	HIGH	Bus, Address Hold, Backoff

5.3 Architecture Block Diagram

5.3.1 IntelDX2™ AND IntelDX4™ OverDrive® PROCESSORS

Figure 5-1 shows a block diagram of the IntelDX2 and IntelDX4 OverDrive Processor Architecture. There are a few minor architectural differences between each of the OverDrive processors. These differences are summarized below, with respect to Figure 5-1.

The IntelDX4 OverDrive processor contains a clock tripling circuit, as opposed to the clock doubling circuit used in the IntelDX2 OverDrive processors. This is located in the upper left of the diagram.

The IntelDX4 OverDrive processor contains a 16 KByte cache, as opposed to the 8 KByte cache used in the IntelDX2 OverDrive processors. This is located in the center of the diagram.

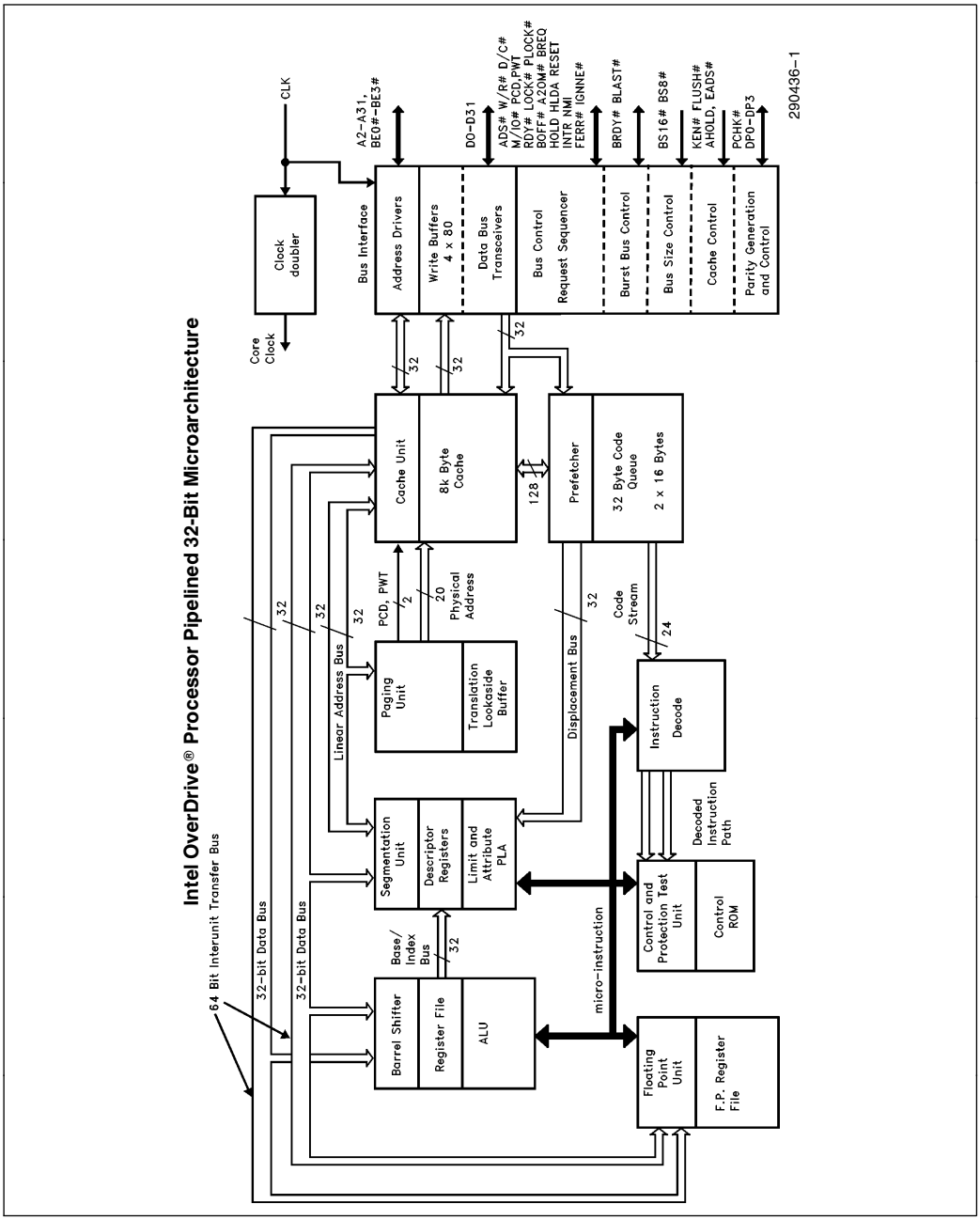


Figure 5-1. OverDrive® Processor Architecture Block Diagram

5.3.2 INTEL Pentium® OverDrive® PROCESSOR

Figure 5-2 shows the Pentium OverDrive processor's two pipelines and floating-point unit that are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating point instruction (under certain circumstances, 2 floating point instructions) in one clock.

The floating-point unit has been completely redesigned over the IntelDX2 processor. Faster algorithms provide at least 3X internal speed-up for common floating point operations including ADD, MUL, and LOAD. With instruction scheduling and overlapped (pipelined) execution, these three performance enhancements can allow many math intensive applications to achieve a 2X performance boost.

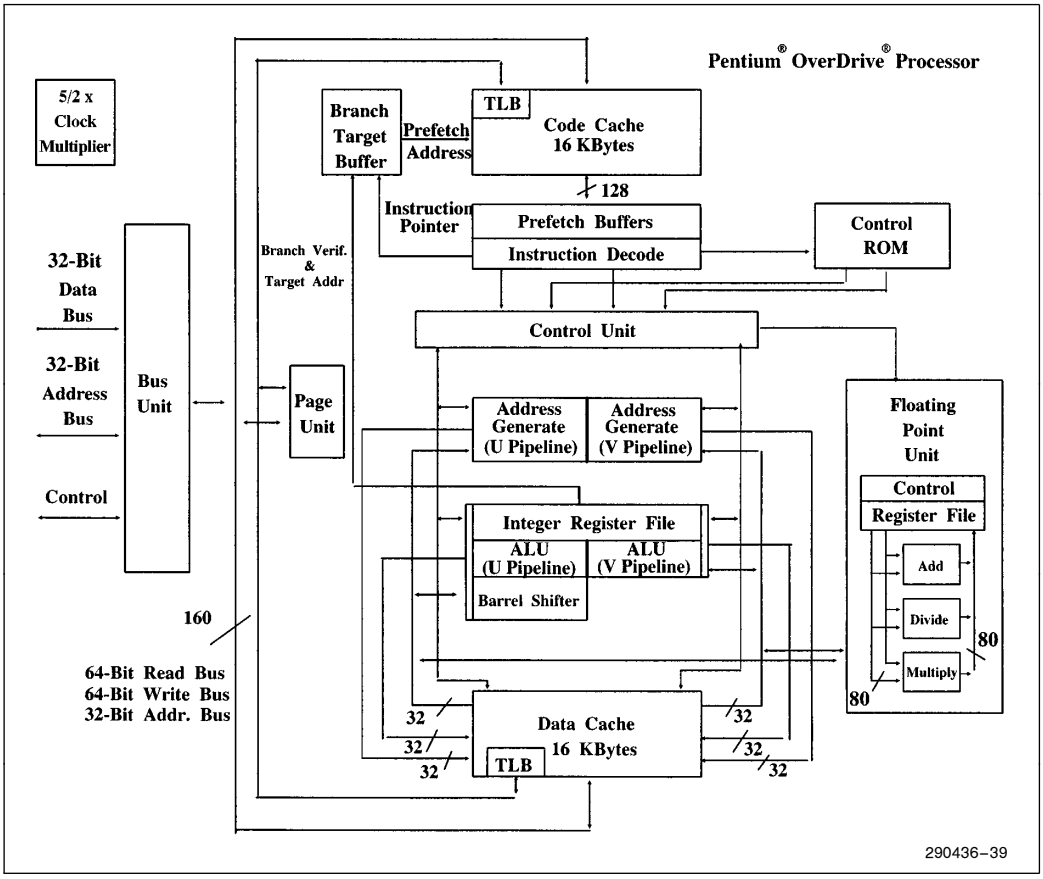


Figure 5-2. Pentium® OverDrive® Processor Block Diagram

The Pentium OverDrive processor implements 32-bit address and data busses.

The block diagram shows that the Pentium OverDrive processor contains two instruction pipelines, the ''u'' pipe and the ''v'' pipe. Both the u- and the v-pipes execute integer instructions, while only the u-pipe executes floating point instructions. The one exception is the FXCH instruction which may also be executed in the v-pipe. Therefore, the Pentium OverDrive processor is capable of executing two integer instructions in each clock, or one floating point instruction in each clock. Floating point instructions can be paired in certain conditions(1). Each pipeline has its own address generation logic, arithmetic logic unit and data cache interface.

NOTE:

1. Refer to the *Pentium Processor Data Book* for more information on instruction execution timing and pairing.

Note that there are two separate caches, a code cache and a data cache. The data cache has three tag ports, one for each of the two pipes and one dedicated to handle snoops from other processors. It has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium OverDrive processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so that the Pentium OverDrive processor can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium OverDrive processor architecture. The control ROM unit has direct control over both pipelines.

6.0 DIFFERENCES IN FUNCTIONALITY BETWEEN THE IntelDX2™ AND IntelDX4™ OverDrive® PROCESSOR FAMILY AND THE Intel486™ SX AND Intel486™ DX PROCESSORS

The IntelDX2 and IntelDX4 OverDrive processors are an enhanced family of Intel486 microprocessors. There are, however, four functional differences. First, the IntelDX2 and IntelDX4 OverDrive processors have an internal clock doubling (IntelDX2) or clock tripling (IntelDX4) circuit which decreases the time required to execute instructions. Second, the IntelDX2 and IntelDX4 OverDrive processor family does not support the JTAG boundary scan test feature. Third, the IntelDX2 and IntelDX4 OverDrive processors have different processor revision identifications than the Intel486 SX or Intel486 DX processors. Finally, the IntelDX4 OverDrive processor contains a 16 KByte cache, as opposed to the 8 KByte cache on the IntelDX2 OverDrive processors. These four differences are described in the following sections, according to how they affect the processor functionality.

6.1 Hardware Interface

The bus of the Intel OverDrive processors has been designed to be identical to the Intel486 Microprocessor bus. Although the external clock is internally doubled or tripled, and data and instructions are manipulated in the processor core at twice or three times the external frequency, the external bus is functionally identical to that of the Intel486 processor.

The four boundary scan test signals (TCK, Test clock; TMS, Test Mode select; TDI, Test Data Input; TDO, Test Data Output), defined for some Intel486 processors, are not specified for the Intel486 DX2 OverDrive processor.

The UP# (Upgrade Present) signal, which is defined as an input for some Intel486 processors, is an output signal on the Intel OverDrive processor. The UP# pin on the Intel OverDrive processor provides a logical low output signal which can be used to enable logic to recognize and configure the system for the Intel OverDrive processor. This signal is identical to the MP# output defined for the Intel487 SX Math CoProcessor.

The DX register always contains the component identifier at the conclusion of RESET. The Intel OverDrive processor has a different revision identifier in the DL register than the Intel486 SX or Intel486 DX microprocessors (refer to Section 11.1). When the OverDrive processor is installed in a system the component identifier is supplied by the OverDrive processor, rather than the original processor. The stepping identification portion of the component identification will change with different revisions of the OverDrive processor. The designer should only assume that the component identification for the OverDrive processor will be 043x for the IntelDX2 OverDrive processor and 148x or 048x for the IntelDX4 OverDrive processor, where "x" is the stepping identifier.

6.2 Testability

As detailed in Section 6.1, the Intel OverDrive processor does not support the JTAG boundary scan testability feature.

6.3 Instruction Set Summary

The Intel OverDrive processor supports all Intel486 extensions to the 8086/80186/80286 instruction set. In general, instructions will run faster on the Intel OverDrive processors than on the Intel486 microprocessor. Specifically, an instruction that only uses memory from the on-chip cache executes at the full core clock rate while all bus accesses execute at the bus clock rate. To calculate the elapsed time of an instruction, the number of clock counts for that instruction must be multiplied by the clock period for the system. The instruction set clock count summary tables from the Intel486 SX and Intel486 DX Microprocessor Data Sheets can be used for the OverDrive processor with the following modifications:

— Clock counts for a cache hit: This value represents the number of internal processor core clocks for an instruction that requires no external bus accesses or the base core clocks for an instruction requiring external bus accesses.

— Penalty clock counts for a cache miss: This value represents the worst-case approximation of the additional number of external clock counts that are required for an instruction which must access the external bus for data (a cache miss). This number must be multiplied by 2 (for the IntelSX2 and IntelDX2 OverDrive processors) or 3 (for the IntelDX4 OverDrive processor) to convert it to an equal number of internal processor core clock counts and added to the base core clocks to compute the number of core clocks for this instruction.

The actual number of core clocks for an instruction with a cache miss may be less than the base clock counts (from the cache hit column) plus the penalty clock counts (2 times the cache miss column number for the IntelSX2 and IntelDX2, 3 times the cache miss column number for the IntelDX4). The clock counts in the cache miss penalty column can be a cumulative value of external bus clocks (for data reads) and internal clocks for manipulating the data which has been loaded from the external bus. The number of clocks which are related to external bus accesses are correctly represented in terms of internal core clocks by multiplying by two. However, the clock counts related to internal data manipulation should not be multiplied by two. Therefore the total number of processor core clock counts for an instruction with a cache miss represents a worst-case approximation.

To calculate the execution time for an OverDrive processor instruction, multiply the total processor core clock counts by the core clock period. For example, in a 25 MHz system upgraded with a 50 MHz IntelDX2 OverDrive processor, the core clock period is 20 ns (1/50 MHz).

Additionally, the assumptions specified below should be understood in order to estimate instruction execution time.

A cache miss will force the OverDrive processor to run an external bus cycle. The Intel486 microprocessor 32-bit burst bus is defined as r−b−w.

Where:

r = The number of bus clocks in the first cycle of a burst read or the number of clocks per data cycle is a non-burst read.

b = The number of bus clocks for the second and subsequent cycles in a burst read.

w = The number of bus clocks for a write.

The fastest bus the OverDrive processor can support is 2−1−2 assuming 0 waits states. The clock counts in the cache miss penalty column assume a 2−1−2 bus. For slower busses add r−2 clocks to the cache miss penalty for the first dword accessed. Other factors also affect instruction clock counts.

Instruction Clock Count Assumptions

1. The external bus is available for reads or writes at all times. Else add bus clocks to reads until the bus is available
2. Accesses are aligned. Add three core clocks to each misaligned access.
3. Cache fills complete before subsequent accesses to the same line. If a read misses the cache during a cache fill due to a previous read or prefetch, the read must wait for the cache fill to complete. If a read or write accesses a cache line still being filled, it must wait for the fill to complete.
4. If an effective address is calculated, the base register is not the destination register of the preceding instruction. If the base register is the destination register of the preceding instruction add 1 to the core clock counts shown. Back-to-back PUSH and POP instructions are not affected by this rule.
5. An effective address calculation uses one base register and does not use an index register. However, if the effective address calculation uses an index register. 1 core clock may be added to the clock shown.
6. The target of a jump is in the cache. If not, add r clocks for accessing the destination instruction of a jump. If the destination instruction is not completely contained in the first dword read, add a maximum of 3b bus clocks. If the destination instruction is not completely contained in the first 16 byte burst, add a maximum of another r+3b bus clocks.
7. If no write buffer delay, w bus clocks are added only in the case in which all write buffers are full.
8. Displacement and immediate not used together. If displacement and immediate used together, 1 core clock may be added to the core clock count shown.
9. No invalidate cycles. Add a delay of 1 bus clock for each invalidate cycle if the invalidate cycle contends for the internal cache/external bus when the OverDrive processor needs to use it.
10. Page translation hits in TLB. A TLB miss will add 13, 21 or 28 bus clocks + 1 possible core clock to the instruction depending on whether the Accessed and/or Dirty bit in neither, one or both of the page entries needs to be set in memory. This assumes that neither page entry is in the data cache and a page fault does not occur on the address translation.
11. No exceptions are detected during instruction execution. Refer to interrupt core Clock Counts Table for extra clocks if an interrupt is detected.
12. Instructions that read multiple consecutive data items (i.e., task switch, POPA, etc.) and miss the cache are assumed to start the first access on a 16-byte boundary. If not, an extra cache line fill may be necessary which may add up to (r+3b) bus clocks to the cache miss penalty.

7.0 DIFFERENCES BETWEEN THE Intel486™ FAMILY AND THE Pentium® OverDrive® PROCESSOR

This section covers the differences between the Intel486 family of microprocessors and the Pentium OverDrive processor.

7.1 Software

The Pentium OverDrive processor is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2*, and UNIX*. In addition to being binary compatible with the Intel architecture based processors which preceded the Pentium processor, it can also run programs which have been compiled to utilize Pentium processor instructions. This allows pairing of instructions to take advantage of the Superscalar Architecture and adds floating point instructions if replacing an Intel486 SX or IntelSX2 processor.

7.2 Hardware

The Pentium OverDrive processor is in a 235-Pin Grid Array package while the Intel486 family uses a 168-Pin Grid Array package. These extra pins are used for extra power and ground pins, including separate power and ground for the fan heatsink, also the internal cache write-back signals are on these pins.

8.0 DIFFERENCES BETWEEN THE Pentium® PROCESSOR AND THE Pentium® OverDrive® PROCESSOR

There are several differences between the Pentium processor and the Pentium OverDrive processors. These differences are covered in the next two sections.

8.1 Software

The following paragraphs are provided as a reference for software differences between the Pentium OverDrive processor and the Pentium processor. Unless otherwise stated, it can be assumed that the Pentium OverDrive processor will have the same software characteristics as the Pentium processor. For more information on the software characteristics of the Pentium Processor, please see the *Pentium Processor Data Book* or *Programmers Reference Manual*.

The Pentium OverDrive processor does not support machine check exception. As a result, CR4.MCE is not useful. It will be forced to a zero by the hardware. However, any attempt by the software to set this bit to 1 will not create a general protection exception.

The Pentium OverDrive processor allows two different page sizes: 4 KB and 4 MB. Please contact Intel for more information on the use of 4 MB pages.

The behavior of INVD, WBINVD and INVPLG instructions are similar to the Pentium processor. If the processor is in **the enhanced bus mode,** the WBINVD instruction will write back all dirty lines first, flush the cache and run two special cycles (the write back special cycle followed by the flush special cycle) on the bus. INVD will flush the cache and run one special cycle (The flush special cycle) on the bus. INVD will not write back the dirty lines, if any. All three instructions are privileged level 0 and should be executed by BIOS or operating system code only.

On the IntelDX2 processor, when paging is disabled, and/or when instructions that are not affected by paging are executed, the **PCD** and **PWT** pins are driven with values from CR3.PCD and CR3.PWT bits, respectively. On the Pentium OverDrive processor, when paging is disabled and/or when instructions that are not affected by paging are executed, the **PWT** pin will be drive LOW and the **PCD** pin will reflect the value of the CR0.CD bit.

When the CPUID instruction is performed with EAX = 1, the Pentium OverDrive processor will return the following values to the EDX register. These bits indicate what features the processor has.

The various bit positions have the following meaning:

Table 8-1. Feature Bit Assignment

Bit	Value	Meaning
0	1	FPU: Floating Point Unit On-Chip
1	1	VME: Virtual-8086 Mode Enhancements
2	1	DE: Debugging Extensions
3	1	PSE: Page Size Extension
4	1	TSC: Time Stamp Counter
5	1	MSR: Pentium Processor-Style MSR
6	R	Reserved
7	R	Reserved
8	1	CX8: CMPXCHG8B Instruction
9–31	R	Reserved

A value of ''R'' means that the corresponding bit is reserved and the software should not depend on its value.

8.2 Hardware

This section covers the hardware differences between the Pentium processor and the Pentium OverDrive processor.

The Pentium processor has a 64-bit data bus while the Pentium OverDrive processor has a 32-bit data bus. This is required in order for the Pentium OverDrive processor to work in an Intel486 architecture based system.

The size of the data bus requires a similar decrease in the internal cache line size. A burst memory access is four bus widths of data this is the length of each line in the cache. For an Intel486 based architecture system that is 16-Bytes, for a Pentium processor based system this is 32-bytes. The internal cache in the Pentium processor is expecting 32-bytes. This would require two burst reads. Therefore the cache line size was reduced to 16-bytes wide.

The cache on the Pentium processor is split into two 8 KByte caches. One is for data and the other is the instruction or code cache. The Pentium OverDrive processor keeps the idea of two separate caches but increases the size to 16 KBytes each.

The Pentium OverDrive processor does not have the JTAG boundry scan capabilities that the Pentium processor has.

The package is different. The Pentium processor is packaged in a 273-Pin Grid Array while the Pentium OverDrive processor uses a 235-Pin Grid Array package.

The Pentium OverDrive processor has the integrated fan heatsink attached. This integrated fan informs the processor if the fan has slowed or stopped. This reduces the internal frequency to 1x multiplier from the previous 2.5x. The part can run indefinitely at the lower frequency without incurring any damage. This allows the Pentium OverDrive processor to continue in the system until a replacement fan can be installed.

9.0 IntelDX2™ AND IntelDX4™ OverDrive® PROCESSOR CIRCUIT DESIGN

9.1 Upgrade Circuit for Intel486™ Processor-Based Systems with UP#

Figure 9-1 shows the IntelDX2 and IntelDX4 OverDrive processor socket circuit for Intel486 processor-based systems using UP#. The Upgrade Present input, UP# pin, allows the Intel486 processor to directly recognize when the Intel OverDrive processor socket is populated. When the UP# pin is driven active to the Intel486 processor, the Intel486 processor tri-states all of its output pins and enters power-down mode.

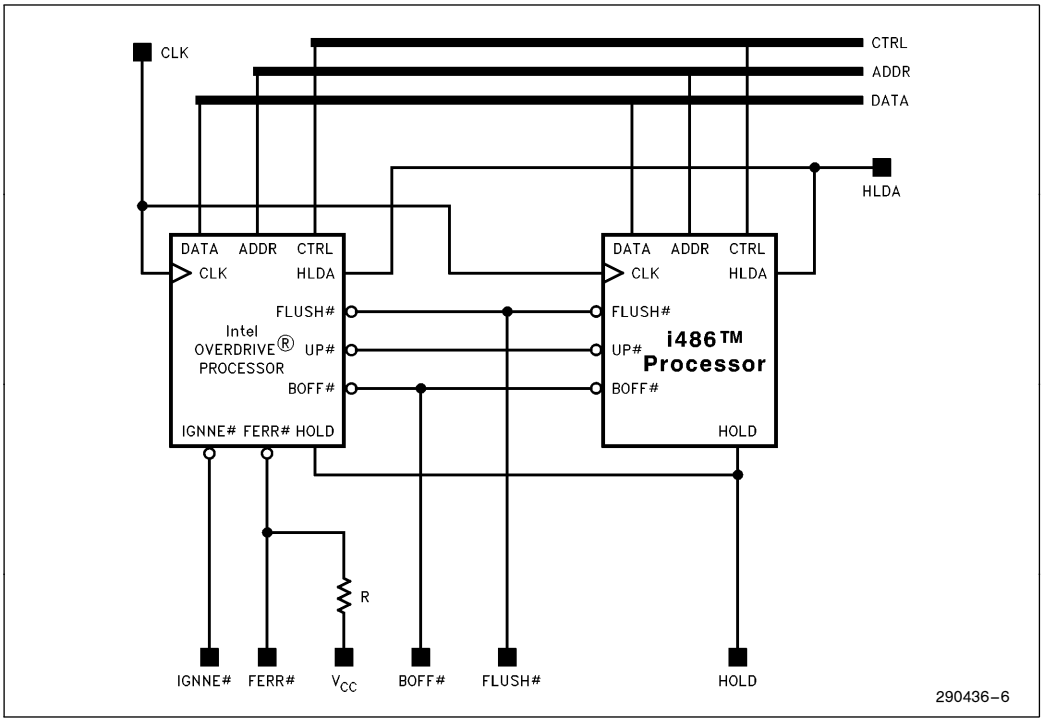


Figure 9-1. Intel OverDrive® Socket Circuit Diagram for Systems Based on Intel486™ Processors That Have the UP# Input Pin

10.0 Pentium® OverDrive® PROCESSOR DESIGN CONSIDERATIONS

10.1 Hardware Design Considerations

10.1.1 INTRODUCTION

This section describes the organization of the Translation Lookaside Buffers (TLBs), write buffers and the buffering scheme used in the Pentium OverDrive processor. Other important Pentium OverDrive Processor design specific details are also included as well as the use of the **WB/WT#** pin as an input to determine the fundamental cache operation mode of the processor.

10.1.1.1 Cache Consistency Cycles

The external system can check and invalidate cache lines in the internal processor cache using inquire cycles (snooping). Snooping allows the external system to keep cache coherency throughout the system. Snoop cycles may be performed using **AHOLD, BOFF#,** or **HLDA** and then asserting **EADS#** to inform the processor that the snoop address is available on the bus. The following table summarizes the snoop mechanism initiated by any of these three control signals.

The snoop cycle begins by checking whether a particular cache line has been ''cached'' and invalidates the line based on the state of the **INV** pin. If the Pentium OverDrive processor is configured in the Standard Bus Mode, the processor will always invalidate the cache line on snoop hits. If the processor is configured in the Enhanced Bus Mode, the system must drive **INV** high to invalidate a particular cache line. The Pentium OverDrive processor will invalidate the line and write back an E-state line if the system snoop hits either S-state, E-state, or M-state line, provided **INV** was driven high during **EADS#** assertion. If **INV** is driven low, a modified line will be written back to memory and will remain in the cache as a write-back line. If **INV** is driven low, a shared line also will continue to remain in the cache as a shared line.

Table 10-1. Snoop Cycles under AHOLD, BOFF#, or HLDA

AHOLD	Tri-states the address bus. **ADS#** will be asserted under **AHOLD** only to initiate a snoop writeback cycle. An ongoing burst cycle will complete under an **AHOLD.** For non-burst cycles, a specific non-burst transfer (**ADS# – RDY#** transfer) will complete under **AHOLD** and will be fractured (interrupted) before the next assertion of **ADS#.** A snoop writeback cycle will be reordered ahead of a fractured non-burst cycle. Should an **ADS#** be required to start the next cycle while **AHOLD** is asserted, the processor will only perform snoop write back cycles. If the processor issues and **ADS#** while **AHOLD** is asserted, it is the responsibility of the system to determine the address of the snoop write back from the snoop address driven with **EADS#.** An interrupted non-burst cycle will be completed only after the snoop writeback cycle is completed, provided there are no other snoop writeback cycles scheduled and **AHOLD** is deasserted. If **BLEN#** is driven inactive (disabling bursted writes), the processor will drive four individual **ADS# – RDY#** cycles to complete the cycle while **AHOLD** is active.
BOFF#	Overrides **AHOLD;** takes effect in the next clock. Ongoing bus cycles will stop in the clock following **BOFF#** being asserted and resumes when **BOFF#** is deasserted, in the same manner as the standard Intel486 processor bus. A snoop writeback will be reordered ahead of the backed off cycle. The snoop writeback cycle begins after **BOFF#** is deasserted followed by any backed off cycle.
HOLD	**HOLD** will be acknowledged only between bus cycles, except for a non-cacheable, non-bursted code prefetch cycle. In a non-cacheable, non-bursted code prefetch cycle, **HOLD** is acknowledged after the system returns **RDY#** or if **BOFF#** is asserted. Once **HLDA** is active, the processor blocks all bus activities until the system releases the bus (by de-asserting **HOLD**).

After asserting **AHOLD** or **BOFF#,** the external master driving a snoop cycle must wait at least two clocks before asserting **EADS#.** If snooping is done after **HLDA** assertion, then the master performing a snoop must wait for at least one clock cycle before driving the snoop addresses and asserting **EADS#. INV** should be driven low during bus master read operations to minimize invalidations. **INV** should be driven high to invalidate a cache line during bus master write operations. The Pentium OverDrive processor asserts **HIT#** and **HITM#** if the cycle hits an M state line in the cache or **HIT#** only if the cycle hits an E or S state line. These output signals become valid two clock periods after **EADS#** is valid on the bus. **HITM#** will remain asserted at least until the last **RDY#** or **BRDY#** of the snoop writeback cycle is returned. The **HIT#** signal will continue to drive the result of the last snoop until the next external snoop occurs. Most timing diagrams in the following sections do not include the **HIT#** signal since it is not necessary for single processor system designs. Snoop operations may interrupt an ongoing bus operation in both the Standard Bus Mode and Enhanced Bus Mode.

The Pentium OverDrive processor can accept EADS# in every clock period while in the Standard Bus Mode. In the Enhanced Bus Mode, the processor can accept EADS# every other clock period until the external snoop hits an M-state line. Any **EADS#** assertion after the **EADS#** that hit a modified line will be ignored. The processor will not accept any further **EADS#** assertions until the snoop writeback operation is completed and **HITM#** is deasserted. Figure 10-1 shows the allowable **EADS#** window for the different snooping mechanisms (**AHOLD, HOLD, BOFF#**). **For the Enhanced bus mode, EADS# must not be asserted outside the windows presented in the diagrams below.**

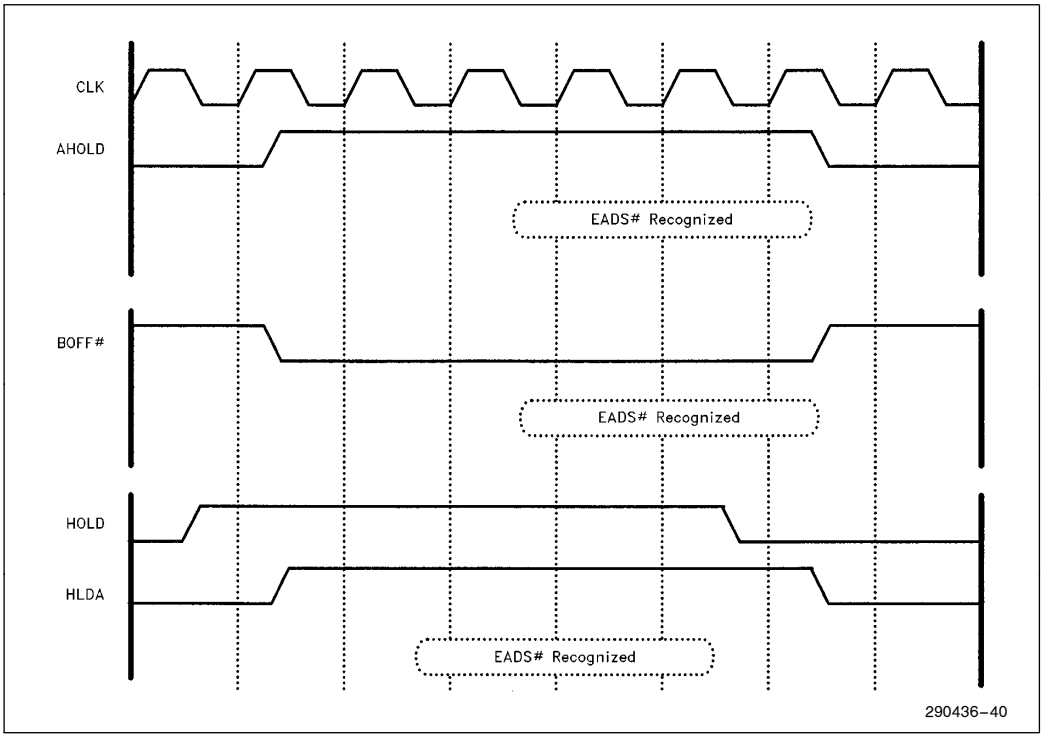


Figure 10-1. EADS# Snooping Window

Figure 10-2 shows that the processor can accept an **EADS#** assertion only every other clock while in enhanced bus mode.

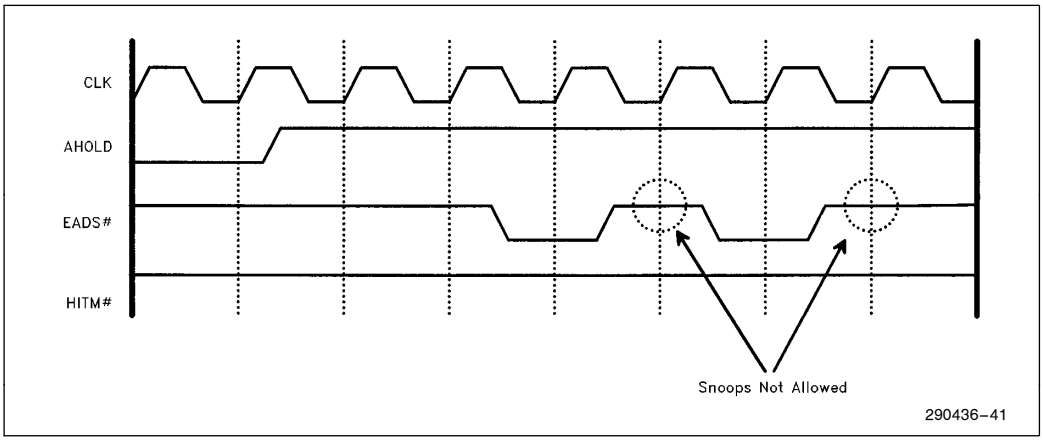


Figure 10-2. EADS# Snooping Frequency in Enhanced Bus Mode

10.1.1.2 Write Back Cycles

Writeback cycles may be bursted or non-bursted by returning **RDY#** or **BRDY#.** All writeback operations write 16 bytes of data to memory corresponding to the modified line in the cache. **BS8# and BS16# are not allowed during writeback cycles.**

The state of **BLEN#** determines how a 16 byte line is written back. When **BLEN#** is LOW, the write back is done as a 16-byte burst transfer. **BRDY#** or **RDY#** may terminate each transfer. At the fourth transfer, **BLAST#** will signify the end of the write back. A write back when **BLEN#** is LOW but **RDY#** is used rather than **BRDY#** is shown in Figure 10-4. When **BLEN#** is HIGH, the 16-byte write back will be done as four consecutive 4 byte writes, each with its own **ADS#** and **BLAST#.** (See Figure 10-5).

BLEN# is not a dynamic pin since it cannot be toggled on a cycle per cycle basis. It cannot be changed once power has been applied to the system, so it should be tied HIGH or LOW.

The **CACHE#** pin is used to indicate that a cache operation is taking place. **CACHE#** is active with the first **ADS#** for both write backs and line fills, and is terminated by the first **RDY#/BRDY#.** An occurrence of **ADS#** = 0, **W/R#** = 1, and **CACHE#** = 0 indicates that a replacement write back is starting. The occurrence of **HITM#** = 0 during the above operation signifies that a snoop write back is occurring. Write back cycles begin at address 0x0 of the 16-byte line being pushed out. The burst order is the standard Intel486 Processor order of 0x0, 0x4, 0x8 and 0xC. If the write back is done as four separate writes, then each write will push out four bytes starting at byte 0x0. **PCD** and **CACHE#** are low during write back cycles, while **KEN#** is ignored.

BS8#, BS16# are ignored during write back cycles. After the last **BRDY#/RDY#** of a write back cycle is asserted, the Pentium OverDrive Processor will wait at least one **CLK** before issuing the next **ADS#.** In other words, a dead clock is inserted by the processor after the last transfer in a write back cycle. The dead clock is between the last **BRDY#/RDY#,** and the next **ADS#.** The dead clock appears only after the write back is complete, so there are no dead clocks between individual transfers of a write back. This dead clock time is used by the Pentium OverDrive processor to complete internal cache operations.

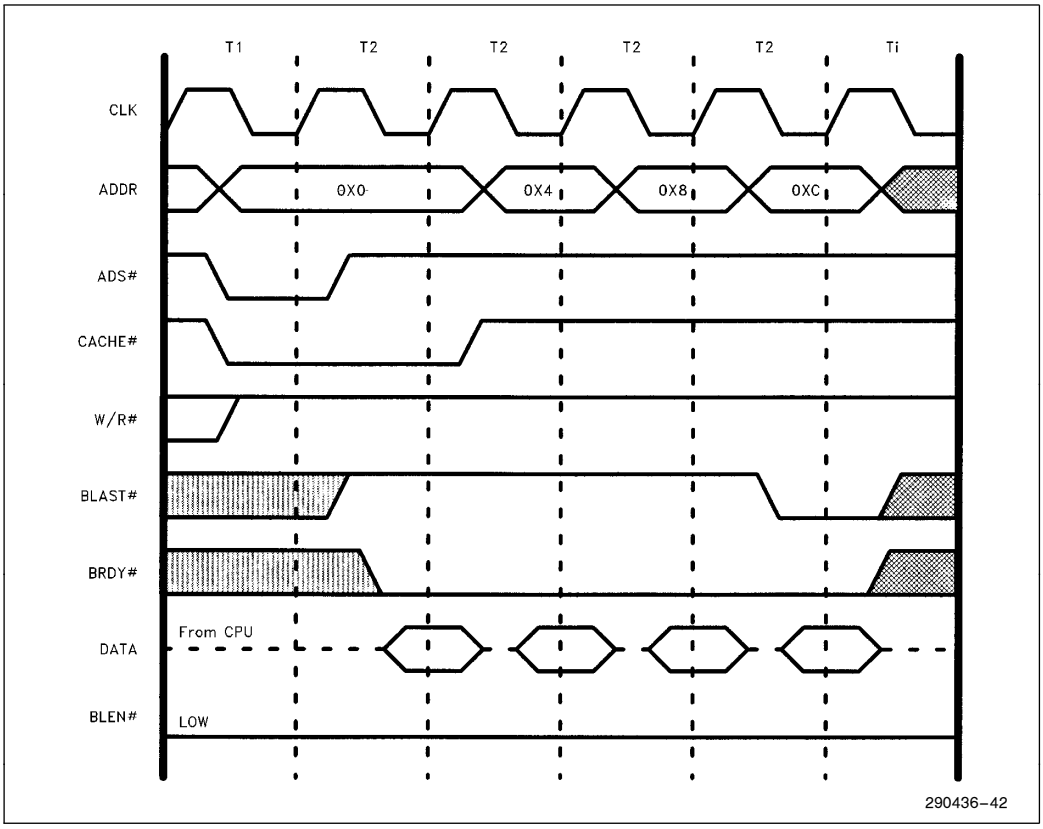


Figure 10-3. Write Back Operation—BLEN# Active

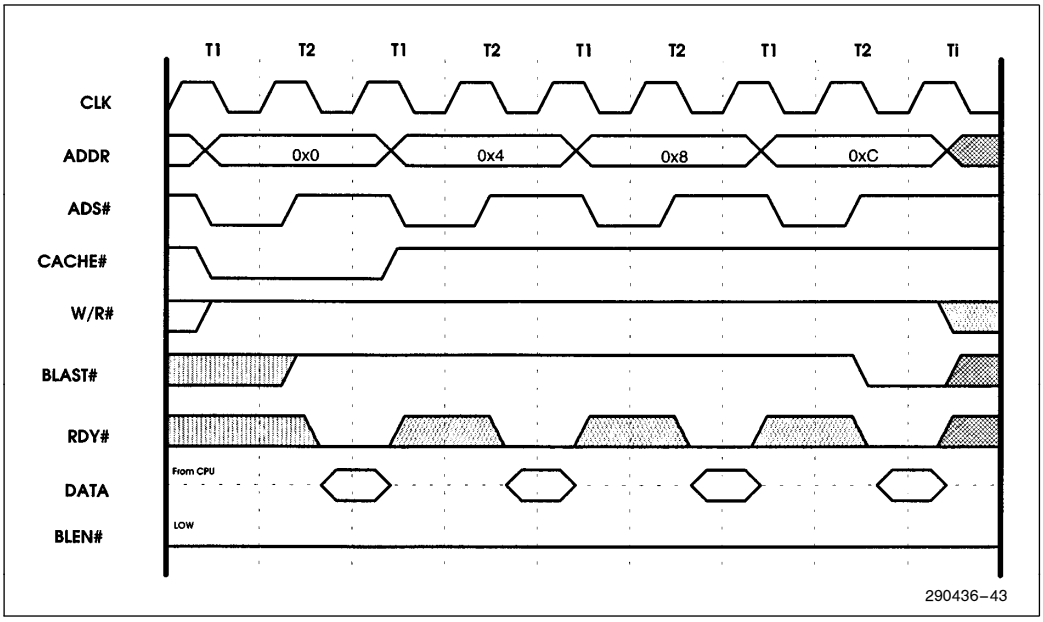


Figure 10-4. Write Back with BLEN# Active Using RDY#

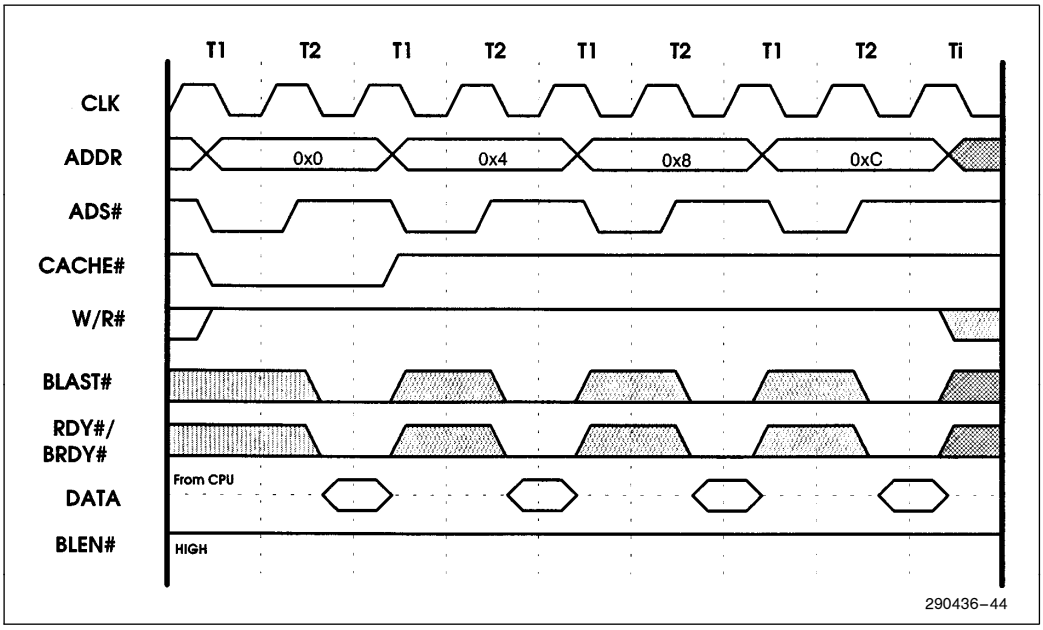


Figure 10-5. Write Back as Four 4-Byte Transfers (BLEN# Inactive)

10.1.2 WB/WT# AS AN INITIALIZATION INPUT

To make the Pentium OverDrive processor more compatible with the IntelDX2 processor, several small enhancements have been added to the processor to help distinguish different processor modes of operation. These two modes will be referred to as **"standard bus mode" (Write through processor cache only)** and "enhanced bus mode" (Write back processor enabled and are discussed in the following paragraphs.

In order to allow the Pentium OverDrive processor to operate in more of an IntelDX2 processor manner, the **WB/WT#** pin is used as an initialization input to configure the operating mode of the processor. At the falling edge of **RESET,** the processor can be configured to operate in a write through only (IntelDX2 CPU compatible) L1 cache mode (**standard bus** mode), or in a write back L1 cache mode (enhanced bus mode). Once a mode is selected, the processor will continue to operate in the selected mode and can only be changed to a different mode by starting the **RESET** process again. Assertion of **INIT** will not change the operating mode of the processor. **WB/WT#** has an internal pulldown that will force any design that leaves **WB/WT#** unconnected into the write through mode of operation. Table 10-2 lists the two modes of operation and the differences between them.

For more information on the effect of the mode operation on the various signals mentioned above, please see the *Intel486 Microprocessor Family Data Book*. Unless otherwise mentioned, all other functions of the Pentium OverDrive processor remain identical in both operating modes.

10.1.3 INIT FUNCTIONALITY

INIT behaves like an edge triggered interrupt on the Pentium OverDrive processor while in both enhanced bus mode (**WB/WT#** = HIGH at **RESET**) and standard bus mode (**WB/WT#** = LOW at **RESET**). Therefore, when **INIT** is asserted, there is a high probability that one or more bus cycles will be run by the processor while **INIT** is HIGH. The following figures demonstrate two scenarios of how the processor can issue an **ADS#** while **INIT** is asserted. Although the figures assume that an initial I/O write causes the **INIT** to be asserted by the support logic, these cases apply whenever **INIT** is HIGH. The first figure describes cycles being run by the processor before **INIT** is recognized. The second details cycles being run after **INIT** has been recognized.

Figure 10-6 shows the **INIT** signal being triggered by an I/O write. Even though **INIT** is asserted immediately, there is a pending prefetch which executes before the **INIT** is recognized.

Table 10-2. Effects of WB/WT# Initialization

State of WB/WT# at Reset Falling	Affect on Processor Operation
WB/WT# = LOW	Processor is in **Standard Bus** Mode ** IntelDX2 Processor Compatible ** 1: No Special **FLUSH#** Acknowledge Cycles are run on the bus after the assertion of the FLUSH# pin. 2: When **FLUSH#** is asserted, the caches will be invalidated in 15–20 system **CLKs**. 3: All Write Back specific inputs are ignored—(**BLEN#, EWBE#, WB/WT#, INV**) 4: **EADS#** is sampled at any time.
WB/WT# = HIGH	Processor is in **Enhanced Bus** Mode ** Intel486 Processor Write Back Bus Operation ** 1: The special **FLUSH#** Acknowledge Cycles will be run on the bus after the assertion of the **FLUSH#** and all the cache write backs (if any) are complete. 2: Write backs will be performed if a cache flush is requested (i.e.: **FLUSH#, WBINVD** inst . . .). The flush will take about 2000+ clocks. The system must watch for the FLUSH# special cycles to determine the end of the flush. 3: **WB/WT#** is sampled on a line by line basis to determine the storage state of a cache line on reads and writes. 4: The **BLEN#, EWBE#** and **INV** are no longer ignored. 5: **EADS#** is sampled only when the processor is an a **HOLD, AHOLD,** or **BOFF#** state. 6: **PLOCK#** is inactive and driven HIGH.

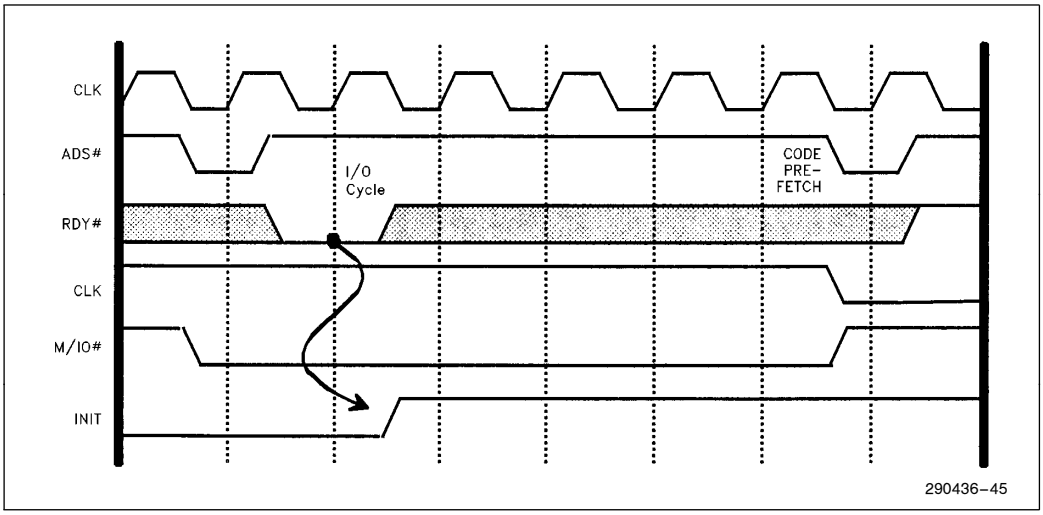


Figure 10-6. ADS# Issued during INIT: Case 1

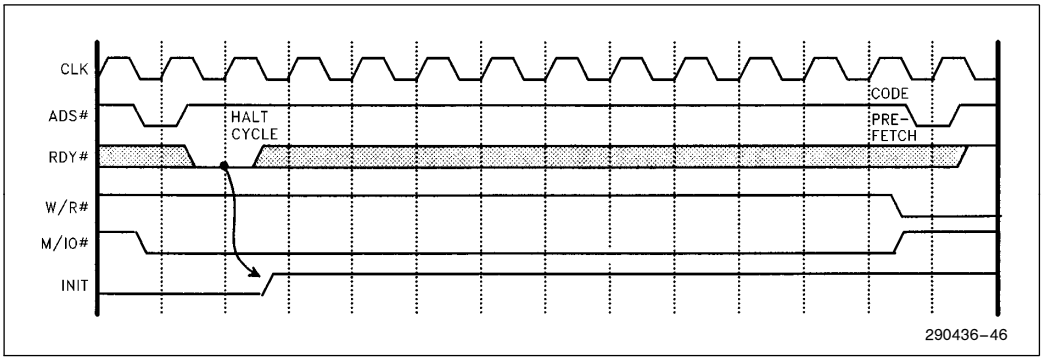


Figure 10-7. ADS# Issued during INIT: Case 2

Figure 10-7 assumes that an I/O cycle was used to generate the **INIT,** but the system waited until all bus activity had stopped (by monitoring the HALT special cycle) before asserting the **INIT** pin. In this case, the processor recognizes **INIT,** and starts a prefetch before **INIT** is deasserted. The prefetch may be from any location, and not necessarily the F..F0h address, even though **INIT** has been recognized.

On other Intel486 write through cache processors (Write-Back Enhanced IntelDX2 in standard bus mode and SL-Enhanced CPUs), the **SRESET** pin is executed immediately, in a manner similar to the **RESET** pin. This means that no cycles will be run after **SRESET** is asserted on these processors. With the Pentium OverDrive processor, it is the responsibility of the system to ensure that any cycles that are issued while INIT is active are completed properly to prevent data corruption, lost bus cycles or system lock-ups.

10.1.4 INSTRUCTION PREFETCH

The Pentium OverDrive processor contains a prefetch buffer of several bytes, and can prefetch a significant number of bytes beyond the end of the last executed instruction. In addition, the processor implements a dynamic branch prediction algorithm which speculatively runs code fetch cycles to addresses corresponding to instructions executed some time in the past. Such code fetch cycles are run based on past execution history, regardless of whether the instructions retrieved are relevant to the currently executing instruction sequence.

The effect of both mechanisms is that the Pentium OverDrive processor may run code fetch bus cycles to retrieve instructions which are never executed. Although the opcodes retrieved are discarded, the system must complete the code fetch bus cycle by returning **RDY#/BRDY#.** It is particularly important that the system return **RDY#/BRDY#** for all code fetch cycles, regardless of the address.

Furthermore, it is possible that the processor may run speculative code fetch cycles to addresses beyond the end of the current code segment. Although the processor may prefetch beyond the CS limit, it will not attempt to execute beyond the CS limit, it will raise a GP fault instead. Thus, segmentation cannot be used to prevent speculative code fetches to inaccessible areas of memory. On the other hand, the processor will never run code fetch cycles to inaccessible pages, so the paging mechanism guards against both the fetch and execution of instructions in inaccessible pages.

If the processor has been placed in a halt state with the **HLT** instruction, and the processor has issued the halt cycle, or the processor has run a shutdown cycle, one of the methods of exiting this condition is to assert an interrupt. Once the interrupt is asserted, the Pentium OverDrive processor may issue a prefetch before the interrupt is acknowledged with an interrupt cycle, or the action desired by the interrupt is performed. For example, if the processor is in a halt state, and the **FLUSH#** interrupt is asserted, the processor could exit the halt state, perform a prefetch, and then start driving the write backs for the flush operation. Prefetches of this type may be run after any interrupt, including **INTR.**

For memory reads and writes, both segmentation and paging prevent the generation of bus cycles to inaccessible regions of memory.

10.2 Upgrade Circuit Design

10.2.1 DUAL PROCESSOR SITE DESIGN

The Pentium OverDrive processor can reside on the same processor bus as an Intel486 processors. The Pentium OverDrive processor specifies a **UP#** output (Upgrade Present) pin which should be connected directly to the **UP#** input pin of the Intel486 microprocessor. When the Pentium OverDrive processor occupies the Pentium OverDrive processor socket, the UP# signal (active low) forces the Intel486 microprocessor to tri-state all outputs and reduce power consumption. When the Pentium OverDrive processor is not present, a pull-up resistor, internal to the Intel486 microprocessor, drives **UP#** inactive and allows the Intel486 microprocessor to control the processor bus.

10.2.2 SINGLE PROCESSOR SITE DESIGN

A single processor site is defined as a system design that can accept all Intel486 processors in a single socket location. Doing a single socket design requires that certain pins are connected via the **INC** pins of the Pentium OverDrive processor. See Section 9 for more details on how to design a single socket processor site compatible other Intel486 processors.

10.2.3 CIRCUIT CONSIDERATIONS FOR WRITE BACK CACHE SUPPORT

The Pentium OverDrive processor is specified to support the MESI write back protocol for the on-chip cache. To support the write back protocol, seven new signals , are defined for the Pentium OverDrive processor, four of which are present on the Write-Back Enhanced IntelDX2 processor. The new signals defined for MESI write back capability are **WB/WT#, INV, HIT#, HITM#, CACHE#, EWBE#,** and **BLEN#.** Another new pin, **INIT,** is used to facilitate warm resets. These new signals are defined in detail in Section 5.2. For more information on designing a system for processor write back cache support that is compatible with the Write-Back Enhanced IntelDX2 processor, please see Appendix B.

10.3 Software Considerations

10.3.1 EXTERNAL BUS CYCLE ORDERING

10.3.1.1 Write Buffers and Memory Ordering

The Pentium OverDrive processor has write buffers to enhance the performance of consecutive writes to memory. Writes in these buffers are driven out on the external bus in the order they were generated by the processor core. No reads (as a result of cache miss) are reordered around previously generated writes sitting in the write buffers (Unlike the IntelDX2 processor). The implication of this is that the write buffers will be emptied before a subsequent processor generated bus cycle is run on the external bus.

It should be noted that only memory writes are buffered and I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write. The OUT instruction or a serializing instruction needs to be executed to synchronize writes with the next instruction. Please refer to the *Pentium Processor Programmers Reference Manual* for information on serializing instructions.

No re-ordering of read cycles occurs on the Pentium OverDrive processor. Specifically, the write buffers are emptied before the IN instruction is executed.

10.3.1.2 External Event Synchronization

When the value of **NMI, INTR, FLUSH#, SMI#** or **INIT** changes as the result of executing an OUT instruction, these inputs must be at a valid state three clocks before **RDY#/BRDY#** is returned to ensure that the new value will be recognized before the next instruction is executed.

Note that if an OUT instruction is used to modify **A20M#,** this will not affect previously prefetched instructions. A serializing instruction must be executed to guarantee recognition of **A20M#** before a specific instruction.

10.3.2 MODEL SPECIFIC REGISTERS

The Pentium OverDrive processor defines certain Model Specific Registers that are used in execution tracing, performance monitoring and testing. They are unique to the Pentium OverDrive processor and may or may not be implemented in the same way in future processors.

Please contact Intel for more information on the model specific registers.

10.3.3 EXCEPTION PRIORITIES

Exceptions are serviced and recognized on the boundary between instructions. The instruction pointer pushed onto the stack for the interrupt handler points to the next instruction. The priority among simultaneous exceptions is as follows (interrupt vector numbers are shown in decimal in parentheses):

Trap on the previous instruction:

- Breakpoint (#3)

External Interrupts:

- **FLUSH#**
- **SMI#**
- **INIT**
- **NMI**
- **INTR**

Floating Point Errors:

- **FERR#**

External Interrupt:

- **STPCLK#**

Faults on Fetching Next Instruction:

- Code Seg Limit Violation (#13), Page Fault on prefetch (#14) (the relative priority unpredictable)

Faults in Decoding the next Instruction:

- Invalid Opcode (#6), Device Not Available (#7)
- General Protection Fault for Instruction Length > 15B (#13)

Faults on Executing an Instruction (These may occur in a manner that varies from implementation to implementation as necessary to insure functional correctness. They are not listed in any particular order):

- General Detect (#1)
- FP Error (from previous FP instruction) (#16)
- Interrupt on Overflow (#4)
- Bound (#5)
- Invalid TSS (#10)

- Segment Not Present (#11)
- Stack Exception (#12)
- General Protection (#13)
- Data Page Fault (#14)
- Alignment Check (#17)

10.3.3.1 External Interrupt Considerations

The Pentium OverDrive processor recognizes the following external interrupts: **FLUSH#, SMI#, INIT, NMI, INTR** and **STPCLK#.** They are listed in priority order, however, they are subject to the considerations listed below.

FLUSH#

Note that unlike the Intel486 CPU which invalidates its cache a small fixed number of clocks after **FLUSH#** is asserted, the **FLUSH#** pin on the Pentium OverDrive processor is an interrupt and therefore is only recognized at the boundary between instructions. While **FLUSH#** is being serviced, all the dirty lines in the data cache are written back to main memory. This may take several thousand clocks. During this time no instructions are executed and no other interrupts are recognized. If the processor is in the HALT or Shutdown state, **FLUSH#** is still recognized. The processor will return to the HALT or Shutdown state after servicing the **FLUSH#.**

11.0 BIOS AND SOFTWARE

The following should be considered when designing a system for upgrade with an Intel OverDrive processor.

11.1 Intel OverDrive® Processor Detection

The component identifier and the stepping/revision identifier for the Intel OverDrive processors is readable in the DH and DL registers, respectively, immediately after RESET. The value loaded into each register is defined in Table 11-1. The ''x'' value defines the device stepping.

Table 11-1. CPU ID Values

Processor	DH Reg.	DL Reg.
Intel486DX	04h	0xh, 1xh
Intel486SX	04h	2xh
IntelSX2 OverDrive	04h	5xh
IntelDX2 OverDrive	04h	3xh
IntelDX4 OverDrive	14h, 04h	8xh
Pentium OverDrive	15h	3xh

As it is difficult to differentiate between Intel486 DX processor and some of the Intel OverDrive processors in software, it is recommended that the BIOS save the contents of the DX register immediately after RESET. This will allow the information to be used later, if required, to identify an Intel OverDrive processor in the system.

Alternately, for those OverDrive processors supporting it, the CPUID instruction can be used to identify the processor. Refer to the Intel486 Microprocessor Data Book for additional information on the CPUID instruction and its use.

NOTE:
Initialization routines for IntelSX2 OverDrive processor and Intel486 SX processor-based systems should check for the presence of a floating point unit and set the CR0 register accordingly (refer to the Intel486 SX Microprocessor Data Book for specific details). In addition, the BIOS should check for the presence of the 16 KByte cache in the IntelDX4 OverDrive processor.

11.2 Timing Dependent Loops

The Intel OverDrive processors execute instructions at two times (for the IntelSX2 and IntelDX2 OverDrive processors) or three times (for the IntelDX4 OverDrive processor) the frequency of the input clock. Thus, software (or instruction based) timing loops will execute faster on the Intel OverDrive processor than on the Intel486 DX or Intel486 SX processor (at the same input clock frequency). Instructions such as NOP, LOOP, and JMP $+2, have

been used by BIOS to implement timing loops that are required, for example, to enforce recovery time between consecutive accesses for I/O devices. These instruction based timing loop implementations may require modification for systems intended to be upgradable with the Intel OverDrive processors.

In order to avoid any incompatibilities, it is recommended that timing requirements be implemented in hardware rather than in software. This provides transparency and also does not require any change in BIOS or I/O device drivers in the future when moving to higher processor clock speeds. As an example, a timing routine may be implemented as follows: The software performs a dummy I/O instruction to an unused I/O port. The hardware for the bus controller logic recognizes this I/O instruction and delays the termination of the I/O cycle to the processor by keeping RDY# or BRDY# deasserted for the appropriate amount of time.

11.3 Test Register Access on the Pentium® OverDrive® Processor

The IntelDX2 processor has test registers which allow OEM's to test the functionality of different areas of the component. These test registers are accessed on the Intel486 processor family using the ''MOV reg, TRx and MOV TRx, reg'' instructions. These instructions are not available on the Pentium OverDrive processor. Any attempt to execute them will cause a invalid opcode exception. The Pentium OverDrive processor uses the Model Specific Registers (MSR's) to implement on chip testing. These MSR's are accessed using the RDMSR and WRMSR instructions. BIOS must recognize this fundamental difference between the Pentium OverDrive processor and the IntelDX2 processor and act accordingly.

12.0 Pentium® OverDrive® PROCESSOR TESTABILITY

12.1 Introduction

This section describes the features which are included in the Pentium OverDrive processor for the purpose of enhancing the testability of the part. The capabilities of the Intel486 processor test hooks are included in the processor, however they are implemented differently. In addition, new test features were added to assure timely testing and production of a system product. All features described here are also present in the Pentium processor.

Internal component testing through the Built In Self Test (BIST) feature of the Pentium OverDrive processor provides 100% single stuck at fault coverage of the microcode ROM and large PLAs. Some testing of the instruction cache, data cache, Translation Lookaside Buffers (TLBs), and Branch Target Buffer (BTB) is also performed. In addition, the constant ROMs are checked.

The production version of the Pentium OverDrive processor will not include the boundary scan or testability pins.

Several test registers are also included in the Pentium OverDrive processor to simplify access to all on-chip caches and TLBs. These test registers on the processor are not compatible with the definitions for the test registers on the IntelDX2 processor, and will be provided by Intel at a later date. For the latest information on these test registers, please contact Intel.

The following list summarizes the Pentium OverDrive processor testability features:

- Built In Self Test
- Cache and TLB Test Registers
- Tristate Test Mode

Table 12-1. Pentium® OverDrive® Processor RESET Modes

RESET	INIT	Type of Reset	Effect on I/D Caches	Effect on FP Registers	Effect on SMM Base Register
0	0	None	Not Applicable	Not Applicable	Not Applicable
0	1	Warm Reset	None	None	None
1	X	Cold Reset (w/ BIST)	Invalidated	Initialized	Invalidated
1	X	Cold Reset (w/o BIST)	Invalidated	Undefined	Invalidated

12.2 Pentium® OverDrive® Processor Reset Pins/BIST Initiation

Two pins, **RESET** and **INIT,** are used to reset the Pentium OverDrive processor in different manners. The following table shows the different types of resets that can be initiated using these pins.

Toggling either the **RESET** pin or the **INIT** pin individually forces the Pentium OverDrive processor to begin execution at address 0FFFFFFF0h. The internal instruction cache and data cache are invalidated when **RESET** is asserted (modified lines in the data cache are NOT written back). The instruction cache and data cache are not altered when the INIT pin is asserted without **RESET.** In neither case are the floating point registers altered. In both cases, the BTB, the segment descriptor cache and both TLBs are all invalidated.

Reset with self test is initiated by holding the **AHOLD** pin HIGH for 2 clocks before and 2 clocks after **RESET** is driven from HIGH to LOW. The instruction cache and data cache are invalidated and the floating point registers are initialized. The processor begins execution at address 0xFFFFFFF0h. The BTB, the segment descriptor cache and both TLBs are all invalidated before execution begins.

At the conclusion of reset, with or without self test, the DX register will contain a component identifier. The upper byte will contain 15h and the lower byte will contain a stepping identifier.

Table 12-2 defines the processor state after **RESET, INIT** and **RESET** with BIST (built in self test).

Table 12-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
EAX	0	0 if pass	0
EDX	1530 + stepping	1530 + stepping	1530 + stepping
ECX, EBX, ESP EBP, ESI, EDI	0	0	0
EFLAGS	2	2	2
EIP	0FFF0	0FFF0	0FFF0
CS	selector = F000	selector = F000	selector = F000
	base = FFFF0000	base = FFFF0000	base = FFFF0000
	limit = FFFF	limit = FFFF	limit = FFFF
DS,ES,FE,GS,SS	selector = 0	selector = 0	selector = 0
	base = 0	base = 0	base = 0
	limit = FFFF	limit = FFFF	limit = FFFF

Table 12-2. Register State after RESET, INIT and BIST
(Register States are given in Hexadecimal Format)

Storage Element	RESET (no BIST)	RESET (BIST)	INIT
IDTR	base = 0	base = 0	base = 0
	limit = FFF	limit = FFF	limit = FFF
GDTR,LDTR,TR	undefined	undefined	undefined
CR0	60000010	60000010	Note 1
CR2,3,4	0	0	0
DR3–0	0	0	0
DR6	FFFF0FF0	FFFF0FF0	FFFF0FF0
DR7	00000400	00000400	00000400
Time Stamp Counter	0	0	UNCHANGED
Control and Event Select	0	0	UNCHANGED
TR12	0	0	UNCHANGED
All Other MSR's	undefined	undefined	UNCHANGED
CW	undefined	37F	UNCHANGED
SW	undefined	0	UNCHANGED
TW	undefined	FFFF	UNCHANGED
FIP,FEA,FCS, FDS,FOP	undefined	0	UNCHANGED
FSTACK	undefined	undefined	UNCHANGED
Data and Code Cache	invalid	invalid	UNCHANGED
Code Cache TLB, Data Cache TLB, BTB, SDC	invalid	invalid	invalid

NOTE:
1. CD and NW are unchanged, bit 4 is set to 1, all other bits are cleared.
   State of output pins after RESET:
   High: **LOCK#, ADS#, PCHK#, HIT#, HITM#, FERR#, SMIACT#**
   Low: **HLDA, BREQ**
   High Impedance: **D31–D0**
   Undefined: **A31–A3, BE3#–BE0#, W/R#, M/IO#, D/C#, PCD, PWT, CACHE#**

12.3 Built In Self Test (BIST)

Self test is initiated by holding the **AHOLD** pin HIGH for the clock before **RESET** changes from HIGH to LOW. If asserted asynchronously, AHOLD must be asserted two clocks before and two clocks after **RESET** to guarantee recognition.

No bus cycles are run by the Pentium OverDrive processor during self test. The duration of self test is approximately 2^{19} internal clocks. Approximately 70% of the devices in the processor are tested by BIST.

The Pentium OverDrive processor BIST consists of two parts: hardware self test and microcode self test.

During the hardware portion of BIST, the microcode and all large PLAs are tested. All possible input combinations of the microcode ROM and PLAs are tested.

The constant ROMs, BTB, TLBs, and all caches are tested by the microcode portion of BIST. The array tests (caches, TLBs, and BTB) have two passes. On the first pass, data patterns are written to arrays, read back and checked for mismatches. The second pass writes the complement of the initial data pattern, reads it back, and checks for mismatches. The constant ROMs are tested by using the microcode to add various constants and check the result against a stored value.

Upon completion of BIST, the cumulative result of all tests are stored in the EAX register. If EAX contains 0x0h, then all checks passed; any non-zero result indicates a faulty unit.

During BIST, **EADS#** should not be used to perform snoops, otherwise false **HITM#** indications, with no corresponding write back cycles, can occur.

12.4 Tri-State Test Mode

The Pentium OverDrive processor provides the ability to float all its outputs and bi-directional pins. This includes pins that are floated during bus hold as well as some pins that are not normally floated during normal operation. When the Pentium OverDrive processor is in tri-state test mode, external testing can be used to test on board connections.

The tri-state test mode is invoked by driving **FLUSH#** low for 2 clocks before and 2 clocks after **RESET** going low. The outputs are guaranteed to tri-state no later than 10 clocks after **RESET** goes low. The processor will remain in tri-state test mode until the next **RESET.**

12.5 Cache, TLB and BTB Test Registers

The Pentium OverDrive processor contains several test registers. The purpose of the test registers is to provide direct access to the processor caches, TLBs, and BTB, so user programs can easily exercise these structures. Because the architecture of the caches, TLBs, and BTB is different, a different set of test registers (along with a different test mechanism) is required for each. Most test registers can be shared between the code and data caches.

Since much of the testability hardware is used for other purposes during normal operation of the Pentium OverDrive processor, some restrictions may exist on what software may do while testability operations are being run.

Please contact Intel for more information on the Pentium OverDrive processor Cache, TLB, and BTB Test Registers.

12.6 Fan Protection Mechanism and THermal ERRor Bit

The Pentium OverDrive processor employs an active fan/heatsink unit to assist in cooling the processor. Another integral part of this cooling solution is the ability for software to poll the status of the fan to determine if the fan has fallen to a speed that is unacceptable to cool the processor. Should the fan fall into a speed range that is too slow, a control register will record the event. (For more information, please contact Intel.)

13.0 ELECTRICAL DATA

The following sections describe recommended electrical connections for the Intel OverDrive processor, and its electrical specifications.

13.1 Power and Grounding

13.1.1 POWER CONNECTIONS

Power and ground connections must be made to all external V_{CC} and GND pins of the Intel OverDrive processor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must be likewise connected on a GND plane.

13.1.2 Intel OverDrive® PROCESSOR DECOUPLING CAPACITORS

Because of the fast internal switching speeds of the Intel OverDrive processor, it is important that the Intel OverDrive processor use a liberal amount of decoupling capacitors. For proper V_{CC} transient response, Intel recommends that a system design employ at least 4 each of 47 μF bulk capacitors and 9 each of 0.1 μF and 0.01 μF capacitors. It is recommended that surface mount capacitors be used for decoupling the Intel OverDrive processor. This style of capacitor introduces less inductance than leaded capacitors, so fewer are needed to achieve the same results. The capacitors should be added around the Intel OverDrive processor in a manner that ensures they are evenly spread about and close to the processor location.

13.1.3 OTHER CONNECTION RECOMMENDATIONS

N.C. pins should always remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Active LOW inputs should be connected to V_{CC} through a pullup resistor. Pullups in the range of 20 KΩ are recommended. Active HIGH inputs should be connected to GND.

13.2 Maximum Ratings

Table 13-1 lists the absolute maximum ratings for each of the OverDrive processors. This table is a stress rating only, and functional operation at the maximums is not guaranteed. Functional operating conditions are given in Section 13.3, DC Specifications, and Section 13.4, AC Specifications.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Intel OverDrive processors contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

13.3 DC Specifications

The DC specifications for each of the OverDrive processors are contained in the tables in Sections 13.3.1, 13.3.2, and 13.3.3. For additional information, refer to the appropriate Intel microprocessor handbook.

Table 13-1. Absolute Maximum Ratings

	IntelDX2™ OverDrive®	IntelDX4™ OverDrive®	Pentium® OverDrive®
Case Temperature under Bias	−65°C to +110°C	−30°C to +110°C	−30°C to +110°C
Fan/Heat sink Temperature under Bias	N/A	N/A	−5°C to +60°C
Storage Temperature	−65°C to +150°C	−30°C to +125°C	−30°C to +125°C
Fan/Heat sink Storage Temperature	N/A	N/A	−40°C to +70°C
Voltage on any Pin with Respect to Ground	−0.5V to (V_{CC} + 0.5V)	−0.5V to (V_{CC} + 0.5V)	−0.5V to (V_{CC} + 0.5V)
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V	−0.5V to +6.5V	−0.5V to +6.5V

13.3.1 IntelDX2™ OverDrive® PROCESSOR DC SPECIFICATIONS

Table 13-2 details the DC Specifications of the IntelDX2 OverDrive processor.

Table 13-2. DC Specifications for the IntelDX2™ OverDrive® Processor

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 2)
V_{OH}	Output High Voltage	2.4		V	(Note 3)
I_{CC}	Power Supply Current CLK = 33 MHz CLK = 25 MHz		 1200 950	 mA	 (Note 4)
I_{LI}	Input Leakage Current		±15	μA	(Note 5)
I_{IH}	Input Leakage Current		200	μA	(Note 6)
I_{IL}	Input Leakage Current		−400	μA	(Note 7)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		13	pF	F_C = 1 MHz(8)
C_O	I/O or Output Capacitance		17	pF	F_C = 1 MHz(8)
C_{CLK}	CLK Capacitance		15	pF	F_C = 1 MHz(8)

NOTES:
1. The function operating temperature range is:
   OverDrive processor—25 MHz, T_{sink} = 0°C to +95°C
   OverDrive processor—33 MHz, T_{sink} = 0°C to +95°C
2. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
3. This parameter is measured at:
   Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
4. Typical supply current:
   775 mA @ CLK = 25 MHz
   975 mA @ CLK = 33 MHz
5. This parameter is for inputs without internal pullups or pulldowns and $0 \leq V_{IN} \leq V_{CC}$.
6. This parameter is for inputs with internal pulldowns and V_{IH} = 2.4V.
7. This parameter is for inputs with internal pullups and V_{IL} = 0.45V.
8. Not 100% tested.

13.3.2 IntelDX4™ OverDrive® PROCESSOR DC SPECIFICATIONS

Table 13-3 details the DC Specifications of the IntelDX4 OverDrive processor.

Table 13-3. DC Specifications for the IntelDX4™ OverDrive® Processor

Functional operating range: V_{CC} = 5V + 5%, T_{SINK} = 0°C to +95°C.

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA
I_{CC}	Power Supply Current CLK = 25/75 MHz CLK = 33/100 MHz		 1200 1550	 mA	(Note 2)
I_{CC} Stop Grant	Power Supply Current in Stop Grant State CLK = 25/75 MHz CLK = 33/100 MHz		 85 110	 mA mA	(Note 3)
I_{CC} Stop Clock	Power Supply Current in Stop Clock State		20	mA	(Note 4)
I_{LI}	Input Leakage Current		±15	µA	(Note 5)
I_{IH}	Input Leakage Current		200	µA	(Note 6)
I_{IL}	Input Leakage Current		−400	µA	(Note 7)
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		13	pF	F_C = MHz(8)
C_O	I/O or Output Capacitance		17	pF	F_C = MHz(8)
C_{CLK}	CLK Capacitance		15	pF	F_C = MHz(8)

NOTES:
1. This parameter is measured at:
   4.0 mA: Address, Data, BEn
   5.0 mA: Definition, Control
2. The maximum and typical values shown here are design estimates. Typical supply current:
   I_{CC} = 835 mA @ CLK = 25 MHz
   I_{CC} = 1085 mA @ CLK = 33 MHz
3. The I_{CC} Stop Grant specification refers to the I_{CC} value once the IntelDX4 OverDrive processor enters the Stop Grant or Halt Auto Powerdown State.
4. The I_{CC} Stop Clock specification refers to the I_{CC} value once the IntelDX4 OverDrive processor enters the Stop Clock State. V_{IH} and V_{IL} levels must be V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specification.
5. This parameter is for inputs without pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
6. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
7. This parameter is for inputs with pullups and V_{IL} = 0.45V.
8. Not 100% tested.

13.3.3 Pentium® OverDrive® PROCESSOR DC SPECIFICATIONS

Table 13-4 provides the DC operating conditions for the Pentium OverDrive processor.

Functional operating range: $V_{CC} = 5V \pm 5\%$; $T_{A(IN)} = 10°C$ to $+55°C$ @33 MHz and 25 MHz.

Table 13-4. DC Specifications for the Pentium® OverDrive® Processor

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK = 25 MHz CLK = 33 MHz		 2200 2600	mA	
I_{LI}	Input Leakage Current		±15	μA	(Note 3)
I_{IH}	Input Leakage Current		200	μA	(Note 4)
I_{IL}	Input Leakage Current		−400	μA	(Note 5)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		13	pF	F_c = 1 MHz (6)
C_O	I/O or Output Capacitance		17	pF	F_c = 1 MHz (6)
C_{CLK}	CLK Capacitance		15	pF	F_c = 1 MHz (6)

NOTES:
1. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
3. This parameter is for inputs without pullups or pulldowns and $0 < V_{IN} < V_{CC}$.
4. This parameter is for inputs with pulldowns and $V_{IH} = 2.4V$.
5. This parameter is for inputs with pullups and $V_{IL} = 0.45V$.
6. Not 100% tested.

13.4 AC Specifications

The AC specifications for each of the OverDrive processors are contained in the tables in Sections 13.4.1, 13.4.2 and 13.4.3. These specifications consist of output delays, input setup requirements and input hold requirements. All AC specifications are relative to the rising edge of the CLK signal.

AC specification measurements are defined by Figures 13-1 through 13-6. All timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the voltage levels indicated by Figure 13-3 when AC specifications are measured. Intel OverDrive processor output delays are specified with minimum and maximum limits, measured as shown. The minimum Intel OverDrive processor delay times are hold times provided to external circuitry. Intel OverDrive processor input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous signal must be stable for correct Intel OverDrive processor operation.

Table 13-5 defines the AC timing specifications for a 33 MHz system. Table 13-7 defines the AC timing specifications for a 25 MHz system. Table 13-8 defines the AC timing specifications for a 20 MHz system. Table 13-8 defines the AC timing specifications for a 16 MHz system.

Each Intel OverDrive processor meets the AC specifications for the processor it is upgrading. For example, a 100 MHz IntelDX4 OverDrive processor meets the system AC timing specifications for the 33 MHz processor it is upgrading.

Refer to Sections 13.4.1 through 13.4.3 for any timing differences from those specified in the following tables.

For additional information, refer to the appropriate Intel microprocessor handbook.

13.4.1 IntelDX2™ OverDrive® PROCESSOR AC SPECIFICATIONS

The IntelDX2 OverDrive processor can be placed into an existing 16 MHz, 20 MHz, 25 MHz or 33 MHz Intel486 system, doubling the internal processor speed to 32 MHz, 40 MHz, 50 MHz or 66 MHz, respectively.

Tables 13-5 through 13-8 contain the AC timing specifications for the processors in those systems.

13.4.2 IntelDX4™ OverDrive® PROCESSOR AC SPECIFICATIONS

The IntelDX4 OverDrive processor can be placed into an existing 16 MHz, 20 MHz, 25 MHz or 33 MHz Intel486 system, tripling the internal processor speed to 48 MHz, 60 MHz, 75 MHz or 100 MHz, respectively.

Tables 13-5 through 13-8 contain the AC timing specifications for the processors in those systems.

Table 13-5. 33 MHz Intel Processor Characteristics(1)

V_{CC} = 5V ±5%; T_{sink} = See Note 6; C_l = 50 pF unless otherwise specified(3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	33	MHz		1X Clock Driven to OverDrive processor
t_1	CLK Period	30	125	ns	13-1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	11		ns	13-1	at 2V
t_3	CLK Low Time	11		ns	13-1	at 0.8V
t_4	CLK Fall Time		3	ns	13-1	2V to 0.8V
t_5	CLK Rise Time		3	ns	13-1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, SMIACT#, FERR#, BREQ, HLDA Valid Delay	3	14	ns	13-5	(Note 4)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		20	ns	13-6	(Note 2)
t_8	PCHK# Valid Delay	3	22	ns	13-4	(Note 4)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	20	ns	13-5	(Note 4)
t_9	BLAST#, PLOCK# Float Delay		20	ns	13-6	(Note 2)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	18	ns	13-5	(Note 4)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		20	ns	13-6	(Note 2)
t_{12}	EADS# Setup Time	5		ns	13-2	
t_{13}	EADS# Hold Time	3		ns	13-2	
t_{14}	KEN#, BS16#, BS8# Setup Time	5		ns	13-2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	13-2	
t_{16}	RDY#, BRDY# Setup Time	5		ns	13-3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	13-3	
t_{18}	HOLD, AHOLD Setup Time	6		ns	13-2	
t_{18a}	BOFF# Setup Time	7		ns	13-2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	13-2	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, IGNNE# Setup Time	5		ns	13-2	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, IGNNE# Hold Time	3		ns	13-2	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	13-2, 13-3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	13-2, 13-3	

NOTES:
1. To be used for 66 MHz IntelDX2 and 100 MHz IntelDX4 OverDrive processors.
2. Not 100% tested. Guaranteed by design characterization.
3. All timing specifications assume C_L = 50 pF.
4. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
5. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. T_{SINK} temperatures are:
   IntelDX2 OverDrive processor: 0°C to +95°C
   IntelDX4 OverDrive processor: 0°C to +95°C

Table 13-6. 25 MHz Intel Processor Characteristics(1)

V_{CC} = 5V ±5%; T_{sink} = See Note 6; C_l = 50 pF unless otherwise specified(3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	25	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	40	125	ns	13-1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	14		ns	13-1	at 2V
t_3	CLK Low Time	14		ns	13-1	at 0.8V
t_4	CLK Fall Time		4	ns	13-1	2V to 0.8V
t_5	CLK Rise Time		4	ns	13-1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#, Valid Delay	3	19	ns	13-5	(Note 4)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		28	ns	13-6	(Note 2)
t_8	PCHK# Valid Delay	3	24	ns	13-4	(Note 4)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	24	ns	13-5	(Note 4)
t_9	BLAST#, PLOCK# Float Delay		28	ns	13-6	(Note 2)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	20	ns	13-5	(Note 4)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	13-6	(Note 2)
t_{12}	EADS# Setup Time	8		ns	13-2	
t_{13}	EADS# Hold Time	3		ns	13-2	
t_{14}	KEN#, BS16#, BS8# Setup Time	8		ns	13-2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	13-2	
t_{16}	RDY#, BRDY# Setup Time	8		ns	13-3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	13-3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	8		ns	13-2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	13-2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	8		ns	13-2	
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	3		ns	13-2	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	13-2, 13-3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	13-2, 13-3	

NOTES:
1. To be used for 50 MHz or 60 MHz IntelDX2 and 75 MHz or 100 MHz IntelDX4 OverDrive processors.
2. Not 100% tested. Guaranteed by design characterization.
3. All timing specifications assume C_L = 50 pF.
4. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
5. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. T_{SINK} temperatures are:
   IntelDX2 OverDrive processor: 0°C to +95°C
   IntelDX4 OverDrive processor: 0°C to +95°C

Table 13-7. 20 MHz Intel Processor Characteristics(1)

V_{CC} = 5V ±5%; T_{SINK} = See Note 6; C_l = 50 pF unless otherwise specified(3)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	20	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	50	125	ns	13-1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	16		ns	13-1	at 2V
t_3	CLK Low Time	16		ns	13-1	at 0.8V
t_4	CLK Fall Time		6	ns	13-1	2V to 0.8V
t_5	CLK Rise Time		6	ns	13-1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT# Valid Delay	3	23	ns	13-5	(Note 4)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		37	ns	13-6	(Note 2)
t_8	PCHK# Valid Delay	3	28	ns	13-4	(Note 4)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	28	ns	13-5	(Note 4)
t_9	BLAST#, PLOCK# Float Delay		37	ns	13-6	(Note 2)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	26	ns	13-5	(Note 4)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		37	ns	13-6	(Note 2)
t_{12}	EADS# Setup Time	10		ns	13-2	
t_{13}	EADS# Hold Time	3		ns	13-2	
t_{14}	KEN#, BS16#, BS8# Setup Time	10		ns	13-2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	13-2	
t_{16}	RDY#, BRDY# Setup Time	10		ns	13-3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	13-3	
t_{18}	HOLD, AHOLD, Setup Time	12		ns	13-2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	13-2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	12		ns	13-2	(Note 5)
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	3		ns	13-2	(Note 5)
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	13-2, 13-3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	13-2, 13-3	

NOTES:
1. To be used 50 MHz or 60 MHz IntelDX2 and 75 MHz or 100 MHz IntelDX4 OverDrive processors.
2. Not 100% tested. Guaranteed by design characterization.
3. All timing specifications assume C_L = 50 pF.
4. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
5. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. T_{SINK} temperatures are:
   IntelDX2 OverDrive processor: 0°C to +95°C
   IntelDX4 OverDrive processor: 0°C to +95°C

Table 13-8. 16 MHz Intel Processor Characteristics(1)

V_{CC} = 5V ±5%; T_{SINK} = See Note 6; C_l = 50 pF unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	16	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	62.5	125	ns	13-1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	20		ns	13-1	at 2V
t_3	CLK Low Time	20		ns	13-1	at 0.8V
t_4	CLK Fall Time		8	ns	13-1	2V to 0.8V
t_5	CLK Rise Time		8	ns	13-1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT# Valid Delay	3	26	ns	13-5	(Note 4)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		42	ns	13-6	(Note 2)
t_8	PCHK# Valid Delay	3	35	ns	13-4	(Note 4)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	35	ns	13-5	(Note 4)
t_9	BLAST#, PLOCK# Float Delay		42	ns	13-6	(Note 2)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	30	ns	13-5	(Note 4)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		42	ns	13-6	(Note 2)
t_{12}	EADS# Setup Time	12		ns	13-2	
t_{13}	EADS# Hold Time	4		ns	13-2	
t_{14}	KEN#, BS16#, BS8# Setup Time	12		ns	13-2	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	13-2	
t_{16}	RDY#, BRDY# Setup Time	12		ns	13-3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	13-3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	13-2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	13-2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	14		ns	13-2	(Note 5)
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	4		ns	13-2	(Note 5)
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	10		ns	13-2, 13-3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	13-2, 13-3	

NOTES:
1. To be used for 50 MHz or 60 MHz IntelDX2 and 75 MHz or 100 MHz IntelDX4 OverDrive processors.
2. Not 100% tested. Guaranteed by design characterization.
3. All timing specifications assume C_L = 50 pF.
4. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
5. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. T_{SINK} temperatures are:
   IntelDX2 OverDrive processor: 0°C to +95°C
   IntelDX4 OverDrive processor: 0°C to +95°C

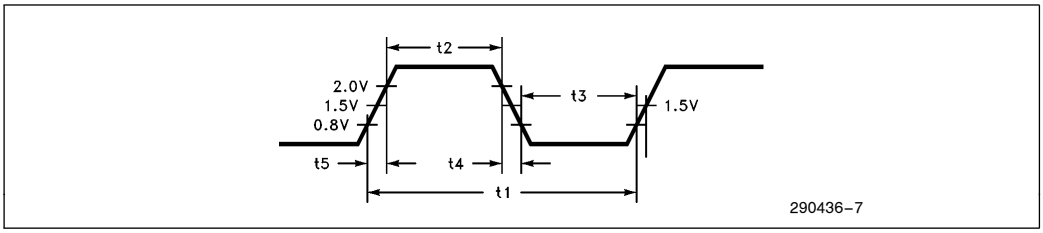


Figure 13-1. CLK Waveforms

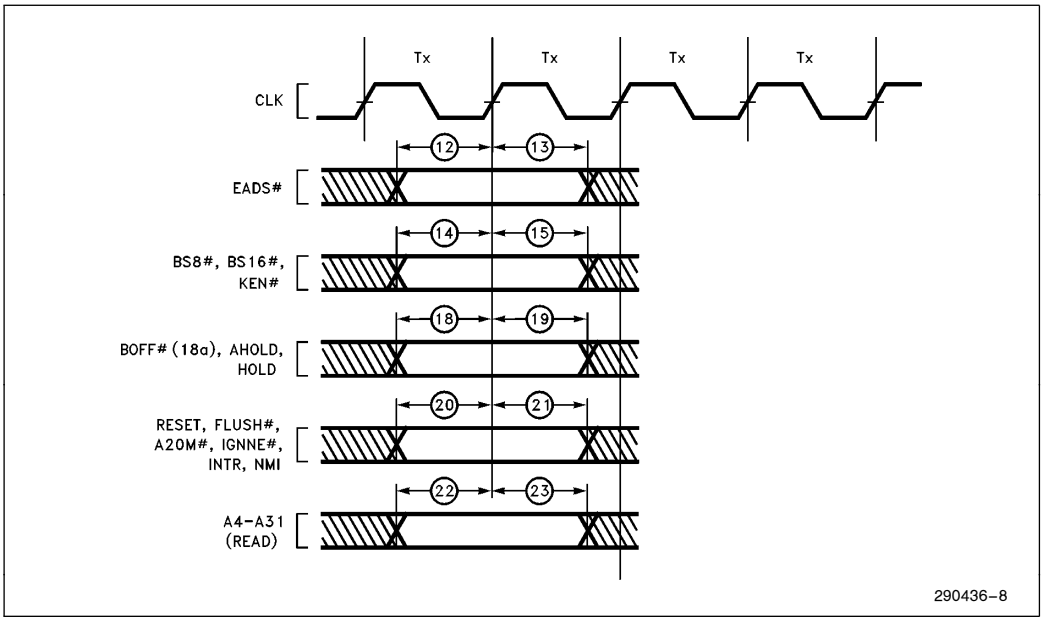


Figure 13-2. Input Setup and Hold Timing

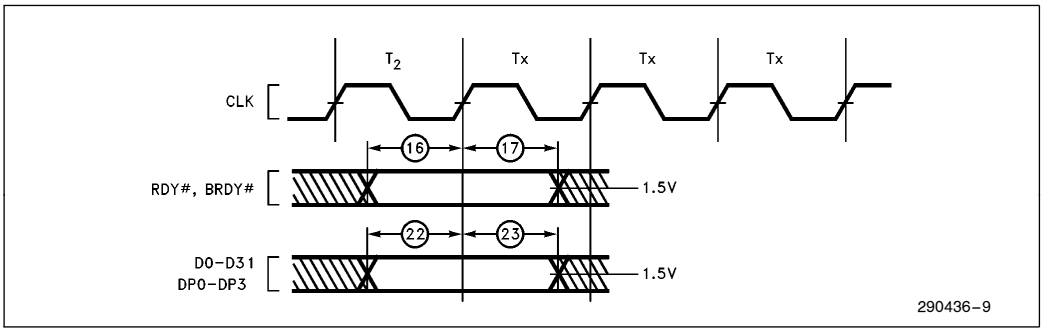


Figure 13-3. Input Setup and Hold Timing

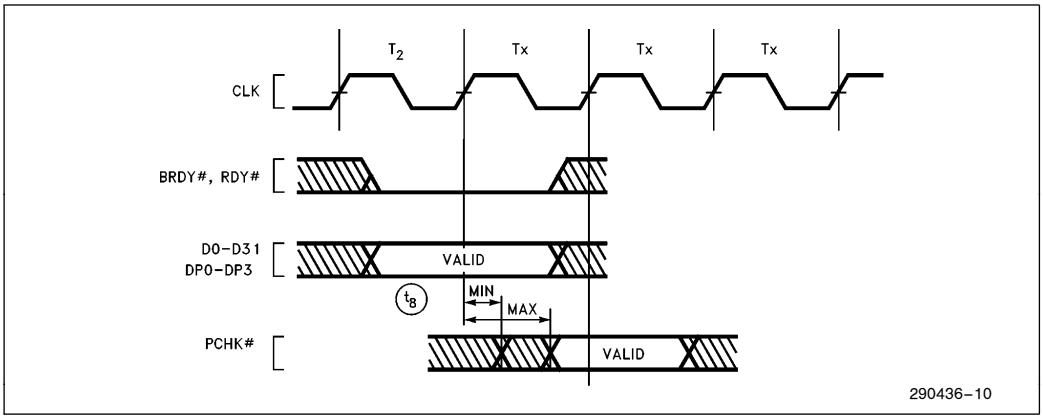


Figure 13-4. PCHK# Valid Delay Timing

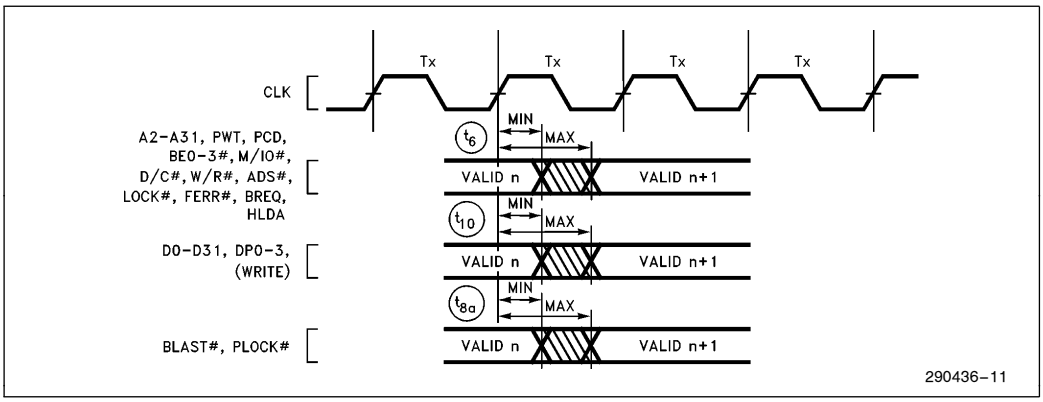


Figure 13-5. Output Valid Delay Timing

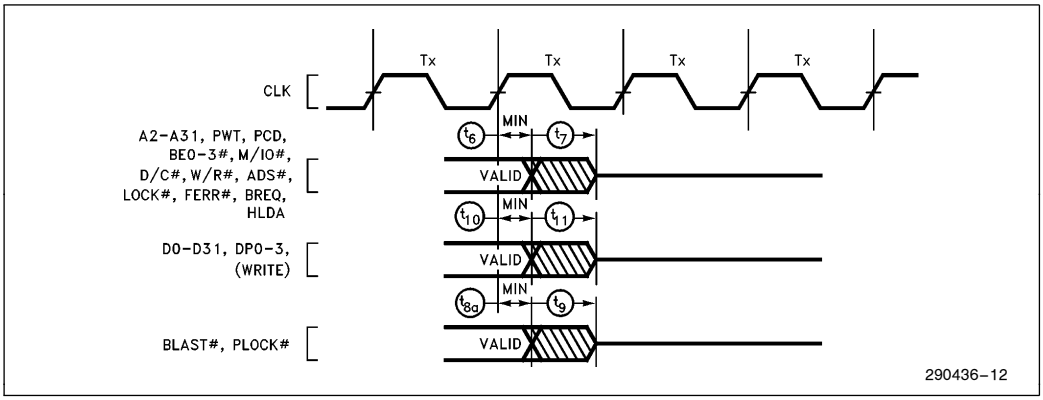


Figure 13-6. Maximum Float Delay Timing

13.4.3 Pentium® OverDrive® PROCESSOR AC SPECIFICATIONS

Tables 13-9 and 13-10 provide the AC specifications for the Pentium OverDrive processor at external clock frequencies of 25 MHz and 33 MHz respectively. They consist of output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the rising edge of the input system clock unless otherwise specified. Internal core frequencies will be a multiple of the system bus frequency.

13.4.3.1 V_{CC} Transient Specification

Due to the on-board voltage regulator, the V_{CC} of the Pentium OverDrive processor is allowed to exceed the DC Voltage specifications (V_{CC} = 5V + 5%) when the processor creates a large current transient, as would be the case in a full operation to Autohalt transition (2.5A to 200 mA I_{CC} change). The width of the pulse that exceeds 5V + 5% should be no wider than 1ms, and can not exceed 5.5V. V_{CC} is not allowed to go below the DC specification of 5V − 5% at any time. This specification applies to the Pentium OverDrive processor only and can not be applied to any other Intel processors. Figure 13-7 shows an example of the V_{CC} transient specification.

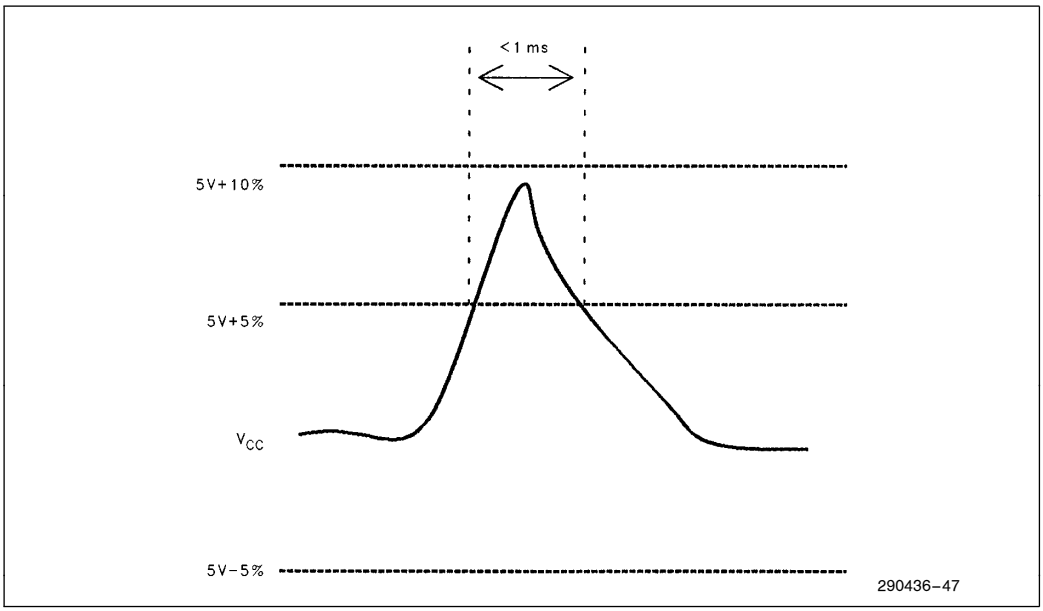


Figure 13-7. V_{CC} Transient Example

Table 13-9. Pentium® OverDrive® Processor—25 MHz AC Characteristics

V_{CC} = 5V + 5%; $T_{A(IN)}$ = 10°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	25	MHz		1X Clock Input to Processor
t_1	**CLK** Period	40	125	ns	13-8	
t_{1a}	CLK Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	14		ns	13-8	at 2V
t_3	**CLK** Low Time	11		ns	13-8	at 0.8V
t_4	**CLK** Fall Time		4	ns	13-8	2V to 0.8V
t_5	**CLK** Rise Time		4	ns	13-8	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	19	ns	13-10	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#** Float Delay		28	ns	13-10	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	24	ns	13-10	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	24	ns	13-10	
t_9	**BLAST#, PLOCK#** Float Delay		28	ns	13-10	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	20	ns	13-10	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		28	ns	13-10	After Clock Edge(2)
t_{12}	**EADS#** Setup Time	8		ns	13-9	
t_{13}	**EADS#** Hold Time	3		ns	13-9	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	8		ns	13-9	

Table 13-9. Pentium® OverDrive® Processor—25 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 10°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	13-9	
t_{16}	**RDY#, BRDY#,** Setup Time	8		ns	13-9	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	13-9	
t_{18}	**HOLD, AHOLD** Setup Time	8		ns	13-9	
t_{18a}	**BOFF#, SMI#** Setup Time	8		ns	13-9	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	13-9	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	8		ns	13-9	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT Hold Time**	3		ns	13-9	
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	13-9	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	13-9	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	8		ns	13-9	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	13-9	
t_{40}	**INV Setup Time**	8		ns	13-9	
t_{41}	**INV** Hold Time	3		ns	13-9	
t_{42}	**HIT#, HITM#** Valid Delay	3	19	ns	13-10	
t_{43}	**HIT#, HITM#** Float Delay		28	ns	13-10	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	19	ns	13-10	
t_{45}	**CACHE#** Float Delay		28	ns	13-10	
t_{46}	**STPCLK#** Setup Time	5		ns	13-9	
t_{47}	**STPCLK#** Hold Time	3		ns	13-9	

NOTES:
1. All timing specifications assume C_L = 50 pF. Section 14.3.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

Table 13-10. Pentium® OverDrive® Processor—33 MHz AC Characteristics

V_{CC} = 5V + 5%; $T_{A(IN)}$ = 10°C to +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
	Frequency	8	33	MHz		1X Clock Input to Processor
t_1	**CLK** Period	30	125	ns	13-8	
t_{1a}	**CLK** Period Stability		250	ps		Adjacent Clocks
t_2	**CLK** High Time	11		ns	13-8	At 2V
t_3	**CLK** Low Time	8		ns	13-8	At 0.8V
t_4	**CLK** Fall Time		3	ns	13-8	2V to 0.8V
t_5	**CLK** Rise Time		3	ns	13-8	0.8V to 2V
t_6	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#,** Valid Delay	3	14	ns	13-10	
t_7	**A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# BP3, BP2,** Float Delay		20	ns	13-10	After Clock Edge(2)
t_8	**PCHK#** Valid Delay	3	14	ns	13-10	
t_{8a}	**BLAST#, PLOCK#** Valid Delay	3	14	ns	13-10	
t_9	**BLAST#, PLOCK#** Float Delay		20	ns	13-10	After Clock Edge(2)
t_{10}	**D0–D31, DP0–3** Write Data Valid Delay	3	14	ns	13-10	
t_{11}	**D0–D31, DP0–3** Write Data Float Delay		20	ns	13-10	After Clock Edge(2)

Table 13-10. Pentium® OverDrive® Processor—33 MHz AC Characteristics (Continued)
V_{CC} = 5V + 5%; $T_{A(IN)}$ = 10°C TO +55°C; C_L = 50 pF (1) Unless Otherwise Specified

Symbol	Parameter	Min	Max	Units	Figure	Notes
t_{12}	**EADS#** Setup Time	5		ns	13-9	
t_{13}	**EADS#** Hold Time	3		ns	13-9	
t_{14}	**KEN#, BS16#, BS8#** Setup Time	5		ns	13-9	
t_{15}	**KEN#, BS16#, BS8#** Hold Time	3		ns	13-9	
t_{16}	**RDY#, BRDY#,** Setup Time	5		ns	13-9	
t_{17}	**RDY#, BRDY#,** Hold Time	3		ns	13-9	
t_{18}	**HOLD, AHOLD** Setup Time	6		ns	13-9	
t_{18a}	**BOFF#, SMI#** Setup Time	7		ns	13-9	
t_{19}	**HOLD, AHOLD, BOFF#, SMI#** Hold Time	3		ns	13-9	
t_{20}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Setup Time	5		ns	13-9	
t_{21}	**RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, INIT** Hold Time	3		ns	13-9	
t_{22}	**D0–D31, DP0–3, A4–A31** Read Setup Time	5		ns	13-9	
t_{23}	**D0–D31, DP0–3, A4–A31** Read Hold Time	3		ns	13-9	
t_{38}	**WB/WT#** and **EWBE#** Setup Time	5		ns	13-9	
t_{39}	**WB/WT#** and **EWBE#** Hold Time	3		ns	13-9	
t_{40}	**INV** Setup Time	5		ns	13-9	
t_{41}	**INV** Hold Time	3		ns	13-9	
t_{42}	**HIT#, HITM#** Valid Delay	3	14	ns	13-10	
t_{43}	**HIT#, HITM#** Float Delay		20	ns	13-10	Only during Three State Test Mode
t_{44}	**CACHE#** Valid Delay	3	14	ns	13-10	
t_{45}	**CACHE#** Float Delay		20	ns	13-10	
t_{46}	**STPCLK#** Setup Time	5		ns	13-9	
t_{47}	**STPCLK#** Hold Time	3		ns	13-9	

NOTES:
1. All signal timings except Boundary Scan timing specifications assume C_L = 50 pF. Section 14.3.1 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
2. Not 100% tested, guaranteed by design characterization.

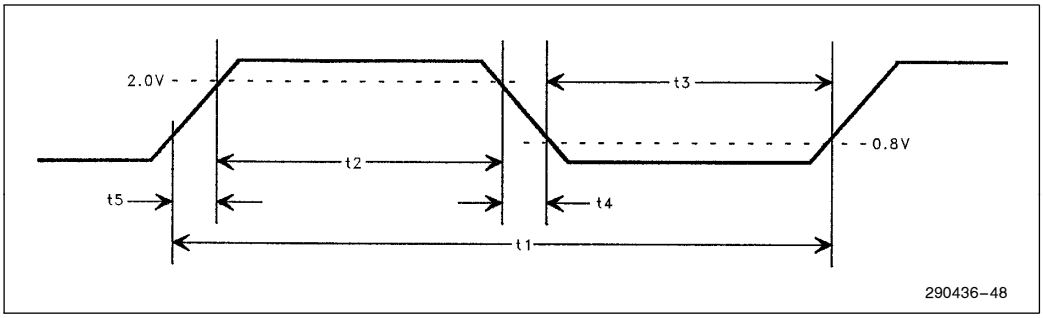


Figure 13-8. CLK Waveform

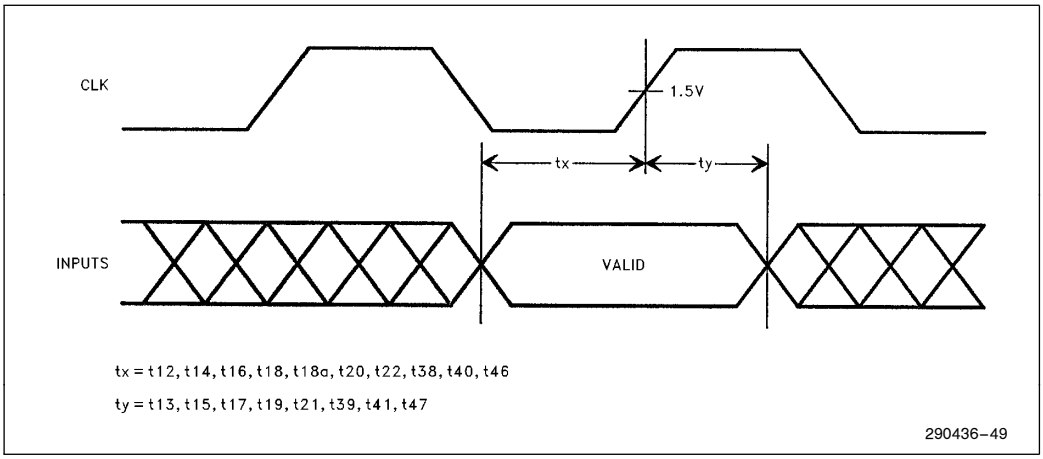


Figure 13-9. SETUP and HOLD Timings

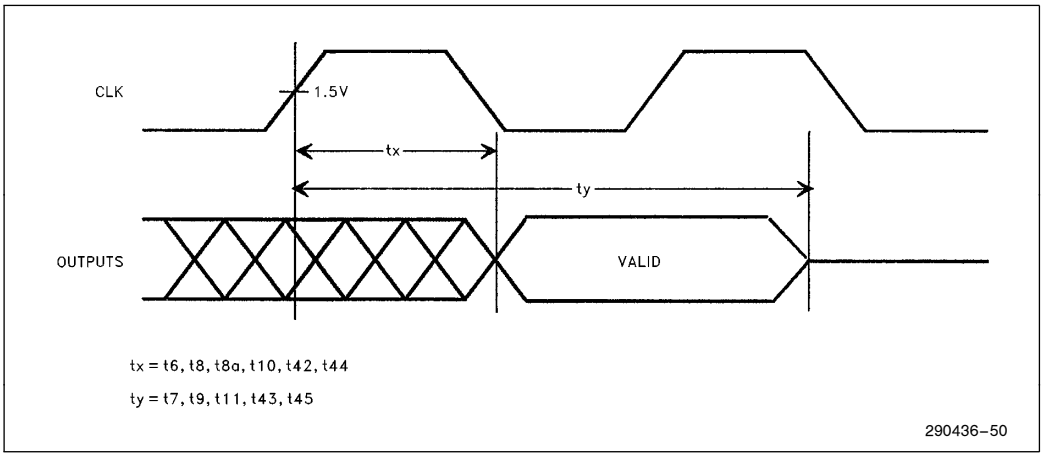


Figure 13-10. Valid and Float Delay Timings

13.4.3.2 Derating I/O Specifications

Figures 13-11 and 13-12 can be used to determine the amount of derating necessary for a given amount of lumped capacitive load. This delay due to derating must be added accordingly to the specification values listed in Tables 13-9 and 13-10 for the Pentium OverDrive processor. These values are design estimates.

Refer to the Pentium Processor Data Book for more information on instruction execution timing and pairing.

A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

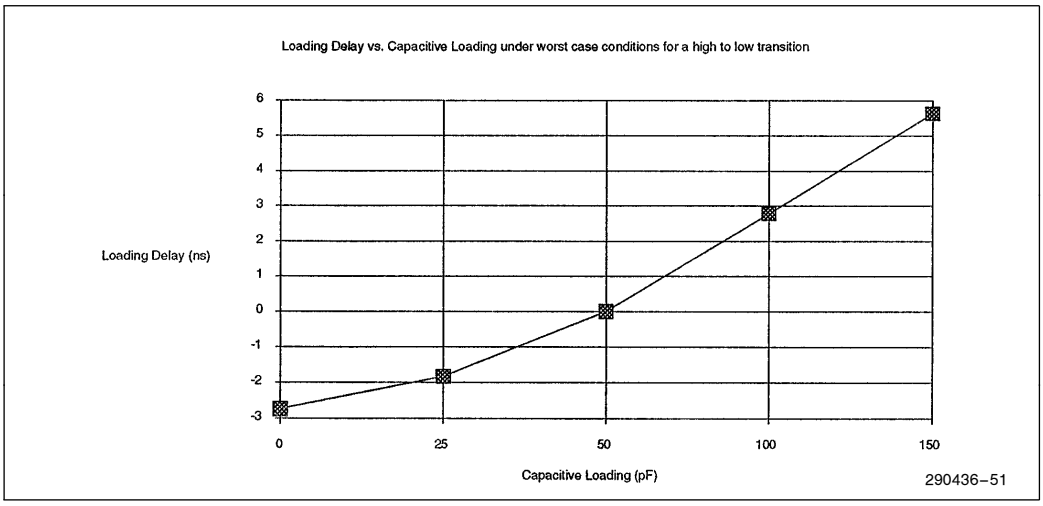


Figure 13-11. Loading Delay vs Load Capacitance (High to Low Transition)

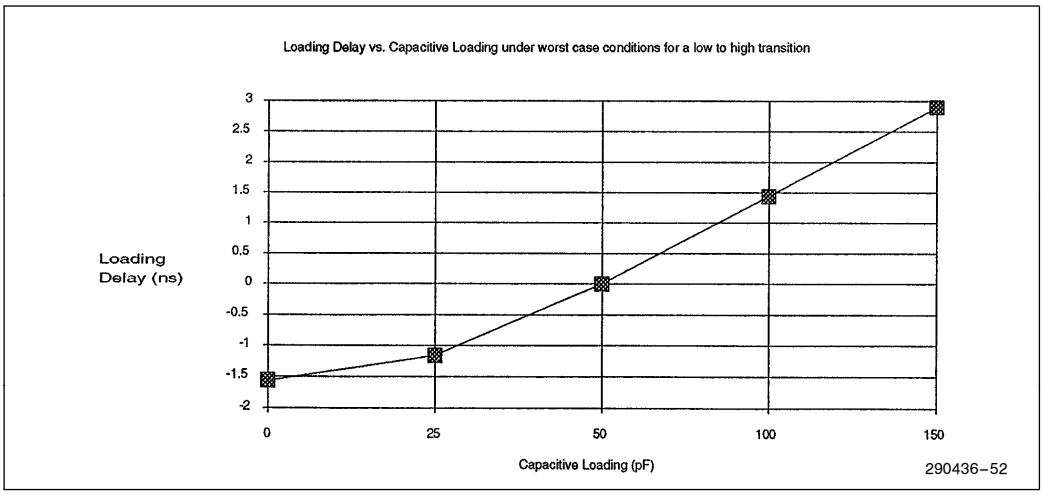


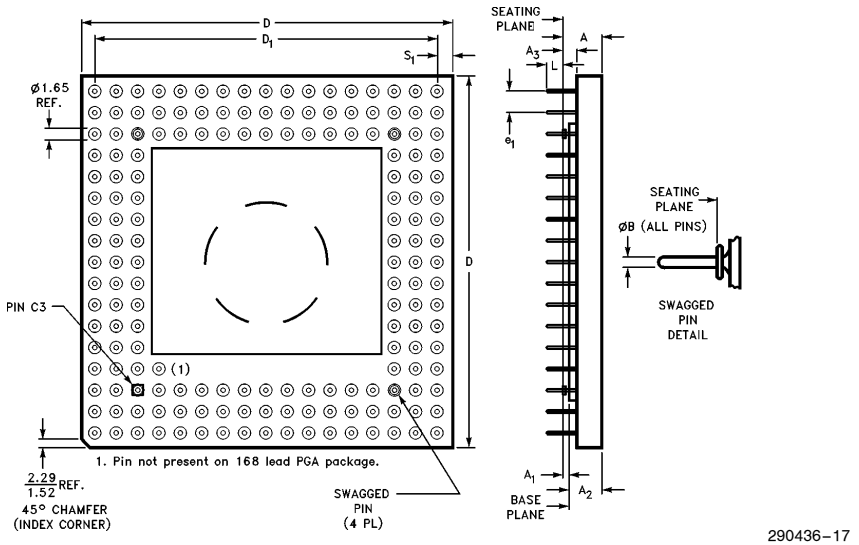
Figure 13-12. Loading Delay vs Load Capacitance (Low to High Transition)

14.0 MECHANICAL DATA

The following sections describe the physical dimensions of the OverDrive processor packages and heat sinks.

14.1 Package Dimensions for the IntelDX2™ and IntelDX4™ OverDrive® Processors

Figure 14-1 describes the physical dimensions of the PGA packages (168-lead PGA and 169-lead PGA) used with the IntelDX2 and IntelDX4 OverDrive processors.



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	SOLID LID	0.025	0.045	SOLID LID
A_2	2.8	3.5	SOLID LID	0.110	0.140	SOLID LID
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168, 169			168, 169		
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS REV X 7/15/88					

Figure 14-1. OverDrive® Processor Package Dimensions

14.2 Heat Sink Dimensions

There are two different passive heat sinks and one fan heat sink used on the Intel OverDrive processors. The IntelDX2 OverDrive processor uses the 0.25″ heat sink. The IntelDX4 OverDrive processor uses the 0.6″ heat sink. The Pentium OverDrive processor uses an integrated fan heat sink. All three heat sinks are described in the following sections.

14.2.1 0.25″ PASSIVE HEAT SINK

Figure 14-2 describes the physical dimensions of the 0.25″ heat sink used with the IntelDX2 OverDrive processor. Table 14-1 lists the physical dimensions.

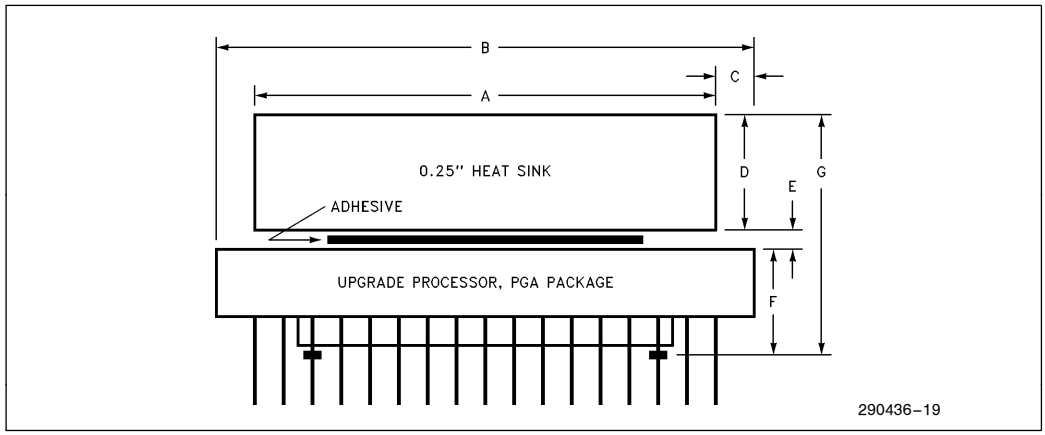


Figure 14-2. Dimensions, IntelDX2™ OverDrive® Processor with 0.25″ Heat Sink

Table 14-1. 0.25″ Heat Sink Dimensions

Dimension (inches)	Minimum	Maximum
A. Heat Sink Width	1.520	1.550
B. PGA Package Width	1.735	1.765
C. Heat Sink Edge Gap	0.065	0.155
D. Heat Sink Height	0.212	0.260
E. Adhesive Thickness	0.008	0.012
F. Package Height from Stand-Offs	0.140	0.180
G. Total Height from Package Stand-Offs to Top of Heat Sink	0.360	0.452

14.2.2 0.6″ PASSIVE HEAT SINK

Figure 14-3 describes the physical dimensions of the 0.6″ heat sink used with the IntelDX4 OverDrive processors. The maximum and minimum dimensions for the PGA package with heat sink are shown in Table 14-2. As the table shows, the maximum height of the IntelDX4 OverDrive processor from the pin stand-offs to the top of the heat sink, including the adhesive thickness, is 0.780 inches. A minimum clearance of 0.25″ should be allowed above the top of the heat sink.

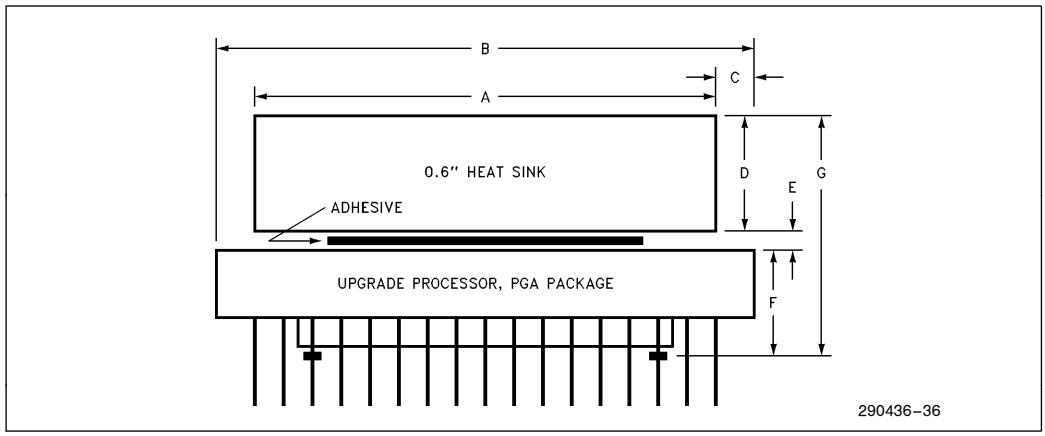


Figure 14-3. Dimensions, IntelDX4™ OverDrive® Processor with 0.6″ Heat Sink

Table 14-2. 0.6″ Heat Sink Dimensions

Dimension (inches)	Minimum	Maximum
A. Heat Sink Width	1.520	1.550
B. PGA Package Width	1.735	1.765
C. Heat Sink Edge Gap	0.065	0.155
D. Heat Sink Height	0.580	0.600
E. Adhesive Thickness	0.006	0.012
F. Package Height from Stand-Offs	0.140	0.180
G. Total Height from Package Stand-Offs to Top of Heat Sink	0.720	0.780

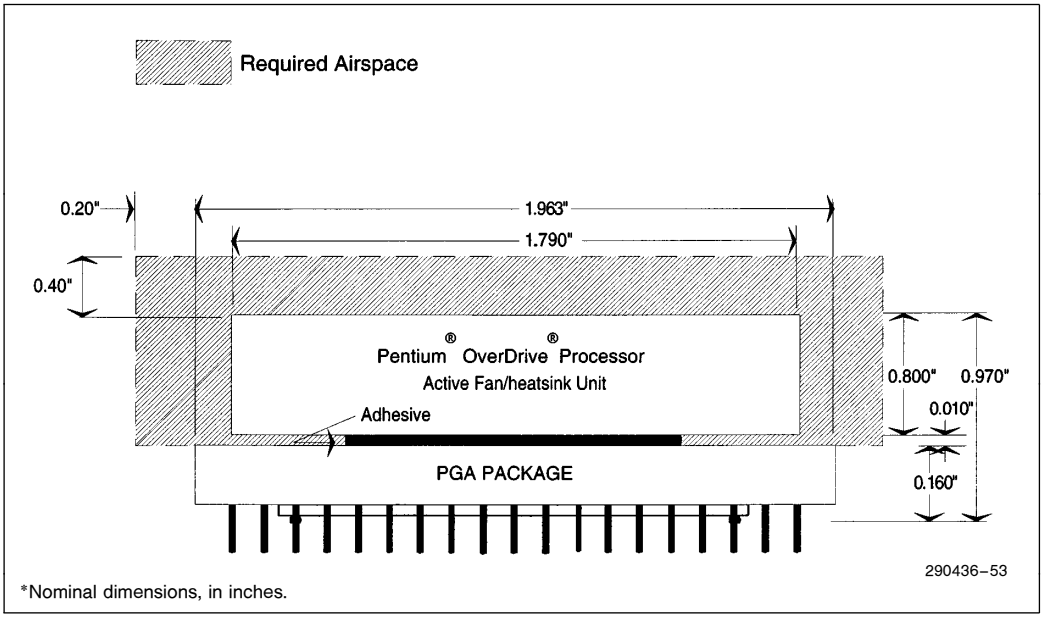
14.2.3 Pentium® OverDrive® PROCESSOR ACTIVE HEAT SINK

The Pentium OverDrive processor is designed to fit in a standard 240-lead (19 x 19) PGA socket with four corner pins removed. The Pentium OverDrive processor will use an active heat sink, and therefore requires more vertical clearance. For more discussion on the Pentium OverDrive processor active heat sink, please see the following section.

The maximum and minimum dimensions of the Pentium OverDrive processor package with the active heat sink are shown in Table 14-3. The active heat sink unit is divided into the size of the actual heat sink, and the required free space above the heat sink. The total height required for the Pentium OverDrive processor from the motherboard will depend on the height of the PGA socket. The total external height given in the table below is only measured from the PGA pin stand-offs. Table 14-3 also details the minimum clearance needed around the PGA package.

Table 14-3. Pentium® OverDrive® Processor, 235-Pin, PGA Package Dimensions with Active Heat Sink Attached

Component (inches)	Length and Width		Height	
	Min	Max	Min	Max
PGA Package	1.950	1.975	0.140	0.180
Adhesive	N/A	N/A	0.008	0.012
Fan/Heat Sink	1.77	1.82	0.790	0.810
Required Airspace	0.200	N/A	0.400	N/A
External Pkg. Total	1.950	1.975	0.938	1.002
Min. Ext. w/ Airspace Fixture	2.150		1.338	



*Nominal dimensions, in inches.

Figure 14-4. 235-Pin, PGA Package with Active Heat Sink Attached

14.2.3.1 ACTIVE HEAT SINK DETAILS

Since the Pentium OverDrive processor dissipates more power than the Intel486 Family, it requires a larger cooling capacity. To accomplish the task of cooling the Pentium OverDrive processor, an active heat sink is attached to the top of the part. The active heat sink will use a heat sink/fan combination to provide airflow at high velocity to the Pentium OverDrive processor. No external connections (Power, etc . . .) will be required for the active heat sink. All the needed connections will be made through the pins of the processor. The amount of extra power needed for the fan is taken into account in the I_{CC} numbers of the processor.

The fan/heat sink unit also supports an integrated thermal protection mechanism that will allow the fan to signal the processor if the speed of the fan should become insufficient to cool the processor. Should this occur, the processor will modify its internal core frequency to match the **CLK** input in a manner that is transparent to the external system. The fan/heat sink has been designed so that should the fan stop, it will have the capability to properly cool the processor in a still air environment. The fan unit is removable so that the unit may be easily replaced. If the fan is removed, or power to the fan is lost, the processor will treat these conditions as if the fan has failed. Figure 14-5 below gives a functional representation of the Pentium OverDrive processor and heat sink unit.

As can be seen in the mechanical dimensions in Table 14-3, the actual height required by the heat sink is less than the total space allotted. Since the Pentium OverDrive processor employs an active heat sink, a certain amount of space is required above the heat sink unit to ensure that the airflow is not blocked. Figure 14-6 shows unacceptable blocking of the airflow for the Pentium OverDrive processor heat sink unit. Figure 14-7 details the minimum space needed around the PGA package to ensure proper heat sink airflow.

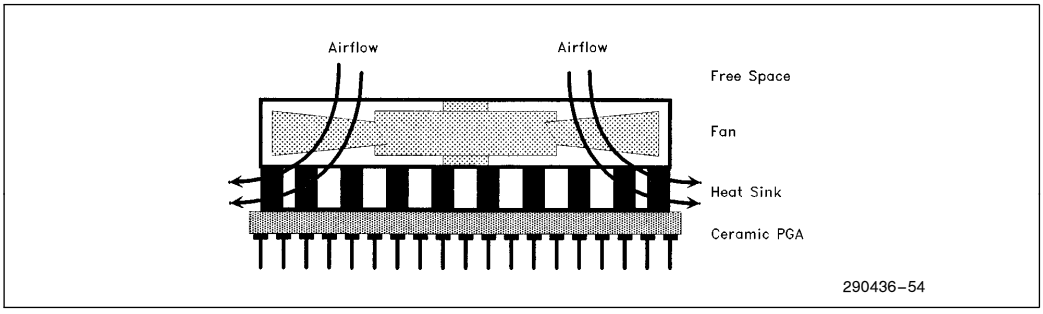


Figure 14-5. Active Heat Sink Example

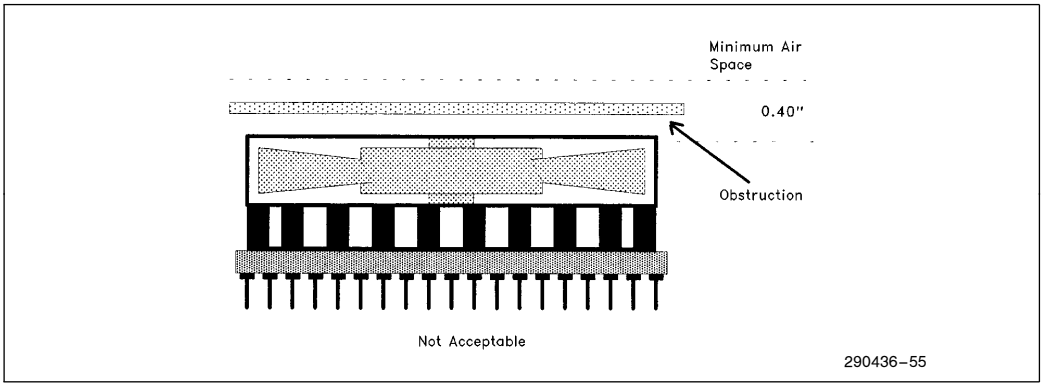


Figure 14-6. Active Heat Sink Top Space Requirements

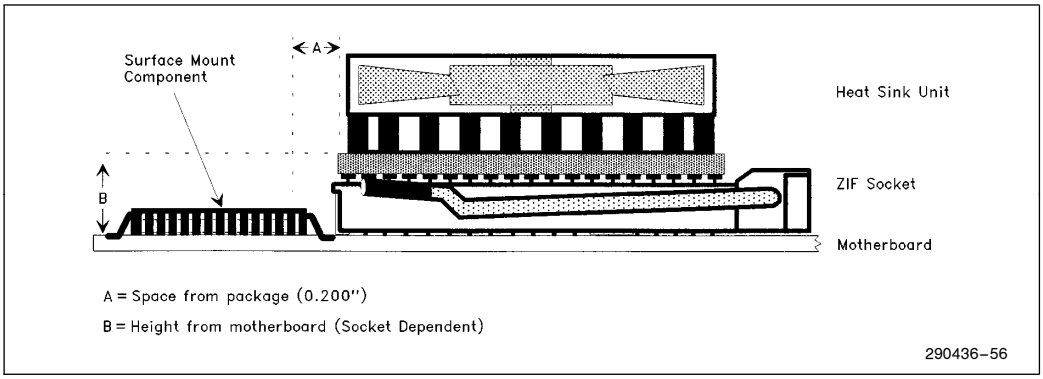


Figure 14-7. Required Free Space from Sides of PGA Package

As shown in Figure 14-7, it is acceptable to allow any device to enter within the free space distance of 0.2″ from the PGA package if it is not taller than the level of the heat sink base. In other words, if a component is taller than height ''B'', it can not be closer to the PGA package than distance ''A''. This applies to all four sides of the PGA package, although the back and handle sides of a ZIF socket will generally automatically meet this specification since they have widths larger than distance ''A''.

14.3 Pentium® OverDrive® Processor Socket

14.3.1 SOCKET BACKWARD COMPATIBILITY

The Pentium OverDrive processor socket is designed specifically for the requirements of the Pentium OverDrive processor. In addition the socket can accept and is pin compatible with the IntelDX2 and IntelDX4 OverDrive processors. This added compatibility may be useful during system troubleshooting and debug.

The Pentium OverDrive processor defines a fourth row of contacts around the outside of the 169 contacts defined for the IntelDX2 and IntelDX4 OverDrive processors. The three inner rows of the socket are 100% compatible with the IntelDX2 and IntelDX4 OverDrive processors. For backward compatibility, the inner row key pin location (E5) must be included in any socket that is to accept the Pentium OverDrive processor. For proper operation of the Pentium OverDrive processor, all the power and ground pins in the outer row of pins must be connected.

14.3.2 SOCKET 3 PINOUT

Socket 3 is the ZIF (Zero Insertion Force) socket recommended for the Pentium OverDrive processor. To ensure proper orientation, four corner pins have been removed from the outer row of pins. Additionally, the three inner rows of pins are compatible with the IntelDX2 and IntelDX4 OverDrive processors. This includes the ''key'' pin in the inside corner. Figure 14-8 shows an example of the pinout of Socket 3.

Socket 2, a previous ZIF socket definition for the Pentium OverDrive processor, is compatible to the IndelDX2, IntelDX4, and Pentium OverDrive processors. This definition has been replaced with the socket 3 definition so it will not be discussed.

Product Highlights

- Distinctive socket with the ''Socket 3'' marking
- Rapid end user access to Socket 3
- Keyed ZIF socket for easy and correct Pentium OverDrive processor installation

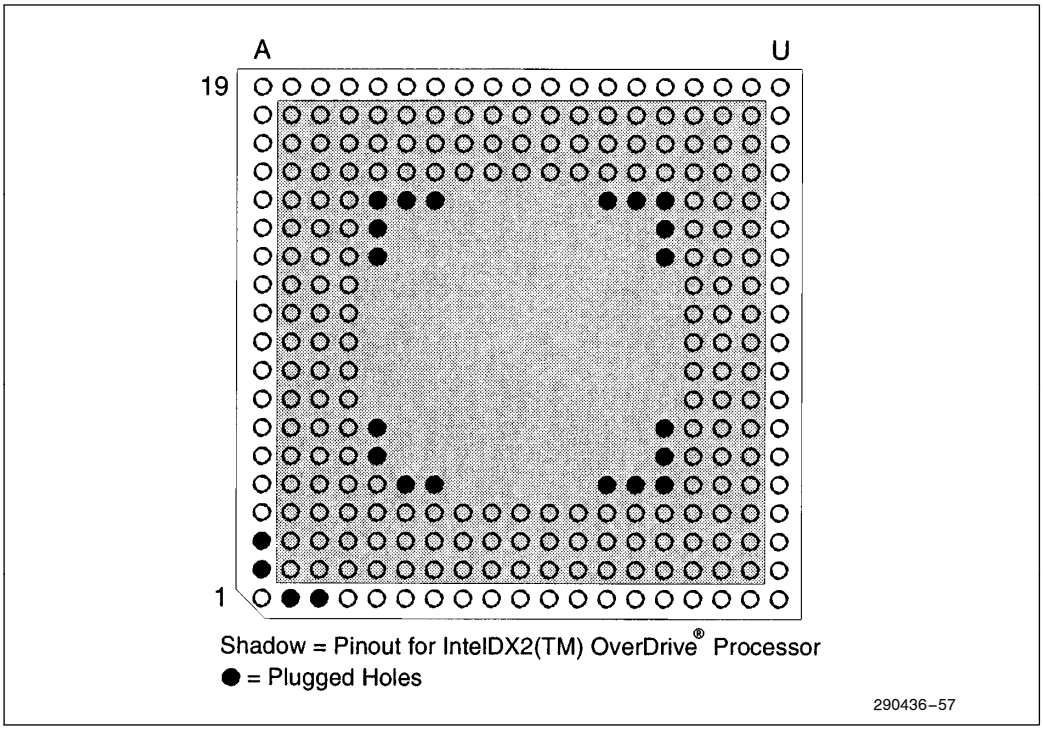


Figure 14-8. 237-Pin, PGA ZIF Socket 3

Table 15-1. Thermal Resistance, IntelDX2™ OverDrive® Processor with Attached Heat Sink

θ_{JS} = 2.5°C/W	Airflow (LFM)				
	0	200	400	600	800
θ_{JA}(°C/W)	14.0	10.0	7.5	6.2	5.7

Table 15-2. Thermal Resistance, IntelDX4™ OverDrive® Processor with Attached Heat Sink

θ_{JS} = 2.0°C/W	Airflow (LFM)			
	0	50	100	200
θ_{JA}(°C/W)	11.5	10.7	9.5	7.0

15.0 THERMAL MANAGEMENT

The heat generated by the Intel OverDrive processor requires that heat dissipation be managed carefully. All OverDrive processors are supplied with a heat sink attached with adhesive to the package. System designs must, therefore, provide sufficient clearance (a minimum of 0.25″ above the heat sink) for the processor and the attached heat sink.

Section 14 contains the physical dimensions for each of the heat sinks and packages used.

The standard product markings and logo for the Intel OverDrive processor with the attached heat sink will be included on a $1in^2$ plate located on the top, center of the heat sink.

The heat sink is omni-directional, allowing air to flow from any direction in order to achieve adequate cooling. The thermal resistance values for the OverDrive processors with an attached heat sink are shown in Table 15-1 through Table 15-3.

The Pentium OverDrive processor and system chassis have several unique design requirements due to the attached active heat sink. The following sections provide sample maximum system operating temperature calculations so that systems may be designed to comply with the thermal requirements of the Pentium OverDrive processor.

15.1 Thermal Calculations for a Hypothetical System

The following equation can be used to calculate the maximum operating temperature of a system.

$T_{A(IN)} = T_{SINK} - (Power * \theta_{SI})$

The parameters are defined as follows:

$T_{A(IN)}$: The temperature of the air going **into** the heat sink fan unit.

T_{SINK}: Temperature of heat sink base, as measured in the center.

Power: Dissipation in Watts = $V_{CC} * I_{CC}$

θ_{SI}: Heat Sink to Internal Temperature [$T_{A(IN)}$] Thermal Resistance

$T_{A(OUT)}$: The temperature of the air outside the system.

Since the Pentium OverDrive processor uses an active heat sink, θ_{SI} is relatively constant, regardless of the airflow provided to the processor. The θ_{SI} is provided in Table 15-3. Table 15-4 details the maximum current requirements of the Pentium OverDrive processor. The maximum allowable $T_{A(IN)}$ is 55°C for both 25 MHz and 33 MHz with the heat sink attached.

Table 15-3. Thermal Resistance (°C/W) θ_{SI}

Processor Type	θ_{SI}—°C/W
Active Heat Sink	2.4

Table 15-4. Pentium® OverDrive® Processor Typical and Maximum I_{CC} Values

System Frequency (MHz)	Processor Typical I_{CC} (mA)	Processor Maximum I_{CC} (mA)
25	TBD	2200
33	TBD	2600

I_{CC} is dependent upon the V_{CC} level of the system, processor bus loading, software code sequences, and silicon process variations. For the Pentium OverDrive processor specifications, the maximum I_{CC} value is derived by testing a sample of components under the following worst case conditions: V_{CC} = 5.3V, full DC current loads on all output pins, and running a file with the predicted worst case software code sequences at the specified frequency. The typical I_{CC} value published is the I_{CC} corresponding to the worst observed I_{CC} value for an average component running under the above worst case conditions. No additional margin is added to this value. I_{CC} typical is not a guaranteed specification.

15.2 Airflow

Since the Pentium OverDrive processor employs an active heat sink, it is not as important that the processor heat sink receive direct airflow, rather that the system has sufficient capability to remove the warm air that the Pentium OverDrive processor will generate. This implies that enough airflow exists at the Pentium OverDrive processor socket site to keep localized heating from occurring. This can be accomplished by a standard power supply fan with a clear path to the processor. Figure 15-1 shows how system design can cause localized heating to occur by limiting the airflow in the area of the processor. The airflow supplied in the system should also be enough to insure that the OEM processor shipped with the system will meet the OEM processor thermal specifications before the system is upgraded with the Pentium OverDrive processor.

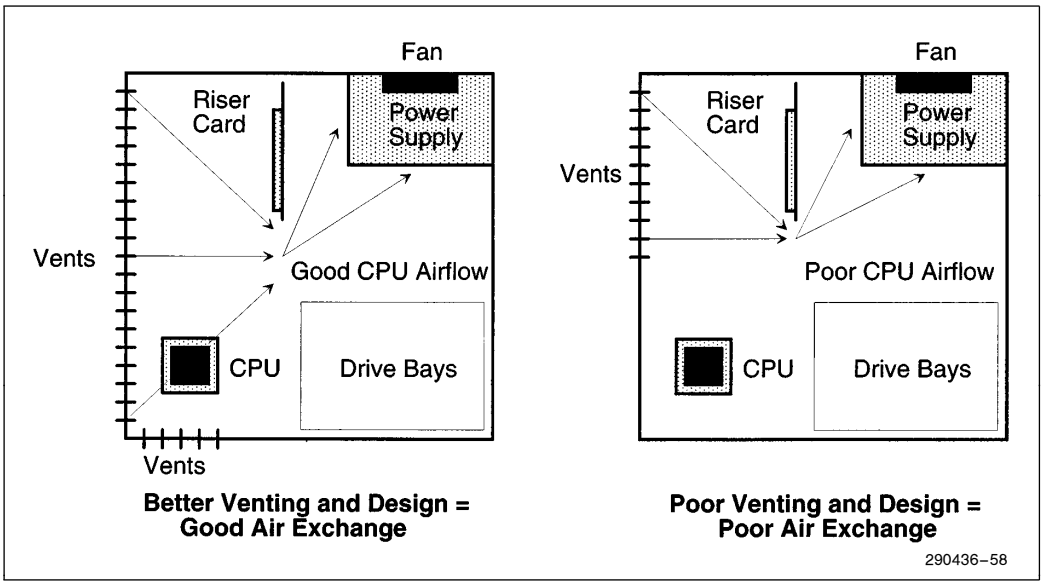


Figure 15-1. Pentium® OverDrive® Processor Airflow Design Examples

APPENDIX A
CACHE FUNCTIONALITY

Cache Introduction

Special hooks are provided to support the Pentium OverDrive processor on-chip write back cache and to maintain cache consistency. The external environment can dynamically change the caching policy of the Pentium OverDrive processor on a line by line basis.

The Pentium OverDrive processor has separate code and data caches. Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. The data cache follows the MESI cache consistency protocol while the code cache follows a subset of that protocol. For a complete description of the cache see the *Intel486 Microprocessor Family Data Book*(2).

NOTE:
2. A generic discussion on the operation of cache memories can be found in the Intel Cache Tutorial available from your Intel sales representative or from Intel's Literature department, order #296543-002.

Cache Organization

The Pentium OverDrive processor includes separate code and data caches on chip to meet its performance goals. The code and data caches can be accessed simultaneously. The code cache can provide up to 16 bytes of raw opcodes and the data cache can provide data for two data references all in the same clock. Each of the caches are accessed with physical addresses and each cache has its own TLB (translation look aside buffer) to translate linear addresses to physical addresses. A cache consistency protocol called the **MESI** protocol is implemented in the data cache to ensure data consistency in a multiprocessor environment.

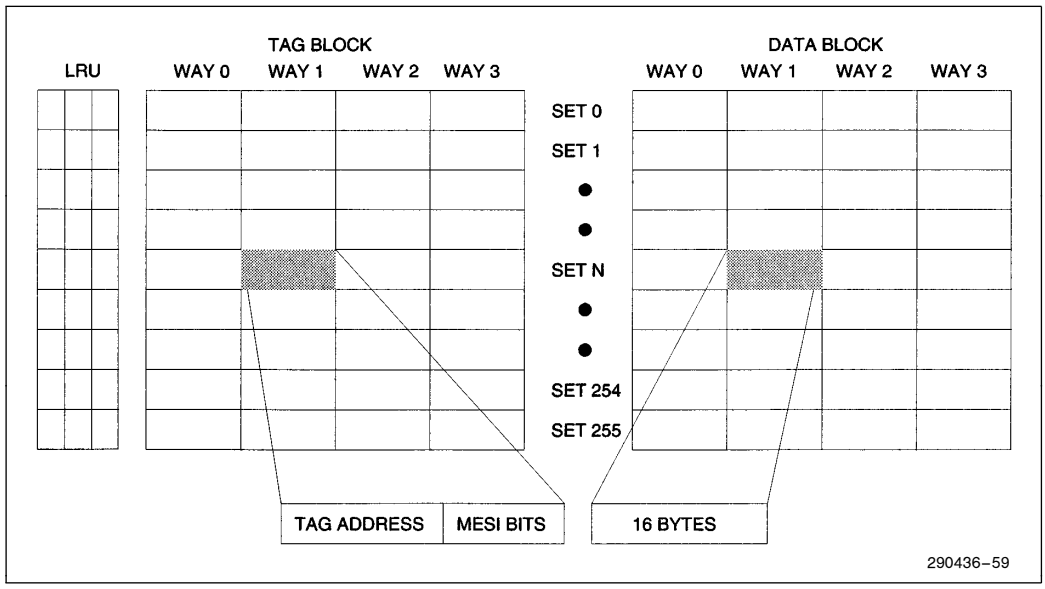


Figure A-1. Conceptual Organization of Data Cache

Each of the caches are 16 Kbytes in size and each is organized as a 4-way set associative cache. There are 256 sets in each cache, each set containing 4 lines. Each cache line is 16 bytes wide. Replacement in both the data and instruction caches is handled by a pseudo LRU mechanism which requires three bits per set in each of the caches. A conceptual diagram of the organization of the data cache is shown in Figure A-1.

The data cache can support two data references simultaneously in one clock, one from each of the two pipelines. It is a write back cache with full support for data consistency in a multimaster environment. This is implemented with two status bits associated with each cache line. The data cache can optionally be configured in write through mode on a line by line basis when in write back cache mode. The storage array in the data cache is single ported but interleaved on 4 byte boundaries to be able to provide data for two simultaneous accesses to the same cache line. The tags in the data cache are triple ported. One of the ports is dedicated to snooping while the other two are used to lookup two independent addresses corresponding to data references from each of the pipelines. The code cache tags are also triple ported. Again, one port is dedicated to support snooping and other two ports facilitate split line accesses (simultaneously accessing upper half of one line and lower half of the next line).

The data cache has a 4-way set associative, 64-entry TLB for 4 KB pages and a separate 4-way set associative, 8-entry TLB to support 4 MB pages. The code cache has one 4-way set associative, 32-entry TLB for 4 KB pages as well as 4 MB pages which are cached in 4 KB increments. The TLBs associated with the instruction cache are single ported whereas the data cache TLBs are fully dual ported to be able to translate two independent linear addresses for two data references simultaneously. Replacement in the TLBs is handled by a pseudo LRU mechanism (similar to the Intel486™ CPU) that requires 3 bits per set. The tag and data arrays of the TLBs are parity protected with a parity bit associated with each of the tag and data entries in the TLBs.

State Transition Tables

Lines cached in the Pentium OverDrive processor can change state because of Pentium OverDrive processor generated activity or as a result of activity on the Pentium OverDrive processor bus generated by other bus masters (snooping). As shown in the following tables, state transitions occur because of Pentium OverDrive processor generated transactions (memory reads/writes) and snooping by the external system. This protocol has minor differences from the MEI protocol of the Write-Back Enhanced IntelDX2 processor as detailed in Appendix B.

READ CYCLE

The state transitions for the data cache during reads are shown in Table A-1. For a cache line that is in the M (Modified), E (Exclusive) or S (Shared) states, the data is transferred from the cache to the core, with no bus cycle generated.

Three different cases can occur when a cache read occurs for an I-state (Invalid) line. An access to an invalid line indicates a miss in the cache, so a read cycle will be generated. If the **CACHE#** and **KEN#** pins are sampled low, and **WB/WT#** is high, then the line will be stored in the E-state in the cache. **WB/WT#** is sampled with the first **BRDY#** or **RDY#** of the transfer, while **KEN#** is sampled one clock before the first **RDY#** or **BRDY#.** If the **CACHE#** and **KEN#** are low, and **WB/WT#** is low, then the cache will be defined as write-through. If **PWT** is HIGH, cache line fills will always be stored as shared lines, even if **WB/WT#** is high. This will cause the line to be stored in a S state. If either **CACHE#** or **KEN#** is high, then the line is non-cacheable, so it will remain in the I state.

Table A-1. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Unlocked Read Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
E	n/a	E	Read hit; data is provided to the Pentium OverDrive processor core by cache. No bus cycle is generated.
S	n/a	S	Read hit; Data is provided to the Pentium OverDrive processor by the cache. No bus cycle is generated.
I	**CACHE#** low AND **KEN#** low AND **WB/WT#** high AND **PWT** low	E	Data item does not exist in cache (MISS). A bus cycle (read) will be generated by the Pentium OverDrive processor. This state transition will happen if **WB/WT#** is sampled high with first **BRDY#** or **RDY#.**
I	**CACHE#** low AND **KEN#** low AND **(WB/WT#** low OR **PWT** high)	S	Same as previous read miss case except that **WB/WT#** is sampled low with first **BRDY#** or **RDY#.** If **PWT** is high, **WB/WT#** is ignored and the resulting line state is always ''S''.
I	**CACHE#** high OR **KEN#** high	I	**KEN#** pin inactive; the line is not intended to be cached in the Pentium OverDrive processor.

NOTE:
The transition from I to E or S-states (based on **WB/WT#)** happens only if the line is cacheable. If **KEN#** is sampled high, the line is not cached and remains in the I-state.

WRITE CYCLE

The state transitions of data cache lines during Pentium OverDrive processor generated write cycles are illustrated in Table A-2. Writes to SHARED lines in the data cache are always sent out on the bus along with updating the cache with the write item. The status of the **PWT** and **WB/WT#** pins during these write cycles on the bus determines the state transitions in the data cache during writes to S-state lines.

A write to a SHARED line in the data cache will generate a write cycle on the Pentium OverDrive processor bus to update memory and/or invalidate the contents of other caches. If the **PWT** pin is driven high when the write cycle is run on the bus, the line will be updated, and will stay in the S- state regardless of the status of the **WB/WT#** pin that is sampled with the first **BRDY#** or **RDY#.** If **PWT** is driven low, the status of the **WB/WT#** pin sampled along with the first **BRDY#** or **RDY#** for the write cycle determines what state (E or S) the line transitions to.

The state transition from S to E is the only transition in which the data and the status bits are not updated at the same time. The data will be updated when the cycle is written to the Pentium OverDrive processor write buffers. The state transition does not occur until the write has completed on the bus (last **BRDY#** or **RDY#** has been returned). Writes to the line after the transition to the E-state will not generate bus cycles. However, it is possible that writes to the same line that were buffered before the transition to the E-state will generate bus cycles after the transition to E-state.

An inactive **EWBE#** input will stall subsequent writes to an E- or an M- state line until **EWBE#** is returned active.

Table A-2. Data Cache State Transitions for Pentium® OverDrive® Processor Initiated Write Cycles

Present State	Pin Activity	Next State	Description
M	n/a	M	Write hit; update data cache. No bus cycle generated to update memory.
E	n/a	M	Write hit; update cache only. No bus cycle generated; line is now MODIFIED.
S	**PWT** low AND **WB/WT#** high	E	Write hit; data cache updated with write data item. A write through cycle is generated on bus to update memory and/or invalidate contents of other caches. All subsequent writes to E- or M-state lines are held off until completion of write cycle is known and state transition happens.
S	**PWT** low AND **WB/WT#** low	S	Same as above case of write to S-state line except that **WB/WT#** is sampled low.
S	**PWT** high	S	Same as above cases of writes to S-state lines except that this is a write hit to a line in a write-through page; status of **WB/WT#** pin is ignored.
I	n/a	I	Write MISS; a write through cycle is generated on the bus to update external memory. No allocation is done.

NOTE:
Memory writes are buffered while I/O writes are not. There is no guarantee of synchronization between completion of memory writes on the bus and instruction execution after the write.

INQUIRE CYCLES (SNOOPING)

The purpose of inquire cycles is to check whether the address being presented is contained within the caches in the Pentium OverDrive processor. Inquire cycles may be initiated with or without an invalidation request (**INV** = 1 or 0). The processor samples the snoop address during the clock that **EADS#** is active. An inquire cycle is run through the data and code caches through a dedicated snoop port to determine if the address is contained in one of the Pentium OverDrive processor caches. If the address is in a Pentium OverDrive processor cache, the **HIT#** pin is asserted. If the address hits a modified line in the processor , the **HITM#** pin is also asserted and the modified line is then written back to external memory.

Table A-3 shows the state transitions for inquire cycles.

Processor Code Cache Consistency Protocol

The Pentium OverDrive processor code cache follows a subset of the MESI protocol. Access to lines in the code cache are either a Hit (Shared) or a Miss (Invalid). In the case of a read hit, the cycle is serviced internally to the Pentium OverDrive processor and no bus activity is generated. In the case of a read miss, the read is sent to the external bus and may be converted to a line fill.

Lines are never overwritten in the code cache. Writes generated by the Pentium OverDrive processor are snooped by the code cache. If there is a hit, the line is invalidated. If there is a miss, no action is taken by the code cache.

Warm Reset Cache Behavior

The **INIT** pin can be used to reset the Pentium OverDrive processor without invalidating the on-chip cache. The Pentium OverDrive processor state after **INIT** is the same as the state after **RESET** except that the internal caches, floating point registers, and SMM Base Register retain whatever values they had prior to recognition of **INIT**. The **INIT** signal can be used instead of **RESET** for warm resets when the cache contents need to be maintained. However, **INIT** cannot be used in lieu of **RESET** after power up. For more information on the INIT and the Pentium OverDrive processor, please see Section 10.3.

Table A-3. Cache State Transitions during Inquire Cycles

Present State	Next State INV = 1	Next State INV = 0	Description
M	I	S	Snoop hit to a MODIFIED line indicated by **HIT#** and **HITM#** pins low. Pentium OverDrive processor schedules the writing back of the modified line to memory.
E	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
S	I	S	Snoop hit indicated by **HIT#** pin low; no bus cycle generated.
I	I	I	Address not in cache; **HIT#** pin high.

APPENDIX B
DESIGNING FOR Write-Back Enhanced IntelDX2™/ Pentium® OverDrive® PROCESSOR COMPATIBILITY

End Users have made upgradability an expected feature in any personal computer purchase. The Pentium OverDrive Processor is the intended upgrade for systems based on the Write-Back Enhanced IntelDX2 processor, an IntelDX2 processor with an on-board write back cache. When installed in a system designed to support a write back processor cache, the Pentium OverDrive processor can reach its full performance potential.

To make the task of designing an upgradable system easier, the Write-Back Enhanced IntelDX2 and the Pentium OverDrive processor have been designed to be compatible with one another. However, since the Pentium OverDrive processor retains many of its Pentium processor features, certain system design considerations must be taken into account to ensure that a Write-Back Enhanced IntelDX2 processor system can be upgraded seamlessly.

Throughout this section, a ''Single Socket Design'' will refer to a motherboard design that has only one processor site. This means that the Write-Back Enhanced IntelDX2 processor must be removed from the socket before the Pentium OverDrive processor can be installed. A ''Dual Socket Design'' refers to a two socket motherboard, one in which the Write-Back Enhanced IntelDX2 resides in a fixed location, and the Pentium OverDrive processor is installed into an empty upgrade socket. This section will make reference to both types of designs, but concentrates on the single socket design strategy.

The following section provides a list of considerations that must be examined to allow a Pentium OverDrive processor to operate properly in a system designed to support the Write-Back Enhanced IntelDX2 processor and a write back processor cache. The considerations listed here are only intended to be relevant to the Write-Back Enhanced IntelDX2 processor Enhanced Bus Mode although some may still be valid for the Standard Bus Mode. These considerations are provided as guidelines only, and should be used in conjunction with the rest of this document to ensure proper Pentium OverDrive processor operation.

Pinout Differences

The Pentium OverDrive processor pinout is based on a 19x19 PGA package as opposed to the Write-Back Enhanced IntelDX2 processor 17x17 PGA package. Most of the signals that are common between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor exist on the same pin on both parts (assuming that pin A1 on the Write-Back Enhanced IntelDX2 processor = Pin B2 on the Pentium OverDrive processor).

NOTE:
All references to Pentium OverDrive processor pins are with respect to a 19x19 grid, while references to Write-Back Enhanced IntelDX2 processor pins are on a 17x17 grid.

ADDITIONAL PINS ON THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor defines signal pins that provide functionality that the Write-Back Enhanced IntelDX2 processor does not have. These pins are defined in Table B-1.

Table B-1. Additional Pentium® OverDrive® Processor Pins

Signal Name	Pentium® OverDrive® Processor Pin/ Write-Back Enhanced IntelDX2 Processor Pin	Comment
BLEN# (Input)	A7/Not Present	**BLEN#** (Burst Length) controls write bursting on the Pentium OverDrive processor. It can not be toggled and should be tied high, low, or left unconnected. It must be driven LOW if the system is able to accept burst write backs. If **BLEN#** is driven HIGH to force write backs to be written out as four separate write cycles, HOLD will not be recognized until all four cycles have completed, even though each cycle will have its own **ADS#** and **BLAST#.**
EWBE# (Input)	P1/Not Present	**EWBE#** (External Write Buffer Empty) will allow writes to E or M state lines when asserted LOW. If it is sampled HIGH the processor will hold off writes to E or M state lines until asserted LOW again.
HIT# (Output)	U2/Not Present	**HIT#** provides an indication that an external snoop has hit a M,E or S state line in the internal cache.
UP# (Output)	C15/B14	**UP#** is driven LOW to indicate to the system that an upgrade processor is installed. In a single socket design, it shares a pin with the Write-Back Enhanced IntelDX2 processor signal, **TMS.** In a dual socket design, it should be connected to the Write-Back Enhanced IntelDX2 processor **UP#** (Input).

Due to its larger package and the ability to consume more power, the Pentium OverDrive processor also defines a number of extra V_{CC} and V_{SS} pins that the Write-Back Enhanced IntelDX2 processor does not support. The extra pins are listed in Table B-2.

Table B-2. Additional V_{CC} and V_{SS} Pins

V_{CC}	V_{SS}	V_{SS}	V_{CC}	V_{SS}	V_{SS}
	A5	U3	K19	G19	
A9	A8	U5	L1	H1	
A10	A12	U6	L19	H19	
A11	A13	U7	R1	M1	
A16	A14	U8	R19	M19	
D1	A15	U12	U4	N19	
D19	A17	U13	U9	Q1	
J1	C19	U14	U10	Q19	
J19	E1	U15	U11	S1	
K1	E19	U17	U16	S19	

PINS NOT SUPPORTED BY THE Pentium® OverDrive® PROCESSOR

The Pentium OverDrive processor supports all of the pins on the Write-Back Enhanced IntelDX2 processor except those required for JTAG boundary scan functionality and the **UP#** input pin. Single socket designs should ensure that if boundary scan features are implemented, they will not interfere with the operation of the Pentium OverDrive processor. Dual socket designs should not route the Pentium OverDrive processor into the boundary scan chain. Table B-3 lists the location of the pins that exist on the Write-Back Enhanced IntelDX2 processor, and the corresponding different signals on the Pentium OverDrive processor.

Table B-3. Unsupported Write-Back Enhanced IntelDX2 Processor Pins

Write-Back Enhanced IntelDX2 Processor Signal Name/Pin	Pentium® OverDrive® Processor Signal Name/Pin	Comment
TCK (Input) Pin A3	**INC** Pin B4	Pin B4 on the Pentium OverDrive processor is defined as an **INC** pin so that **TCK** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDI (Input) Pin A14	**INC** Pin B15	Pin B15 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDI** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TDO (Output) Pin B16	**INC** Pin C17	Pin C17 on the Pentium OverDrive processor is defined as an **INC** pin so that **TDO** can be used by the Write-Back Enhanced IntelDX2 processor in a single socket design without requiring a jumper.
TMS (Input) Pin B14	**UP#** (Output) Pin C15	If the Write-Back Enhanced IntelDX2 processor boundary scan features are used in a single socket design, the design should ensure that **TMS** will not conflict with the Pentium OverDrive processor **UP#** when the upgrade is installed.
UP# (Input) Pin C11	**INC** Pin D12	Pin D12 on the Pentium OverDrive Processor is defined as an **INC** pin so that there can be no conflict with **UP#** (Input).

SHARED SIGNALS LOCATED ON DIFFERENT PINS

There are several signals that the Pentium OverDrive Processor has in common with the Write-Back Enhanced IntelDX2 processor, but which are located on different pins. An example of this would be the **HITM#** signal. On the Pentium OverDrive processor, it is located in the outer row of pins, while on the Write-Back Enhanced IntelDX2 processor, it is located on one of the inner row processors. Single socket designs require that these signals be tied together so that the use of a jumper to reroute the signal is unnecessary. This is done through the use of the **INC** pin.

INC pins, by definition are ''internally not connected'' and may be used for routing of signals. Certain Pentium OverDrive processor **INC** pins should be connected to the signals that correspond to the Write-Back Enhanced IntelDX2 processor write back signals and the **SRESET** signal. Table B-4 details pins that should be routed together. Please note that the last two columns in Table B-4 are the pins on the Pentium OverDrive socket which must be routed together.

Table B-4. Single Socket Compatibility Signals

Signal	Write-Back Enhanced IntelDX2 Processor Signal Pin	Pentium® OverDrive® Processor Signal Pin	Pentium® OverDrive® Processor INC Pins
INV	A10	N1	B11
HITM#	A12	U1	B13
CACHE#	B12	G1	C13
WB/WT#	B13	T1	C14
INIT	C10	F19	D11
FERR#	C14	B14	D15

Figure B-1 shows an example of how the INC pins shown in Table B-4 should be connected together to allow single socket compatibility between the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor. The figure is provided as an example only and is not intended to be guide for how the signals should actually be routed on a motherboard.

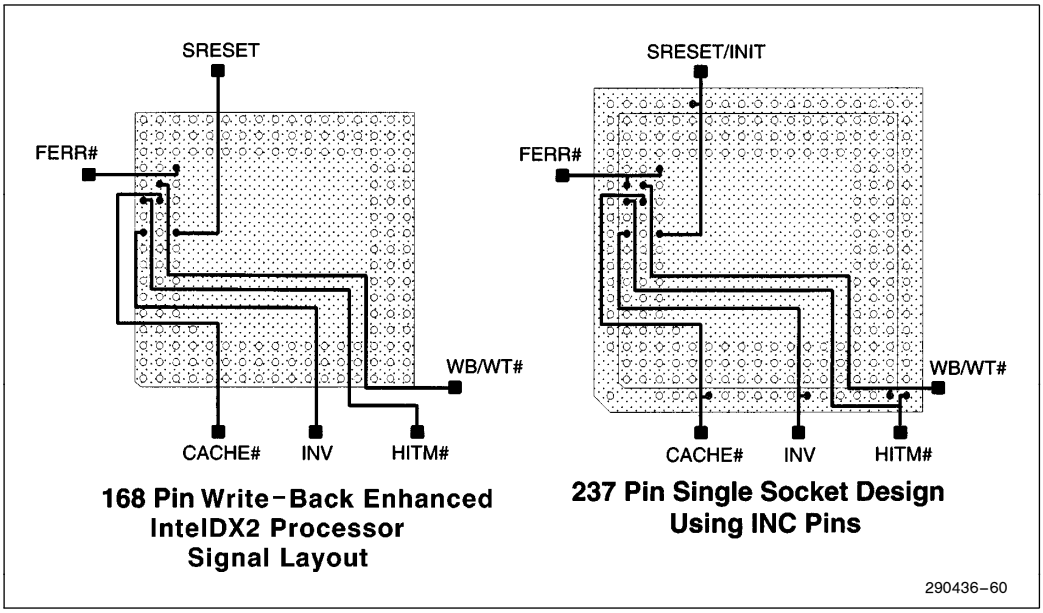


Figure B-1. Sample Routing of INC Pins

Functional Differences

The Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor have been designed to be functionally alike, but because the Pentium OverDrive processor is based on the advanced Pentium processor core, there are some minor differences that should be accounted for to ensure that a Pentium OverDrive processor will operate properly in a Write-Back Enhanced IntelDX2 processor-based system.

WRITE BACK PROCESSOR CACHE CONSIDERATIONS

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor support an internal write back processor cache. The Pentium OverDrive processor carries over the Pentium processor cache protocol which supports multiple processors in the same system. The Write-Back Enhanced IntelDX2 processor cache coherency protocol is designed for single processor systems and is a subset of the Pentium OverDrive processor MESI protocol. If implemented correctly, a system can be designed that will support both protocols without sacrificing functionality. The differences of the cache cycles between the two processors are described below in Table B-5.

For any cache read cycle (read hit or line fill), the Pentium OverDrive processor behaves in the same manner as the Write-Back Enhanced IntelDX2 processor.

As detailed in the Table B-5, the Pentium OverDrive processor allows cache transitions on write through cycles (write hits to 'S' state lines). If **PWT** is driven low, the processor will use the state of **WB/WT#** to determine the final state of the entire cache line, even if only part of the line was written out by the write through cycle. If **WB/WT#** is driven HIGH, the state of the line will be changed to the 'E' state. If driven LOW, the line will remain in the 'S' state. This differs from the Write-Back Enhanced IntelDX2 processor and its dedicated 'S' state which always enforces the write through properties of a line stored in the 'S' state. If a system allows regions of memory to be stored as write through only via the **WB/WT#** pin, and other memory regions are stored as write back lines, then **WB/WT#** must toggle properly to

Table B-5. Differences in Cache Cycles

Type of Cycle	Pentium® OverDrive® Processor Line State Transition	Write-Back Enhanced IntelDX2 Processor Line State Transition	Comments
Cache Write Hit to 'S' State Line	'S' to 'E' OR 'S' to 'S'	'S' to 'S'	The Pentium OverDrive processor samples **WB/WT#** on write through cycles if **PWT** is LOW to determine what kind of transition should occur.
External Snoop Hit **INV** = 0	'M' to 'S' 'E' to 'S' 'S' to 'S'	'M' to 'E' 'E' to 'E' 'S' to 'S'	The assumption that a Write-Back Enhanced IntelDX2 processor will operate in a single processor system allows for direct transitions to the 'E' state.

ensure that 'S' state lines are never changed to write back 'E' lines. If the cache is used in a write back mode only (linefills are never stored in the 'S' state), then there will be no cache coherency issues, but there can be a performance issue due to snoop hits with **INV** = LOW.

For external snoop hits into the cache, the Pentium OverDrive processor differs in behavior from the Write-Back Enhanced IntelDX2 processor only in external snoop hits that drive **INV** = LOW. As shown in Table 10-5, any time a snoop hit occurs with **INV** = LOW, the Pentium OverDrive processor will change the cache line state to 'S'. The Write-Back Enhanced IntelDX2 processor will allow lines defined as write back ('M' and 'E') to transition to the initial write back line state of 'E'. If the line started out in the 'S' state, the Write-Back Enhanced IntelDX2 processor will protect the write through status of the line by keeping it in the 'S' state. On the Pentium OverDrive processor, if a system design supports snoop cycles with INV = LOW, this could result in write back lines ('M' or 'E') being stored in a write through state ('S'). This will not cause memory coherency issues, but any time a write cycle to the line is generated, the cycle will be driven to the bus, rather than simply stored in the cache in the 'M' state. To avoid performance issues, systems that can drive **INV** = LOW should drive **WB/WT#** = HIGH when a write through cycle to such a line occurs on the bus. As shown in Table B-5, this will ensure that a write back line that has accidentally been converted to a write through line will not cause more than one unnecessary write cycle on the bus.

STANDARD/ENHANCED BUS DIFFERENCES

Both the Write-Back Enhanced IntelDX2 processor and the Pentium OverDrive processor use the **WB/WT#** pin as an initialization input on the falling edge of **RESET.** Several signals behave differently depending on if the processors are operating in enhanced bus mode or standard bus mode. Some of these behaviors are slightly different between the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor, and are listed below in Table B-6.

Table B-6. Differences in Bus Modes

Functionality	Pentium® OverDrive® Processor	Write-Back Enhanced IntelDX2 Processor
Standard Bus Mode CPUID	0153xh x = 0 to F	0043xh x = 0 to F
Enhanced Bus Mode CPUID	0153xh x = 0 to F	0047xh x = 0 to F
Standard Bus Mode **INIT**	**INIT** is treated as an Interrupt	SRESET is not an interrupt
Standard Bus Mode **FLUSH#**	**FLUSH#** will take about 15 Bus CLKs No Write Backs	**FLUSH#** will take 1 Bus CLK No Write Backs

One item to note in Table B-6 is that the **INIT** pin on the Pentium OverDrive processor is treated as an edge triggered interrupt in both the standard and enhanced bus modes. This means that **INIT** will not be recognized until instruction boundaries, and after **INIT** has been asserted and recognized, more ADS# cycles can be started, even if **INIT** has not been deasserted.

SOFTWARE DIFFERENCES

Due to the Pentium processor features found on the Pentium OverDrive processor, there are several software visible differences that should be accounted for in any system specific firmware or BIOS routines.

Cache Testing and Test Registers

The cache of the Pentium OverDrive processor is structured as separate code and data caches, each 16 KBytes in size. Because of this structure, the Pentium OverDrive processor supports Model Specific Registers (MSR's) for cache testing, rather than the Write-Back Enhanced IntelDX2 processor Test Registers. Any attempt to access the Write-Back Enhanced IntelDX2 processor test registers on the Pentium OverDrive processor will result in invalid opcode exceptions. For more information on testing the caches of the Pentium OverDrive processor, please contact Intel.

Timing Loops

Timing loops (i.e.: executing a tight loop that does nothing) are a common method of providing a software based delay for I/O recovery. Because of the Pentium processor core and an increased core speed, the Pentium OverDrive processor will be able to execute instructions must faster than previous generations of processors. It is suggested that timing loops be avoided, and that a hardware based delay scheme be developed, such as writing to a dummy I/O port that will delay the returning of **RDY**# for a fixed amount of time.

EXTERNAL SNOOPING REQUIREMENTS ON EADS#

The specification set out in the Hardware Design Considerations Section (Sections 10.1.1.1 and 10.1.1.2) must be observed to ensure that EADS# will be recognized properly by both the Pentium OverDrive processor and the Write-Back Enhanced IntelDX2 processor.

DIFFERENCES IN STOP GRANT STATE OPERATION

If the **STPCLK**# pin is asserted and the Pentium OverDrive processor issues the stop grant special cycle, the processor is in the stop grant state. While in this state, the following conditions apply:

1) If any of the following interrupts are asserted, they will be latched and serviced as soon as the **STPCLK**# pin is released and the processor exits the stop grant state:

   FLUSH#, SMI#, NMI, INIT

   If an interrupt is asserted and then released while the processor is in the stop grant state, it will be recognized once the processor exits the stop grant state even though the interrupt may be deasserted. This behavior is different than that of the Write-Back Enhanced IntelDX2 processor, which requires these interrupts to be held until the processor has exited the stop grant state.

   NOTE:
   INTR is a level triggered interrupt and will not be latched. It must be held until the interrupt acknowledge cycle to guarantee recognition.

2) Unlike the Write-Back Enhanced IntelDX2 processor, if **INIT** is asserted while in the stop grant state, the processor will not automatically exit the stop grant state and perform the **INIT.** As mentioned above, **INIT** is latched and will be recognized once the processor exits the stop grant state when **STPCLK**# is deasserted.