StrongARM® SA-1101 Microprocessor Companion Chip

Specification Update

January 1999

Notice: The name of product may contain design defects or errors known as errata. Characterized errata that may cause the name of product's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278231-004

Contents

Revision History

Date	Version	Description
01/28/99	004	The documentation changes have been removed from the specification update and applied to the developer's manual. Under Affected Documents/Related Documents, removed SA-1101 Datasheet to show discontinuance; added registered trademark to the title.
01/15/99	003	Under Document Changes, changed buffer control signal in the PCCR.
11/03/98	002	Under Document Changes, added new Table 21-2.
10/19/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
StrongARM™ SA-1101 Microprocessor Companion Chip Technical Reference Manual	278170-001
StrongARM™ SA-1101 Microprocessor Companion Chip Brief Datasheet	278171-001

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	D	#	#			
1	X			12	NoFix.	Snooped Writes After Sleep May Fail
2	X			12	NoFix.	Bus Lock-Up on Entering Sleep
3	X			13	NoFix.	Set-Up Violation When Exiting From Sleep
4	X			13	Fix.	IrefEN and VCOON Are Not Reset on Entry to Sleep
5	X			13	Eval.	Length of USB Port Reset Pulse Too Short on Power Up
6	X			13	Fix.	USB Pad Transistors Do Not Turn Off on Entry to Sleep

Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	#	#			
					None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES

Identification Information

Markings

DE-S1101-AA.

Markings	Package
DE-S1101-AA	256 mBGA

This document contains errata for the StrongARM® SA-1101 Microprocessor Companion Chip (SA-1101). The SA-1101 device revision that is affected by this errata can be identified as order number DE-S1101-AA.

Related Information

As of May 17, 1998, Digital Equipment Corporation's StrongARM, PCI Bridge, and Networking component businesses, along with the chip fabrication facility in Hudson, Massachusetts, were acquired by Intel Corporation. As a result of this transaction, certain references to web sites, telephone numbers, and fax numbers have changed in the documentation. Updates to this information are planned for the next version of this manual. Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling:

1-800-332-2717 or by visiting Intel's website for developers at:

http://developer.intel.com

The Intel Massachusetts Customer Technology Center services your StrongARM Product, Bridge Product, and Network Product technical inquiries. Please use the following information lines for support:

For Documentation and General Information	For Technical Support
Intel Massachusetts Information Line	**Intel Massachusetts Customer Technology Center**
United States: 1–800–332–2717	Phone (U.S. and international): 1–978–568–7474
Outside United States: 1–303–675–2148	Fax: 1–978–568–6698
Electronic mail address: techdoc@intel.com	Electronic mail address: techsup@intel.com

Errata

1. Snooped Writes After Sleep May Fail

Problem: This problem exists if BAT_FLT or VDD_FLT assert while there is new data in the Update FIFO (snooped but not yet written to the “dedicated” FB DRAM). This problem only exists in dedicated display memory mode of operation. Unified display memory mode of operation does not use the Update FIFO.

Implication: Several pixels, which were correctly snooped and written to the Update FIFO, might not be written correctly to the dedicated FB DRAM until the screen is redrawn.

Workaround: There are two workarounds.

1. Software can rewrite the pixels most recently snooped by the SA-1101 before the BAT_FLT or VDD_FLT condition is asserted. BAT_FLT or VDD_FLT assertion is a relatively rare and severe low-power event and should not impact performance.
2. Software-initiated sleep can disable snoop mode and empty the Update FIFO before shutting off BCLK and the Video Memory Controller (VMC). This ensures that all snooped pixels are flushed from the FIFO and written to the DRAM before going into the sleep condition. Update FIFO “fullness” and “empty” status flags in the Update FIFO Status Register (UFSR) can be read via register reads.

Status: NoFix.

2. Bus Lock-Up on Entering Sleep

Problem: This problem exists on entering the sleep condition via setting the sleep bit in the Control Register (SKCR) of the SA-1100 interface and Shared Memory Controller (SMC).

Implication: There is a narrow window of time in which a UsbReq or VidReq may assert and cause MBREQ to go high. The SA-1100 grants the bus to the SA-1101, but the SA-1101 has initiated the sleep sequence and does not do the expected USB or video cycle to shared memory, thus holding and locking up the SA-1100 bus.

Workaround: There are two workarounds.

1. For software-initiated sleep, set the sleep bit in the SKCR to disable the video and USB.
2. For BAT_FLT-induced sleep or VDD_FLT-induced sleep, assert BAT_FLT/VDD_FLT for more than 1 microsecond to allow the sleep state machine to shut off on-chip systems. While asserted they will prevent USB and video from requesting the SA-1100 bus. They should not be allowed to glitch.

Status: NoFix.

3. Set-Up Violation When Exiting From Sleep

Problem: A problem with the self-refresh logic exists when exiting from sleep on one of the Video Memory Controller (VMC) state machine bits (VMCstate[3] FF).

Implication: The Self-Refresh Request signal (SRReq) might change shortly before BCLK and violate set-up time. The sleep state machine is clocked by the external clock; the VMC is clocked by BCLK.

Workaround: To enter software-controlled sleep, set the Force Self-Refresh bit (VMCCR bit 31) before setting the sleep command bit. To exit software-controlled sleep, get out of the sleep condition and clear the Force Self-Refresh bit. Analysis of the VMC state machine indicates that, even if there was a metastability event, the VMC state machine will not enter “illegal” or unknown states. The VMC state machine will return unconditionally to “idle” state and then to “self-refresh” sequence as requested.

Status: NoFix.

4. IrefEN and VCOON Are Not Reset on Entry to Sleep

Problem: The phase-locked loop (PLL) is not shutting off when the SA-1101 enters sleep mode.

Implication: Only bit PLLEn (VCO Bypass) in the Control Register (SKCR) is cleared by the sleep state machine in its process of shutting down the SA-1101. The PLL continues operating and using power. The two bits that control power for the PLL (IrefEn and VCOON) are not reset on entry to sleep.

Workaround: External to the SA-1101, the IREF current can be supplied from a source that is switched on (asserted HIGH) for normal operation and off (LOW) for sleep mode. Cutting off the IREF current shuts down the PLL and reduces power. Any CMOS output in the system with the correct logical behavior will work because it is a low-current requirement. Care must be taken to filter IREF on the source side of the IREF resistor to prevent noise on the SA-1101 side.

Status: Fix.

5. Length of USB Port Reset Pulse Too Short on Power Up

Problem: The length of an USB Port Reset pulse is less than 10 microseconds although the specification requirement is >10 milliseconds. The reset pulse duration is generated by hardware counting out 1ms units of time from a timer, in response to setting the PRS bit in the RhPortStatus register of the USB Host Controller.

Implication: The nSimScaleDownClk bit in the USTCSR register substitutes a faster clock source for the 1ms clock. The SA-1101 powers up with this bit LOW, enabling the fast clock and causing the reset pulse to be too short.

Workaround: During the USB Host Controller reset sequence, set the nSimScaleDownClk bit in the USTCSR register HIGH before clearing the ForceHCReset bit.

Status: Eval.

6. USB Pad Transistors Do Not Turn Off on Entry to Sleep

Problem: This problem exists when the SA-1101 enters the sleep mode. The measure IDD is approximately 180 µA (dependent on temperature), compared to a specification maximum of 20 µA.

Implication: Excess current in the current path in the USB pad driver.

Workaround: None.

Status: Fix.

Specification Changes

None for this revision of this specification update.

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

None for this revision of this specification update.


ARM
POWERED
TM