*StrongARM** SA-1100 Microprocessor Evaluation Platform*

User's Guide

October 1998

Order Number: 278172-001

Contents

Figures

Tables

Introduction 1

This document describes the Intel StrongARM** SA-1100 Microprocessor Evaluation Platform.

For more detailed information about the SA-1100 microprocessor, refer to the *SA-1100 Microprocessor Technical Reference Manual*.

1.1 Document Organization

The user's guide contains the following chapters and one appendix:

- Chapter 1, "Introduction", provides an overview of the SA-1100 platform and describes the major components. It also includes information about switches, LEDs, trim pots, and test points.
- Chapter 2, "Installation", describes the physical and power specifications and the hardware and software requirements for using the SA-1100 platform. It also provides detailed SA-1100 platform installation instructions.
- Chapter 3, "System Startup", provides a memory map and describes system design hints and considerations. It also provides sample test programs for your configuration.
- Appendix A, "Support, Products, and Documentation", contains technical support and ordering information.

1.2 Conventions

The following terminology and conventions are used in this document.

Caution: Cautions provide information to prevent damage to equipment or loss of data.

1.3 Data Units

The following table describes data-unit terminology used throughout this document.

Table 1-1. Data-unit Terminology

Quantity			
Term	**Words**	**Bytes**	**Bits**
Byte	½	1	8
Word[a]	1	2	16
Dword	2	4	32

a) Some SA-1100 documentation use word to refer to a 32-bit quantity.

Note: Notes emphasize important information.

1.4 Numbering

All numbers are decimal or hexadecimal unless otherwise indicated. For example, 19 is decimal, but 19h and 19A are hexadecimal. In ambiguous cases, a subscript indicates the radix of nondecimal numbers.

1.5 Signal Names

All signal names (except SA-1100 signals) are printed in lowercase type. SA-1100 signal names are printed in uppercase type.

A lowercase, n prefix indicates a low-active SA-1100 signal (for example, nCS2). A # suffix on a SA-1100 platform indicates a low-active signal on the board.

Warning: Warning indicates the potential for personal injury.

This chapter provides an overview of the Intel SA-1100 Microprocessor Evaluation Platform and includes the following topics:

- Overview
- Major Components
- Switches
- LEDs and Trim Pots
- External Connectors
- Test Points

1.6 Overview

The SA-1100 evaluation platform is intended to provide evaluation and silicon verification for the SA-1100 processor and is designed to meet the following requirements:

- Provide a powerup vehicle for the SA-1100 microprocessor
- Provide an evaluation board for the SA-1100 microprocessor
- Provide a software development environment

1.7 Major Components

The following subsections describe the major components of the SA-1100 platform.

1.7.1 SA-1100 Microprocessor

The SA-1100 microprocessor is a high-performance, low-power integrated processor configured to run at speeds ranging from 133 MHz to 200 MHz. The SA-1100 packaging is a 208-pin TQFP and is attached to the board via a ZIF socket. The SA-1100 requires two separate voltages to be supplied (1.5 V core and 3.3 V I/O). Please refer to the *SA-1100 Microprocessor Technical Reference Manual* for more detailed information.

1.7.2 Memory System

The memory system on the SA-1100 evaluation board contains memory configurations that allow most aspects of the SA-1100 memory controller to be exercised. The memory provided on the SA-1100 evaluation board contains:

- 512 KB of SRAM
- 16 MB of self-refresh capable EDO DRAM
- Switch to enable either SRAM or DRAM
- 256 KB of 32-bit wide or 128 KB of 16-bit wide (switch selectable) 3.3 V only Flash
- 256 KB of 32-bit wide or 128 KB of 16-bit wide (switch selectable) 3.3 V only ROM
- Socket allowing installation of an operating system Boot ROM SIMM (3.3 V, 5 V, or 12 V)
- Footprints for one pair of 1 M x 16 higher performance Flash components

The EDO DRAM is 60 ns, with an approximate data bandwidth of 100 MB/s. The 16 MB of DRAM is implemented in four banks of 4 MB each. Each of the banks is implemented with two 1 M x 16 memory components.

Because the majority of signals issued by the SA-1100 to memory are programmable, glue logic is generally not required, provided that the drive capabilities of the SA-1100 are not exceeded. On the SA-1100 evaluation board, there were two concerns driving the use of buffers on the address and data buses.

First, because of multiple modes of operation, the memory bus was heavily loaded. Second, because the SA-1100 evaluation board is for initial silicon evaluation, buffering was required to protect sensitive memory devices from electrical abnormalities caused by potentially defective silicon. Buffering isolates the memory components from the SA-1100, removing the possibility of widespread damage.

The SA-1100 evaluation board also uses both SRAM and DRAM on the same board, and the selection is determined via use of a switch. Under normal circumstances, the SA-1100 drives only the address and data buses for either SRAM or DRAM, and only one type of memory can be used at a time. On the SA-1100 evaluation board, however, there was concern that the capacitive loading would exceed the SA-1100 drive capabilities because of this extra memory, so buffering was added. Along with the buffers, an additional security measure was implemented in a complex programmable logic device (CPLD) by controlling the output enables and direction of the data transceivers. This assures that data moves toward the SA-1100 only during a read operation.

The ROM is actually Flash with the WE# signal tied high.

1.7.3 PCMCIA

The PCMCIA implementation on the SA-1100 evaluation board is intended to provide the maximum possible flexibility while supporting one or two socket PCMCIA implementations. The PCMCIA portion of the logic was designed to support the voltage switching required for 3.3 V and 5 V cards as well as hot insertion (with power on) of the card. A low-power CPLD is implemented to support the majority of the Boolean logic required to support a dual-socket implementation, and also to provide an additional level of protection by controlling the drive enables to and from the PCMCIA cards. Also provided is a dual PCMCIA socket, a card cage, and the power controllers for the card and socket interface.

1.7.4 External Register

An external register is implemented and performs the following functions:

- Controls application of 12 V to the PCMCIA card (Flash)
- Controls application of 5 V to the PCMCIA card
- Monitors the voltage sense pins

1.7.5 Clocks

The SA-1100 evaluation board uses the following clocks:

- 32.768 KHz crystal
- 3.6864 MHz crystal
- Oscillators
- Coax connectors (to pulse generators)

Note: The 32.768 KHz and 3.6864 MHz crystals use resistor dividers to assure the voltage level of the clock driven into the SA-1100 is not greater than 1 V. All clocks coming from the external clock sources must NOT have voltage levels higher than 1 V because this will create problems with the 1.5 V CPU core operation on the SA-1100.

In addition, the SA-1100 evaluation board can accept clock sources from test equipment (for example, clock generators) through the connectors J17 and J21.

1.7.6 LCD Screen

The SA-1100 evaluation board is designed to operate with two different LCD panels.

- Kyocera KCS3224ASTT-X1 8 bpp color, STN, with a resolution of 320 x 240 single panel
- Sharp LQ64D341 18 bpp color (16 used), TFT, with a resolution of 640 x 480 single panel

Most of the SA-1100 evaluation boards are shipped with the Kyocera panel, which is a passive color panel. The Sharp LQ64D341 connector is on the board so that functional tests can be performed with the SA-1100 driving TFT panels. Because of cost reasons, this panel will not be shipped with the SA-1100 evaluation board.

1.7.7 Audio Accessories

The SA-1100 evaluation board provides the support for the SA-1100 to connect to various analog devices. The SA-1100 evaluation board includes a telephone jack and a direct access arrangement (DAA) approved for North America and Japan, a microphone, and a speaker. For debugging purposes, a 7-segment LED is provided, along with two discrete LEDs that indicate board and software status. Two footprints are on the board to allow either a Philips UCB1200 or Cirrus CS4271 to interface to the speaker, telecommunication functions, touch screen, and the microphone. (PCB footprints exist for both Philips and Cirrus devices, but only one may be soldered to the SA-1100 platform at any given time.)

1.7.8 Touch Screen

The SA-1100 evaluation board touch-screen panel is used for data input. It is connected to either the UCB1200 or the CS4271.

1.7.9 Keyboard Interface

When the SA-1100 serial channel 4 is running the multimedia codec interface protocol, it is possible to also use the SPI function of serial channel 4 by specifying the use of gpio pins 10 through 13 for alternate functions. The SPI protocol on the SA-1100 interfaces to a USAR Systems UR5HCSPI-06-FB keyboard controller on the SA-1100 evaluation board. The controller then interprets input from the Fujitsu FKB1406 keyboard. The SA-1100 evaluation board provides a pair of connectors to the keyboard. The SA-1100 evaluation board also provides an LED (D16) to indicate that the Caps Lock key is pressed.

1.7.10 Serial I/O Interfaces

The following types of serial I/O interfaces are available:

- A universal serial bus (USB) “device” port (cannot be a “master” or a “hub”) is supplied along with the necessary circuitry.
- IrDA infrared support. The TFDS6000D is a dual-speed IrDA transceiver (115 kb/s or 4 Mb/s). The transceiver receives digital data output from the SA-1100 and converts the data to infrared pulses or receives infrared pulses and converts them to digital data for the SA-1100.
- Synchronous data link controller (SDLC) port configuring Platelike, GeoPort*, or differential RS-422 type interface. Serial port 1 transmit and receive signals are used, and four gpio pins are used for the handshaking signals.
- Two universal asynchronous receiver-transmitter (UART) ports support computer-to-computer connections only (no modem). SA-1100 serial port 3 transmit and receive pins are used. The UART function of serial port 1 is also used on gpio pins 14 and 15 to support an additional UART channel (and SDLC simultaneously).

1.7.11 Power Supply and Power Regulation

The system power requirements are as follows:

- External power transformer (wall unit): +5 V, +3.3 V, +12 V
- Onboard voltage regulators

1.7.12 Miscellaneous Debug and Evaluation Logic

The SA-1100 contains the following debug and evaluation logic:

- Test points for test equipment (such as volt meters, oscilloscopes, and so on)

Note: To observe the SA-1100 signals, the simplest method of operation is to use the Tektronix TLA 711 Logic Analyzer with the P6434 mass termination probes.

- Logic analyzer connectors for observing all SA-1100 signals
- LEDs connected to SA-1100 gpio pins for software debug assistance

1.8 Switches

There are 22 switches on the SA-1100 evaluation board. Figure 1-1 shows the switch locations and Table 1-2 describes the switch functions. These switches (with the exception of S7) are single-pole double-throw (SPDT) minislide switches that have settings showing either a DOT or NO DOT. With the slide in one of its two positions, a DOT is visible on the physical switch. With the slide in the other position, NO DOT is visible.

S7 is a 3-position switch to be placed in the ON position when power is applied to the board.

Figure 1-1. Minislide Switch Locations

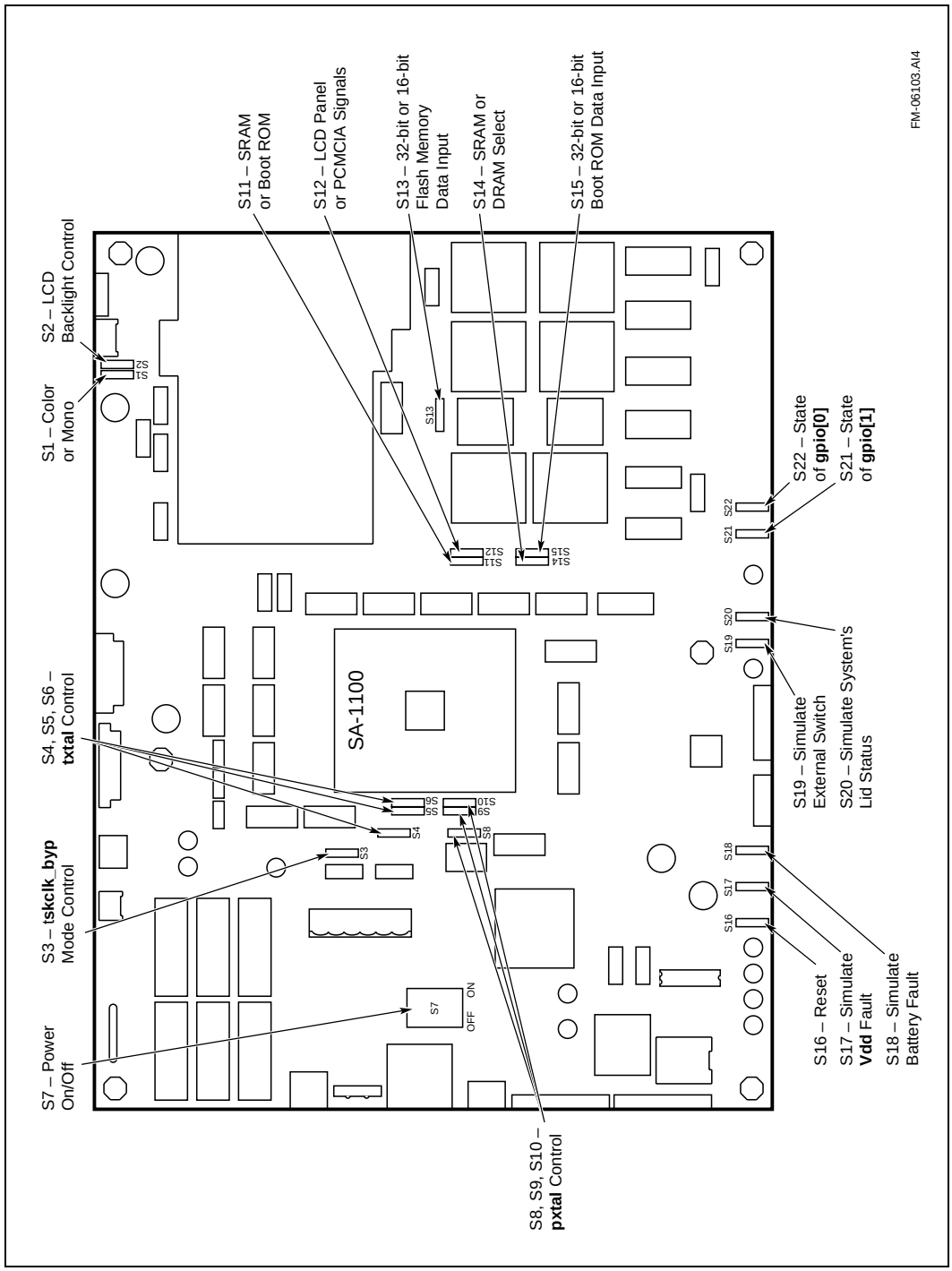


Table 1-2. Minislide Switch Descriptions

Switch	Function	DOT	NO DOT	Schematic[a] Page Number	Initial Setting (Default)
S1	Determines which mode the SA-1100 LCD controller is configured for.	Color	Mono	26	Dot
S2	ON/OFF control for LCD backlight.	OFF	ON	26	No dot
S3	tsclk_byp mode control.	VDDX	GND	3	No dot
S4 through S6	Varies frequency into txtal. txtal can be driven from a pulse generator connected to J17 (load of 0.0 V to 1.0 V, 50 ohms impedance).	Standard	External Input	3	S4 no dot S5 dot S6 dot
S7	Power on/off switch as marked on board.	—	—	30	Left position
S8 through S10	Varies frequency into pxtal. pxtal can be driven from a pulse generator connected to J17 (load of 0.0 V to 1.0 V, 50 ohms impedance).	Standard	External Input	3	S8 no dot S9 dot S10 dot
S11	SA-1100 nCS2 signal for either SRAM component enables or chip select for external Boot ROM (pin 7 of J28).	SRAM	External Boot ROM	20	Dot
S12	Selects whether GPIO signals are used for PCMCIA signals or by SA-1100 to drive 16-bit LCD panel.	LCD	PCMCIA	18	No dot
S13	SA-1100 bit width access to Flash memory.	32 bits	16 bits	15	Dot
S14	Selects either SRAM or DRAM to communicate with data bus.	SRAM	DRAM	9	Dot
S15	SA-1100 bit width access to Boot ROM.	32 bits	16 bits	13	Dot
S16	Reset switch for SA-1100 evaluation board.	Off	On	30	No dot
S17	Simulates a Vdd (+5 V) fault.	No Fault	Fault	31	No dot
S18	Simulates a battery fault.	No Fault	Fault	31	No dot
S19	Simulates an external switch that asserts a signal when the user presses the switch.	Active	Not Active	24	Dot
S20	Simulates a sensor that reports when the system lid (on a portable device) is open or closed.	Open	Closed	24	Dot
S21	Controls gpio[1] state.	gpio[1] High	gpio[1] Low	24	Dot
S22	Controls gpio[0] state.	gpio[0] High	gpio[0] Low	24	Dot

a. Schematics are provided in the kit in PDF format.

1.9 LEDs and Trim Pots

There are twelve LEDs and five trim pots on the SA-1100 evaluation board. Figure 1-2 shows the LED and trim pot locations. Table 1-3 describes the functions of the LEDs and Table 1-4 describes the functions of the trim pots. Certain LEDs are dedicated to specific functions while other LEDs are programmable. All trim pots come preset and can be adjusted by the user for their specific development. All trim pot adjustments operate as follows: turning the trim pot clockwise increases the value or illumination of the display and turning the trim pot counterclockwise decreases the value or illumination of the display.

Figure 1-2. LEDs and Trim Pot Locations

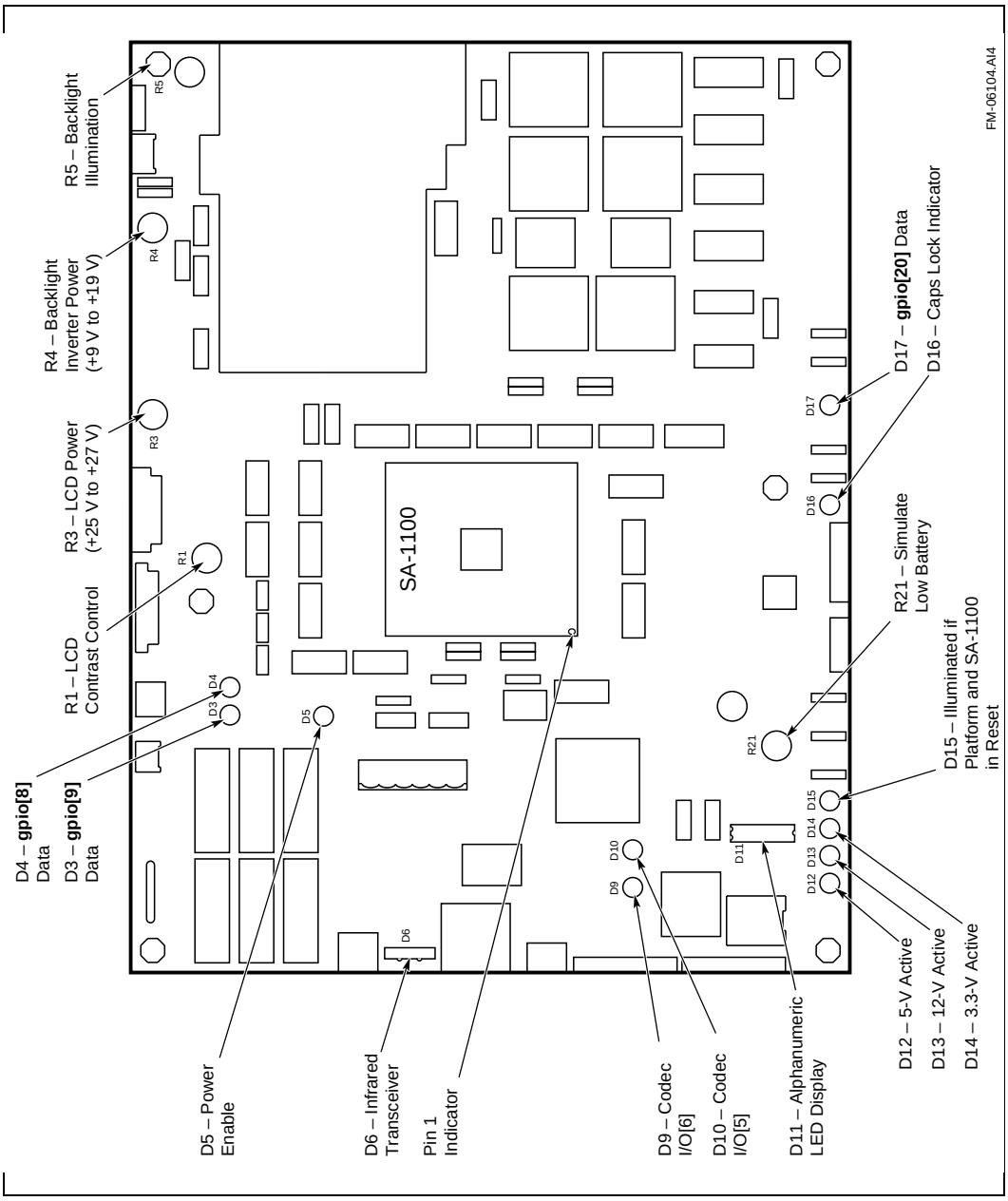


Table 1-3. LED Descriptions

LED	Function	Color	Active State	Programmable	Schematic[a] Page Number
D3	gpio[9] data.	Green	Low	Yes	24
D4	gpio[8] data.	Green	Low	Yes	24
D5	Power enable.	Green	Low[b]	Yes	31
D6	Infrared transceiver communicates via infrared pulses (not to SA-1100).	—	—	—	25
D9	Codec I/O[6].	Red	Low	Yes	27
D10	Codec I/O[5].	Green	Low	Yes	27
D11	Alphanumeric LED display.	—	—	—	27
D12	5.0-V active.	Green	Low	No	30
D13	12-V active.	Green	Low	No	30
D14	3.3-V active.	Green	Low	No	30
D15	Indicates if Reset switch is active.	Red	Low	No	31
D16	Programmer can verify that keyboard is active.	Green	Low	Yes	24
D17	gpio[20] data.	Red	Low	Yes	24

a. Schematics are provided in the kit in PDF format.

b. The SA-1100 asserts pwr_en high and gates it through an inverter for this function.

Table 1-4. Trim Pot Descriptions

Trim Pot	Function	Schematic[a] Page Number
R1	Itsy LCD contrast control	21
R3	Adjust LCD power between +25 V and +27 V	32
R4	Adjust backlight inverter power between +9 V and +19 V	32
R5	Kyocera backlight illumination control	26
R21	Voltage divider (simulates a low battery)	27

a. Schematics are provided in the kit in PDF format.

1.10 External Connectors

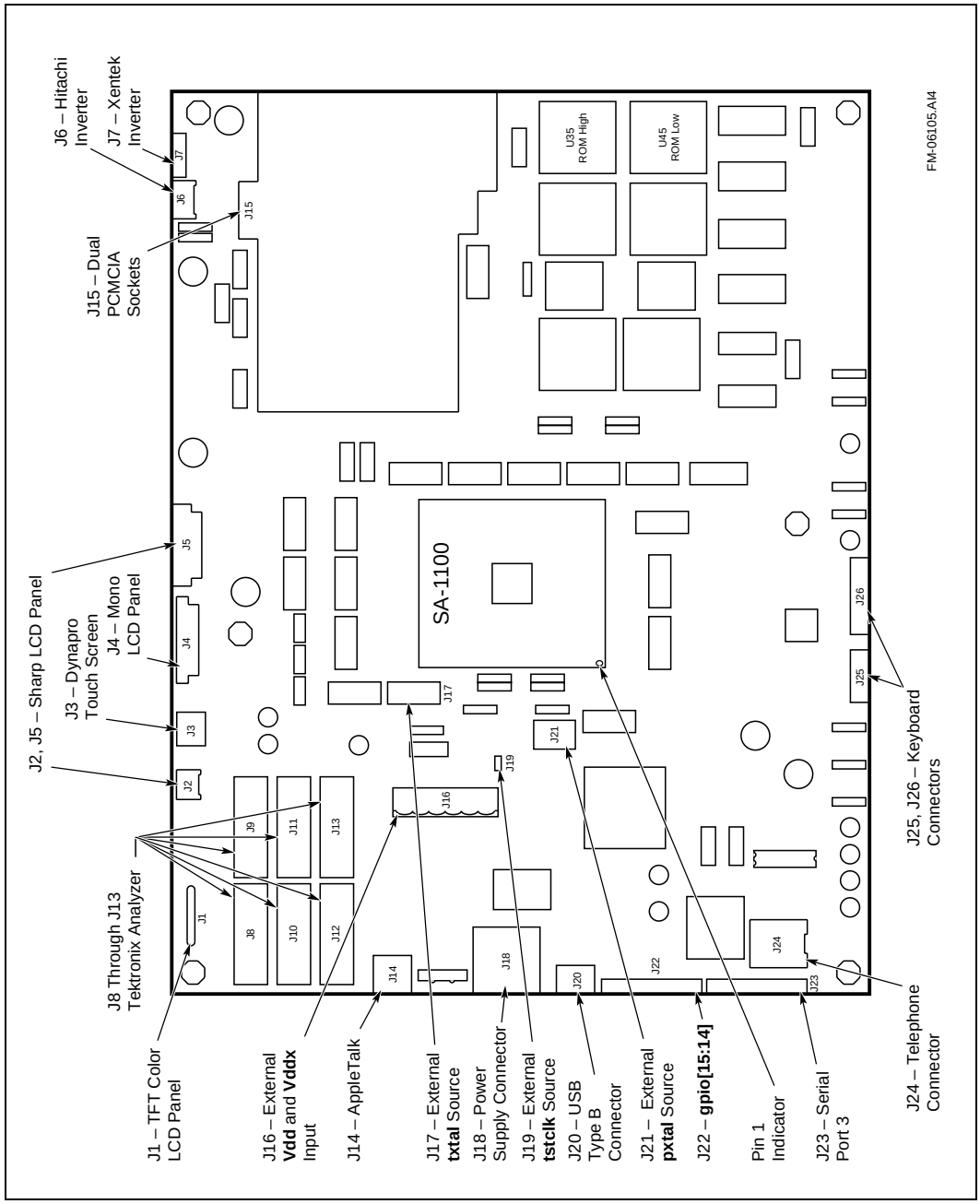
There are 26 external connectors located on the SA-1100 evaluation board. Figure 1-3 shows the locations of the connectors and Table 1-5 describes their functions

Table 1-5. Connector Functions

Connector	Functions	Schematic[a] Page Number
J1	Supports the TFT color LCD panel	25
J2, J5	Interface for Sharp LMSH40TA mono LCD panel	25
J3	Interface for Dynapro touch screen	27
J4	Supports a small mono LCD panel (Itsy)	25
J6	Interface for Hitachi PH-BLCO8-12 inverter for backlight to Kyocera LCD	26
J7	Interface for Xentek inverter	26
J8 through J13	Connectors for Tektronix Logic Analyzer	28
J14	Interface for AppleTalk*	25
J15	Dual PCMCIA sockets	18
J16	External Vddx and Vdd input	31
J17	Can drive txtal signal externally	3
J18	Power supply connector	30
J19	Drives tstclk signal externally	3
J20	Interface for universal serial bus (USB Type B)	25
J21	Can drive pxtal signal externally	3
J22	Serial port 1 (UART to gpio[15:14])	25
J23	Serial port 3	25
J24	Telephone connector	27
J25, J26	Keyboard connectors	24
J27	Kyocera color LCD	25
J28	Connector for ROM card	14

a. Schematics are provided in the kit in PDF format.

Figure 1-3. Connector Locations



1.11 Test Points

There are 96 test points available on the SA-1100 evaluation board's component board. Table 1-6 describes these test points.

Table 1-6. Test Point Descriptions (Sheet 1 of 3)

Test Point	Function	Color	Schematic[a] Page Number
TP1	+13 V to +21 V (LCD power)	Red	26
TP2	Ground	Black	26
TP3	+9 V to +19 V (inverter power)	Red	26
TP4	External +12 V for Xentek inverter (used with Sharp color LCD)	Red	26
TP5	External +12 V for Xentek inverter (used with Sharp color LCD)	Red	26
TP6	Ground	Black	26
TP7	0.0 V to 2.5 V for Xentek inverter (Brightness control used with Sharp color LCD)	Red	26
TP8	+5 V (Sharp LCD LQ64D341)	Red	26
TP9	Ground	Black	30
TP10	TSMY (touch screen minus Y)	Yellow	27
TP11	TSPY (touch screen positive Y)	Yellow	27
TP12	TSPX (touch screen positive X)	Yellow	27
TP13	TSMX (touch screen minus X)	Yellow	27
TP14	+25 V to +27 V (LCD power)	Red	26
TP15	Ground	Black	26
TP16	gpio[9] (data)	Yellow	24
TP17	gpio[8] (data)	Yellow	24
TP18	Ground	Black	30
TP19	Ground	Black	17
TP20	P1_Vpp	Red	17
TP21	P1_12 V	Red	17
TP22	P0_12 V	Red	17
TP23	P0_Vpp	Red	17
TP24	P1_Vcc	Red	17
TP25	gpio[26] (data)	Yellow	28
TP26	gpio[27] (data)	Yellow	28
TP27	Reset	Yellow	31
TP28	Vddx	Red	31
TP29	Power on pwr_en (power enable)	Yellow	31
TP30	P0_Vcc	Red	17
TP31	Power island 1	Red	31
TP32	Power island 1	Red	31

Table 1-6. Test Point Descriptions (Sheet 2 of 3)

Test Point	Function	Color	Schematic[a] Page Number
TP33	Ground	Black	31
TP34	IrDA_Vcc	Red	25
TP35	3.3 V	Red	25
TP36	Ground	Black	25
TP37	Power island 2	Red	31
TP38	Power island 2	Red	31
TP39	Vdd	Red	31
TP40	txtal override	Yellow	3
TP41	P0_INPACK#	Yellow	18
TP42	P1_INPACK#	Yellow	19
TP43	+12 V	Red	30
TP44	+3.3 V	Red	30
TP45	Ground	Black	31
TP46	tstclk	Yellow	3
TP47	Ground	Black	3
TP48	PCMCIA card 0 fully inserted	Yellow	18
TP49	PCMCIA card 1 fully inserted	Yellow	19
TP50	Flash memory, 16- and 32-bit selection	Yellow	15
TP51	+12 V	Red	14
TP52	+3.3 V	Red	14
TP53	+5 V	Red	14
TP54	Ground	Black	14
TP55	+5 V	Red	30
TP56	Ground	Black	30
TP57	pxtal override	Yellow	3
TP58	PCMCIA or 16-bit LCD switch selection	Yellow	18
TP59	+12 V	Red	30
TP60	usbudc+	Yellow	25
TP61	Ground	Black	25
TP62	usbudc-	Yellow	25
TP63	SA-1100 tms	Yellow	2
TP64	SA-1100 tck	Yellow	2
TP65	Vccusb	Red	25
TP66	Ground	Black	25
TP67	USB pull-up power	Red	25
TP68	Ground	Black	30
TP69	SA-1100 tdo	Yellow	2

Table 1-6. Test Point Descriptions (Sheet 3 of 3)

Test Point	Function	Color	Schematic[a] Page Number
TP70	SA-1100 ntrst	Yellow	2
TP71	SA-1100 tdi	Yellow	2
TP72	SRAM and DRAM selection	Yellow	9
TP73	Boot ROM, 16- and 32-bit selection	Yellow	13
TP74	Ground	Black	27
TP75	PCMCIA speaker	Yellow	27
TP76	spkr-	Yellow	27
TP77	spkr+	Yellow	27
TP78	Battery fault	Yellow	31
TP79	Vdd fault	Yellow	31
TP80	+5 V	Red	30
TP81	Ground	Black	30
TP82	+3.3 V	Red	30
TP83	Agnd UCB1200	Black	27
TP84	Agnd UCB1200	Black	27
TP85	Codex A/D input [1]	Yellow	27
TP86	Ground	Black	30
TP87	Agnd CS4271	Black	27
TP88	Codex A/D input [3]	Yellow	27
TP89	Codex A/D input [2]	Yellow	27
TP90	Codex A/D input [0]	Yellow	27
TP91	Agnd CS4271	Black	27
TP92	Reset switch pull-up	Yellow	30
TP93	gpio[20] (data)	Yellow	24
TP94	Ground	Black	24
TP95	Ground	Black	24
TP96	Ground	Black	30

a. Schematics are provided in the kit in PDF format.

Installation 2

This chapter provides information about the SA-1100 evaluation board specifications, and the hardware and software requirements for using the SA-1100 platform. It also describes how to install the SA-1100 platform.

2.1 Specifications

The physical and power specifications for the SA-1100 evaluation board are as follows:

- Dimensions (mounted):
  - Height: 20.3 cm (8 in)
  - Width: 33 cm (13 in)
  - Length: 45.7 cm (18 in)
- Power Requirements:
  - +5 V (4 A maximum current, protected by 7 A fuse)
  - +12 V (0.5 A maximum current, protected by 0.5 A fuse)
  - +3.3 V (4 A maximum current, protected by 7 A fuse)

2.2 Hardware Requirements

The following equipment is required to use the SA-1100 platform:

- A computer running a terminal emulator or ARM** tool debugger (not included in kit)
- A null modem cable (included in kit)
- A power supply (included in kit)

2.3 Software Requirements

To test the SA-1100 platform, an ARM software developer's toolkit (SDT) (containing source code and tool debugger) or a third-party tool ported to the StrongARM** CPU is required. The ARM tool debugger (part number QR-21BB1-11) can be ordered directly from Intel.

2.4 Installation Procedure

The installation procedure assumes that the ARM SDT kit is being used on your PC. Install the SA-1100 platform as follows:

Warning: **High voltage is used to drive the LCD display and caution should be used when operating the evaluation platform. The high-voltage inverter is located on the back of the raised LCD mounting platform.**

1. Verify that the SA-1100 microprocessor is installed with pin 1 located at the front left corner of the socket.
2. Put all switches in the default configuration (refer to Table 2-1).
3. Set all trim pots to their middle positions.

Note: The version of Demon* used on the SA-1100 platform is part of the ARM code. The full source code of Demon and Angel* are supplied as part of the ARM SDT. The Flash ROM is currently programmed with the ARM Demon remote debugger. Updates will be made available as further development is completed. Intel is currently planning to release an ARM Angel version shortly. The Flash ROM is located in sockets U35 and U 45. The devices are Atmel AT29LV1024.

4. Verify the installation of the Demon ROM: high in U35 and low in U45 (see Figure 1-3 “Connector Locations” on page 1-13).
5. Connect Tektronix Logic Analyzer (model number TEK TLA 711 Logic Analyzer) to J8 through J13.
6. Install the ARM SDT.
7. Connect the null modem cable to comm port 2 of your PC.
8. Connect the other end of the null modem cable to the SA-1100 evaluation board connector J23.
9. Connect the power supply to J18. Connect the power supply ac cable to the wall outlet.
10. Apply power to the SA-1100 evaluation board.

Note: S7 is a 3-position switch. Position the switch to the ON (rightmost) position to apply power to the board.

11. Apply power to the platform by switching S7 to the ON position.
12. LEDs D12, D13, D14, D15, and D5 light. Nothing is displayed on the screen.
13. Slide Reset switch S16 to the DOT position. LED D15 goes out, LED 17 flashes momentarily, and LEDs D3 and D4 light.

This completes the installation procedure. For sample programs that can be run, refer to Section 3.3, “Sample Programs” on page 3-2.

Table 2-1. Default Minislide Switch Settings

Switch	Setting	Selection
S1	DOT	Color LCD installed
S2	NO DOT	LCD backlight turned on
S3	NO DOT	tstclk_byp = 0 (inactive)
S4	NO DOT	ext_tx connected to sw_ext_tx
S5	DOT	Use 32.768-kHz crystal
S6	DOT	Use 32.768-kHz crystal
S7	—	Power switch in left position
S8	NO DOT	ext_px connected to sw_ext_px
S9	DOT	Use 3.6864-MHz crystal
S10	DOT	Use 3.6864-MHz crystal
S11	DOT	nCS2 addresses SRAM
S12	NO DOT	PCMCIA signals driven back to gpio[7:2]
S13	DOT	32-bit wide Flash
S14	DOT	SRAM (for DRAM, default should be NO DOT)
S15	DOT	32-bit wide ROM
S16	NO DOT	Entire board held in reset (to run, slide to DOT)
S17	NO DOT	batt_fault = 0
S18	NO DOT	Vdd_fault = 0
S19	DOT	kbc_xsw floating
S20	DOT	LID_CLOSED# = 1
S21	DOT	gpio[1] = 1
S22	DOT	gpio[0] = 1

System Startup 3

This chapter contains the following system startup information:

- The SA-1100 evaluation board memory map locations
- System design hints and considerations
- Sample programs

3.1 SA-1100 Evaluation Board Memory Map

Table 3-1 lists the SA-1100 evaluation board memory map locations.

Table 3-1. SA-1100 Evaluation Board Memory Map

Memory Space	SA-1100 Address Range	SA-1100 Evaluation Board Addressable Space
Static Memory Bank 0 (ROM)	0000 0000 to 07FF FFFF	0000 0000 to 0010 0000
Static Memory Bank 1 (Flash)	0800 0000 to 0FFF FFFF	0800 0000 to 0810 0000
Static Memory Bank 2 (SRAM)	1000 0000 to 17FF FFFF	1000 0000 to 1008 0000
Static Memory Bank 3 (External Register)	1800 0000 to 1FFF FFFF	1800 0000 to 1FFF FFFF
DRAM Bank 0	C000 0000 to C7FF FFFF	C000 0000 to C040 0000
DRAM Bank 1	C800 0000 to CFFF FFFF	C800 0000 to C840 0000
DRAM Bank 2	D000 0000 to D7FF FFFF	D000 0000 to D040 0000
DRAM Bank 3	D800 0000 to E000 0000	D800 0000 to D840 0000

3.2 System Design Hints and Considerations

The following subsections contain system design hints and considerations for the SA-1100 evaluation board.

3.2.1 Mixing SRAM and DRAM in a Single System

If byte-write capability is not required, SRAM contents can be placed into Flash memory space (that is, into the MSCx registers). Set RT=0 (rather than RT=1 for SRAM) for a Flash, nonburst ROM. This keeps the column address strobe (CAS) from toggling on reads and writes. Bursts of 32-bit writes will work, but 8-bit and 16-bit writes will not work.

3.2.2 PCMCIA nPWAIT Signal Considerations

DRAM refresh cycles can occur during PCMCIA accesses. No other memory access can take place if there is a PCMCIA access in progress. Because of this, the system software should assure that the PCMCIA's nPWAIT signal is not held longer than the time that it takes for the 16-entry FIFO on the LCD controller channel to empty. An interrupt occurs at the FIFO half-empty point, alerting the software that the LCD display could be starved for data if it is not direct memory accessed (DMA'd) within 1.5 µs for the largest active display supported. This is a common occurrence on laptops and other display-dependent devices that incorporate PCMCIA sockets.

3.2.3 Decoupling Capacitors

There is one Vddx at pin 193 and one Vdd pin at 188 that require external decoupling. It is not a requirement in a relatively quiet system, but to be safe, the following is recommended:

- Vdd at pin 188 provides the power to the two onchip PLLs, so a quiet supply here lessens clock jitter.
- Vddx at pin 193 is used in the reference for the onchip voltage regulators. A quiet supply is important on this pin as well.

3.3 Sample Programs

Sample programs and sample pictures displayed on the screen can now be run on the SA-1100 evaluation platform.

Simple examples are provided to help run the code using the ARM toolkit. These examples assume that you are using the latest version of the ARM toolkit. It assumes you are running the files from your A drive. (If desired, you can copy all the files provided on the disk to your C drive.)

Note: The following dialog assumes that your serial port cable is plugged into port 2 on your computer.

1. From the ARM toolkit directory, start the debugger using Angel as your configuration.
2. The console window displays the following response, verifying that the Angel Demon was loaded and located.

   Angel Debug Monitor for Brutus (FIQ), MMU on, Clock Switching on (serial) 1.00 (Advanced Risc Machines unreleased) rebuilt on Oct 24 1997 at 14:07:08

   If you do not get this message, check that the ARM toolkit and system are set up correctly.

Use the following example commands to run the sample code provided. The required C code has been provided for the examples, excluding Example 3-4. Feel free to modify and copy the C code during your development using the SA-1100 evaluation platform.

Example 3-1.

1. Under the File menu, click Load and enter the file name.
   a:kb
2. After the file loads, highlight and press **go**.

Note: You may encounter a break point during execution. If this occurs, simply press **go** again and the program will start.

3. You can now type on the SA-1100 keyboard and observe the command response on the PC screen.
4. To quit, under the Execute tab, press Stop.

Example 3-2.

1. Under the File menu, click Load and enter the file name.
   a:kbin
2. After the file loads, highlight and press **go**.
3. You can now type on the SA-1100 keyboard and observe the appropriate response on the SA-1100 LCD.
4. To quit, under the Execute tab, press Stop.

Example 3-3 sets up the LCD screen as a terminal screen. Example 3-4 describes what can be displayed on your LCD screen. Intel does not provide the software to create the files in Example 3-4.

Example 3-3.

1. Under the File menu, click Load and enter the file name.
   a:cterm
2. After the file loads, highlight and press **go**.
3. All characters will be displayed on your screen and the file will terminate automatically.

Example 3-4.

1. Under the File tab, click on the following:
   get
   a:toura
   and put into address 0x20000
2. This display creates and displays the image in the file.
3. Repeat this example with the other files (such as **tour2**) that are provided.

Example 3-5 regenerates a creative line drawing effect on the screen. The source code is provided for this example.

Example 3-5.

1. Under the File menu, click Load and enter the file name.
   a:bounce
2. After the file loads, highlight and press **go**.
3. The screen regenerates a line drawing effect repeatedly.
4. To quit, under the Execute tab, press Stop.

Support, Products, and Documentation

If you need technical support, a *Product Catalog*, or help deciding which documentation best meets your needs, visit the Intel World Wide Web Internet site:

`http://www.intel.com`

Copies of documents that have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling **1-800-332-2717** or by visiting Intel's website for developers at:

`http://developer.intel.com`

You can also contact the Intel Massachusetts Information Line or the Intel Massachusetts Customer Technology Center. Please use the following information lines for support:

For Documentation and General Information	
Intel Massachusetts Information Line	
United States:	1–800–332–2717
Outside United States:	1–303-675-2148
Electronic mail address:	techdoc@intel.com

For Technical Support	
Intel Massachusetts Customer Technology Center	
Phone (U.S. and international):	1–978–568–7474
Fax:	1–978–568–6698
Electronic mail address:	techsup@intel.com

ARM POWERED™
StrongARM