StrongARM** SA-1101 Microprocessor Companion Chip

Brief Datasheet

Product Features

The SA-1101 Microprocessor Companion Chip (SA-1101) allows developers to utilize a cost-effective and power-efficient solution for portable applications. The SA-1101, when coupled with the SA-1100 Microprocessor (SA-1100), provides additional standard interface functions needed for general-purpose handheld computing. The SA-1101 adds video display capabilities to the SA-1100's existing LCD controller function. The unique SA-1101 design, which can share memory with the SA-1100 or operate with a separate DRAM frame buffer, affords designers the ability to use the configuration that best suits market needs and demands.

- PLL clock generator
  - —32- to 72-MHz video pixel clock
  - —144-MHz memory controller clock
- CRT controller
  - —Blanked/active display timing
- Three 8-bit RAMDACs with lookup table (LUT)
  - —@72 MHz pixel rate
- SA-1100 memory interface
  - —Unified Display Memory Mode
  - —Dedicated Display Memory Mode
- SA-1100 interface
- PCMCIA interface
  - — Two 16-bit interfaces supporting 8- and 16-bit peripherals
- General-purpose I/O (GPIO) interface
  - —15 general-purpose open-drain pins
- USB host controller
  - —Open HCI-compatible
  - —Windows95* USBD-compatible
  - —USB-Rev 1.0 compatible
- Keypad/mouse interface
  - —Multipin bus for keypad interface
  - —Identical PS/2 serial ports for track pointer and mouse interface
- IEEE 1284 parallel port interface
  - —Supports IEEE 1284 specification
- Pulse Width Modulated (PWM) interface
  - —Two PWM outputs suitable for creating analog voltages
- 256 mini-ball grid array (mBGA)

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Benefits

- Two modes of storing video frame buffer data allows flexibility of design configuration.
- Selective clock-gating allows lower power dissipation.
- Dedicated memory controller reduces bandwidth demands to maximize system performance.
- Complete suite of software and hardware tools speeds time to market.
- Compatibility with ARM** and the availability of key third-party development tools (real-time operating systems) reduces design effort and cost.

Applications

- Handheld personal computers (HPCs)
- Smart phones
- Digital cameras
- Subnotebooks
- Wallet personal computers
- Portable network computers

Operating Systems for the SA-1100

- Microsoft
  - — Windows CE*
- Wind River
  - — VxWorks*
- Lucent
  - — Inferno*
- Sun Microsystems
  - — JavaOS*
- Microware
  - — OS-9*
- Chorus
  - — Jazz*
- Psion
  - — EPOC32*
- Integrated Systems, Inc.
  - — pSOS*
- JMI
  - — C EXECUTIVE*

Description

The SA-1101 is an integrated circuit incorporating a video subsystem, an USB Master, a PS/2 (mouse and trackpad), a 15 general-purpose I/O (GPIO), an IEEE 1284, and a PCMCIA. The video subsystem includes a phase-locked loop (PLL) clock generator, a CRT controller, a triple 8-bit RAMDAC with lookup tables, a SA-1100 interface, and a memory interface that supports two modes of storing display data. The video subsystem requests display data from the CRT frame buffer, synchronizes it to the pixel clock, and generates analog RGB signals based on pixel values to send to the display monitor. The system generates VESA-standard video timing.

SA-1100 Architecture

The SA-1101 consists of the following analog standard cell functions, predesigned functions, and functions of a new design unique to the SA-1101.

PLL Clock Generator

The SA-1101 input clock is a single 3.6864-MHz clock generated by the SA-1100 and sent from the GP[27] to the CLK pin on the SA-1101. This clock is blocked during sleep mode, which minimizes SA-1101 power dissipation. A standard on-chip PLL multiplies the clock by programmable values

to generate the higher frequencies required by the SA-1101 CRT controller for video output and for its DRAM controller.

Each of the functional blocks make use of selective clock-gating and can be individually powered up or powered down under software control from the SA-1100. This allows the SA-1101 to dissipate lower power while not using these functions and only power them up as needed. It also allows functions to be quickly restarted when required.

The PWMs (acting as DACs) are clocked ungated from the 3.6864-MHz output from the SA-1100. This allows their use for brightness and contrast/control of the LCD even when all other functions are turned off.

CRT Controller

The CRT controller is a programmable subsystem that generates sync and blanking (blanked/active display timing) for a variety of VESA-standard display resolutions. In future generations, it may generate interlaced timing for use with an external NTSC encoder.

The CRT controller consists of a set of programmable counters. Horizontal counters generate the horizontal active/blanked timing and H Sync for each scan line; vertical counters count lines and generate the vertical active/blanked timing and V Sync.

Three LUT RAMDACs

The output of each LUT RAM passes into an 8-bit DAC. In normal 256-color operation, the 8-bit value representing each pixel addresses all three RAMs in parallel.

Each RAM's 8-bit output connects to a video DAC that converts the value to an analog voltage representing red, blue, or green video. The DAC output is a current source capable of driving a 37.5 ohm double-terminated load. The DACs can be turned off to reduce power consumption when the video display function is not being used.

SA-1100 Memory Interface

The SA-1101 interfaces to the SA-1100 functions in two distinct ways, depending on the video mode.

In unified display memory mode, video display data and LCD display data are both stored in dedicated areas of the SA-1100 main memory. Because the memory is shared, the SA-1101 needs to periodically access the SA-1100 memory to feed CRT display data to its video controller. During this transaction, the SA-1101 has control of the system bus. Other processor functions remain under SA-1100 control, synchronized by SA-1100 clocks, and continue operating independently. Unified display memory mode meets the needs of medium resolution video displays (640 x 480).

In dedicated display memory mode, suitable for 800 x 600 or 1024 x 768 video displays, the SA-1101 has its own DRAM attached to a separate memory interface. Display data for the video (CRT) display is kept in this memory and the high bandwidth accesses required to refresh the video display are therefore restricted to this memory interface and do not interrupt SA-1100 memory operations.

In dedicated display memory mode, the SA-1100 writes into an area of its own memory dedicated to CRT display. The SA-1101 is programmed to “snoop” all writes to that range of addresses and exactly duplicates the contents of that area of SA-1100 memory in its own CRT display memory.

SA-1100 Interface

The main interface between the SA-1100 and the SA-1101 are the memory data and address buses and the point-to-point control signals. Of these control signals, ten control the PCMCIA bus, two are for the memory handoff (MBREQ and MBGNT), and four are miscellaneous pins for clock, battery, fault, interrupt and reset functions (CLK, Batflt, INT, and nRESET).

PCMCIA Interface

The PCMCIA support logic interfaces to two PCMCIA cards. It provides glue logic between the SA-1100’s PCMCIA interface and actual card sockets. This interface allows the building of two card sockets with the SA-1100 requiring only the addition of external address and data buffers.

General-Purpose I/O (GPIO) Interface

The GPIO interface is an APB peripheral that provides 15 bits of programmable I/O divided into two ports: an 8-bit port A and a 7-bit port B. Each pin is configurable as either input or output. At system reset, both ports default to input.

USB Host Controller

The USB host controller is Open HCI-compatible, Windows95* USBD-compatible, and USB-Rev 1.0 compatible. It supports both low- (1.5 Mbps) and high-speed (12 Mbps) USB devices. It is an USB Master interface and it can request DMA transfers between the SA-1101 and the SA-1100 main memory.

Keypad Interface

This block connects directly to a matrix keypad and provides the SA-1100 with needed information to decode these key press signals. The keypad interface consists of two bidirectional ports: an 8-bit port X and a 16-bit port Y. Each of the pins on these ports has an open drain output and can be driven low, or left undriven by using the data write registers. The input or status of each pin can be read at any time using the data read registers or can signal an interrupt.

PS/2 Trackpad and Mouse Interface

The PS/2 trackpad and mouse interfaces are identical, differing only in the names of the external pins. The interfaces are designed to communicate with a standard PS/2 trackpad, keyboard, or mouse, via a two-pin serial link.

IEEE 1284 Parallel Port Interface

The IEEE 1284 interface implements the IEEE 1284 specification providing a signalling method for bidirectional parallel communications with printers and other peripheral devices. The IEEE 1284 specification defines five modes of operation: compatibility mode, nibble mode, byte mode,

extended capabilities port (ECP) mode, and enhanced parallel port (EPP) mode.

Both forward (host-to-peripheral) and reverse (peripheral-to-host) data flows are supported through single register or FIFO access from the AMBA bus.

Pulse Width Modulated (PWM) Interface

Two 8-bit PWMs provide brightness and contrast control suitable for an LCD display. The PWM counter is clocked at CLK frequency, which gives a carrier frequency of 14.4 kHz at the recommended frequency of 3.6864 MHz for CLK.

System Overview

The SA-1100 and SA-1101 chipset provide additional standard interface functions needed for a general-purpose handheld computing device. Figure 1 shows how the SA-1100 and the SA-1101 can be used in a handheld computing device when controlling DRAM for display on both an LCD (from the SA-1100) and a video CRT (from the SA-1101). The two display devices can have separate DRAM frame buffers as shown in Figure 1, or they can share common DRAM storage using the SA-1100 main memory. With separate memories, the LCD frame buffer is controlled by the SA-1100 and the CRT frame buffer is controlled by the SA-1101.

Figure 1. System Block Diagram

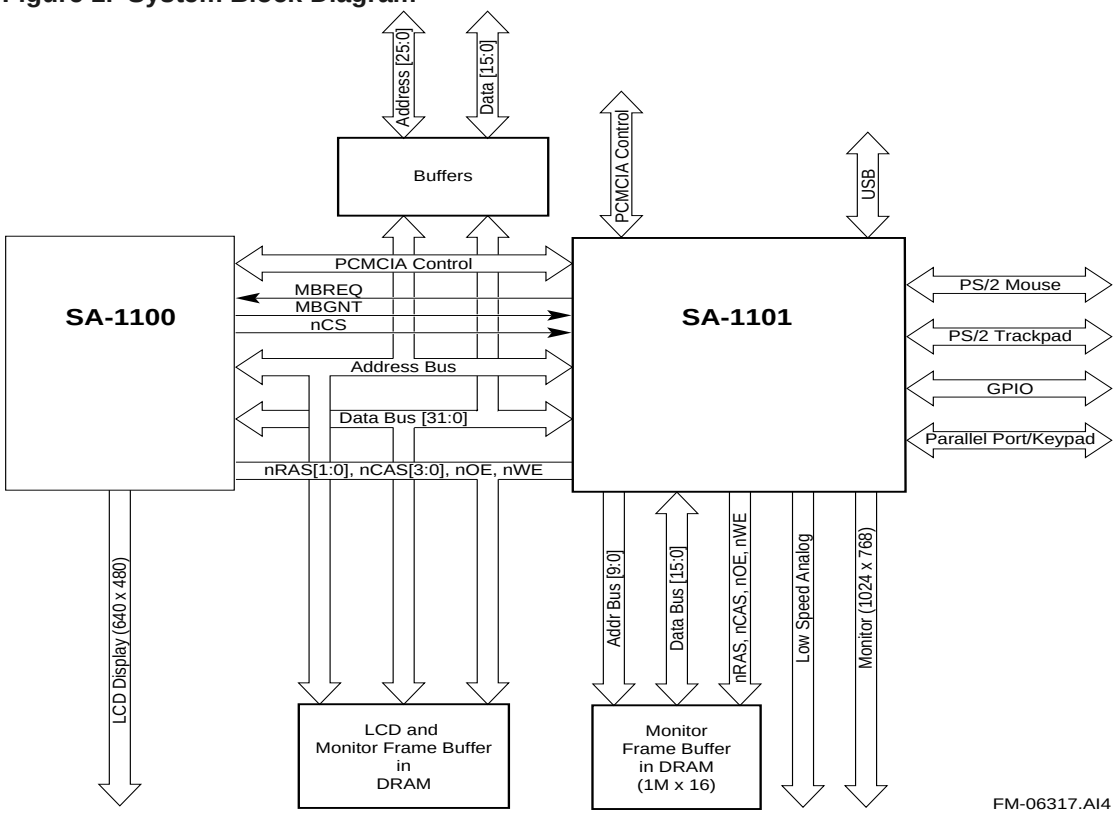
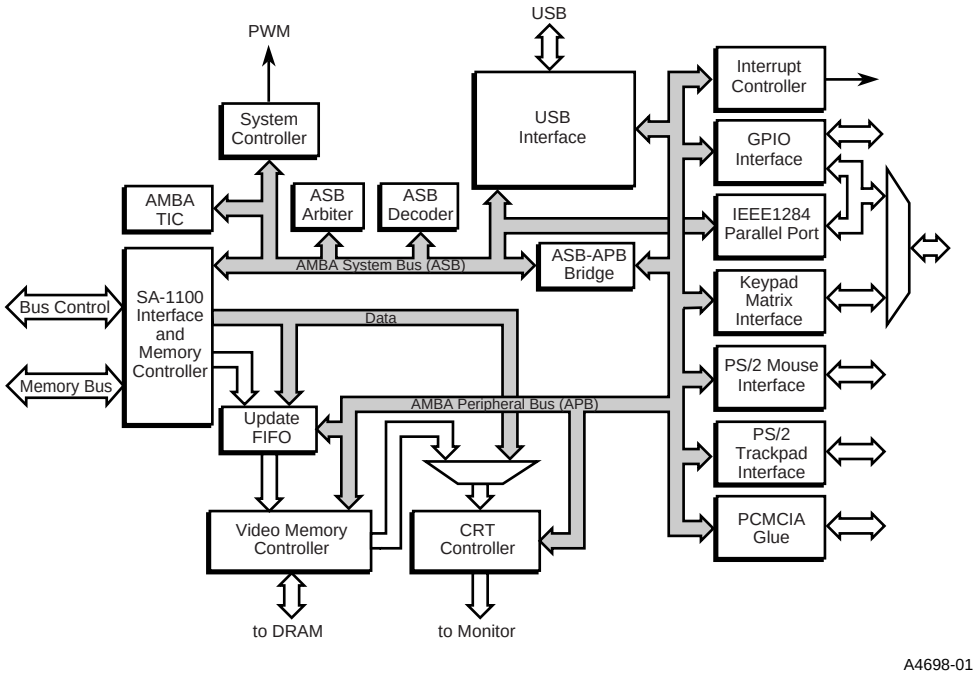


Figure 2. SA-1101 Block Diagram



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