83C196LD

Specification Update

November, 1998

Notice: The 83C196LD may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 273181-003

Contents

Revision History

Date	Version	Description
11/3/98	003	Changed Errata 2 Status to “NoFix”, was “Fixed”.
08/12/98	002	Added Errata 2 and Document Changes 1 and 2.
05/21/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet	272805
8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual	272973

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	Errata
	A-1	B-0	#			
1	X			7	Fixed	EPA Missed Interrupts
2	X	X		7	NoFix	RSTSRC Register Functionality

Specification Changes

No.	Steppings		Page	Status	Specification Changes
	A-1	B-0			
1		X	8	DOC	Pull-Up Resistor on EA# Pin
2		X	8	DOC	Additional Test ROM Execution Mode Entry Scheme
3		X	8	DOC	Strong Pull-up Resistor Removed from V_{PP} Pin
4		X	8	DOC	PPW Value in Test ROM Changed
5		X	8	DOC	Additional SIO Programming Mode Entry Scheme
6		X	9	DOC	EA# Pin V_{IL} Max Specification Change

Specification Clarifications

No.	Steppings			Page	Status	Specification Clarifications
	A-1	B-0	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	Documentation Changes
1	272973-001	11	Doc	Page 6-1, Figure 6-1
2	272973-001	11	Doc	Page 6-2, Figure 6-3

Identification Information

Markings

Bottom mark: AN83C196LD

Errata

1. EPA Missed Interrupts

Issue: When a read-modify-write instruction is used to change the contents of the EPA interrupt pending register (i.e., andb epa pend1, #0fbh), an EPA interrupt may not get serviced if it occurs at the same time that the interrupt pending register is being read from.

Implication: EPA interrupts in the application may not get serviced.

Workaround: Use normal "**ldb**" or "**stb**" instructions instead of read-modify-write instructions to modify the EPA interrupt pending registers.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

2. RSTSRC Register Functionality

Issue: The RSTSRC register was designed to be initialized to 00h on a V_{CC} power-up condition. However, due to a product erratum, the RSTSRC register may not be initialized to 00h on a V_{CC} power-up condition. As a result, the state of the RSTSRC register on a V_{CC} power-up condition is indeterminate.

Implication: Applications that rely on the RSTSRC register to be 00h on V_{CC} power-up may be adversely affected.

Status: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

Specification Changes

1. Pull-Up Resistor on EA# Pin

Issue: A weak pull-up resistor was added to the EA# pin to ensure that the device stays in internal memory execution mode when the pin is not driven.

Implication: The EA# pin can be left floating in the application and still stays in internal execution mode. The EA# pin can be driven to zero volts if external memory mode is desired.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805, *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual* - 272973

2. Additional Test ROM Execution Mode Entry Scheme

Issue: An additional method for entering Test ROM Execution mode was added for easier Test ROM entry. If P0.4 and P0.5 are driven high out of reset, the device jumps into Test ROM Execution Mode.

Implication: Fewer pins are needed to enter Test ROM Execution mode. P0.4 and P0.5 cannot both be driven high out of reset if Test ROM entry is not desired.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805, *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual* - 272973

3. Strong Pull-up Resistor Removed from V_{PP} Pin

Issue: The strong pull-up resistor was removed from the V_{pp} pin. This pin floats if it is not driven.

Implication: None.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805, *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual* - 272973

4. PPW Value in Test ROM Changed

Issue: The PPW register value in the Test ROM was changed from 8000h to 8001h.

Implication: Baud rate for serial transmissions and receptions in SIO programming mode has changed from 1.25 MHz at 20 MHz to 625 KHz at 20 MHz.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805, *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual* - 272973

5. Additional SIO Programming Mode Entry Scheme

Issue: An additional method for entering the SIO Programming routine through the Test ROM Execution mode was added for easier entry. If P2.6 is driven high out of reset after the device is put into Test ROM Execution mode, the device automatically selects the SIO Programming mode.

Implication: Fewer pins are needed to enter SIO Programming Mode. P2.6 cannot be driven high out of reset while entering Test ROM Execution mode if SIO Programming mode is not desired.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805, *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA Microcontroller Family User's Manual* - 272973

6. EA# Pin V_{IL} Max Specification Change

Issue: V_{IL} max specification on the EA# pin was changed from 0.3 V_{CC} to 0.2 V_{CC}. This only affects the EA# pin.

Implication: Intel does not guaranty that the device recognizes a “0” value on the EA# pin for input voltages greater than 0.2 V_{CC}.

Affected Docs: *83C196LD CHMOS 16-Bit Microcontroller Automotive Datasheet* - 272805

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. Page 6-1, Figure 6-1

Issue: SSIO0-CLK register address is incorrect. The SSIO0-CLK address should be 1FB5h.

- Old
  Address: 1F95h
- New
  Address: 1FB5h

Affected Docs: *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)

2. Page 6-2, Figure 6-3

Issue: SSIO1-CLK register address is incorrect. The SSIO1-CLK address should be 1FB7h.

- Old
  Address: 1F97h
- New
  Address: 1FB7h

Affected Docs: *8XC196Lx Supplement to 8XC196Kx, 8XC196Jx, 87C196CA User's Manual* (order number 272973)