8XC196KD AUTOMOTIVE APPLICATION SPECIFICATION UPDATE

Release Date: May, 1998
Order Number: 272839-003

Notice: The 8XC196KD may contain design defects or errors known as errata. Characterized errata that may cause the name of product's behavior to deviate from published specifications are documented in this specification update.

CONTENTS

REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
05/13/97	002	Specification clarification 007 and documentation change 054.
05/19/98	003	Added steppings “A-1 and C-0” to Errata and Specification Clarification tables. Changed “P629.9 to P629.5” for “A-1” stepping and added “C-0” stepping to Identification Information.

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
*87C196KD 16-bit High-performance CHMOS Microcontroller Automotive d*atasheet	272168
8XC196KC/8XC196KD User's Manual (1992)	272238

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC196KD product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Rev. Date	Steppings			Page	Status	ERRATA
	A-1	C-0	#			
9600001	X			9	Fixed	Missing External Interrupt Requests (EXTINT EXTINT1 NMI)
9600002	X	X		9	NoFix	SIO Mode 0 Maximum Baud Rate

Specification Changes

Rev. #	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

Rev. #	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A-1	C-0	#			
001	X	X		10		Memory Map
002	X	X		10		CDE Pin Removed
003	X	X		10		EPROM Programming
004	X	X		11		ONCE Mode Entry
005	X	X		11		Port 5 Operation During Bus HOLD
006	X	X		11		Reset Pulse Width
007	X	X		11		Specification changes in Table 14-12.

Documentation Changes (Sheet 1 of 2)

New #	Prev #	Document Revision	Page	Status	DOCUMENTATION CHANGES
001		001	12	DOC	Page 4-1
002		001	12	DOC	Page 4-2
003		001	12	DOC	Page 4-4
004		001	12	DOC	Page 4-9
005		001	12	DOC	Page 5-4
006		001	13	DOC	Page 5-6
007		001	13	DOC	Page 5-7
008		001	13	DOC	Page 5-7
009		001	13	DOC	Page 5-8
010		001	14	DOC	Page 5-9
011		001	14	DOC	Page 5-16
012		001	14	DOC	Page 5-16
013		001	14	DOC	Page 5-18
014		001	14	DOC	Page 5-19
015		001	15	DOC	Page 5-25
016		001	15	DOC	Page 5-26
017		001	15	DOC	Page 6-10
018		001	15	DOC	Page 7-1
019		001	15	DOC	Page 7-8
020		001	16	DOC	Page 7-9
021		001	16	DOC	Page 8-11
022		001	16	DOC	Page 9-2
023		001	16	DOC	Page 10-2
024		001	17	DOC	Page 11-1
025		001	17	DOC	Page 11-2
026		001	17	DOC	Page 11-3
027		001	18	DOC	Page 11-6
028		001	19	DOC	Page 11-8
029		001	20	DOC	Page 12-2
030		001	20	DOC	Page 12-7

Documentation Changes (Sheet 2 of 2)

031		001	20	DOC	Page 13-2
032		001	20	DOC	Page 13-9
033		001	20	DOC	Page 14-9
034		001	20	DOC	Page 14-11
035		001	20	DOC	Page 14-12
036		001	20	DOC	Page 14-15
037		001	21	DOC	Page 14-19
038		001	21	DOC	Page 14-29
039		001	21	DOC	Page A-23
040		001	21	DOC	Page A-28
041		001	21	DOC	Page A-35
042		001	21	DOC	Page A-36
043		001	21	DOC	Page A-37
044		001	21	DOC	Page A-38
045		001	22	DOC	Page A-39
046		001	22	DOC	Page A-45
047		001	22	DOC	Page B-6
048		001	22	DOC	Page C-14
049		001	22	DOC	Page C-45
050		001	22	DOC	Page C-55
051		001	23	DOC	Page C-56
052		001	23	DOC	Page C-57
053		001	23	DOC	Page C-65
054		002	23		Subtitle change on page 8-23.

IDENTIFICATION INFORMATION

Markings

Product	Stepping	Marking (FPO Number Suffix)
87C196KD - P629.5, F6	A-1	B
87C196KD - P629.8S, F6	C-0	F

ERRATA

9600001. Missing External Interrupt Requests (EXTINT EXTINT1 NMI)

PROBLEM: It is possible for the device to fail to recognize an interrupt on EXTINT, for both P2.2 and P0.7, and NMI. The problem is most likely to occur on P0.7 while the device is operating at low voltage (<4.7V), high frequency (16 MHz) and high temperature (>85(C). There is a window of about 2 ns near the falling edge of CLKOUT during which these interrupts may be missed.

IMPLICATION: Systems using NMI or EXTINT on P2.2 or P0.7 may experience missed interrupts.

WORKAROUND: Latch these signals on the rising edge of CLKOUT using external hardware.

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. SIO Mode 0 Maximum Baud Rate

PROBLEM: In synchronous mode 0, the minimum baud value is 0001H for transmissions and 0002H for receptions.

In asynchronous modes 1, 2, and 3, the minimum baud value is 0000H when using the internal clock signal and 0001H when using an external clock signal on T2CLK. At 16 MHz, maximum baud rate is 2.76 Mbaud for mode 0 and 1.0 Mbaud for modes 1, 2, 3.

Bits 14:0 of the BAUD_RATE register specify the baud value. (Bit 15 selects either the internal clock signal or an external clock signal on T2CLK.) Using a value less than the minimums listed above results in incorrect data. For mode 0 receptions, whatever data is present on the RXD pin when TXD begins clocking is treated as the least-significant bit, each remaining bit is shifted left by one bit, and the most-significant bit from the transmitter is never shifted in.

IMPLICATION: Any customer who uses synchronous mode 0 will be affected. Use a baud value that is equal to or greater than the minimum value listed above. This will result in slower baud rates, but should result in correct data.

WORKAROUND: None. Use a baud value that is equal to or greater than the minimum value:

- for synchronous mode 0, 0002H for receptions or 0001H for transmissions

- for asynchronous modes 1, 2, and 3, 0001H when using an external clock source or 0000H when using the internal clock signal

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. Memory Map

PROBLEM: The 87C196KD has 512 bytes of RAM/SFRs and 32 Kbytes of EPROM/OTPROM (the 87C196KB has only 256 bytes of RAM/SFRs and 8 Kbytes of EPROM/OTPROM). The 87C96KD's extra 256 bytes of RAM reside in locations 100H-1FFH and the extra 24 Kbytes of EPROM reside in locations 4000H-9FFFH. These are external memory locations on the 87C196KB.

002. CDE Pin Removed

PROBLEM: The CDE pin on the 87C196KB was replaced by a V_{SS} pin on the 8XC196KD to support 16MHz operation.

003. EPROM Programming

PROBLEM: The 87C196KD has a different programming algorithm from that of the 87C196KB, to support 32 Kbytes of EPROM/OTPROM. When performing run-time programming, use the following section of code:

```
PROGRAM:
      LD  ADDR_TEMP,2[SP];get address passed from calling routine
      LD  DATA_TEMP,4[SP];get data passed from calling routine
      PUSHA;clear PSW, WSR, INT_MASK, INT_MASK1
      LD  COUNT,#5;set up for 5 programming cycles
LOOP:
      LDB INT_MASK, #ENABLE_SWT;enable HSO interrupt
      LDB HSO_COMMAND,#SWT0_OVF;enable HSO software timer 0
```

```
      ADD HSO_TIME,TIMER1,#PGM_PULSE;load HSO_TIME with TIMER1+PGM_PULSE
      EI      ;enable unmasked interrupt
      ST DATA_TEMP,[ADDR_TEMP];store passed data at passed address
      IDLPD #1;enter idle mode until SWT0 expires
      DJNZ COUNT, LOOP;loop 5 times
      POPA;restore PSW, WSR, INT_MASK, INT_MASK1
SWT0_EXPIRED:
      RET     ;service software timer 0 and return
```

004. ONCE Mode Entry

PROBLEM: The ONCE mode is entered on the 87C196KD by driving the TXD pin low on the rising edge of RESET#. The TXD pin is held high by a pullup that is specified at 1.4mA and remains at 2.0V. This pullup must not be overridden or the 87C196KD will enter the ONCE mode.

005. Port 5 Operation During Bus HOLD

PROBLEM: During the bus hold state, the 87C196KD weakly holds RD#, WR#, ALE, BHE#, and INST in their inactive states. The 87C196KB holds only ALE in its inactive state.

006. Reset Pulse Width

PROBLEM: A reset pulse (e.g., from a watchdog timer overflow) from the 87C196KD is 16 states, rather than 4 states as on the 87C196KB. This provides a longer reset pulse for other devices in the system.

007. Specification changes in Table 14-12.

PROBLEM: Table 14-12, ROM-Dump Mode Memory Map should read

Device	Internal OTPROM Address	External Memory Address
8XC196KD*	2000H-9FFFH	4000H-BFFFH
8XC196KC*	2000H-5FFFH	4000H-7FFFH
8XC196KD Security Key*	2000H-202FH	4020H-402FH
8XC196KC Security Key*	2000H-202FH	4020H-402FH

* Must use bank Switching; P1.0-P1.2 replaces A13-A15.

DOCUMENTATION CHANGES

001. Page 4-1

ITEM: Remove asterisked statement '*Always write Ports 3 and 4 as a single word." These ports can be written as bytes or as a word.

002. Page 4-2

ITEM: Note 2 and the first sentence in Section 4.2.

003. Page 4-4

ITEM: Figure 4-2 omits the top address of the special purpose memory in the blow-up of this memory section. The top reserved memory section starting at 205Eh, ends at **207Fh**.

004. Page 4-9

ITEM: Add the following sentence after the paragraph, **'NOTE:** If the WSR is set to a reserved Hwindow value, it may cause unpredictable results. The only way to reset the WSR is to reset the device or use POPA to restore a proper value.'

005. Page 5-4

ITEM: There are a couple of errors in the code example shown for modifying interrupt priorities. The DI instruction is unnecessary, and the example omits three lines of code. The corrected code is as follows:

```
SERIAL_RI_ISR:

      PUSHA           ;Save PSW, INT_MASK, INT_MASK1, & ;WSR
                      ;(This disables all interrupts.)
      LDB INT_MASK1, #01000000b;Enable EXTINT only
      EI              ;Enable servicing of interrupts
                      ;
                      ; Service the RI interrupt
                      ;
      POPA            ; Restore PSW, INT_MASK, INT_MASK1,
                      ;& WSR
      RET

CSEG AT 2038H    ; Fill in interrupt vector table

      DCW SERIAL_RI_ISR
      END
```

006. Page 5-6

ITEM: In the explanation of the handling of interrupt service routines, there are several mistakes in steps #2 and #6. The following text shows the corrected points in these steps.

> 2) The PUSHA instruction, which is **now** guaranteed to execute, saves the contents of the PSW, **INT_MASK**, INT_MASK1, and the Window Select Register (WSR) onto the stack and then clears the PSW, **INT_MASK**, and INT_MASK1. In addition to the arithmetic flags, the PSW contains the global interrupt bit (I), and the PTS enable bit (PSE). By clearing the PSW and the interrupt mask registers, **PUSHA** effectively masks all maskable interrupts,... (the remaining text is correct).
>
> 6) At the end of the service routine, the POPA instruction restores the original contents of thePSW, **INT_MASK**, INT_MASK1 and WSR registers;... (the remaining text is correct).

007. Page 5-7

ITEM: Table 5-2 has a few mistakes in the Minimum Pulse Width and the Sample During phase. Despite differences in the circuitry of these interrupt sources (HSI.0, NMI, P0.7, P2.2, Timer 2 Capture), all of their pulse widths should be >1 state time. Note that the pulse width must be greater than 1 state time. If the pulse width is exactly 1 state time or less, there is statistical chance that the interrupt could be missed. Also changes to the first paragraph in Section 5.3 need to be made to reflect this.

Change Sampled Phase for NMI and Timer 2 Capture from Phase 2 to Phase 1.

Change Sampled Phase for P0.7 EXTINT from Phase 1 to Phase 2.

008. Page 5-7

ITEM: Table 5-3 omits two other instructions, **EPTS** and **DPTS**, which inhibit interrupts from being acknowledged until after the next instruction is executed.

> DPTS -Disables the PTS
>
> EPTS -Enables the PTS

009. Page 5-8

ITEM: In Section 5.3.2, the calculation of latency incorrectly states the response time for standard interrupts. The third bullet under the sentence ‘To calculate latency, add the following terms’ should read as:

* The response time (**11** state times for an internal stack or **13** for an external stack) for standard interrupts only.

Also, in Section 5.3.2.1, the first sentence incorrectly outlines the maximum delay for a standard interrupt. The paragraph should begin with the following sentence:

The maximum delay for a standard interrupt is **56** state times (4+39+**13**).

010. Page 5-9

ITEM: Figure 5-3 displays the incorrect number of state times it takes to service a call. This figure shows that it takes 16 state times when a call is forced; this actually should be **11** state times. And the 61 state times should be changed to **56**.

011. Page 5-16

ITEM: The third sentence in Section 5.6.2 should read as following: 'The PTS mode defines the functions of the other bits; see Table **5-7** for Single and Block Transfer modes and Table 5-8 **for A/D Scan, HSI and HSO modes.'**

012. Page 5-16

ITEM: In Table 5-6, the selected modes for the respective bit 7-5 combinations are incorrect for the following PTS modes: Single Transfer, HSI, HSO, and Block Transfer. The following is correct for Table 5-6.

0	0	0	Block Transfer
0	0	1	HSO Mode
0	1	1	HSI Modes
1	0	0	Single Transfer

013. Page 5-18

ITEM: In Table 5-9, the PTSCON should equal **95h** instead of 15h.

014. Page 5-19

ITEM: In Table 5-10, the PTSCON should equal **17h** instead of 97h.

015. Page 5-25

ITEM: In Table 5-17, the PTSCON should equal **6Ah** instead of 2Ah.

016. Page 5-26

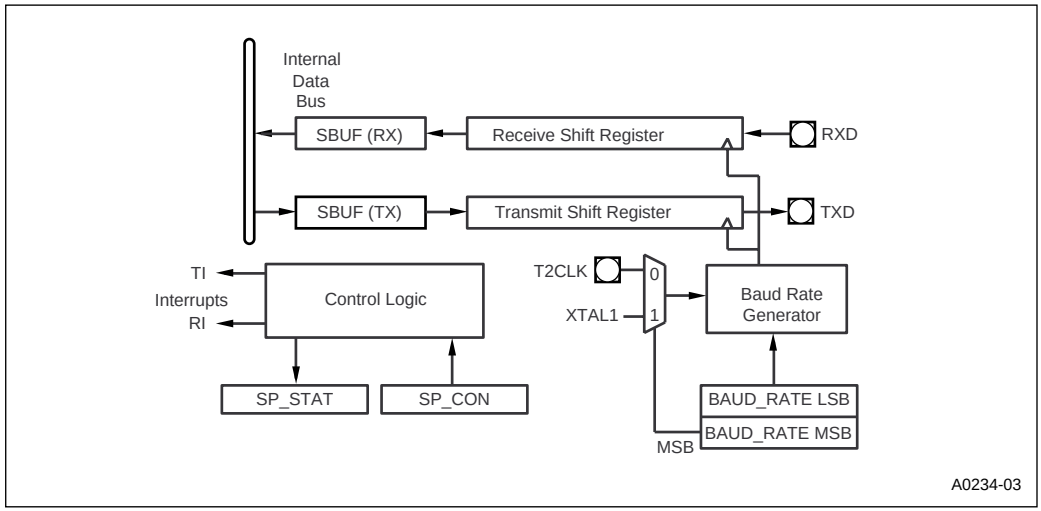
ITEM: In Table 5-19, the PTSCON should equal **2Ah** instead of 6Ah.

017. Page 6-10

ITEM: Remove the second sentence in Section 6.2.3.

018. Page 7-1

ITEM: The following block diagram will be included in future manuals.



Serial Port Block Diagram

019. Page 7-8

ITEM: In the second paragraph of Section 7.3.3, the first sentence refers to the 8096H. This actually should be the **8096BH**.

020. Page 7-9

ITEM: In Table 7-5, the BAUD_RATE value in Mode 0 at 1200 should be **9A0Ah** instead of 8A9Ah, and at 300 should be **E82Ah** instead of E82Bh.

021. Page 8-11

ITEM: The last paragraph of page 8-11 explains the operation of the divide-by-eight counter incorrectly. Replace the last paragraph with the following:

Writing to the HSI_MODE register always resets the HSI module's divide-by-eight counter.

If you write HSI_MODE to configure an HSI, and another HSI was previously configured for "eight positive transitions" mode, the counter reset causes the previously configured HSI to lose up to seven accumulated events. For this reason, we recommend that you use a single write to HSI_MODE to configure all HSI inputs at once.

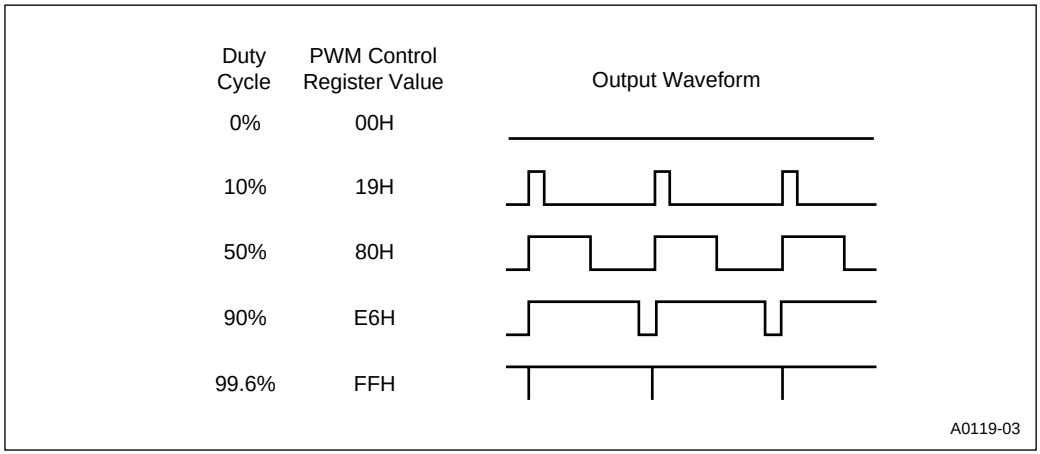
022. Page 9-2

ITEM: The fifth bullet under Section 9.2, should read '80**C**196KB-compatible mode.'

023. Page 10-2

ITEM: On page 10-2, add the following sentences to the second paragraph after the first sentence: 'Since the value written to the control register is buffered, you can write a new 8-bit value to PWMx_CONTROL before the counter overflows. The new value is used during the next period of PWMx.'

The following figure replaces Figure 10-2:



024. Page 11-1

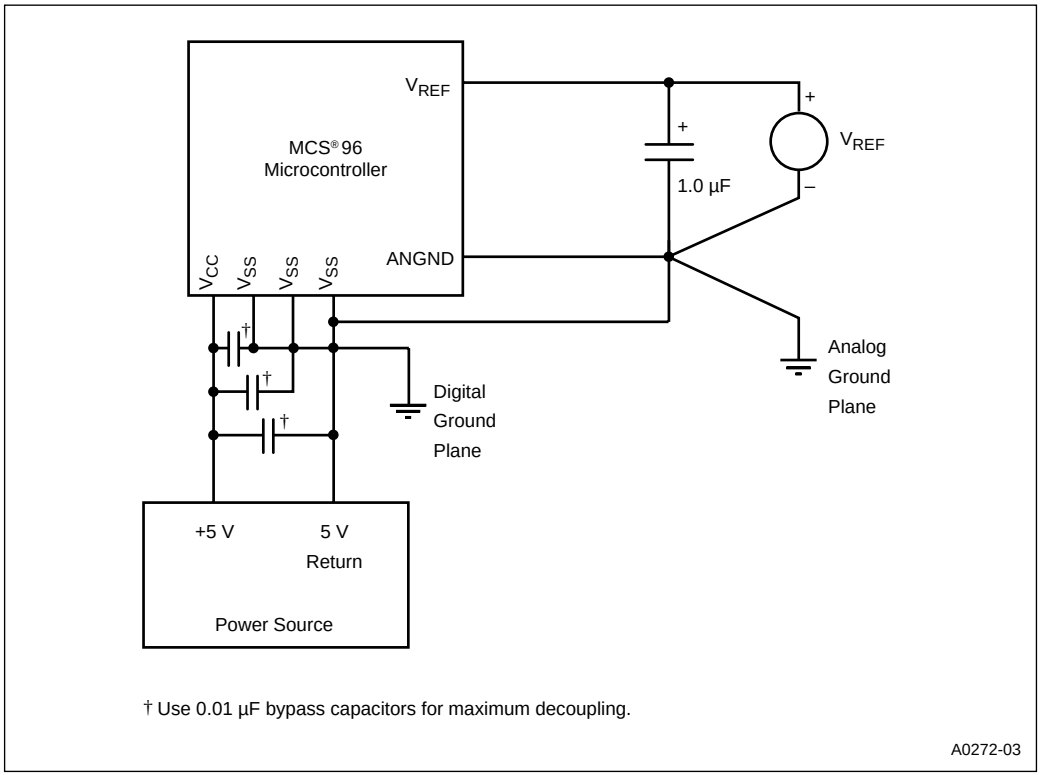
ITEM: The last sentence in Section 11.1 should read: . . . '**Figure 11-1**' not Figure 14-1.

025. Page 11-2

ITEM: In Figure 11-1, the recommended capacitor value between V_{CC} and V_{SS} is **0.01 µF** or greater. Thus, the 0.1 µF shown can be used.

026. Page 11-3

ITEM: In Figure 11-2, the recommended capacitor value between V_{CC} and V_{SS} is **0.01 µF** or greater. Also the recommended capacitor value between V_{REF} and ANGND is **1.0 µF**. The following figure replaces Figure 11-2:



In Section 11.2.1, the reason for these capacitors is explained. However, the second to last line of the first paragraph should read as follows:

'Connect a 0.01-µF bypass capacitor between V_{CC} and each V_{SS} pin and a 1.0-µF capacitor between V_{REF} and ANGND.'

027. Page 11-6

ITEM: In Figure 11-6, the timing diagram incorrectly represents the T_{xlxl} and T_{xhxl} timing specifications. The timing diagram below replaces Figure 11-6.

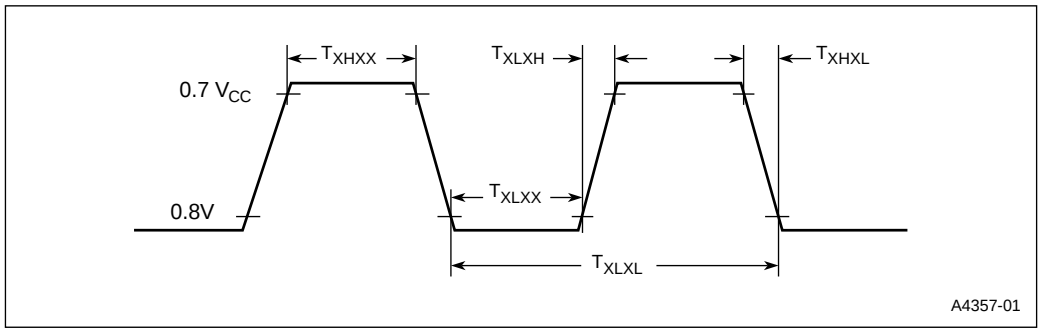


Figure 11-6. External Clock Drive

028. Page 11-8

ITEM: Figure 11-8 shows the reset pin internal circuit. However, there are a couple of mistakes; the following figure shows the corrected version. The **inverter** at the Reset State Machines Trigger input and the **OR gate** at the SET input of the latch are the corrections to this figure.

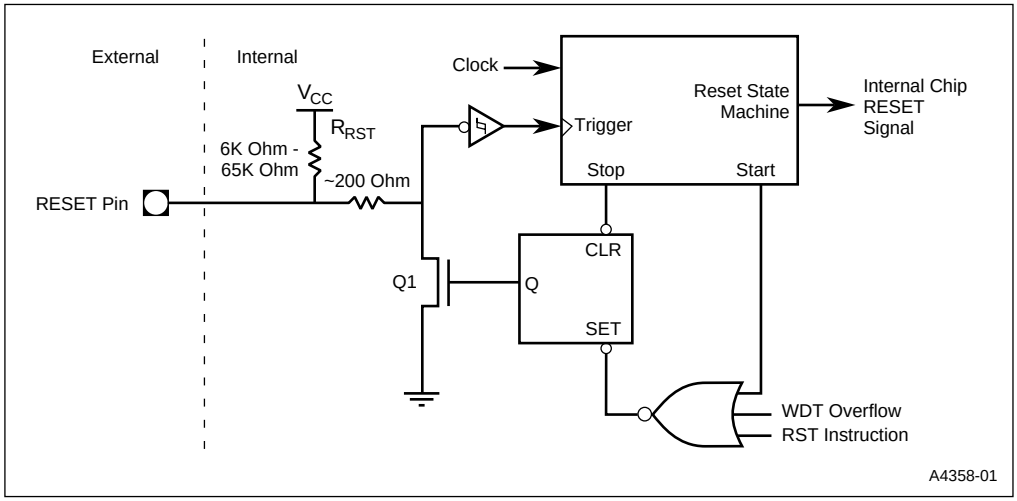


Figure 11-8. Reset Pin Internal Circuit

029. Page 12-2

ITEM: In the second paragraph, the last two sentence refer to the EA# pin, but they should be switched. As I/O ports, **EA# = 1** and as address/data bus, **EA# = 0**.

030. Page 12-7

ITEM: In Section 12.3, remove the first sentence of the second paragraph and replace with: 'See Table B-3 in Appendix B for pin values during ONCE mode.'

031. Page 13-2

ITEM: In Table 13-1, the INST pin description should read as follows: 'Instruction Fetch. The signal is valid only during external memory **bus** cycles.....'

032. Page 13-9

ITEM: In the second paragraph of Section 13.4, the explanation about the Ready line should read, '...the external memory device **deasserts** the READY signal..'

033. Page 14-9

ITEM: The last description in Table 14-4 should read as, 'No programming modes allowed. Reads of internal OTPROM are not allowed if program execution is external.'

034. Page 14-11

ITEM: In Figure 14-5, the EA# and V_{PP} pins should be tied to V_{PP} through a switch, not V_{CC}. And on the PALE# pin, the push button and resistor to ground should be swapped.

Also, the third sentence in the first paragraph should read, 'You can read the USFR from location 1FF6h, but must program these bits by...'.

035. Page 14-12

ITEM: The first paragraph should read, 'Setting **USFR.3**....' and the second paragraph, 'Setting **USFR.2'.....**.

036. Page 14-15

ITEM: The second paragraph should read,'....either 5 (8XC196KD devices) or 25 (8XC196KC devices)'

037. Page 14-19

ITEM: In Figure 14-8, the A0-A7 and A8-A12 address bus should only be pointing toward the 27512.

038. Page 14-29

ITEM: In Figure 14-15, the first block spells ‘Security’ incorrectly.

039. Page A-23

ITEM: The operation for XCH and XCHB should have the arrow pointing both ways. The instruction format for XCH and XCHB should label the top opcode as **direct** and the bottom as **indexed**.

040. Page A-28

ITEM: Opcodes 04 and 14 should be labeled as **direct**. Opcodes 0B and 1B should be labeled as **indexed.**

041. Page A-35

ITEM: The instruction length for ANDB (2 ops) with long-indexed is **5** and for ANDB (3 ops) with long-indexed is **6**.

042. Page A-36

ITEM: The instruction length for LJMP with long-indexed is **3**.

043. Page A-37

ITEM: The instruction length for all conditional jumps (except DJNZ, DJNZW, JBC, and JBS) is **2** instead of 1.

044. Page A-38

ITEM: The opcode value for RST is **FF** not FE.

045. Page A-39

ITEM: The instruction length for all single instructions is 2, with the exception of CMPL which is 3.

046. Page A-45

ITEM: The following changes are required in the “Special” section of Table A-10:

Mnemonic	Direct	Immed.
IDLPD Valid key	—	8 (1)
Invalid key	—	28 (2)
RST	4	—

Notes:

1. The instruction takes 8 state times, but the effects of powerdown and idle may take longer.
2. Includes the time required for reset.

047. Page B-6

ITEM: In the description for P3 and P4, remove the sentence, ‘Ports 3 and 4 can be read and written only as a word, at location 1FFEH.’

048. Page C-14

ITEM: The first formula for Synchronous Mode 0 should be Baudrate **x 2**, not x8.

In the table, the BAUD_RATE value in Mode 0 at 300 should be **E82Ah** instead of E82Bh.

049. Page C-45

ITEM: Remove the last sentence in the paragraph,’Ports 3 and 4 can be read.....’

050. Page C-55

ITEM: The PTSBLOCK is offset 6 from PTS Control Block, not 7.

051. Page C-56

ITEM: The PTS mode bit settings are interchanged. The correct mode settings are as follows:

Mode	Bit 7	Bit 6	Bit 5
Block transfer	0	0	0
Single transfer	1	0	0

052. Page C-57

ITEM: The PTS mode bit settings are interchanged for HSO and HSI modes. The correct mode settings are as follows:

Mode	Bit 7	Bit 6	Bit 5
HSO	0	0	1
HSI	0	1	1
A/D	1	1	0

053. Page C-65

ITEM: In the paragraph, the references to PTSDST should be to PTSSRC. The corrected text is as follows:

The PTSSRC register is used in single transfer, block transfer, and HSO modes. PTSSRC points to the source memory location. PTSSRC is optionally incremented at the end of a PTS cycle. In single transfer mode, PTSCON.1 and PTSCON.3 control whether PTSSRC is incremented. In block transfer mode, PTSCON.1 controls whether PTSSRC is incremented after each transfer, and PTSCON.3 controls whether PTSSRC retains its final value or reverts to its original value. In HSO mode, PTSCON.3 determines whether PTSSRC is updated at the end of the PTS cycle.

054. Subtitle change on page 8-23.

ITEM: On page 8-23, Section 8.3.2.7, the subtitle should read “Using HSO.0-HSO.6 As Output Pins” instead of “Using HSO.0-HSO.5 As Output Pins”.