8XC196KD COMMERCIAL APPLICATION SPECIFICATION UPDATE

Release Date: May, 1997
Order Number: 272833-002

The 8XC196KD may contain design defects or errors known as errata. Characterized errata that may cause the 8XC196KD's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-7641

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REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
05/13/97	002	Documentation change 054 and specification clarification 022.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
8XC196KC/KC20 Commercial CHMOS Microcontroller datasheet	272145
Embedded Microcontrollers	270646
8XC196KC/KD User's Manual (1992)	272238
8XC196KC Quick Reference	272112
80C196KC User's Guide	270704
8XC196KB/KC/KD Programming Support Fact Sheet	272225
Development Tools Handbook	272326
ApBUILDER Interactive Application Programming Package Disk	272216
Project Builder 196 "FREE" Demo Software	272329

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC196KD product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Rev. Date	Prev. #	Steppings							Page	Status	ERRATA
		A0	A1	B	B	B0	B0	C0			
Device		87C196KC	87C196KD	83C196KD	87C196KD	83C196KD	83C196KD	87C196KD			
9600001	116	X	R	X	X	X	X	X	11	NoFix	Indirect Shift Count Value
9600002	147	X	R	X	X	X	X	X	11	NoFix	Write Cycle During Reset
9600003	214	R							13	Fixed	ONCE Mode Entry
9600004		X	X	X					13	Fixed	Missing External Interrupt Requests (EXTINT, EXTINT1, and NMI)
9600005		X	R	X	X	X	X		16	NoFix	BMOVI Windowing Count Register (Functional Description)
9600006		X	R	X	X	X	X	X	16	NoFix	SIO Mode O Max Baud (Functional Description)
9600007		X	X	X	X	X	X	X	17	NoFix	HSI Events (9 or More)
9600008		X	R	X	X	X	X	X	18	NoFix	Writing HSI_MODE Resets the Divide-by-Eight Counter
9600009			R	X	X	X	X		19	Fixed	IPD Hump

Specification Changes

Rev. #	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update

Specification Clarifications (Sheet 1 of 2)

Rev. #	Prev. #	Steppings						Page	Status	SPECIFICATION CLARIFICATION
		A0	A1	B	B	B0	B0			
Device		87C196KC	87C196KD	83C196KD	87C196KD	83C196KD	83C196KD			
										Clarifications 1 - 21 apply to document #272238, 8XC196KC/KD User's Manual
001		X	X	X	X	X	X	19	DOC	Page 5-10
002		X	X	X	X	X	X	20	DOC	Page 8-4
003		X	X	X	X	X	X	20	DOC	Page 8-18
004		X	X	X	X	X	X	21	DOC	Page 9-3
005		X	X	X	X	X	X	21	DOC	Page 10-2
006		X	X	X	X	X	X	22	DOC	Page 11-3
007		X	X	X	X	X	X	23	DOC	Page 12-1
008		X	X	X	X	X	X	23	DOC	Page 13-4
009		X	X	X	X	X	X	23	DOC	Page 13-22
010		X	X	X	X	X	X	24	DOC	Page 14-15
011		X	X	X	X	X	X	24	DOC	Page 14-17
012		X	X	X	X	X	X	25	DOC	Page 14-31
013		X	X	X	X	X	X	25	DOC	Page 14-33
014		X	X	X	X	X	X	25	DOC	Page B-9
015		X	X	X	X	X	X	25	DOC	Page B-9

Specification Clarifications (Sheet 2 of 2)

Rev. #	Prev. #	Steppings						Page	Status	SPECIFICATION CLARIFICATION
		A0	A1	B	B	B0	B0			
Device		87C196KC	87C196KD	83C196KD	87C196KD	83C196KD	83C196KD			
016		X	X	X	X	X	X	26	DOC	Page C-5
017		X	X	X	X	X	X	26	DOC	Page C-16
018		X	X	X	X	X	X	27	DOC	Page C-33
019		X	X	X	X	X	X	27	DOC	Page C-37
020		X	X	X	X	X	X	27	DOC	Page C-45
021		X	X	X	X	X	X	27	DOC	Page C-51
022								27		Specification changes in Table 14-12.

Documentation Changes (Sheet 1 of 3)

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					Changes 1 - 53 apply to document #272238, 8XC196KC/KD User's Manual
001			28	DOC	Page 4-1
002			28	DOC	Page 4-2
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004			28	DOC	Page 4-9
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010			30	DOC	Page 5-9
011			30	DOC	Page 5-16

Documentation Changes (Sheet 2 of 3)

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012			30	DOC	Page 5-16
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Documentation Changes (Sheet 3 of 3)

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043			37	DOC	Page A-37
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045			38	DOC	Page A-39
046			38	DOC	Page A-45
047			38	DOC	Page B-6
048			38	DOC	Page C-14
049			38	DOC	Page C-45
050			38	DOC	Page C-55
051			39	DOC	Page C-56
052			39	DOC	Page C-57
053			39	DOC	Page C-65
054			39		Subtitle change on page 8-23.

IDENTIFICATION INFORMATION

Markings

Product	Stepping	Marking (FPO Number Suffix)
87C196KD - P629.5	A-0	A or none
87C196KD - P629.5	A-1	B
83C196KD - P629.9	B	D
87C196KD - P629.5	B	E
83C196KD - P648.6	KD-B0	F
83C196KD - Alternate	B-0	G
87C196KD - P629.8s	C-0	H

ERRATA

9600001. Indirect Shift Count Value

PROBLEM: The SHRL and SHLL instructions function correctly with count values 0-31, inclusive. However, a shift count value of XX100000b causes 32 shifts, which results in no shift taking place. With all other count values, the upper 3 bits are masked off and the remaining bits specify the number of shifts. Also, a shift count value of XX1XXXXXB causes the overflow flag and the overflow-trap flag to be set.

IMPLICATION: Customers using SHRL and SHLL instructions with a count value greater than 31 will be affected.

WORKAROUND: Ensure that the count value never exceeds 31.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

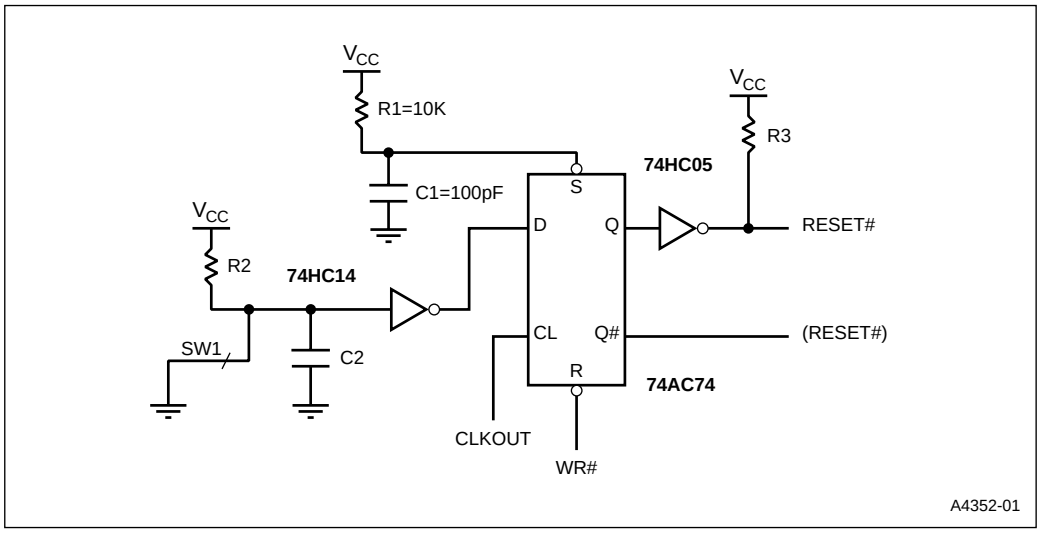
9600002. Write Cycle During Reset

PROBLEM: The data bus floats asynchronously with RESET#. If reset occurs during an external write cycle, the contents of the external device may be corrupted. This is the normal operating condition for reset, and is not considered a bug. It is included on this list for those customers that may encounter corruption of data in external RAM during reset.

IMPLICATION: Anyone who resets a system while writing to external RAM will be affected. May have to add external circuitry if this is a problem.

WORKAROUND: Allow reset to occur only at the rising edge of CLKOUT and only if WR# is high. If a reset occurs during an external bus write cycle, RAM data on the external bus may be corrupted. This describes a logic design that will alleviate the problem.

The following circuit will allow a manual Reset to occur at the rising edge of CLKOUT only if WR# is high (inactive). If WR# is low (active) then RESET# will stay 'high' (inactive). The 74HC14 and 74HC05 are usually already in the system, so the only additional components are the 74AC74, R1, and C1.



Notes:

1. R1 = 10K and C1 = 100 pF.
2. R2 and C2 should allow for Reset state times plus write wait states.

If software resets can occur, use RESET#. If no software resets will occur, eliminate the 74HC05 and use (RESET#).

The R1*C1 time constant is one microsecond to ensure that the flip-flop comes up 'on' after a power-up. The reset flip-flop at the rising edge of CLKOUT after the R2*C2 time constant has expired.

For manual resets, the flip-flop will turn on at the next rising edge of CLKOUT unless WR# is low. If WR# is low, the flip-flop turn on will be delayed until the next rising edge of CLKOUT when WR# is not low. This may occur after any number of wait states. The R2*C2 time constant must be long enough for the normal reset state times plus the maximum number of write wait states.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. ONCE Mode Entry

PROBLEM: In order to enter the ONCE mode, it is necessary to pull the TXD pin 0.5V below V_{SS}. Otherwise, the microcontroller will not enter ONCE mode.

IMPLICATION: Anyone using ONCE mode will be affected. Modification of test equipment required.

WORKAROUND: Test equipment must be modified to pull TXD to V_{SS} -0.5V.

STATUS: Fixed. This has been fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. Missing External Interrupt Requests (EXTINT, EXTINT1, and NMI)

PROBLEM: At low voltages and at high frequencies, it is possible to miss an interrupt occurrence on P0.7. The internal signal driver for P0.7 to the interrupt pending register was not strong enough to set the interrupt pending bit in certain conditions. The missed interrupt occurs at low Vcc and high frequency. The missed interrupt can occur in a window around the falling edge of CLKOUT.

On the B-stepping, the edge-triggered external interrupt EXTINT using P0.7 as the input source has been found to miss interrupts under certain conditions. The missed interrupts occur at high frequencies (greater than 16Mhz) and low voltages (less than 4.7V.) At voltages below spec, 3.1V and 16Mhz, missed interrupts were discovered on EXTINT/P2.2, NMI, and EXTINT1/P2.2. Higher temperatures slightly increased the occurred of the missed interrupts. Missed interrupts have not been seen on HSI.0 or T2CAPTURE. Investigation of the problem has shown that the edge-detect circuit that generates a single state pulse to the interrupt unit does not have enough drive to generate the proper signal at the interrupt unit to set the interrupt pending bit. The driver on P0.7 was found to be about 1/2 the size of the NMI driver, which explains the P0.7 failures occurring at voltages within the normal operating range. The driver on P2.2 is only slightly smaller than the NMI driver, which explains why failures were not seen on P2.2 in the normal operating range.

When an interrupt occurs on the EXTINT pin an internal interrupt signal generates a request to the interrupt unit. The interrupt unit then sets the corresponding interrupt pending bit. The internal interrupt signal must meet a minimum pulse width to set the interrupt pending bit. If the external interrupt occurs in a window of time around the falling edge of CLKOUT, the internal interrupt signal is shortened. The shortened pulse cannot drive the interrupt unit to set the interrupt pending bit. At lower voltage and higher

frequency, the driver of the internal interrupt signal can deactivate before the interrupt pending bit is set.

The missed interrupts occur most often at high frequencies, low voltage and higher temperatures. Testing for the problem was done by skewing a positive pulse edge across the period of a CLKOUT signal and varying the voltage.

The missed interrupt only occurred at a window of time just after the falling edge of CLKOUT. The window was as large as 2ns at 25Mhz and 3.0V on a 80C196KD at room temperature. The voltage was then increased by 0.1V increments. The size of the window would then shrink to about 1.8ns and the window position, where the interrupts are missed, would move about 1ns further from the falling edge of CLKOUT. This procedure was continued until interrupts were no longer observed to be missed. As the voltages got near 4.0V the rate of missed interrupts was about 1 in 150,000 events on P0.7 when all the events were concentrated on a 0.1ns window. Table 1 lists the voltages and frequencies that problems were observed on the various products at room temperature.

Interrupt Pin	Voltage	Frequency	Device
P0.7 EXTINT	2.9V - 4.6V	20Mhz	8XC196KD
P2.2 EXTINT	2.9V - 4.1V *	20Mhz	8XC196KD
NMI	2.9V - 3.5V *	20Mhz	8XC196KD
P2.2 EXTINT1	2.9V - 3.7V *	20Mhz	8XC196KD
P0.7 EXTINT	2.9V - 4.4V *	20Mhz	8XC196KC
P0.7 EXTINT	3.0V - 4.5V	16Mhz	8XC196KB

*. Out of specified operating range.

NOTE:

8XC196KB and 8XC196KD are the only devices which exhibit this failure in the normal operating range on the listed steppings.

IMPLICATION: Some missed interrupts were seen in normal operating region of the device. Therefore, customers using P0.7 for EXTINT may be affected.

On the B-stepping, any application using the EXTINT P0.7 interrupt source at low voltages (< 4.7V) and high frequencies (> 16MHz) should synchronize the interrupt signal to the rising edge of CLKOUT or, if possible, add software to ensure the servicing of the interrupt.

WORKAROUND: Add a latch that synchronizes the interrupt with the rising edge of CLKOUT. Software can be added to monitor P0.7 and check whether the interrupt pending bit is set when a transition occurs on P0.7.

Device Design Fixes: On the B step of the 8XC196KD products, different fixes were implemented in different devices. The following is a history of the fixes implemented.

83C196KD	Buffer Driver Size Increased; errata still marginally exists just out of range of normal operating conditions
87C196KD	Buffer Driver Size Increased and Latch Added; errata fixed

On the B-stepping, synchronizing the input signal to the rising edge of CLKOUT with a flip-flop will prevent an asynchronous signal from occurring in the window near the falling edge of CLKOUT. Software could also detect a missed interrupt by periodically checking whether the external interrupt signal is high at the port pin and the interrupt pending bit is low. If the level of the EXTINT pin has changed, the routine could then set the interrupt pending bit, thus causing an interrupt. This assumes the interrupt signal will remain high until the external interrupt routine acknowledges the interrupt.

EXTINT using P0.7 has been found to miss interrupts when operating at voltages less than 4.7V and frequencies greater than 16 MHz. There is a window near the falling edge of clockout at the above operating conditions that the edge detect circuitry fails to recognize and set the interrupt pending bit. On future steppings of the devices, corrective action will be taken to increase the drive capability of P0.7 and P2.2 and to synchronize the internal interrupt signal to guarantee the correct pulse width to set the interrupt pending bit.

STATUS: Fixed. This has been fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

On the B-Stepping, EXTINT using P0.7 has been found to miss interrupts when operating at voltages less than 4.7V and frequencies greater than 16 MHz. There is a window near the falling edge of clockout at the above operating conditions, that the edge detect circuitry fails to recognize and set the interrupt pending bit. On future steppings of the devices, corrective action will be taken to increase the drive capability of P0.7 and P2.2 and to synchronize the internal interrupt signal to guarantee the correct pulse width to set the interrupt pending bit.

9600005. BMOVI Windowing Count Register (Functional Description)

PROBLEM: When using the BMOVI instruction the count register (or second operand) cannot be windowed. Therefore, the count register must be located in lower RAM address space (1A-FFh). If the count register of the BMOVI instruction is located in the upper register space (100h or above) and an interrupt occurs during the BMOVI instruction execution, the count register will not be updated at the interrupt. The actual number of words moved will be equal to the number of words moved before the interrupt occurred plus the total number of words. The count register is not updated upon the interrupt so it still contains the total number of words after the interrupt completes.

IMPLICATION: Customer must verify that the count register for the BMOVI instruction is located in lower address space (1A-FFh).

WORKAROUND: None.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600006. SIO Mode O Max Baud (Functional Description)

PROBLEM: In synchronous mode 0, the minimum baud value is 0001H for transmissions and 0002H for receptions.

In asynchronous modes 1, 2, and 3, the minimum baud value is 0000H when using the internal clock signal and 0001H when using an external clock signal on T2CLK. At 16 MHz, the maximum baud rate is 2.76 Mbaud for mode 0 and 1.0 Mbaud for modes 1, 2, and 3.

Bits 14:0 of the BAUD_RATE register specify the baud value. (Bit 15 selects either the internal clock signal or an external clock signal on T2CLK.) Using a value less than the minimums listed above results in incorrect data. For mode 0 receptions, whatever data is present on the RXD pin when TXD begins clocking is treated as the least-significant bit, each remaining bit is shifted left by one bit, and the most-significant bit from the transmitter is never shifted in.

IMPLICATION: Any customer who uses synchronous mode 0 will be affected. Use a baud value that is equal to or greater than the minimum value listed above. This will result in slower baud rates, but should result in correct data.

WORKAROUND: None. Use a baud value that is equal to or greater than the minimum value:

- for synchronous mode 0, 0002H for receptions or 0001H for transmissions

- for asynchronous modes 1, 2, and 3, 0001H when using an external clock source or 0000H when using the internal clock signal

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600007. HSI Events (9 or More)

PROBLEM: The HSI FIFO can hold seven events/times, and the holding register can hold an additional event/time, for a total of eight events/times. Reading the HSI_STATUS and HSI_TIME registers unloads the holding register, allowing the next event/time to move from the FIFO into the holding register.

An error occurs if a ninth event occurs while the FIFO and holding register are full. This ninth event sets an internal HSI event latch. When software unloads the first event from the holding register (by reading HSI_STATUS and HSI_TIME), the second event moves into the holding register and the third through eighth events move down one position in the FIFO, leaving a vacancy in the FIFO. Because the internal HSI event latch is set, the ninth event moves into the FIFO. However, the ninth event has no time tag associated with it. A time tag is created at the time the event moves into the FIFO, and the FIFO_FULL and HSI_RDY bits of the IOS1 register reflect the event, so it **appears** that a valid ninth event occurred.

The FIFO_FULL bit, when set, indicates that the FIFO contains six or more events. The HSI_RDY bit, when set, indicates that the holding register contains one event. The following table summarizes the status of the FIFO_FULL and HSI_RDY bits after a series of eight events and after a series of nine events:

Event from FIFO	FIFO_FULL (9 events)	FIFO_FULL (8 events)	HSI_RDY (9 events)	HSI_RDY (8 events)
1	1	1	1	1
2	1	1	1	1
3	1	0	1	1
4	0	0	1	1
5	0	0	1	1
6	0	0	1	1
7	0	0	1	1
8	0	0	1	1
9	0	0	1	0

In summary, the HSI can correctly record only eight events. However, if a ninth event occurs while the FIFO and holding register are both full, the HSI module and the related status bits (FIFO_FULL and HSI_RDY) behave as though nine events were recorded.

IMPLICATION: Any customer using the HSI unit will be affected. Applications should be analyzed to ensure that nine events cannot occur before at least one event is unloaded from the holding register.

WORKAROUND: Analyze the application to ensure that nine events cannot occur before at least one event is unloaded from the holding register. The HSI unit can record an event every 9 state times. The maximum interrupt latency is 56 state times. Using this data, determine how frequently events can occur, and which interrupt should be used (HSI FIFO Full, HSI FIFO Fourth Entry, or HSI Data Available.

The following code can be used to ensure the FIFO is empty before setting up for an HSI event:

```
flush:    ld 0, hsi_time         ; clear event
          skip 0                 ; delay 3 state times
          skip 0                 ; delay 3 state times
          skip 0                 ; delay 3 state times
          jbs ios1, 7, flush     ; repeat until HSI_RDY bit is clear
                                     (the holding register is empty)
```

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600008. Writing HSI_MODE Resets the Divide-by-Eight Counter

PROBLEM: Writing to the HSI_MODE register always resets the HSI module's divide-by-eight counter. If you write HSI_MODE to configure an HSI, and another HSI was previously configured for "eight positive transitions" mode, the counter reset causes the previously configured HSI to lose up to seven accumulated events.

IMPLICATION: Applications that write to HSI_MODE after an HSI is configured for "eight positive transitions" mode will be affected.

WORKAROUND: There are three possible workarounds:

- If any HSI is to be used in "eight positive transitions" mode, use a single write to HSI_MODE to configure all HSI inputs at once.
- Disable the HSI input by clearing the associated bit(s) the IOC0 register, poll the HSI_STATUS register until seven counts have occurred, then enable the HSI to load the FIFO on the eighth transition.

- Configure the HSI for “every transition” mode, and use an external counter to pass through the eight transition.

STATUS: NoFix. There are no plans to fix this. Refer to Summary Table of Changes to determine the affected stepping(s).

9600009. IPD Hump

PROBLEM: Due to a floating node on the clockout disable circuit, an IPD hump of up to 700 (A can be seen. The IPD hump occurs approximately 0.5 seconds to 4 minutes after the device has entered powerdown mode. The hump is a leakage current of up to 700 (A which is present for a period of one second to several minutes in length, depending on the temperature. After the hump has occurred, the device returns and remains at the normal level of powerdown current.

IMPLICATION: If the clockout disable bit (IOC3.1) is cleared, then the IPD hump is not seen. If the clockout disable bit is set and powerdown mode is entered, then the IPD hump may occur.

WORKAROUND: To avoid this problem, enable CLKOUT (clear IOC3.1) before executing the IDLPD instruction. If noise from CLKOUT is an issue in your system, disable CLKOUT (set IOC3.1) upon return from powerdown.

STATUS: Fixed. This has been fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. Page 5-10

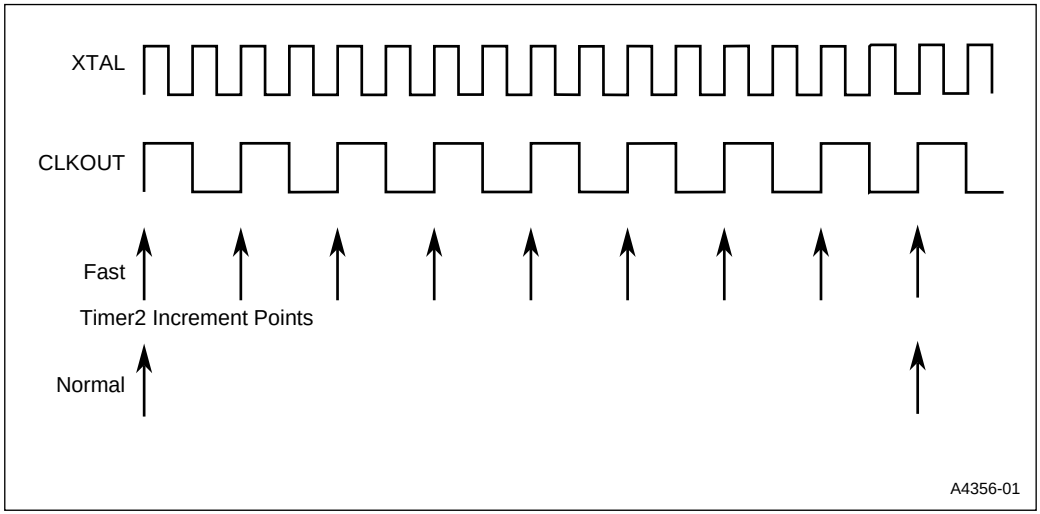
PROBLEM: In section 5.4.3 about NMI, a clarification is necessary regarding the last sentence in this paragraph. It should read as follows for better understanding.

‘If your system does not use the NMI interrupt, **connect the NMI pin to V_{SS}** to prevent spurious interrupts.’

002. Page 8-4

PROBLEM: Confusion has arisen regarding the fourth paragraph of Section 8.1.3.1. The following paragraph clarifies this text:

When FAST_T2_ENA is set (fast increment mode), Timer 2 increments once every state time, at the rate of Fosc/4. When FAST_T2_ENA is cleared (normal increment mode), Timer 2 increments once every eight state times at a rate of Fosc/32. See the timing diagram below for a depiction of the input clock signal, the clockout signal, and the points at which Timer 2 increments in the fast and normal modes.



003. Page 8-18

PROBLEM: It is explained in the second paragraph that external events generate the High-Speed Output interrupt (INT03) and internal events generate the Software Timer interrupt (INT05). An external event is defined as a toggle of one or more of the HSO outputs. An internal event is defined as the other HSO triggered events (see User's Manual). This explanation does not cover the HSO_ALL event interrupt. By these definitions, the HSO_ALL event would generate the High-Speed Output interrupt. Actually, the HSO_ALL event (Command Tag = 0Ch) generates the Software Timer interrupt. Therefore, in the Software Timer interrupt service routine it may be necessary to see whether the HSO_ALL event or one of the internal events (Reset Timer, Start A/D,

Software Timers) caused this interrupt. The HSO event bits in the IOS2 register are set when the HSO_ALL event occurs. Therefore, it will be easy to check if an HSO_ALL event caused the Software Timer interrupt. This is true for the PTS vectors as well. When an HSO_ALL event occurs, the Software Timer PTS vector location determines the PTS control block that is used.

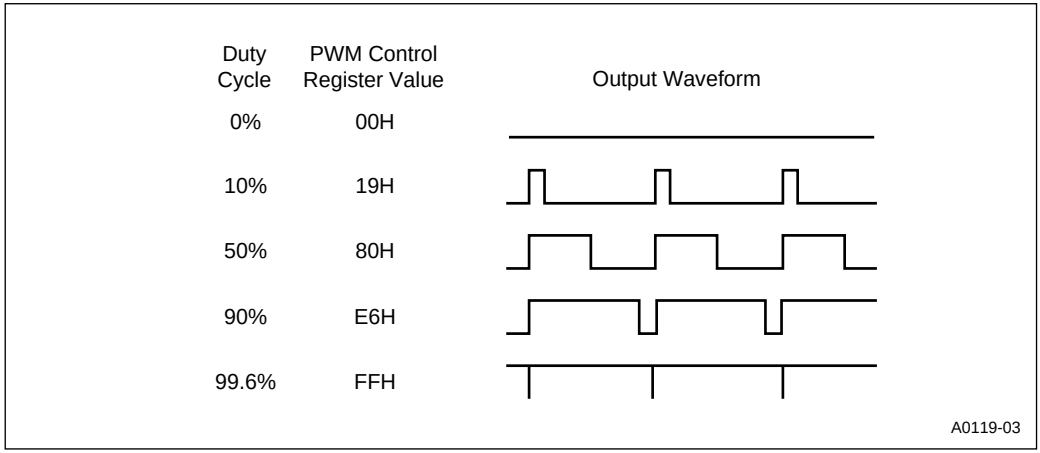
004. Page 9-3

PROBLEM: In Table 9-1, the problem for the INT_PEND register requires some clarification. The second sentence should read, 'Bit 1 is cleared when the interrupt takes the vector located at 2002h.'

005. Page 10-2

PROBLEM: Add the following sentences to the second paragraph after the first sentence: 'Since the value written to the control register is buffered, you can write a new 8-bit value to PWMx_CONTROL before the counter overflows. The new value is used during the next period of PWMx.'

The following figure replaces Figure 10-2.

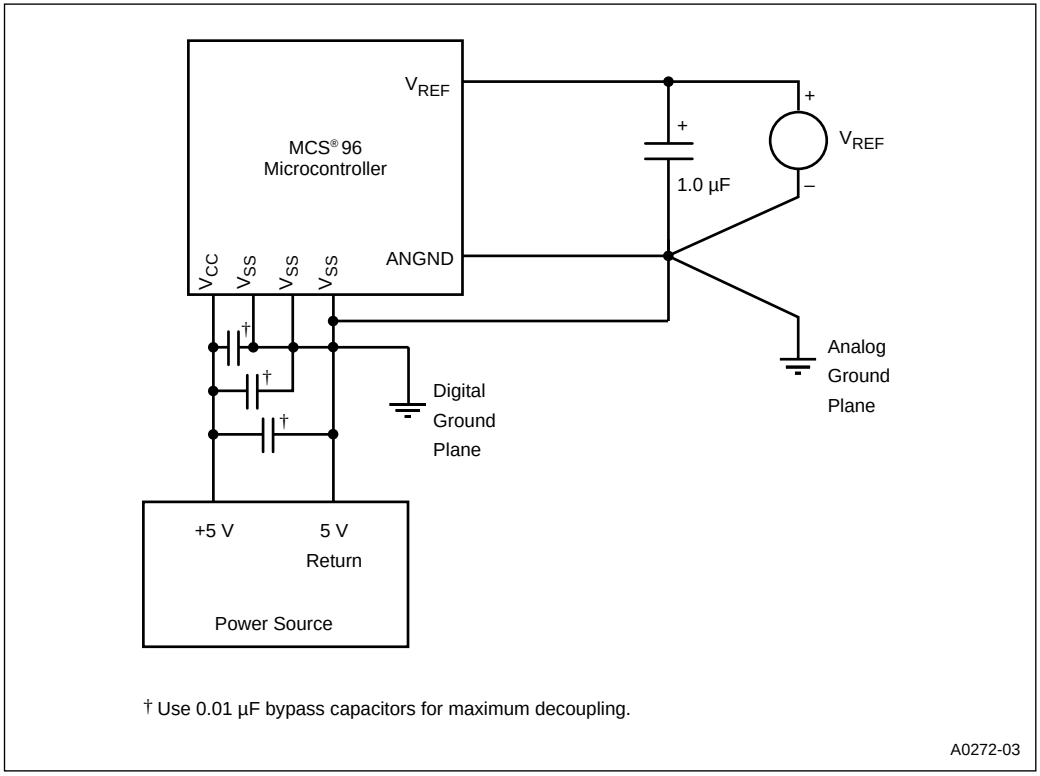


006. Page 11-3

PROBLEM: In Figure 11-2, the recommended capacitor value between V_{CC} and V_{SS} is 0.01 µF or greater. Also the recommended capacitor value between V_{REF} and ANGND is 1.0 µF.

In Section 11.2.1 the reason for these capacitors is explained. However, the second to last line of the first paragraph should read as follows:

'Connect a 0.01-µF bypass capacitor between V_{CC} and each V_{SS} pin and a 1.0-µF capacitor between V_{REF} and ANGND.'



007. Page 12-1

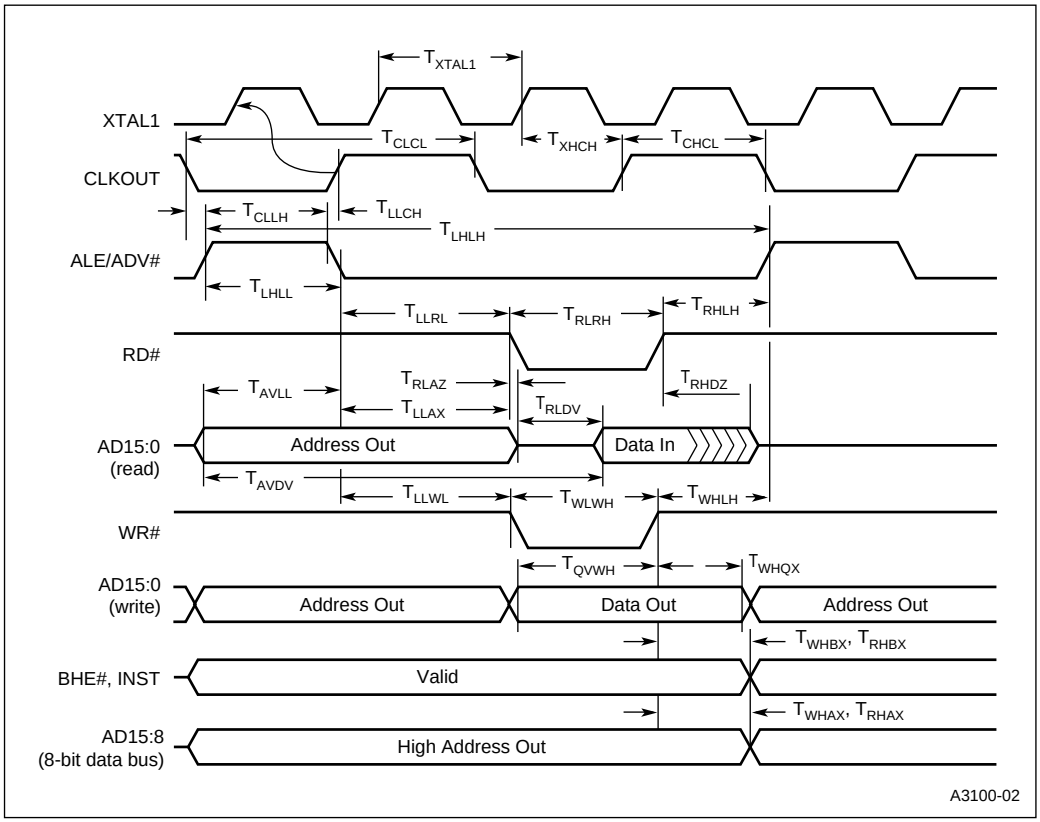
PROBLEM: In Section 12.1, the second sentence of the first paragraph should read as, 'The CPU stops executing instructions, but the special function registers (SFRs) and register RAM retain their data and the peripherals and interrupt system continue functioning.'

008. Page 13-4

PROBLEM: In Section 13.3, the first paragraph does not clearly explain the point made in the last two sentences. 'Some performance degradation can be expected comparing the 16-bit to 8-bit bus systems. A word fetch in a 16-bit bus system is done with a single word fetch. However, any word fetches in an 8-bit bus system must be done with two byte fetches.'

009. Page 13-22

PROBLEM: Figure 13-20 displays the system bus timing. However, there are a couple of mistakes. First, the WR# signal shows a range for the transition from high to low. This is incorrect, it should be a single line. Next, the signal labeled BUS should not refer to 16-bit mode only. This BUS signal shows AD0-7 in 8-bit mode and the entire bus (AD0-15) in 16-bit mode. The following figure replaces Figure 13-20.



010. Page 14-15

PROBLEM: The voltage is calculated by using the following formula:

Voltage= (20 x Test Rom Data)/256

011. Page 14-17

PROBLEM: There has been some confusion with Table 14-8. The external EPROM address for the PPW is 2014H/2015H, if the recommended Auto Programming circuit, shown in Figure 14-8, is used. As the text in Section 14.9.1 explains, the circuit in Figure

14-8 replaces previously recommended circuits that did not use P1.0-P1.2 to generate the upper address bits for the external EPROM.

The actual address output on the address/data bus is 4014H/4015H. However, due to remapping, using P1.0-P1.2 for the upper address lines as shown in Figure 14-8, the PPW will be read from 2014H/2015H.

Therefore, since the circuit in Figure 14-8 uses P1.0-P1.2 as the upper address bits for the external EPROM, the PPW should be stored at 2014H/2015H. If the address lines are used to address the external EPROM, then the PPW should be stored at 4014H/4015H**.**

012. Page 14-31

PROBLEM: Second sentence should read,' A zero on P3.0 selects the Dump Word command.'

013. Page 14-33

PROBLEM: In second sentence of first paragraph, reword 'hold EA# high' to 'pull EA# to V_{CC}'.

014. Page B-9

PROBLEM: The INST pin has a Weak Pull-up during Reset.

015. Page B-9

PROBLEM: Add a column to Table B-3 titled, Pin Status in ONCE.

ACH0-ACH7	FLOAT
PORT1	PULL-UP
TXD	FLOAT
RXD	FLOAT
EXTINT	FLOAT
T2CLK	FLOAT
T2RST	FLOAT
PWM0	FLOAT
P2.6-P2.7	PULL-UP

AD0-AD15	PULL-UP
HSI.0,HSI.1	FLOAT
HSI.2/HSO.4	FLOAT
HSI.3/HSO.5	FLOAT
HSO.0-HSO.3	PULL-DOWN
ALE	FLOAT
BHE#	FLOAT
BUSWIDTH	FLOAT
CLKOUT	FLOAT
EA#	FLOAT
INST	FLOAT
NMI	PULL-DOWN
RD#	FLOAT
READY	FLOAT
RESET#	PULL-UP
WR#	FLOAT

Also add - **Note 5**. The output pins are disconnected from internal circuitry in ONCE mode; therefore, the signal floats. The only current present on the pin is device leakage current which is in the low microamp range.

016. Page C-5

PROBLEM: PROBLEM:

The reset value for T2CAPTURE is **00H**.

The reset value for SP is **XX**.

017. Page C-16

PROBLEM: The reset state for CCR should be ‘XX’, since it is defined by the user’s code.

018. Page C-33

PROBLEM:

The Bit Name for bit 2 should say, ‘Enable **HSI.1** as HSI input’.

The Bit Name for bit 4 should say, ‘Enable **HSI.2** as HSI input’.

The Bit Name for bit 6 should say, ‘Enable **HSI.3** as HSI input’

019. Page C-37

PROBLEM: In the description for Bit 4, 1 = KB fast mode and 0 = KB normal mode.

020. Page C-45

PROBLEM: The description for Port 3 should read, ’Low Address/Data bus, AD0-AD7, during external accesses (EA#=0); otherwise, bidirectional port pins P3.0-P3.7.’

The description for Port 4 should read, ’High Address/Data bus, AD8-AD15, during external accesses (EA#=0); otherwise, bidirectional port pins P4.0-P4.7.’

021. Page C-51

PROBLEM: This is an additional explanation of the PPW. The LSB of the PPW should be located at x014H. The MSB of the PPW should be located at x015H. The upper three bits of the address is dependent on the Auto Programming circuit used. See the explanation under p 14-17.

022. Specification changes in Table 14-12.

PROBLEM: Table 14-12, ROM-Dump Mode Memory Map should read

Device	Internal OTPROM Address	External Memory Address
8XC196KD*	2000H-9FFFH	4000H-BFFFH
8XC196KC*	2000H-5FFFH	4000H-7FFFH
8XC196KD Security Key*	2000H-202FH	4020H-402FH
8XC196KC Security Key*	2000H-202FH	4020H-402FH

* Must use bank Switching; P1.0-P1.2 replaces A13-A15.

DOCUMENTATION CHANGES

001. Page 4-1

ITEM: Remove asterisked statement '*Always write Ports 3 and 4 as a single word." These ports can be written as bytes or as a word.

002. Page 4-2

ITEM: Note 2 and the first sentence in Section 4.2.

003. Page 4-4

ITEM: Figure 4-2 omits the top address of the special purpose memory in the blow-up of this memory section. The top reserved memory section starting at 205Eh, ends at **207Fh**.

004. Page 4-9

ITEM: Add the following sentence after the paragraph, **'NOTE:** If the WSR is set to a reserved Hwindow value, it may cause unpredictable results. The only way to reset the WSR is to reset the device or use POPA to restore a proper value.'

005. Page 5-4

ITEM: There are a couple of errors in the code example shown for modifying interrupt priorities. The DI instruction is unnecessary, and the example omits three lines of code.

The corrected code is as follows:

```
SERIAL_RI_ISR:
      PUSHA           ;Save PSW, INT_MASK, INT_MASK1, & ;WSR
                      ;(This disables all interrupts.)
      LDB INT_MASK1,  #01000000b;Enable EXTINT only
      EI              ;Enable servicing of interrupts
                      ;
                      ; Service the RI interrupt
                      ;
      POPA            ; Restore PSW, INT_MASK, INT_MASK1,
                      ;& WSR
      RET
```

```
CSEG AT 2038H       ; Fill in interrupt vector table
      DCW SERIAL_RI_ISR
      END
```

006. Page 5-6

ITEM: In the explanation of the handling of interrupt service routines, there are several mistakes in steps #2 and #6. The following text shows the corrected points in these steps.

2) The PUSHA instruction, which is **now** guaranteed to execute, saves the contents of the PSW, **INT_MASK**, INT_MASK1, and the Window Select Register (WSR) onto the stack and then clears the PSW, **INT_MASK**, and INT_MASK1. In addition to the arithmetic flags, the PSW contains the global interrupt bit (I), and the PTS enable bit (PSE). By clearing the PSW and the interrupt mask registers, **PUSHA** effectively masks all maskable interrupts,... (the remaining text is correct).

6) At the end of the service routine, the POPA instruction restores the original contents of thePSW, **INT_MASK**, INT_MASK1 and WSR registers;... (the remaining text is correct).

007. Page 5-7

ITEM: Table 5-2 has a few mistakes in the Minimum Pulse Width and the Sample During phase. Despite differences in the circuitry of these interrupt sources (HSI.0, NMI, P0.7, P2.2, Timer 2 Capture), all of their pulse widths should be >1 state time. Note that the pulse width must be greater than 1 state time. If the pulse width is exactly 1 state time or less, there is statistical chance that the interrupt could be missed. Also changes to the first paragraph in Section 5.3 need to be made to reflect this.

Change Sampled Phase for NMI and Timer 2 Capture from Phase 2 to Phase 1.

Change Sampled Phase for P0.7 EXTINT from Phase 1 to Phase 2.

008. Page 5-7

ITEM: Table 5-3 omits two other instructions, **EPTS** and **DPTS**, which inhibit interrupts from being acknowledged until after the next instruction is executed.

DPTS - Disables the PTS

EPTS - Enables the PTS

009. Page 5-8

ITEM: In Section 5.3.2, the calculation of latency incorrectly states the response time for standard interrupts. The third bullet under the sentence 'To calculate latency, add the following terms' should read as:

* The response time (**11** state times for an internal stack or **13** for an external stack) for standard interrupts only.

Also, in Section 5.3.2.1, the first sentence incorrectly outlines the maximum delay for a standard interrupt. The paragraph should begin with the following sentence:

The maximum delay for a standard interrupt is **56** state times (4+39+**13**).

010. Page 5-9

ITEM: Figure 5-3 displays the incorrect number of state times it takes to service a call. This figure shows that it takes 16 state times when a call is forced; this actually should be **11** state times. And the 61 state times should be changed to **56**.

011. Page 5-16

ITEM: The third sentence in Section 5.6.2 should read as following: 'The PTS mode defines the functions of the other bits; see Table **5-7** for Single and Block Transfer modes and Table 5-8 **for A/D Scan, HSI and HSO modes.'**

012. Page 5-16

ITEM: In Table 5-6, the selected modes for the respective bit 7-5 combinations are incorrect for the following PTS modes: Single Transfer, HSI, HSO, and Block Transfer. The following is correct for Table 5-6.

0	0	0	**Block Transfer**
0	0	1	**HSO Mode**
0	1	1	**HSI Modes**
1	0	0	**Single Transfer**

013. Page 5-18

ITEM: In Table 5-9, the PTSCON should equal **95h** instead of 15h.

014. Page 5-19

ITEM: In Table 5-10, the PTSCON should equal **17h** instead of 97h.

015. Page 5-25

ITEM: In Table 5-17, the PTSCON should equal **6Ah** instead of 2Ah.

016. Page 5-26

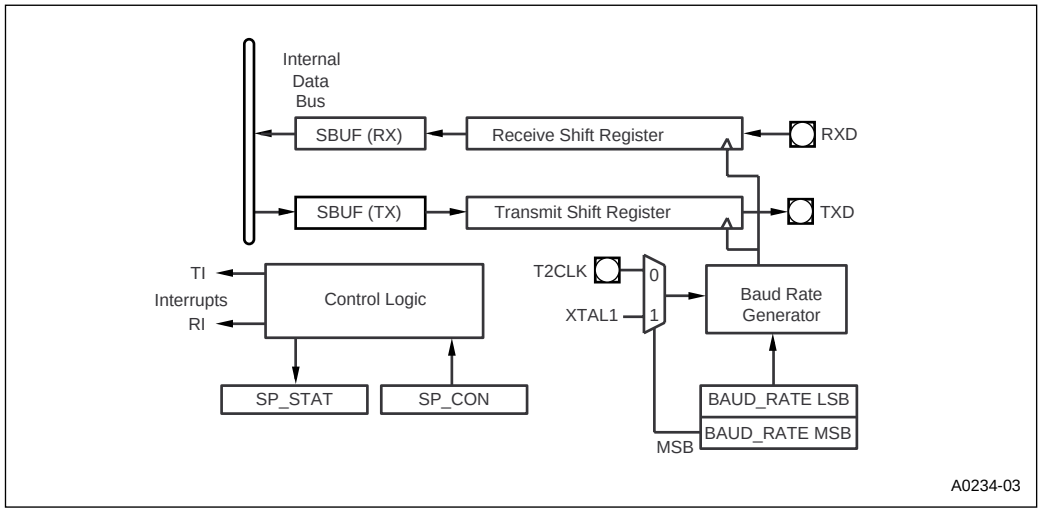
ITEM: In Table 5-19, the PTSCON should equal **2Ah** instead of 6Ah.

017. Page 6-10

ITEM: Remove the second sentence in Section 6.2.3.

018. Page 7-1

ITEM: The following block diagram will be included in future manuals.



Serial Port Block Diagram

019. Page 7-8

ITEM: In the second paragraph of Section 7.3.3, the first sentence refers to the 8096H. This actually should be the **8096BH**.

020. Page 7-9

ITEM: In Table 7-5, the BAUD_RATE value in Mode 0 at 1200 should be **9A0Ah** instead of 8A9Ah, and at 300 should be **E82Ah** instead of E82Bh.

021. Page 8-11

ITEM: The last paragraph of page 8-11 explains the operation of the divide-by-eight counter incorrectly. Replace the last paragraph with the following:

Writing to the HSI_MODE register always resets the HSI module's divide-by-eight counter.

If you write HSI_MODE to configure an HSI, and another HSI was previously configured for "eight positive transitions" mode, the counter reset causes the previously configured HSI to lose up to seven accumulated events. For this reason, we recommend that you use a single write to HSI_MODE to configure all HSI inputs at once.

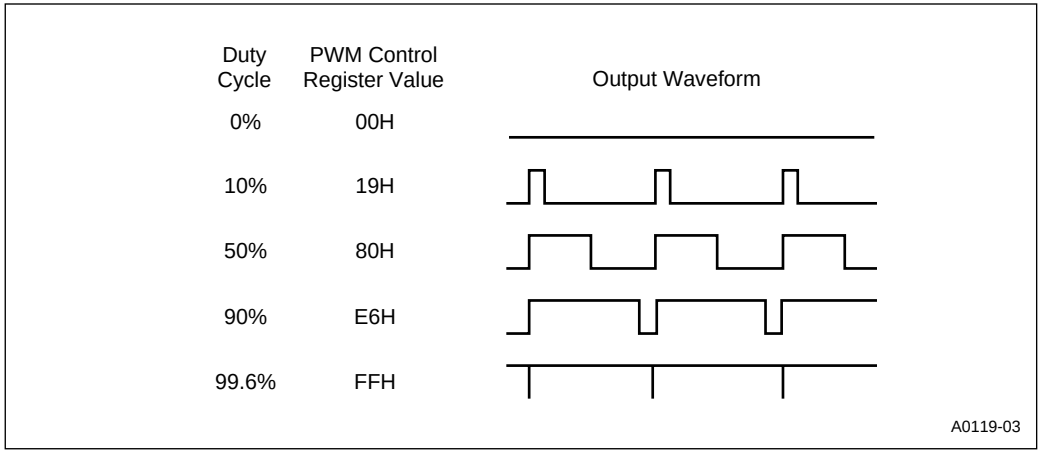
022. Page 9-2

ITEM: The fifth bullet under Section 9.2, should read '80**C**196KB-compatible mode.'

023. Page 10-2

ITEM: On page 10-2, add the following sentences to the second paragraph after the first sentence: 'Since the value written to the control register is buffered, you can write a new 8-bit value to PWMx_CONTROL before the counter overflows. The new value is used during the next period of PWMx.'

The following figure replaces Figure 10-2.



024. Page 11-1

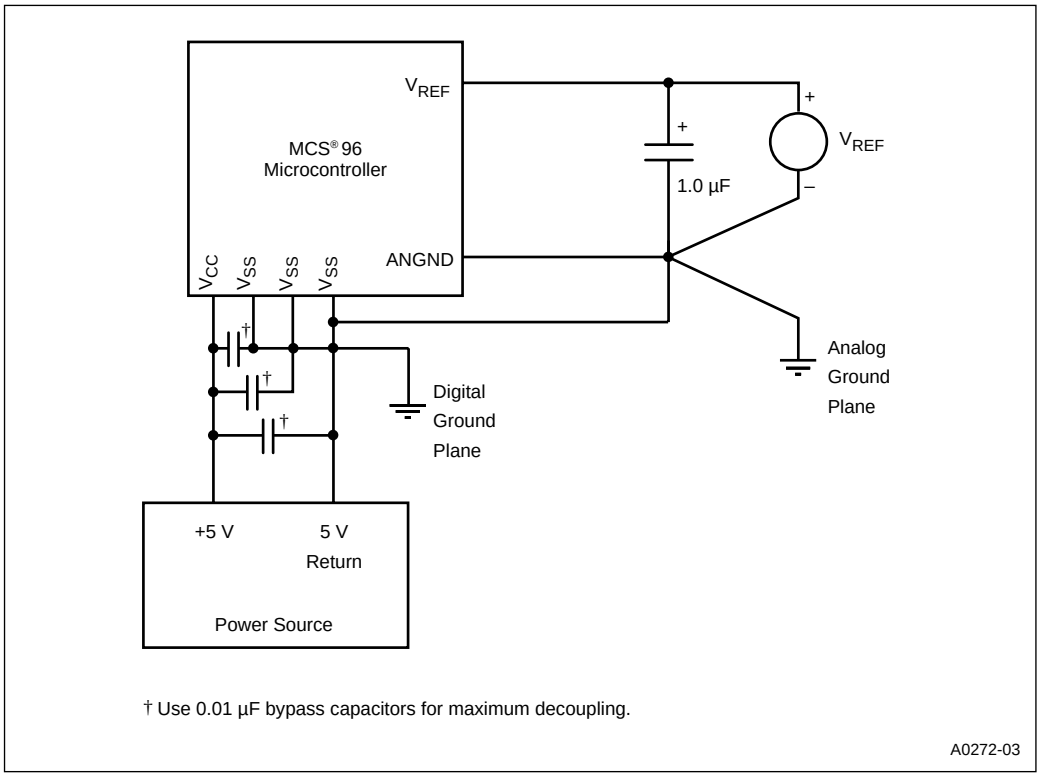
ITEM: The last sentence in Section 11.1 should read: . . . '**Figure 11-1**' not Figure 14-1.

025. Page 11-2

ITEM: In Figure 11-1, the recommended capacitor value between V_{CC} and V_{SS} is **0.01 µF** or greater. Thus, the 0.1 µF shown can be used.

026. Page 11-3

ITEM: In Figure 11-2, the recommended capacitor value between V_{CC} and V_{SS} is **0.01 µF** or greater. Also the recommended capacitor value between V_{REF} and ANGND is **1.0 µF**. The following figure replaces Figure 11-2:



In Section 11.2.1, the reason for these capacitors is explained. However, the second to last line of the first paragraph should read as follows:

'Connect a 0.01-µF bypass capacitor between V_{CC} and each V_{SS} pin and a 1.0-µF capacitor between V_{REF} and ANGND.'

027. Page 11-6

ITEM: In Figure 11-6, the timing diagram incorrectly represents the T_{xlxl} and T_{xhxl} timing specifications. The timing diagram below replaces Figure 11-6.

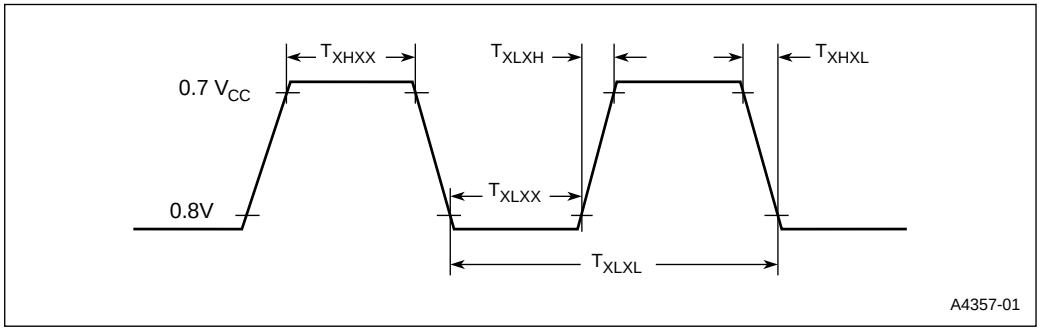


Figure 11-6. External Clock Drive

028. Page 11-8

ITEM: Figure 11-8 shows the reset pin internal circuit. However, there are a couple of mistakes; the following figure shows the corrected version. The **inverter** at the Reset State Machines Trigger input and the **OR gate** at the SET input of the latch are the corrections to this figure.

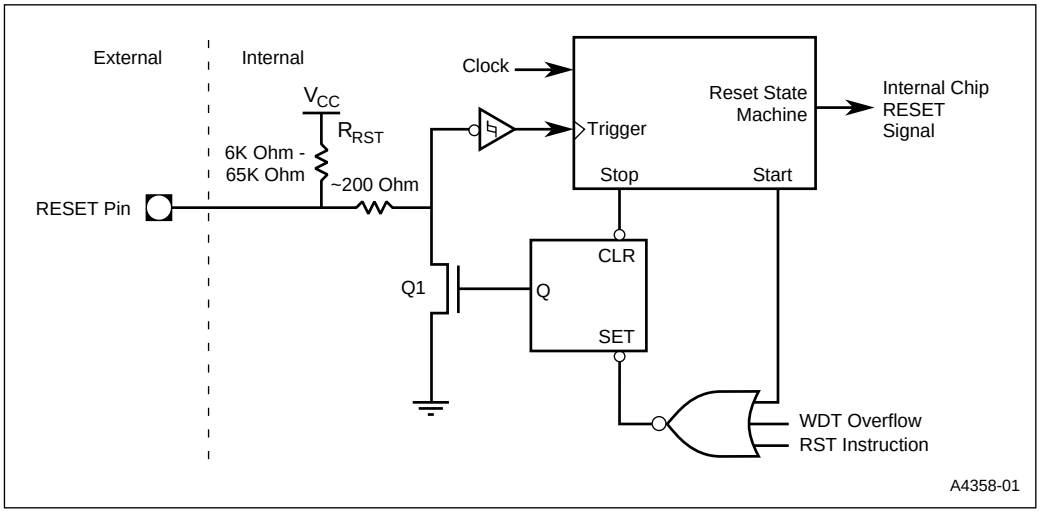


Figure 11-8. Reset Pin Internal Circuit

029. Page 12-2

ITEM: In the second paragraph, the last two sentence refer to the EA# pin, but they should be switched. As I/O ports, **EA# = 1** and as address/data bus, **EA# = 0**.

030. Page 12-7

ITEM: In Section 12.3, remove the first sentence of the second paragraph and replace with: 'See Table B-3 in Appendix B for pin values during ONCE mode.'

031. Page 13-2

ITEM: In Table 13-1, the INST pin description should read as follows: 'Instruction Fetch. The signal is valid only during external memory **bus** cycles.....'

032. Page 13-9

ITEM: In the second paragraph of Section 13.4, the explanation about the Ready line should read, '...the external memory device **deasserts** the READY signal..'

033. Page 14-9

ITEM: The last description in Table 14-4 should read as, 'No programming modes allowed. Reads of internal OTPROM are not allowed if program execution is external.'

034. Page 14-11

ITEM: In Figure 14-5, the EA# and V_{PP} pins should be tied to V_{PP} through a switch, not V_{CC}. And on the PALE# pin, the push button and resistor to ground should be swapped.

Also, the third sentence in the first paragraph should read, 'You can read the USFR from location 1FF6h, but must program these bits by...'.

035. Page 14-12

ITEM: The first paragraph should read, 'Setting **USFR.3**....' and the second paragraph, 'Setting **USFR.2'.....**.

036. Page 14-15

ITEM: The second paragraph should read,'....either 5 (8XC196KD devices) or 25 (8XC196KC devices)'

037. Page 14-19

ITEM: In Figure 14-8, the A0-A7 and A8-A12 address bus should only be pointing toward the 27512.

038. Page 14-29

ITEM: In Figure 14-15, the first block spells ‘Security’ incorrectly.

039. Page A-23

ITEM: The operation for XCH and XCHB should have the arrow pointing both ways. The instruction format for XCH and XCHB should label the top opcode as **direct** and the bottom as **indexed**.

040. Page A-28

ITEM: Opcodes 04 and 14 should be labeled as **direct**. Opcodes 0B and 1B should be labeled as **indexed.**

041. Page A-35

ITEM: The instruction length for ANDB (2 ops) with long-indexed is **5** and for ANDB (3 ops) with long-indexed is **6**.

042. Page A-36

ITEM: The instruction length for LJMP with long-indexed is **3**.

043. Page A-37

ITEM: The instruction length for all conditional jumps (except DJNZ, DJNZW, JBC, and JBS) is **2** instead of 1.

044. Page A-38

ITEM: The opcode value for RST is **FF** not FE.

045. Page A-39

ITEM: The instruction length for all single instructions is **2**, with the exception of CMPL which is **3**.

046. Page A-45

ITEM: The following changes are required in the “Special” section of Table A-10:

Mnemonic	Direct	Immed.
IDLPD Valid key	—	8 (1)
Invalid key	—	28 (2)
RST	4	—

Notes:

1. The instruction takes 8 state times, but the effects of powerdown and idle may take longer.
2. Includes the time required for reset.

047. Page B-6

ITEM: In the description for P3 and P4, remove the sentence, ‘Ports 3 and 4 can be read and written only as a word, at location 1FFEH.’

048. Page C-14

ITEM: The first formula for Synchronous Mode 0 should be Baudrate **x 2**, not x8.

In the table, the BAUD_RATE value in Mode 0 at 300 should be **E82Ah** instead of E82Bh.

049. Page C-45

ITEM: Remove the last sentence in the paragraph,’Ports 3 and 4 can be read.....’

050. Page C-55

ITEM: The PTSBLOCK is offset 6 from PTS Control Block, not 7.

051. Page C-56

ITEM: The PTS mode bit settings are interchanged. The correct mode settings are as follows:

Mode	Bit 7	Bit 6	Bit 5
Block transfer	0	0	
Single transfer	1	0	0

052. Page C-57

ITEM: The PTS mode bit settings are interchanged for HSO and HSI modes. The correct mode settings are as follows:

Mode	Bit 7	Bit 6	Bit 5
HSO	0	0	1
HSI	0	1	1
A/D	1	1	0

053. Page C-65

ITEM: In the paragraph, the references to PTSDST should be to PTSSRC. The corrected text is as follows:

The PTSSRC register is used in single transfer, block transfer, and HSO modes. PTSSRC points to the source memory location. PTSSRC is optionally incremented at the end of a PTS cycle. In single transfer mode, PTSCON.1 and PTSCON.3 control whether **PTSSRC** is incremented. In block transfer mode, PTSCON.1 controls whether **PTSSRC** is incremented after each transfer, and PTSCON.3 controls whether **PTSSRC** retains its final value or reverts to its original value. In HSO mode, PTSCON.3 determines whether **PTSSRC** is updated at the end of the PTS cycle.

054. Subtitle change on page 8-23.

On page 8-23, Section 8.3.2.7, the subtitle should read “Using HSO.0-HSO.6 As Output Pins” instead of “Using HSO.0-HSO.5 As Output Pins”.