82527 SERIAL COMMUNICATIONS CONTROLLER AREA NETWORK PROTOCOL

Express

Advance Information **Datasheet**

Product Features

- Supports CAN Specification 2.0
  - —Standard Data and Remote Frames
  - —Extended Data and Remote Frames
- Programmable Global Mask
  - —Standard Message ldentifier
  - —Extended Message ldentifier
- 15 Message Objects of 8-Byte Data Length
  - —14 Tx/Rx Buffers
  - —1 Rx Buffer with Programmable Mask
- Flexible CPU Interface
  - —8-Bit Multiplexed
  - —16-Bit Multiplexed
  - —8-Bit Non-Multiplexed (Synchronous/ Asynchronous)
  - —Serial Interface
- Programmable Bit Rate
- Programmable Clock Output
- Flexible Interrupt Structure
- Flexible Status Interface
- Configurable Output Driver
- Configurable Input Comparator
- Two 8-Bit Bidirectional I/O Ports
- 44-Lead PLCC Package
- Pinout Compatibility with the 82526

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1.0 INTRODUCTION

The 82527 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The 82527 is Intel's first device to support the standard and extended message frames in CAN Specification 2.0 Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames. Due to the backwardly compatible nature of CAN Specification 2.0, the 82527 also fully supports the standard message frames in CAN Specification 2.0 Part A.

The 82527 features a powerful CPU interface that offers flexibility to directly interface to many different CPUs. It can be configured to interface with CPUs using an 8-bit multiplexed, 16-bit multiplexed, or 8-bit non-multiplexed address/data bus for Intel and non-Intel architectures. A flexible serial interface (SPI) is also available when a parallel CPU interface is not required.

The 82527 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

The 82527 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The 82527 PLCC offers hardware, or pinout, compatibility with the 82526. It is pin-to-pin compatible with the 82526 except for pins 9, 30, and 44. These pins are used as chip selects on the 82526 and are used as CPU interface mode selection pins on the 82527.

The 82527 is fabricated using Intel's reliable CHMOS III 5V technology and is available in 44-lead PLCC for the express temperature range (–40°C to +85°C).

Figure 1. TN82527 - *Express* Block Diagram

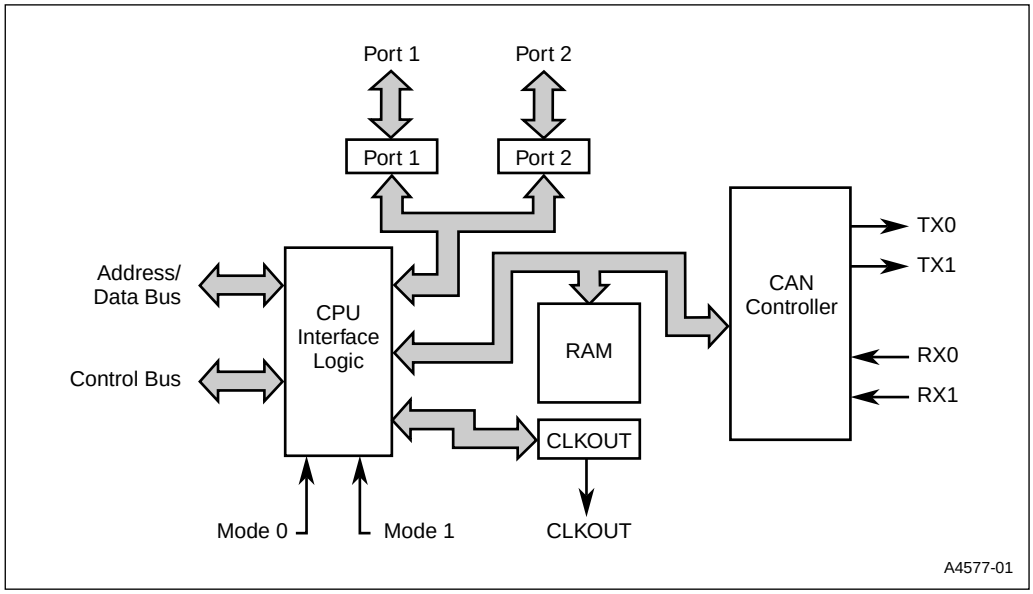
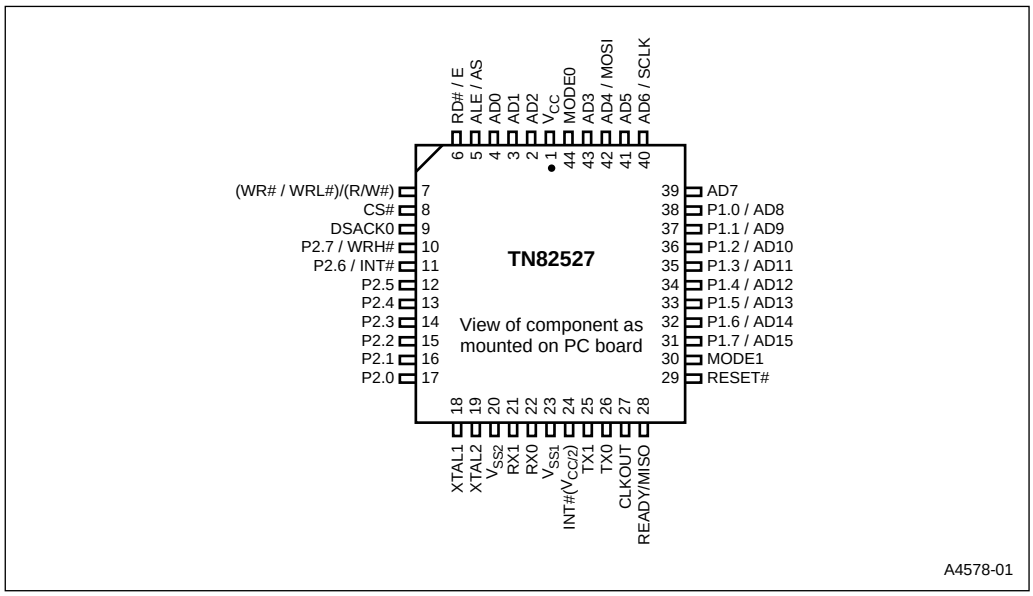


Figure 2. TN82527 44-Pin PLCC Package



2.0 PIN DESCRIPTIONS

The 82527 - *Express* pins are described in this section. Table 1 presents the legend for interpreting the pin types.

Table 1. Pin Type Legend

Symbol	Description
I	Input Only Pin
O	Output Only Pin
I/O	Pin can be either Input or Output

Table 2. Pin Descriptions (Sheet 1 of 2)

Name	Type	Description
V_{SS1}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides digital ground.
V_{SS2}	Ground	GROUND connection must be connected externally to a V_{SS} board plane. Provides ground for analog comparator.
V_{CC}	Power	POWER connection must be connected externally to +5 V DC. Provides power for entire device.
XTAL1	I	Input for an external clock. XTAL1 (along with XTAL2) are the crystal connections to an internal oscillator.
XTAL2	O	Push-pull output from the internal oscillator. XTAL2 (along with XTAL1) are the crystal connections to an internal oscillator. If an external oscillator is used, XTAL2 must be floated, or not be connected. XTAL2 must not be used as a clock output to drive other CPUs.
CLKOUT	O	Programmable clock output. This output may be used to drive the oscillator of the host microcontroller.
RESET#	I	**Warm Reset:** (V_{CC} remains valid while RESET# is asserted), RESET# must be driven to a valid low level for 1 ms minimum. **Cold Reset:** (V_{CC} is driven to a valid level while RESET# is asserted), RESET# must be driven low for 1 ms minimum measured from a valid V_{CC} level. No falling edge on the reset pin is required during a cold reset event.
CS##	I	A low level on this pin enables CPU access to the 82527 device.
INT# (V_{CC}/2)	O O	The interrupt pin is an open-drain output to the host microcontroller. V_{CC}/2 is the power supply for the ISO low speed physical layer. The function of this pin is determined by the MUX bit in the CPU Interface Register (Address 02H) as follows: MUX e 1: pin 24 (PLCC) = V_{CC}/2, pin 11 = INT# MUX e 0: pin 24 (PLCC) = INT#
RX0 RX1	I I	Inputs from the CAN bus line(s) to the input comparator. A recessive level is read when RX0 > RX1. A dominant level is read when RX1 > RX0. When the CoBy bit (Bus Configuration register) is programmed as a “1”, the input comparator is bypassed and RX0 is the CAN bus line input.
TX0 TX1	O O	Serial data push-pull output to the CAN bus line. During a recessive bit TX0 is high and TX1 is low. During a dominant bit TX0 is low and TX1 is high.

Table 2. Pin Descriptions (Sheet 2 of 2)

Name	Type	Description
AD0/A0/ICP AD1/A1/CP AD2/A2/CSAS AD3/A3/STE AD4/A4/MOSI AD5/A5 AD6/A6/SCLK AD7/A7	I/O-I-I I/O-I-I I/O-I-I I/O-I I/O-I-I I/O-I I/O-I-I I/O-I	Address/Data bus in 8-bit multiplexed mode. Address bus in 8-bit non-multiplexed mode. Low byte of A/D bus in 16-bit multiplexed mode. In Serial Interface mode, the following pins have the following meaning: AD0: ICP Idle Clock Polarity AD1: CP Clock Phase AD2: CSAS Chip Select Active State AD3: STE Sync Transmit Enable AD6: SCLK Serial Clock Input AD4: MOSI Serial Data Input
AD8/D0/P1.0 AD9/D1/P1.1 AD10/D2/P1.2 AD11/D3/P1.3 AD12/D4/P1.4 AD13/D5/P1.5 AD14/D6/P1.6 AD15/D7/P1.7	I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O I/O-O-I/O	High byte of A/D bus in 16-bit multiplexed mode. Data bus in 8-bit non-multiplexed mode. Low speed I/O port. P1 pins in 8-bit multiplexed mode and serial mode. Port pins have weak pullups until the port is configured by writing to 9FH and AFH.
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6/INT# P2.7/WRH#	I/O I/O I/O I/O I/O I/O I/O-O I/O-I	P2 in all modes. P2.6 is INT# when MUX = 1 and is open-drain. P2.7 is WRH# in 16-bit multiplexed mode.
Mode0 Mode1	I I	These pins select one of the four parallel interfaces. These pins are weakly held low during reset. Mode1 Mode0 0 0 8-bit multiplexed — Intel 0 0 Serial Interface mode entered when RD# = 0, WR# = 0 upon reset. 0 1 16-bit multiplexed — Intel 1 0 8-bit multiplexed — non-Intel 1 1 8-bit non-multiplexed
ALE/AS	I-I	ALE used for Intel modes. AS used for non-Intel modes, except Mode 3 this pin must be tied high.
RD# E	I I	RD#used for Intel modes. E used for non-Intel modes, except Mode 3 Asynchronous this pin must be tied high.
WR#/WRL# R/W#	I I	WR#in 8-bit Intel mode and WRL# in 16-bit Intel mode. R/W# used for non-Intel modes.
READY MISO	O O	READY is an output to synchronize accesses from the host microcontroller to the 82527. READY is an open-drain output to the host microcontroller. MISO is the serial data output for the serial interface mode.
DSACK0#	O	DSACK0# is an open-drain output to synchronize accesses from the host microcontroller to the 82527.

3.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature –60°C to +150°C

Voltage from Any Pin to
V_{SS} ..... –0.5 V to +7.0 V

Laboratory testing shows the 82527 will withstand up to 10 mA of injected current into both RX0 and RX1 pins for a total of 20 days without sustaining permanent damage. This high current condition may be the result of shorted signal lines. The 82527 will not function properly if the RX0/RX1 input voltage exceeds V_{CC}+0.5 V.

NOTICE: This is a production data sheet. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

3.1 DC CHARACTERISTICS

Operating Conditions:

- V_{CC} = 5 V ±10%
- T_A = –40°C to +85°C

Table 3. DC Characteristics

Sym	Parameter	Min	Max	Conditions
V_{IL}	Input Low Voltage (All except RX0, RX1, AD0±AD7 in Mode 3)	–0.5	0.8 V	
V_{IL1}	Input Low Voltage for AD00–D7 in Mode 3	–0.5	0.5 V	
V_{IL2}	Input Low Voltage (RX0) for Comparator Bypass Mode		0.5 V	
V_{IL3}	Input Low Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU		0.3 V_{CC}	
V_{IH}	Input High Voltage (All except RX0, RX1, RESET#)	3.0 V	V_{CC} + 0.5 V	
V_{IH1}	Input High Voltage (RESET#) Hysteresis on RESET#	3.0 V 200 mV	V_{CC} + 0.5 V	
V_{IH2}	Input High Voltage (RX0) for Comparator Bypass Mode	4.0 V		
V_{IH3}	Input High Voltage for Port 1 and Port 2 Pins Not Used for Interface to Host CPU	0.7 V_{CC}		
V_{OL}	Output Low Voltage (All Outputs except TX0, TX1)		0.45 V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage (All Outputs except TX0, TX1, CLOCKOUT)	V_{CC} – 0.8 V		I_{OH} = –200 µA
V_{OHR1}	Output High Voltage (CLOCKOUT)	0.8 V		I_{OH} = –80 µA
I_{LK}	Input Leakage Current		±10 µA	$V_{SS} < V_{IN} < V_{CC}$
C_{IN}	PIN Capacitance**		10 pF	F_{XTAL} = 1 KHz
I_{CC}	Supply Current		50 mA	F_{XTAL} = 16 KHz(1)
I_{SLEEP}	Sleep Current with V_{CC}/2 Output Enabled, No Load with V_{CC}/2 Output Disabled		700 µA 100 µA	(1)
I_{PD}	Powerdown Current		25 µA	XTAL1 Clocked(1)

NOTES:

**Typical value based on characterization data. Port pins are weakly held after reset until the port configuration registers are written (9FH, AFH).

1. All pins are driven to V_{SS} or V_{CC} including RX0 and RX1.

3.2 PHYSICAL LAYER SPECIFICATIONS

Operating Conditions:

- Load = 100 pF
- V_{CC} = 5 V ±10%
- T_A = –40°C to +85°C

Table 4. DC Characteristics

RX0/RX1 and TX0/TX1	Min	Max	Conditions
Input Voltage	–0.5 V	V_{CC} + 0.5 V	
Common Mode Range	V_{SS} + 1 V	V_{CC} – 1 V	
Differential Input Threshold	±100 mV		
Internal Delay 1: Sum of the Comparator Input Delay and the TX0/TX1 Output Driver Delay		60 ns	Load on TX0, TX1 = 100 pF, +100 mV to –100 mV RX0/RX1 differential
Internal Delay 2: Sum of the RX0 Pin Delay (if the Comparator is Bypassed) and the TX0/TX1 Output Driver Delay		50 ns	Load on TX0, TX1 = 100 pF
Source Current on Each TX0, TX1		–10 mA	$V_{OUT} = V_{CC} – 1$ V
Sink Current on Each TX0, TX1		10 mA	V_{OUT} = 1 V
Input Hysteresis for RX0/RX12		0 V	
$V_{CC}/2$			
$V_{CC}/2$	2.38 V	2.62 V	$I_{OUT} \leq 75$ µA, V_{CC} = 5 V

3.3 CLOCKOUT SPECIFICATIONS

Operating Conditions:

- Load = 50 pF

Table 5. Clockout Specifications

Parameter	Min	Max
CLOCKOUT Frequency	XTAL/15	XTAL

3.4 AC CHARACTERISTICS

3.4.1 8/16-Bit Multiplexed Intel Modes (Modes 0, 1)

Operating Conditions:

- V_{CC} = 5 V ±10%
- V_{SS} = 0 V
- T_A = –40°C to +85ºC
- C_L = 100 pF

Table 6. AC Characteristics 8/16-Bit Multiplexed Intel Modes (Modes 0, 1) (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Conditions
$1/T_{XTAL}$	Oscillator Frequency	8 MHZ	16 MHz	
$1/T_{SCLK}$	System Clock Frequency	4 MHZ	10 MHZ	
$1/T_{MCLK}$	Memory Clock Frequency	2 MHZ	8 MHZ	
T_{AVLL}	Address Valid to ALE Low	7.5 ns		
T_{LLAX}	Address Hold after ALE Low	10 ns		
T_{LHLL}	ALE High Time	30 ns		
T_{LLRL}	ALE Low to RD# Low	20 ns		
T_{CLLL}	CS# Low to ALE Low	10 ns		
T_{QVWH}	Data Setup to WR# High	27 ns		
T_{WHQX}	Input Data Hold after WR# High	10 ns		
T_{WLWH}	WR# Pulse Width	30 ns		
T_{WHLH}	WR# High to Next ALE High	8 ns		
T_{WHCH}	WR# High to CS# High	0 ns		
T_{RLRH}	RD# Pulse Width This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to READ from 04H and 05H (See t RLDV)	40 ns		
T_{RLDV}	RD# Low to Data Valid (Only for Registers 02H, 04H, 05H)	0 ns	55 ns	
T_{RLDV1}	RD# Low Data to Data Valid (for Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write (1) for Read Cycle with a Previous Write (1)		1.5 T_{MCLK} + 100 ns 3.5 T_{MCLK} + 100 ns	
T_{RHDZ}	Data Float after RD# High	0 ns	45 ns	
T_{CLYV}	CS# Low to READY Setup Condition: Load Capacitance on the READY Output: 50 pF		32 ns 40 ns	V_{OL}=1 V V_{OL}=0.45 V
T_{WLYZ}	WR# Low to READY Float for a Write Cycle if No Previous Write is Pending (2)		145 ns	
T_{WHYZ}	End of Last Write to READY Float for a Write Cycle if a Previous Write Cycle is Active (2)		2 T_{MCLK} + 100 ns	

NOTES:

References to WR# also pertain to WRH#.

1. Definition of “read cycle without a previous write”: The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 T_{MCLK}.
2. Definition of “write cycle with a previous write”. The time between the rising edge of WR#/WRH# (for the previous write cycle) and the rising edge of WR#/WRH# (for the current write cycle) is less than 2 T_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Table 6. AC Characteristics 8/16-Bit Multiplexed Intel Modes (Modes 0, 1) (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Conditions
T_{RLYZ}	RD# Low to READY Float (for registers except 02H, 04H, 05H) for Read Cycle without a Previous Write (1) for Read Cycle with a Previous Write (1)		2 T_{MCLK} + 100 ns 4 T_{MCLK} + 100 ns	
T_{WHDV}	WR# High ti Output Data Valid on Port 1/2	T_{MCLK}	2 T_{MCLK} + 100 ns	
T_{COPO}	CLKOUT Period	(CD_V+1) * T_{OSC} (3)		
T_{CHCL}	CLKOUT High Period	(CD_V+1) * ½T_{OSC} –10	(CD_V+1) * ½T_{OSC} –15	

NOTES:

References to WR# also pertain to WRH#.

1. Definition of “read cycle without a previous write”: The time between the rising edge of WR#/WRH# (for the previous write cycle) and the falling edge of RD# (for the current read cycle) is greater than 2 T_{MCLK}.
2. Definition of “write cycle with a previous write'”. The time between the rising edge of WR#/WRH# (for the previous write cycle) and the rising edge of WR#/WRH# (for the current write cycle) is less than 2 T_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Figure 3. 82527 - *Express* System Timings (Modes 0, 1)

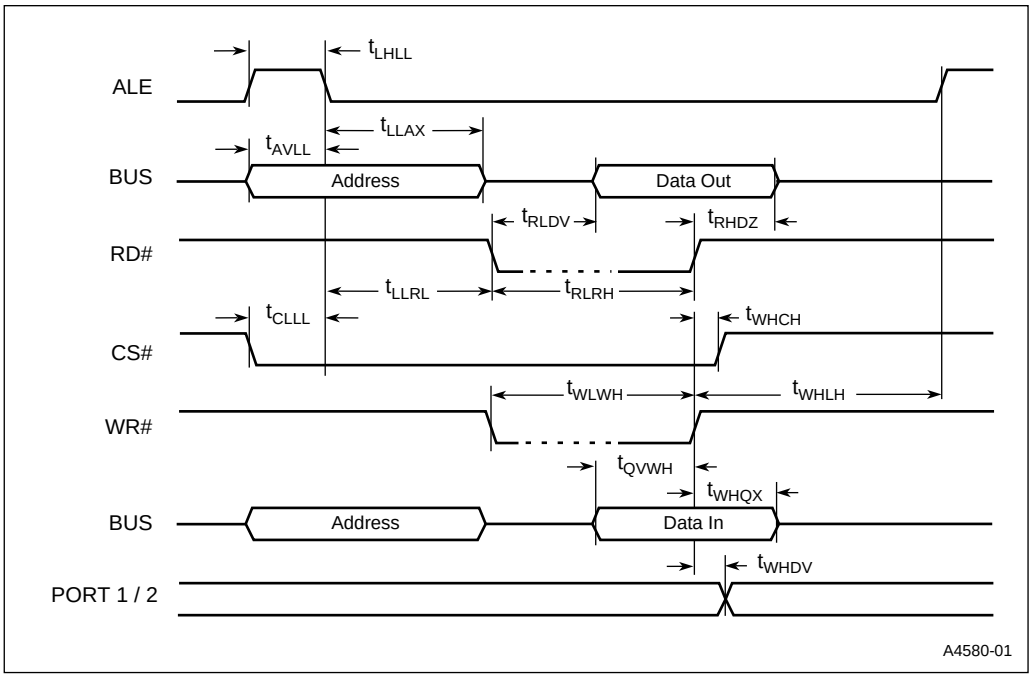


Figure 4. Ready Output Timing for a Write Cycle if No Previous Write is Pending (Modes 0, 1)

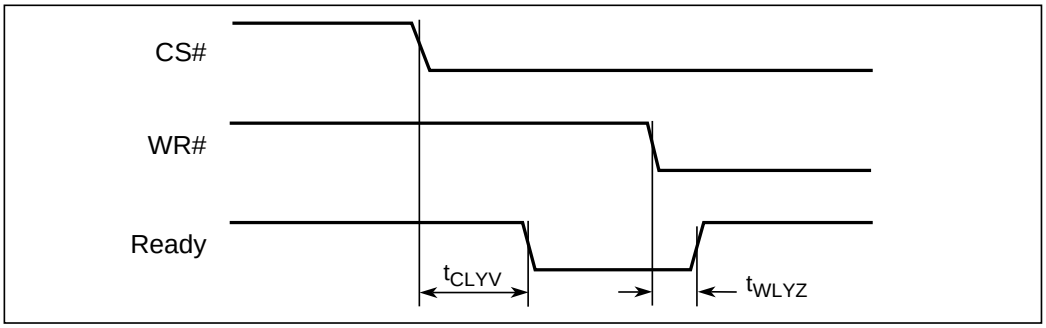


Figure 5. Ready Output Timing for Write Cycle if Previous Write Cycle is Active (Modes 0, 1)

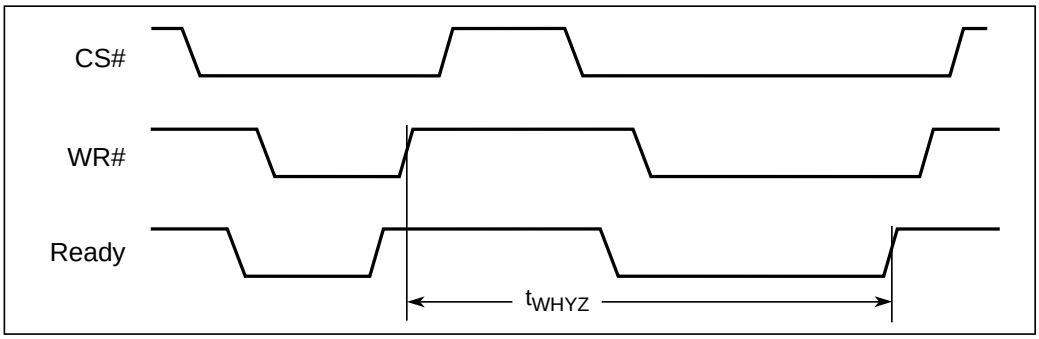
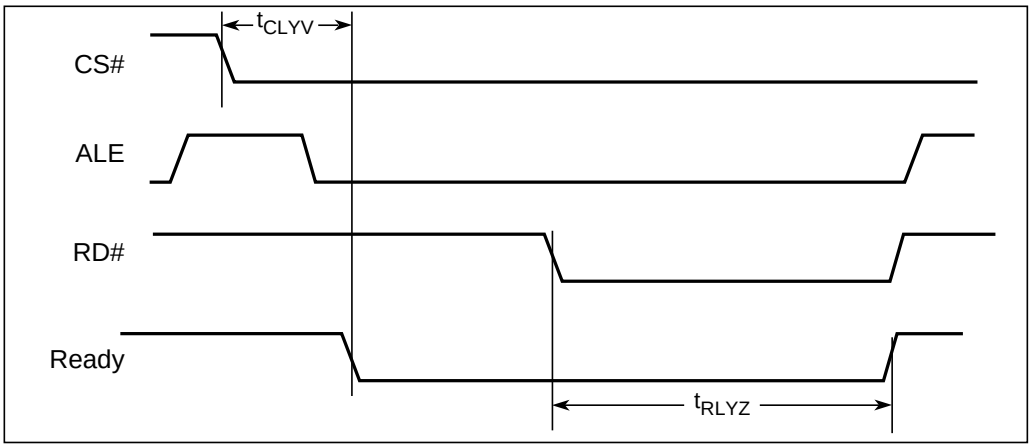


Figure 6. Ready Output Timing for Read Cycle (Modes 0, 1)



3.4.2 8-Bit Multiplexed Non-Intel Mode (Mode 2)

Operating Conditions::

- V_{CC} = 5 V ±10%
- V_{SS} = 0 V
- T_A = –40°C to +85ºC
- C_L = 100 pF

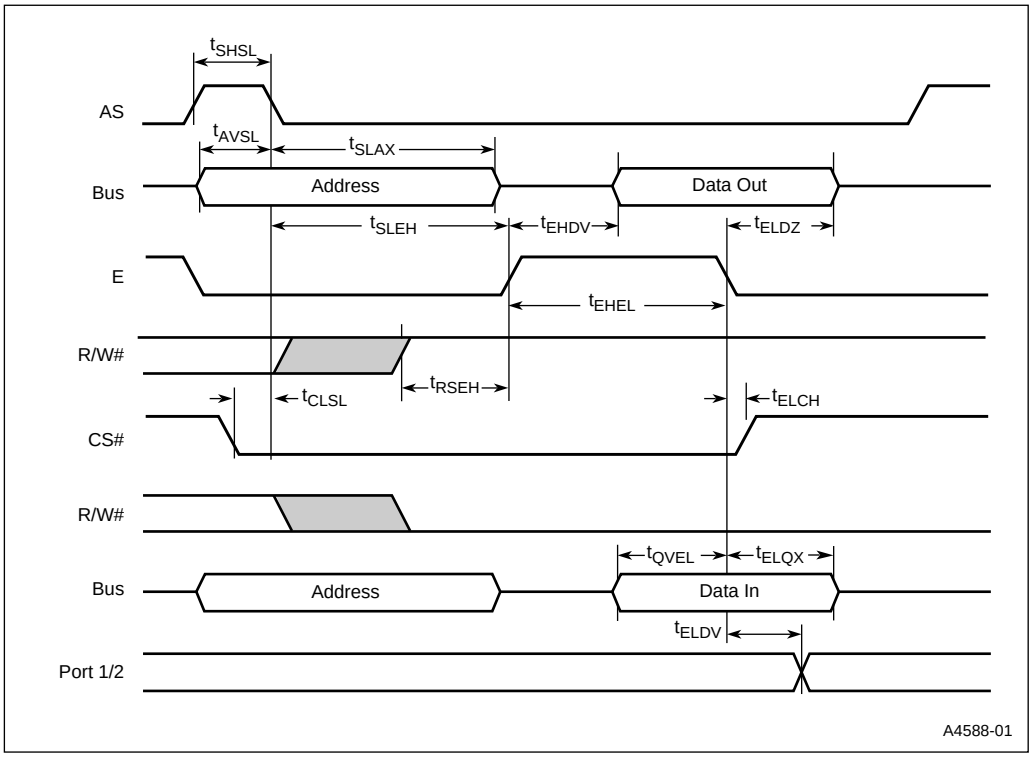
Table 7. AC Characteristics 8-Bit Multiplexed Non-Intel Mode (Mode 2)

Symbol	Parameter	Min	Max
$1/T_{XTAL}$	Oscillator Frequency	8 MHZ	16 MHz
$1/T_{SCLK}$	System Clock Frequency	4 MHZ	10 MHZ
$1/T_{MCLK}$	Memory Clock Frequency	2 MHZ	8 MHZ
T_{AVLL}	Address Valid to AS Low	7.5 ns	
T_{SLAX}	Address Hold after AS Low	10 ns	
T_{ELDZ}	Data Float after E Low	0 ns	45 ns
T_{EHDV}	E High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	for Read Cycle without a Previous Write (1) for Read Cycle with a Previous Write (for Registers except for 02H, 04H, 05H)		1.5 T_{MCLK} + 100 ns 3.5 T_{MCLK} + 100 ns
T_{QVEL}	Data Setup to E Low	30 ns	
T_{ELQX}	Input Data Hold after E Low	20 ns	
T_{ELDV}	E Low to Output Data Valid on Port 1/2	T_{MCLK}	2 T_{MCLK} + 500 ns
T_{EHEL}	E High Time	45 ns	
T_{ELEL}	End of Previous Write (Last E Low) to E Low for a Write Cycle	2 T_{MCLK}	
T_{SHSL}	AS High Time	30 ns	
T_{RSEH}	Setup Time of R/W# to E High	30 ns	
T_{SLEH}	AS Low to E High	20 ns	
T_{CLSL}	CS# Low to AS Low	20 ns	
T_{ELCH}	E Low to CS# High	0 ns	
T_{COPD}	CLKOUT Period	(CD_V+1) * T_{OSC} (3)	
T_{CHCL}	CLKOUT High Period	(CD_V+1) * ½T_{OSC} – 10	(CD_V+1) * ½T_{OSC} + 15

NOTES:

1. Definition of “Read Cycle without a Previous Write”: The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 T_{MCLK}.
2. Definition of “Write Cycle with a Previous Write”'. The time between the falling edge of E (for the previous write cycle) and the falling edge of E (for the current write cycle) is less than 2 T_{MCLK}.
3. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Figure 7. 82527 - *Express* System Bus Timing (Mode 2)



3.4.3 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)

Operating Conditions:

- V_{CC} = 5 V ±10%
- V_{SS} = 0 V
- T_A = –40°C to +85ºC
- C_L = 100 pF

Table 8. AC Characteristics 8-Bit Non-Multiplexed Asynchronous Mode (Mode 3)

Sym	Parameter	Min	Max
$1/T_{XTAL}$	Oscillator Frequency	8 MHZ	16 MHz
$1/T_{SCLK}$	System Clock Frequency	4 MHZ	10 MHZ
$1/T_{MCLK}$	Memory Clock Frequency	2 MHZ	8 MHZ
T_{AVLL}	Address or R/W# Valid to CS# Low Setup	3 ns	
T_{CLDV}	CS# Low to Data Valid for High Speed Registers (02H, 04H, 05H)	0 ns	55 ns
	For Low Speed Registers (Read Cycle without Previous Write) (1)	0 ns	1.5 T_{MCLK} + 100 ns
	For Low Speed Registers (Read Cycle with Previous Write) (1)	0 ns	3.5 T_{MCLK} + 100 ns
T_{KLDV}	DSACK0# Low to Output Data Valid for High Speed Read Register		23 ns
	For Low Speed Read Register	< 0 ns	
T_{CHDV}	82527 Input Data Hold after CS# High	15 ns	
T_{CHDH}	82527 Output Data Hold after CS# High	0 ns	
T_{CHDZ}	CS# High to Output Data Float		35 ns
T_{CHKH1}	CS# High to DSACK0# = 2.4V (3)	0 ns	55 ns
T_{CHKH2}	CS# High to DSACK0# = 2.8V		150 ns
T_{CHKZ}	CS# High to DSACK0# Float	0 ns	100 ns
T_{CHCL}	CS# Width between Successive Cycles	25 ns	
T_{CHAI}	CS# High to Address Invalid	7 ns	
T_{CHRI}	CS# High to R/W# Invalid	5 ns	
T_{CLCH}	CS# Width Low	65 ns	
T_{DVCH}	CPU Write Data Valid to CS# High	20 ns	
T_{CLKL}	CS# Low to DSACK0# Low for High Speed Registers and Low Speed Registers Write Access without Previous Write (2)	0 ns	67 ns
T_{CHKL}	End of Previous Write (CS# High) to DSACK0# Low for a Write Cycle with a Previous Write (2)	0 ns	2 T_{MCLK} + 145 ns
T_{COPD}	CLKOUT Period	(CD_V+1) * T_{OSC} (4)	
T_{CHCL}	CLKOUT High Period	(CD_V+1) * ½T_{OSC}–10	(CD_V+1) * ½T_{OSC}+15

NOTES:

E and AS must be tied high in this mode.

1. Definition of “Read Cycle without a Previous Write”: The time between the rising edge of CS# (for the previous write cycle) and the falling edge of CS# (for the current read cycle) is greater than 2 T_{MCLK}.
2. Definition of “Write Cycle with a Previous Write”'. The time between the rising edge of CS# (for the previous write cycle) and the rising edge of CS# (for the current write cycle) is less than 2 T_{MCLK}.
3. An on-chip pullup will drive DSACK0# to approximately 2.4 V. An external pullup is required to drive this signal to a higher voltage.
4. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Figure 8. Timing of the Asynchronous Mode Read Cycle (Mode 3)

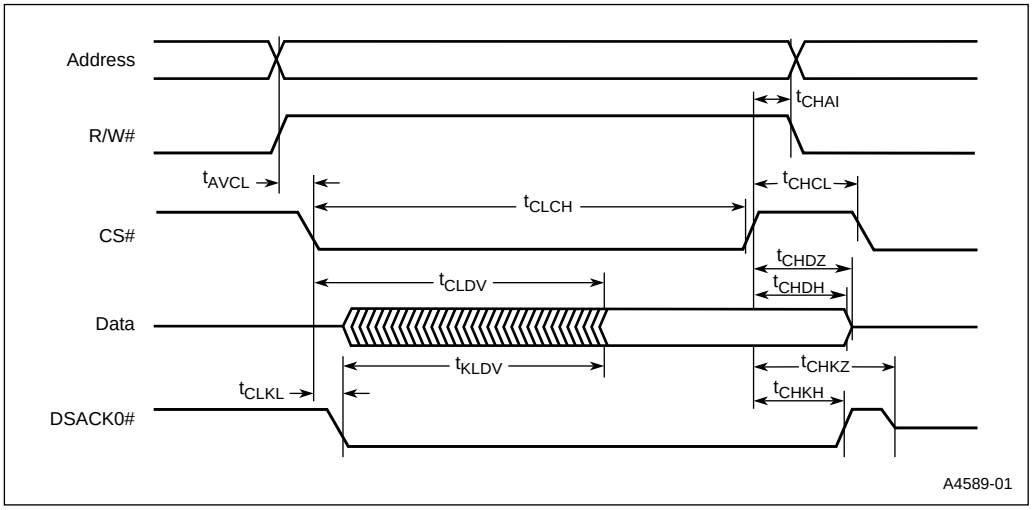
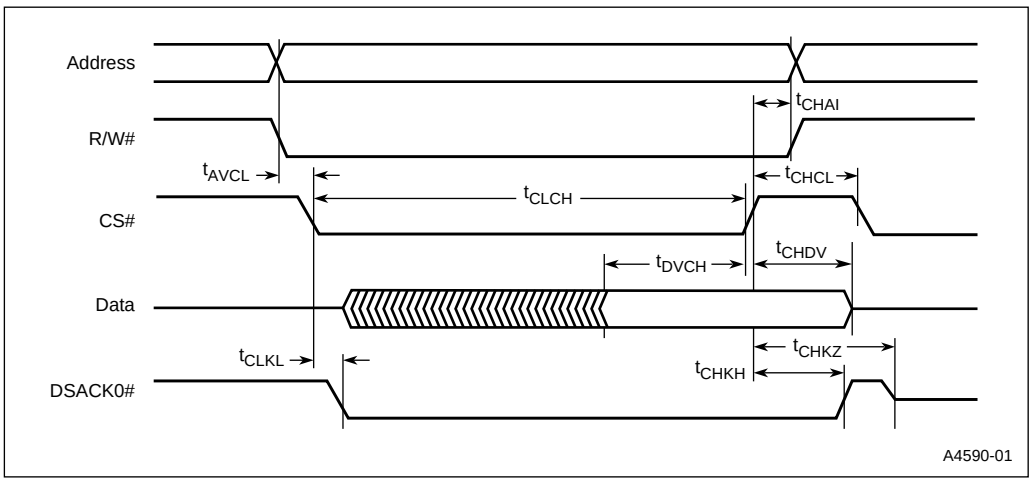


Figure 9. Timing of the Asynchronous Mode Write Cycle (Mode 3)



3.4.4 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Operating Conditions:

- V_{CC} = 5 V ±10%
- V_{SS} = 0 V
- T_A = –40°C to +85ºC
- C_L = 100 pF

Table 9. AC Characteristics 8-Bit Non-Multiplexed Synchronous Mode (Mode 3)

Sym	Parameter	Min	Max
$1/T_{XTAL}$	Oscillator Frequency	8 MHZ	16 MHz
$1/T_{SCLK}$	System Clock Frequency	4 MHZ	10 MHZ
$1/T_{MCLK}$	Memory Clock Frequency	2 MHZ	8 MHZ
T_{EHDV}	E High to Data Valid out of High Speed Register (02H, 04H, 05H)		55 ns
	Read Cycle without Previous Write for Low Speed Registers(1)		1.5 T_{MCLK} + 100 ns
	Read Cycle with Previous Write for Low Speed Registers(1)		3.5 T_{MCLK} + 100 ns
T_{ELDH}	Data Hold after E Low for a Read Cycle	5 ns	
T_{ELDZ}	Data Float after E Low		35 ns
T_{ELDV}	Data Hold after E Low for a Write Cycle	15 ns	
T_{AVEH}	Address and R/W# to E Setup	25 ns	
T_{ELAV}	Address and R/W# Valid after E Falls	15 ns	
T_{CVEH}	CS# Valid to E High	0 ns	
T_{ELCV}	CS# Valid after E Low	0 ns	
T_{DVEL}	Data Setup to E Low	55 ns	
T_{EHEL}	E Active Width	100 ns	
T_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 T_{MCLK}	
T_{AVCL}	Address or R/W# to CS# Low Setup	3 ns	
T_{CHAI}	CS# High to Address Invalid	7 ns	
T_{COPD}	CLKOUT Period	(CD_V+1) * T_{OSC} (2)	
T_{CHCL}	CLKOUT High Period	(CD_V+1) * ½T_{OSC}–10	(CD_V+1) * ½T_{OSC}+15

NOTES:
1. Definition of “Read Cycle without a Previous Write”: The time between the falling edge of E (for the previous write cycle) and the rising edge of E (for the current read cycle) is greater than 2 T_{MCLK}.
2. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Figure 10. Timing of the Synchronous Read Cycle (Mode 3)

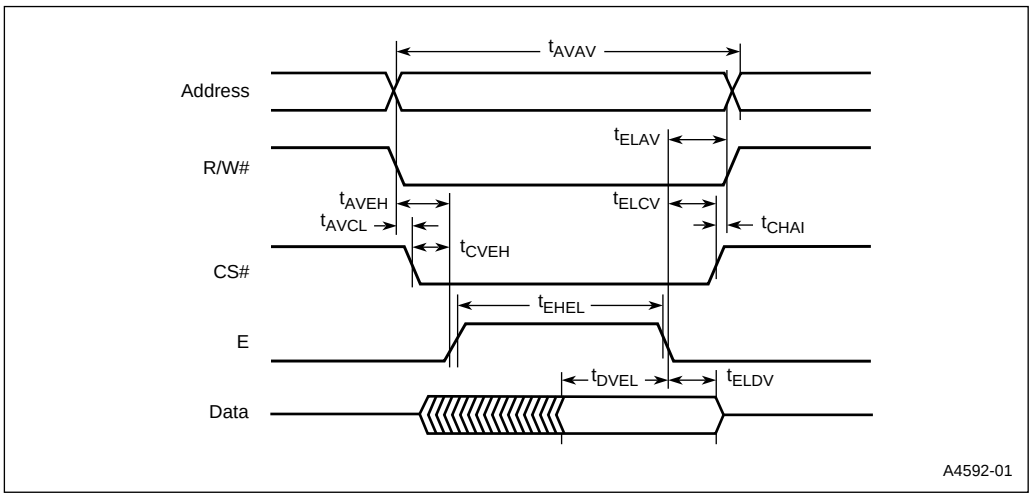
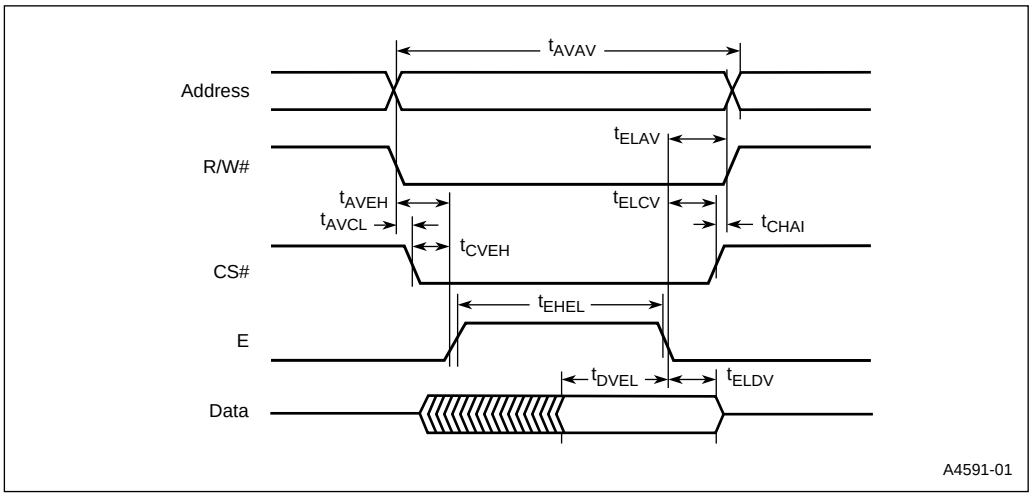


Figure 11. Timing of the Synchronous Write Cycle (Mode 3)



3.4.5 Serial Interface Mode

Operating Conditions:

- V_{CC} = 5.0 V ±10%
- V_{SS} = 0 V
- T_A = –40°C +85°C
- C_L = 100 pF

Table 10. AC Characteristics for Serial Interface Mode

Sym	Parameter	Min	Max
$1/T_{MCLK}$	SPI Clock	0.5 MHZ	8 MHZ
T_{ELDH}	1/SCLK	125 ns	2000 ns
T_{ELDZ}	Minimum Clock High Time	84 ns	
T_{ELDV}	Minimum Clock Low Time	84 ns	
T_{AVEH}	ENABLE Lead Time	70 ns	
T_{ELAV}	Enable Lag Time	109 ns	
T_{CVEH}	Access Time		60 ns
T_{ELCV}	Maximum Data Out Delay Time		59 ns
T_{DVEL}	Minimum Data Out Hold Time	0 ns	
T_{EHEL}	Maximum Data Out Disable Time		665 ns
T_{AVAV}	Minimum Data Setup Time	35 ns	
T_{AVCL}	Minimum Data Hold Time	84 ns	
T_{CHAI}	Maximum Time for Input to go from V_{OL} to V_{OH}		100 ns
T_{CHAI}	Maximum Time for Input to go from V_{OH} to V_{OL}		100 ns
T_{CHAI}	Minimum Time between Consecutive CS# Assertions	670 ns	
T_{COPD}	CLKOUT Period	$(CD_V+1) * T_{OSC}$ (1)	
T_{CHCL}	CLKOUT High Period	$(CD_V+1) * ½T_{OSC}–10$	$(CD_V+1) * ½T_{OSC}+15$

NOTE:
1. Definition of CD_V is the value loaded in the CLKOUT register representing the CLKOUT divisor.

Figure 12. Serial Interface Mode (Priority = 0, Phase = 0)

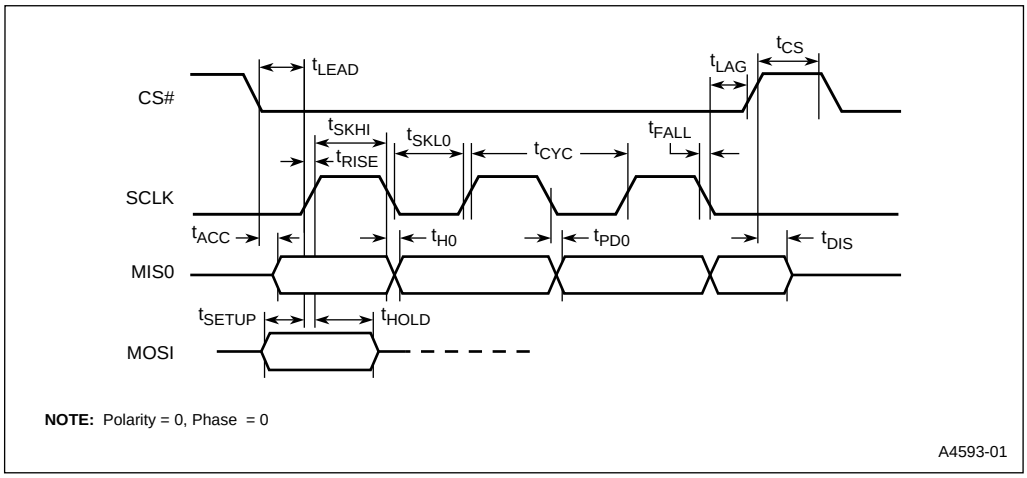
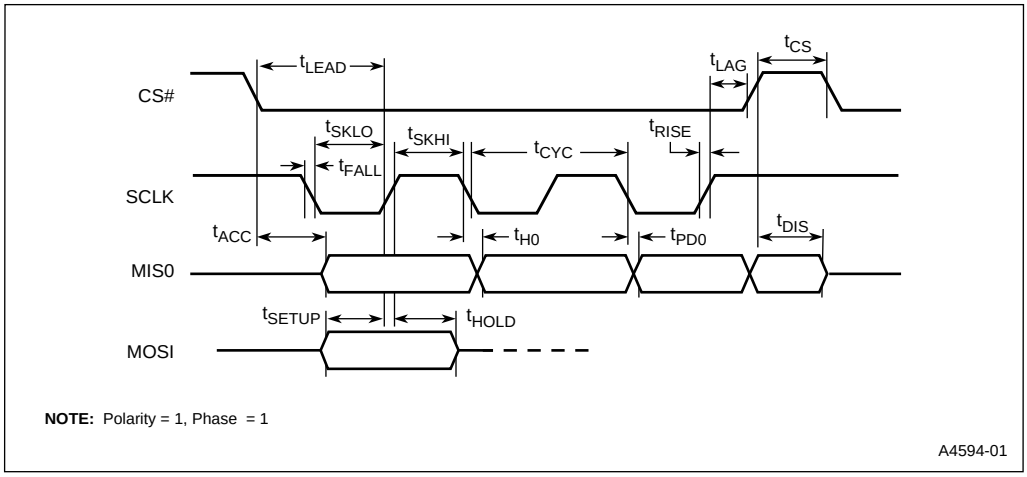
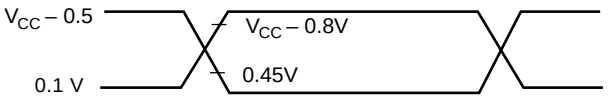


Figure 13. Serial Interface Mode (Priority = 1, Phase = 1)



3.4.6 AC Testing Input

Figure 1. Input, Output Waveforms



NOTE:
AC inputs during testing are driven at V_{CC} – 0.5V for a Logic "1" and 0.1V for a Logic "0". Timing measurements are made at V_{OH} Min for a Logic "1" and V_{OL} Max for a Logic "0".

A4598-01

4.0 DATASHEET REVISION HISTORY

This is the -001 revision of the "82527 - Express" datasheet.