80C32, 8xC52, 8xC54, 8xC58 SPECIFICATION UPDATE

Release Date: December, 1996
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The 80C32, 8XC52, 8xC54, 8xC58 may contan design defects or errors known as errata. Characterized errata that may cause the 80C32, 8XC52, 8xC54, 8xC58's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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France 44-0-1793-421-777, Germany 44-0-1793-421-333, other countries 708-296-9333

CONTENTS

REVISION HISTORY

Rev. Date	Version	Description
11/13/96	001	This is the first release of the Specification Update document. It contains all errata identified to this date.
12/11/96	002	Added specification clarification 001.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270646-008
MCS 51 Microcontroller Family User's Manual	272383-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings				Page	Status	ERRATA
	A	B	C	D			
							None for this revision of the specification update.

Specification Changes

Number	Steppings				Page	Status	SPECIFICATION CHANGES
	A	B	C	D			
001		X	X		7	Doc	New Icc Values in Active and Idle Modes (80C32, 80C52, 80C54)
002		X		X	7	Doc	Lock Bits Moved to UPROM to Enhance Security (87C52, 87C54, 87C58)

Specification Clarifications

Number	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A	B	C	D			
001	X	X	X	X	8	Doc	Port 1 and 3 Reset Values

Documentation Changes

Number	Steppings				Page	Status	ERRATA
	A	B	C	D			
							None for this revision of the specification update.

IDENTIFICATION INFORMATION

Markings

Microcontroller	Stepping	Identifier	Stepping	Identifier
80C32	A	A	C	F
80C52	A	A	C	F
87C52	D	A		
80C54	B	B		
87C54	B	B		
80C58	B	M		
87C58	B	B		

ERRATA

None for this revision of the specification update.

SPECIFICATION CHANGES

001. New Icc Values in Active and Idle Modes (80C32, 80C52, 80C54)

PROBLEM: The 80C32, 80C52, and 80C54 have new maximum and typical values for Icc in Active and Idle Modes.

IMPLICATION: Your design must take these values into consideration.

Frequency (MHz)	Active Mode		Idle Mode	
	Maximum Icc (mA)	Typical Icc (mA)	Maximum Icc (mA)	Typical Icc (mA)
12	25 (was 30)	14.5 (was 15)	9.5 (was 7.5)	8 (was 5)
16	30 (was 38)	18 (was 20)	11.5 (was 9.5)	9.5 (was 6)
24	40 (was 56)	24.5 (was 28)	15.5 (was 13.5)	11.5 (was 7)
33	45 (was 56)	32.5 (was 35)	17 (was 15)	13.5 (was 7)

002. Lock Bits Moved to UPROM to Enhance Security (87C52, 87C54, 87C58)

PROBLEM: To enhance security, the lock bits have been moved from EPROM to UPROM. The UPROM is a secure area on the device; values written to UPROM cannot be changed. The function of the lock bits, the method for programming them, and the use of the encryption array remain unchanged.

IMPLICATION: Verify that your EPROM code is correct before setting any lock bits. Because the lock bits are in UPROM, the lock bits cannot be changed after they are programmed once. If you set only LB1, you can still verify your code, but you cannot reprogram the EPROM (althought you can still erase it using ultraviolet light). If you set LB2, you can no longer verify the EPROM code.

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

SPECIFICATION CLARIFICATIONS

001. Port 1 and 3 Reset Values

PROBLEM: The reset value of all ports is logic “1”; however, the reset value of ports 1 and 3 is sustained by a weak pull-up. It is recommended that applications **not** use the reset value of these ports to drive external loads. If the application requires the use of the reset value of these ports, an external pull-up resistor should be added.

DOCUMENTATION CHANGES

None for this revision of the specification update.