8XC152JX
SPECIFICATION UPDATE

Release Date: July, 1996

Order Number: 272882-001

The 8XC152JX may contain design defects or errors known as errata. Characterized errata that may cause the 8XC152JX's behavior to deviate from published specifications are documented in this specification update.

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REVISION HISTORY

Date of Revision	Version	Description
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the first release of the 8XC152JX Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270646-008
MCS® 51 Microcontroller Family User's Manual	272383-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 8XC152JX product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	B	C	#			
9600001	X	--		7	Fixed	SDLC Flag Recognition Failure Mode
9600002	X	--		8	Fix	Global Serial Channel Failure Mode
9600003	X	--		9	Fix	External Demand DMA Failure Mode
9600004	X	--		11	Fix	DMA Failure Mode

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	B	C	#			
001	X	--		13		Interframe Space
002	X	--		13		NRZI Decoding
003	X	--		14		Global Serial Channel

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

Special identifier of C-stepping for both PDIP and PLCC packages with marking of FFFFFFFFC.

ERRATA

9600001. SDLC Flag Recognition Failure Mode (B-step devices)

PROBLEM: The C152 device does not properly recognize an SDLC flag. SDLC defines a flag to be a 0, followed by six 1s, followed by a 0 (01111110). The C152 recognizes any sequence of 6 or more consecutive 1s followed by a 0 to be a flag. In NRZI, a transition is a 0 and the lack of a transition is a 1. In most SDLC networks, the faulty flag recognition circuitry will not pose a problem, as the first transition following an idle condition is the beginning of a flag. There will only be a problem if the C152 is used in a network where the actual Beginning Of Frame (BOF) flag is preceded by transitions that meet the following criteria:

1. The first transition is preceded by at least six 1s. This is typical, as most frames are preceded by an idle condition, which is 15 consecutive 1s.
2. At least 17 (or 33) bit times elapse between the first transition and the BOF. The 17 or 33 bit times are determined by the length of the selected CRC which can be 16 or 32 bits.
3. During the 17 (or 33) bit times, an abort or flag is not encountered.
4. The pattern following the initial transition (the first 0) can be accepted as a valid address. The following description identifies which patterns will be accepted as valid addresses.

Patterns that can be accepted as a valid address are:

1. The address assigned by the user. The address length can be 8 or 16 bits.
2. A broadcast address consisting of all 1s with the appropriate 0s inserted. The pattern 11111111 would be an abort, the pattern 0111110111 would be an 8-bit broadcast address.
3. Any data pattern if the address recognition circuitry is defeated by writing all 1s to the address mask registers.
4. All patterns that would present a valid address when compared against the assigned address registers combined with the address mask registers.

IMPLICATION: If the C152 erroneously accepts the type of data described here, a CRC error will be indicated when the real BOF is received. In addition, the alignment error bit will probably be set.

WORKAROUND: Software workarounds are feasible but must be determined on a case-by-case basis. Workarounds are not necessary unless all of the preceding conditions may occur. To implement any software workaround, the GAREN bit in PCON must be set. Setting GAREN keeps the receiver enabled after an End Of Frame (EOF) flag or Receive error. This allows the data following the real BOF to be loaded into the receive FIFO. To keep the receive buffer from being overwritten the data must be transferred to another buffer in a timely manner. This is only the first step in whichever workaround is implemented and the user must still determine whether the CRC error is real or a result of this bug.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600002. Global Serial Channel Failure Mode (B-step devices)

PROBLEM: In Global Serial Channel on the 8XC152, RFIFO pointers are not reset when GREN is set. Since the pointers are not reset, RFNE will not be cleared (the error bits will still be reset).

IMPLICATION: Error bits remain reset when GREN is set.

WORKAROUND: The fact that the RFIFO pointers are not reset can be worked around by checking RFNE every time GREN is set. If RFNE = 1, the data must be emptied out under program control as shown in the example below. The emptying of RFIFO must be completed before 24 (40) bit times have elapsed when using the 16 (32) bit CRC. One method of doing this is to move the data into the accumulator. All discussions talking about the users manual also applies to the hardware description found in the ECO handbook. An example of the software that would be executed is:

```
ENABLE_RECEIVER:
        CLR EA
        SETB GREN

CLEAR_RFIFO_LOOP:
        JNB RFNE, CONTINUE
        MOV A,RFIFO
        JMP CLEAR_RFIFO_LOOP

CONTINUE:
        SETB EA
        (USER PROGRAM)
```

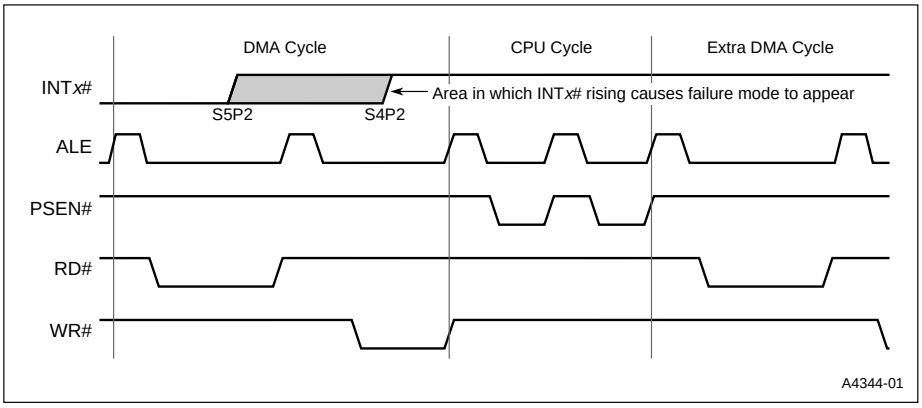
STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600003. External Demand DMA Failure Mode (B-step devices)

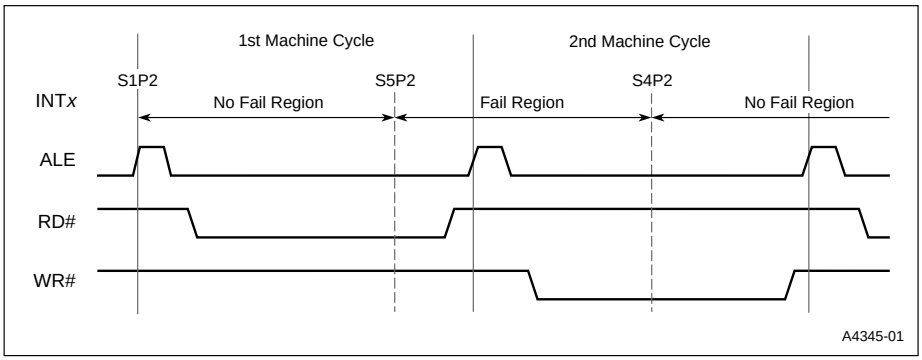
PROBLEM: On the 8XC152JA/JB/JC/JD, a failure mode occurs by using either DMA channel in level-sensitive, external demand mode. If, after a transfer begins, the INTx pin goes high between S5P2 and S4P2 of a DMA cycle, an extra DMA transfer will take place.

IMPLICATION: The condition above applies to all single-machine-cycle transfers. All DMA transfers take one machine cycle except the external-external transfer which takes two. For this mode, the bug appears only if INTx goes high between S5P2 of the first machine cycle, and S4P2 of the second.

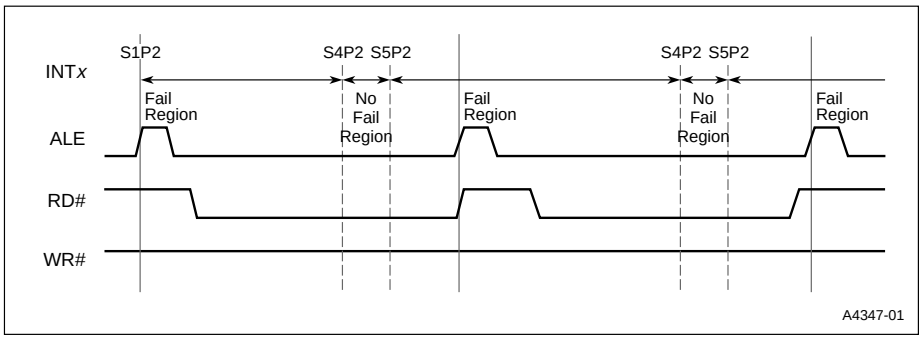
WORKAROUND: At this point there are no known software or hardware workarounds. The following diagram gives a graphical description of the anomaly.



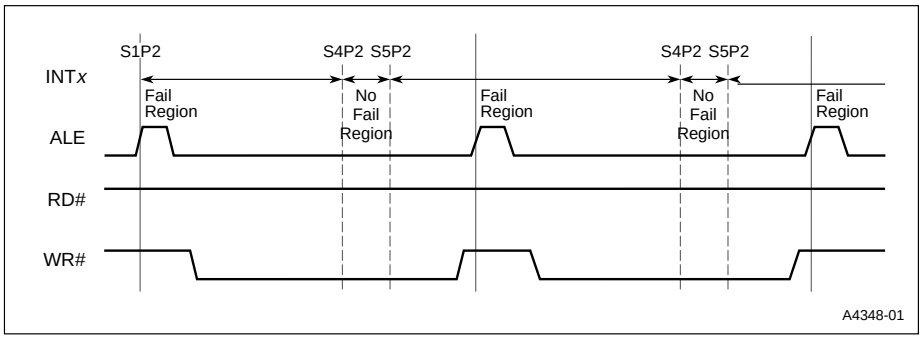
The diagrams below illustrate the areas of a DMA transfer during which the rising edge of the INTx pin will and will not cause the bug to appear. Each of the four transfer modes are shown.



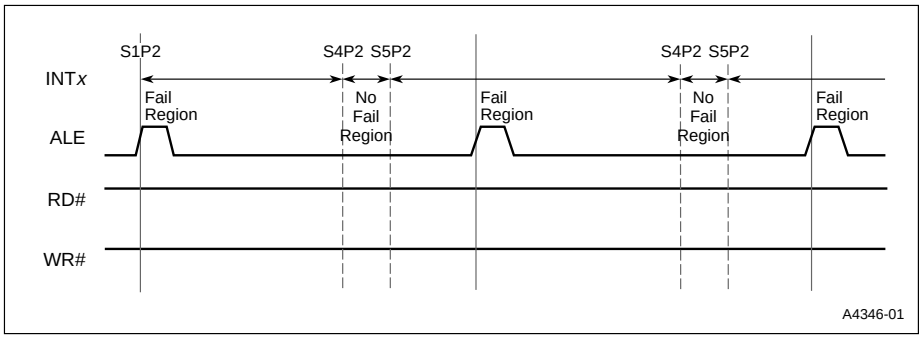
External to External Transfer (1 Transfer Shown)



External to Internal Transfer (2 Transfers Shown)



Internal to External Transfer (2 Transfers Shown)



Internal to Internal Transfer (2 Transfers Shown)

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

9600004. DMA Failure Mode (B-step devices)

PROBLEM: A failure mode on the 8XC152JA/JB/JC/JD shows up as the source address registers of the DMA0 or DMA1 getting overwritten with zeros. It occurs under the following scenario. A DMA1 request is denied by a CPU DMA register access. As DMA1 waits for completion of the register access instructions, a DMA0 request comes in. Because the DMA0 channel has higher priority, the CPU grants its request first. When the CPU grants the DMA0 request, the source address registers will get overwritten with zeros.

After extensive lab testing, the conditions under which the bug will occur were limited to the following:

DMA0 --> Servicing TFIRO/RFIFO
DMA1 --> Servicing RFIFO/TFIFO
Both DMA channels in serial port demand mode, no auto increment
Protocol --> Full duplex SDLC
Baud rate --> Maximum
GSC simultaneously transmitting and receiving causing both DMA channels to be active. While both channels are active, the CPU accesses any DMA register.

These conditions may not always generate the problem. The bug is very dependent on voltage and temperature. At room temperature V_{cc} has to be about 4.2V for the bug to appear. At temperatures around 70C, V_{cc} has to be approximately 5V for the problem to occur.

IMPLICATION: There may be other conditions under which the bug may appear. However after testing numerous software and hardware configurations, no conditions other than those listed above caused the problem to occur.

WORKAROUND: There is a software workaround for the bug. Do not execute any instruction involving a DMA register while both DMAs are active. While this workaround is probably the most straight-forward, some applications require CPU access to DMA registers during a DMA cycle. To satisfy this requirement, another workaround is available. Always follow a CPU DMA register access (while both DMAs are active) with a NOP instruction. This will also prevent the problem from occurring.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

001. Interframe Space (B-step devices)

PROBLEM: The following is an explanation of how to minimize the effects of the interframe space while in SDLC mode. Further explanation of the interframe space is in section 3.2.3 of the 1994 83C152 Hardware Description Manual.

The interframe space is a period of time that all stations are prevented from transmitting after any activity on the serial communication link is detected. The purpose of this waiting period is to give time for a receiver to recover from a previously received frame. The reason for implementing this change was to better support ISDN applications. For those users that do not want to use the interframe space in SDLC mode, the best they can do is to minimize its impact by programming the special function register, IFS, with 02. IRS can only be loaded with even numbers, so 1 cannot be used. After a reset, IFS defaults to 00H which translates into a 256 bit time interframe space. Loading IFS with 02 will prevent a transmission from starting until two bit times after an idle condition on the serial link is detected. An idle condition is defined as a constant 1 on the link for 15 bit times when SDLC mode is selected.

C152 users that have implemented the external GSC clock option on the C152 must be informed that at least 17 clocks must occur after any activity on the link before the next transmission will begin. If an external clock cannot fulfill these requirements, a workaround must be implemented. One way to do this is to switch to the internal baud rate generator after any link activity. The internal clock must be enabled for at least 18 bit times before switching back to external clock mode.

002. NRZI Decoding (B-step devices)

PROBLEM: The way NRZI decoding is described in the 8XC152 Hardware Description is as follows:

"pulses less than four sample periods are ignored, and assumed to be noise."

This statement is true, but could be confusing to some readers. In SDLC mode, the C152 receive pin is sampled at 8 times the bit rate. One could assume that with the above statement, pulses less than 1/2 bit time would be ignored. This is wrong. It turns out that a pulse that is between 3/8 and 1/2 bit time in duration may or may not be sampled 4 times. This is because it takes only 3/8 of a bit time for 4 samples to occur. In the C152, it is indeterminate how a pulse that is 3/8 to 1/2 a bit time will be decoded.

This problem is particularly apparent when interfacing to an 8044 in a network where line drivers are being used. Waveforms produced by the 8044 fall within the range of 3/8 to 1/2 bit time when an 8044 is responding to a master SDLC controller. When this occurs, the C152 may decode the incoming bit stream as random addresses which might match the C152s assigned address.

Currently, there are no specific work-workarounds. Not all 8044 users will have a problem. The customer must look at the waveforms produced by the 8044 in his network to determine if a problem exists. The flag recognition should also be examined for possible consequences.

003. Global Serial Channel (B-step devices)

PROBLEM: The areas that need clarification are: Clearing GREN; Clearing AGREN; Clearing TEN; Multiple error bits getting set; Instruction sequence when using external GSC clocks, Timing of DEN#, and Clearing RFIFO/TFIFO.

- **Clearing GREN.** It turns out that if GREN is cleared after a reception has started the GSC acts as though the reception has ended. The C152 then goes through the process of checking for alignment and CRC errors, which will most likely occur causing error bits to be set many instructions after GREN was initially cleared. This can result in GSC error interrupts, which in turn, will interfere with the user program at a time when the user may assume that no interrupts can occur. This is especially likely when using an extremely low GSC bit rate, as the error conditions are checked on the first clock after GREN is cleared.

  Currently, the only fix for this problem is not to clear GREN when a reception is taking place. One method of identifying when a reception is occurring is to examine the status of LNI. If LNI = 1, GREN can be cleared. If LNI = 0, GREN should not be cleared. It turns out that the timing is such that if GREN is cleared on the twenty-third clock after the first address bit (with 16-bit CRC selected) the transfer to RFIFO occurs on the twenty-fourth clock and the error bits will be set, even thought GREN has been set to zero. It takes 0 to 1 bit times before the internal receive enable becomes inactive after GREN is cleared.

- **Clearing AGREN.** If both AGREN and GREN are set, clearing only one bit and not the other will not disable the receiver. After both bits are cleared, up to one bit time must transpire before the receiver is actually disabled.

- **Clearing TEN.** It takes 0 to one bit times before the internal transmit enable becomes inactive after clearing TEN. This means that after clearing, TEN, the transmitter may remain active for up to one bit time. Those users that are externally clocking the transmitter must take into account the extra clock required to disable the transmitter.
- **Multiple Error Bits Set.** Although not specifically explained in the C152 users manual, it has been shown that multiple error bits, some erroneously, are getting set. This has been seen to occur in CSMA/CD mode only, but may also exist in all modes. Combinations that have shown up in lab experiments are:
- When an abort is simulated, both RCABT and AE bits are set. Depending on when the abort occurs, the misalignment may be a valid error.

  When an alignment error is simulated, both AE and CRCE bits are set. In most cases, when an alignment error occurs, the CRC will likely be wrong. If CRCE is set, it is probably an indication of a valid error. When an overrun error is forced, OVR, AE, and CRCE bits are set. There was no alignment error or CRC bits are set. There was no alignment error or CRC error contained in the transmitted packet.

  If the correct cause of the receiver error must be known, a specific polling sequence should be followed. This sequence is:

  Check RCABT
  Check OVR
  Check CRCE
  Check AE

- **Sequence of Enabling External GSC Clocks.** To enable the use of an external clock with the GSC, there are two bits that must be set, XTCLK and XRCLK. XTCLK is in GMOD and XRCLK is in PCON. It is imperative that SDLC mode is chosen by default (PR = 0). If XRCLK is set before Pr - 1, the C152 would be placed in a mode equivalent to “external receiver clock while in CSMA/CD mode”. This is expressly prohibited in the users manual. The XTCLK bit is in GMOD, as well as the PR bit. In this case, external transmit clock can be set in the same instruction that selects the SDLC protocol (PR = 1) when GMOD is initialized. After SDLC is selected, XRCLK in PCON may be set.

- **DEN# TIMING.** The DEN# timing was changed in the B-step. The timing is such, that DEN# will be actively driven low for two bit times after the last bit of the CRC is transmitted. This is to ensure that the EOF (idle condition for two bit times) is recognized by all stations on the link if an external driver is used. By extending the time DEN# will be low, the user can be assured that the driver will be enabled during the EOF.
- **CLEARING RFIFO/TFIFO.** The hardware description and users manual refer to “clearing RFIFO” or “clearing TFIFO” when GREN is set, TEN is set, or the data is read out. What actually occurs is that the data is not cleared out but the pointers used to reflect the status of the FIFOs are updated. This is a subtle difference, but one that will affect some users, especially those users concerned with the bug shown in the beginning of this tech bit.

DOCUMENTATION CHANGES

None for this revision of this specification update.