8xC51FA, 8xC51FB, 8xC51FC SPECIFICATION UPDATE

Release Date: January, 1997
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The 8xC51FA, 8xC51FB, 8xC51FC may contain design defects or errors known as errata. Characterized errata that may cause the 8xC51FA, 8xC51FB, 8xC51FC's behavior to deviate from published specifications are documented in this specification update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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REVISION HISTORY

Rev. Date	Version	Description
07/01/96	001	This is the original Specification document. It contains all errata identified to this date.
11/13/96	002	Combined the 8XC51FA, 8XC51FB, and 8XC51FC Specification Updates. This document covers the 80C51FA, 83C51FA, 87C51FA, 83C51FB, 87C51FB, 83C51FC, and 87C51FC. It replaces 272879-001, 272881-001, and 272883-001. Added specification changes 001 and 002. Clarified errata numbers 9600001 and 9600002 and specification clarifications 001–007.
12/11/96	003	Added specification clarification 008.

PREFACE

As of July, 1996, Intel has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

This document covers the 80C51FA, 83C51FA, 87C51FA, 83C51FB, 87C51FB, 83C51FC, and 87C51FC. It replaces 272879-001, 272881-001, and 272883-001.

Affected Documents/Related Documents

Title	Order
Embedded Microcontrollers	270648-008
MCS® 51 Microcontroller Family User's Manual	272383-002

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80C31BH, 80C51BH, 80C51BHP, 87C51 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings				Page	Status	ERRATA
	A	B	C	D			
9600001	X				7	Fixed	Port Anomaly (8XC51FC)
9600002	X				7	Fixed	PCA HSO, Software Timer, Timer 2 Baud-rate Generator Anomaly (80C51FA, 80C51FA-1, 83C51FA, 83C51FA-1)

Specification Changes

Number	Steppings				Page	Status	SPECIFICATION CHANGES
	A	B (FB, FC)	C	D (FA)			
001				X	8	Doc	New Icc Values in Active and Idle Modes (80C51FA, 83C51FA)
002		X		X	8	Doc	Lock Bits Moved to UPROM to Enhance Security (87C51FA, 87C51FB, 87C51FC)

Specification Clarifications (1 of 2)

Number	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A	B (FB, FC)	C	D (FA)			
001				X	9	Doc	Powerdown Compatibility with 8xC51BH (8xC51FA, 8xC51FB)
002		X		X	10	Doc	Timer 2 Clockout (8xC51FA, 8xC51FB)
003		X		X	11	Doc	Asynchronous Port Reset (8xC51FA, 8xC51FB)
004		X		X	11	Doc	Four Interrupt Priority Levels (8xC51FA, 8xC51FB)
005		X		X	12	Doc	Program Memory Lock (87C51FA, 87C51FB, 83C51FB)

Specification Clarifications (2 of 2)

Number	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A	B (FB, FC)	C	D (FA)			
006		X		X	13	Doc	EPROM Programming (87C51FA, 87C51FB, 83C51FB)
007		X		X	13	Doc	Signature Bytes (87C51FA, 87C51FB, 83C51FB)
008		X		X	14	Doc	Port 1 and 3 Reset Value

Documentation Changes

Number	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of the Specification Update

IDENTIFICATION INFORMATION

Markings

Microcontroller	Step	Identifier	Step	Identifier	Step	Identifier	Step	Identifier
8xC51FA	A	no mark	B	“A”	C	F	D	A
8xC51FB	A	no mark	B	“A”				
8xC51FC (PDIP, PLCC)	A	no mark	B	xxxxxxxxA				
8xC51FC (MQFP)	A	no mark	B	[M] [C] ‘80 B				

ERRATA

9600001. Port Anomaly (8XC51FC)

PROBLEM: Reset does not turn on the strong pullups on ports 1, 2, and 3. If any port pin is at a low state before reset, it may take several oscillator periods to be pulled up.

IMPLICATION: Additional oscillator periods are required for pullups after reset.

WORKAROUND: Because writing a '1' to a port pin turns on the strong pullup for two oscillator periods, a simple workaround is to write 0H followed by FFH to each port at the beginning of the program.

```
MOV P1,#0
MOV P1,#0FFH
MOV P2,#0
MOV P2,#0FFH
MOV P3,#0
MOV P3,#0FFH
```

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected steppings.

9600002. PCA HSO, Software Timer, Timer 2 Baud-rate Generator Anomaly (80C51FA, 80C51FA-1, 83C51FA, 83C51FA-1)

PROBLEM: When the programmable counter array (PCA) clock input is either Fosc/4 or an external clock and the PCA used for high-speed output (HSO) while another port 1 pin is also being toggled, the HSO output functions improperly. Instead of generating a constant square wave, a half-cycle transition is sporadically omitted and sometimes replaced by a momentary glitch. This malfunction occurs on all five PCA modules and is also seen in PCA software timer mode and Timer 2 baud-rate generator.

The problem does not occur if the program does not toggle another port 1 pin or if the clock input is either Fosc/12 or the Timer 0 overflow.

IMPLICATION: Designs using the PCA in HSO mode may experience unpredictable behavior.

WORKAROUND: None. However, designers can use either Fosc/12 or the Timer 0 overflow as the clock source for the PCA counter (which is slightly slower), or use the B-step (FX-core) 8XC51FA (which may be slightly more expensive).

STATUS: Fixed. Refer to Summary Table of Changes to determine the affected steppings.

SPECIFICATION CHANGES

001. New Icc Values in Active and Idle Modes (80C51FA, 83C51FA)

PROBLEM: The 80C51FA and 83C51FA have new maximum and typical values for Icc in Active and Idle Modes.

IMPLICATION: Your design must take these values into consideration.

Frequency (MHz)	Active Mode		Idle Mode	
	Maximum Icc (mA)	Typical Icc (mA)	Maximum Icc (mA)	Typical Icc (mA)
12	25 (was 30)	14.5 (was15)	11.5 (was 7.5)	10 (was 5)
16	30 (was 38)	18 (was 20)	13.5 (was 9.5)	11.5 (was 6)
24	40 (was 56)	24.5 (was 28)	17 (was 13.5)	13.5 (was 7)
33	45 (was 58)	32.5 (was 35)	17 (was 15)	15.5 (was 7)

002. Lock Bits Moved to UPROM to Enhance Security (87C51FA, 87C51FB, 87C51FC)

PROBLEM: To enhance security, the lock bits have been moved from EPROM to UPROM. The UPROM is a secure area on the device; values written to UPROM cannot be changed. The function of the lock bits, the method for programming them, and the use of the encryption array remain unchanged.

IMPLICATION: Verify that your EPROM code is correct before setting any lock bits. Because the lock bits are in UPROM, the lock bits cannot be changed after they are programmed once. If you set only LB1, you can still verify your code, but you cannot reprogram the EPROM (although you can still erase it using ultraviolet light). If you set LB2, you can no longer verify the EPROM code.

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

SPECIFICATION CLARIFICATIONS

001. Powerdown Compatibility with 8xC51BH (8xC51FA, 8xC51FB)

PROBLEM: The powerdown feature in the 8xC51FA and 8xC51FB differs slightly from that of the 8xC51BH (but identical to that of the 80C52). While the powerdown mode of the 8xC51BH can be terminated only by a valid reset, the 8xC51FA and 8xC51FB have been enhanced to allow the additional option of using an external reset to cause the microcontroller to exit powerdown mode. The interrupt must be configured for level-sensitive mode and it must be enabled before the controller enters powerdown mode.

If an 8xC51FA or 8xC51FB is replacing an 8xC51BH in a design, you will need to modify the software to disable the external interrupt before invoking powerdown mode. Disabling the interrupt prevents an unintentional exit from powerdown.

A problem can otherwise occur in a system designed for the 8xC51BH using powerdown mode with the following conditions:

- An external interrupt is configured for level-sensitive mode.
- The interrupt is enabled before the controller enters powerdown mode.
- The interrupt source remains active while the controller is in powerdown mode.

Under these circumstances, a low-level signal on the interrupt pin will start the oscillator and the rising edge of the same signal will cause the controller to exit powerdown mode.

002. Timer 2 Clockout (8xC51FA, 8xC51FB)

PROBLEM: A 50% duty-cycle clock output function has been added to P1.0. In addition to being a standard I/O pin, P1.0 has two alternate functions: it can input the external clock for timer/counter 2; or it can output a 50% duty-cycle clock ranging from 61 Hz to 4 MHz at operating frequencies up to 16 MHz.

To configure timer/counter 2 as a clock generator, clear the C/T2 bit in T2CON and set the T2OE bit in T2MOD. The TR2 bit in T2CON starts and stops the clock.

The frequency of the clock output depends on the oscillator frequency and the reload value of the Timer 2 capture registers (RCAP2H and RCAP2L), as shown in this equation:

$$\text{Clockout Frequency} = \frac{\text{Oscillator Frequency}}{4 \times (65536 - \text{RCAP2H, RCAP2L})}$$

003. Asynchronous Port Reset (8xC51FA, 8xC51FB)

PROBLEM: The D-step 8xC51FA and 8xC51FB microcontrollers feature an asynchronous port reset. For C-step controllers, the oscillator must be running and at least 19 oscillator periods must occur between the time that a logic 1 is applied to the RESET pin and the time that the port pins are driven to their reset states.

For D-step controllers, the oscillator need not be running. The port pins are driven to their reset states as soon as a valid logic 1 is applied to the RESET pin.

004. Four Interrupt Priority Levels (8xC51FA, 8xC51FB)

PROBLEM: The D-step 8xC51FA and 8xC51FB have a second interrupt-priority register (IPH), allowing four interrupt priority levels.

IPH Register — **Address: 0B7H** **Reset Value: X000 0000**

The interrupt priority high (IPH) register is the MSB of the priority selection bits and the interrupt priority low (IP) register is the LSB.

7							0
—	PPCH	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

The following table shows the bit values and priority levels associated with each combination.

Priority Bits		Interrupt Priority Level (0 is lowest; 3 is highest)
IPH.x	IP.x	
0	0	0
0	1	1
1	0	2
1	1	3

005. Program Memory Lock (87C51FA, 87C51FB, 83C51FB)

PROBLEM: The 87C51FA (D-step), 87C51FB (B-step), and 83C51FB (B-step) have three lock bits and 64-byte encryption arrays for program security. The following table lists the lock bits and their effect on the controller. Specification Clarification 006 on page 13 lists the signals required to program the lock bits and encryption array. Specification Change 002 on page 8 explains that the lock bits have been moved from EPROM to unerasable programmable ROM (UPROM).

Security Level	Lock Bit			Protection Level
	LB3	LB2	LB1	
1	U	U	U	No program lock features are implemented. On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
2	U	U	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is enabled. If you have programmed an encryption array, on-chip program code is encrypted before it is placed onto the data bus for verification.
3	U	P	P	Code executing from external memory cannot fetch code bytes from on-chip code memory (MOVC disabled). On-chip code memory verification is disabled.
4	P	P	P	Code cannot execute from external memory. On-chip code memory verification is disabled.

U = unprogrammed; P= programmed. Other combinations of the lock bits are undefined.

006. EPROM Programming (87C51FA, 87C51FB, 83C51FB)

PROBLEM: A control pin (P3.3) has been added to the programming algorithm (87C51FA D-step, 87C51FB B-step, 83C51FB B-step). This programming algorithm is **not** compatible with previous steppings. Hold P3.3 high to program the EPROM and low to verify it. The following table indicates the levels at which the control and program signals must be held to accomplish each programming and verification task.

Task	RST	PSEN#	ALE/ PROG#	EA#/Vpp	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code	H	L	L †	Vpp ††	L	H	H	H	H
Verify Code	H	L	H	H	L	L	L	H	H
Program Encryption Array	H	L	L †	Vpp ††	L	H	H	L	H
Program Lock Bit 1	H	L	L †	Vpp ††	H	H	H	H	H
Program Lock Bit 2	H	L	L †	Vpp ††	H	H	H	L	L
Program Lock Bit 3	H	L	L †	Vpp ††	H	L	H	H	L
Read Signature Bytes	H	L	H	H	L	L	L	L	L

† ALE/PROG# is pulsed low for 100 µs for programming.

†† Vpp = +12.5V ± 5%

007. Signature Bytes (87C51FA, 87C51FB, 83C51FB)

PROBLEM: A new signature byte has been added to the 87C51FA D-step, 87C51FB B-step, and 83C51FB B-step, increasing the number of signature bytes to three. To read the signature bytes, activate the control pins as shown in the following table and use the procedure for EPROM verification.

Task	RST	PSEN#	ALE/ PROG#	EA#/Vpp	P2.6	P2.7	P3.3	P3.6	P3.7
Read Signature Bytes	H	L	H	H	L	L	L	L	L

The following table lists the locations and contents of the signature bytes.

Location	Contents			Description
	87C51FA	83C51FB	87C51FB	
30H	89H	89H	89H	Identifies the product as an Intel controller
31H	58H	58H	58H	Identifies an FX-core product

Location	Contents			Description
	87C51FA	83C51FB	87C51FB	
60H	51H	5BH	FBH	Identifies the specific FX-core product

008. Port 1 and 3 Reset Value

PROBLEM: The reset value of all ports is logic “1”; however, the reset value of ports 1 and 3 is sustained by a weak pull-up. It is recommended that applications **not** use the reset value of these ports to drive external loads. If the application requires the use of the reset value of these ports, an external pull-up resistor should be added.

DOCUMENTATION CHANGES

None for this revision of this specification update.