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**APPLICATION
BRIEF**

**Software Serial Port
Implemented with the PCA**

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ECO APPLICATIONS ENGINEER

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**SOFTWARE SERIAL PORT
IMPLEMENTED WITH THE
PCA**

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For microcontroller applications which require more than one serial port, the 83C51FA Programmable Counter Array (PCA) can implement additional half-duplex serial ports. If the on-chip UART is being used as an inter-processor link, the PCA can be used to interface the 83C51FA to additional asynchronous lines.

This application uses several different Compare/Capture modes available on the PCA to receive or transmit bytes of data. It is assumed the reader is familiar the PCA and ASM51. For more information on the PCA refer to the "Hardware Description of the 83C51FA" chapter in the Embedded Controller Handbook (Order No. 210918).

Introduction

The figure below shows the format of a standard 10-bit asynchronous frame: 1 start bit (0), 8 data bits, and 1 stop bit (1). The start bit is used to synchronize the receiver to the transmitter; at the leading edge of the start bit the receiver must set up its timing logic to sample the incoming line in the center of each bit. Following the start bit are eight data bits which are transmitted least significant bit first. The stop bit is set to the opposite state of the start bit to guarantee that the leading edge of the start bit will cause a transition on the line. It also provides a dead time on the line so that the receiver can maintain its synchronization.

Two of the Compare/Capture modes on the PCA are used in receiving and transmitting data bits. When receiving, the Negative-Edge Capture mode allows the PCA to detect the start bit. Then using the Software Timer mode, interrupts are generated to sample the incoming data bits. This same mode is used to clock out bits when transmitting.

This Application Note contains four sections of code:

- (1) List of variables
- (2) Initialization routine

- (3) Receive routine
- (4) Transmit routine.

A complete listing of the routines and the test loop which was used to verify their operation is found in the Appendix. A total of three half-duplex channels were run at 2400 Baud in the test program. The listings shown here are simplified to one channel (Channel 0).

Variables

Listing 1 shows the variables used in both the receive and transmit routines. Flags are defined to signify the status of the reception or transmission of a byte (e.g. RCV_START_BIT, TXM_START_BIT). RCV_BUF and TXM_BUF simulate the on-chip serial port SBUF as two separate buffer registers. The temporary registers, RCV_REG and TXM_REG, are used to save bits as they are received or transmitted. Finally, two counter registers keep track of how many bits have been received or transmitted.

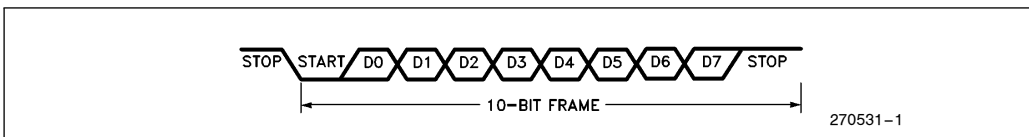
Variables are also needed to define one-half and one-full bit times in units of PCA timer ticks. (One bit time = 1 / baud rate.) With the PCA timer incremented every machine cycle, the equation to calculate one bit time can be written as:

$$\frac{\text{Osc. Freq.}}{(12) \times (\text{baud rate})} = 1 \text{ bit time (in PCA timer ticks)}$$

In this example, the baud rate is 2400 at 16 MHz.

$$\frac{16 \text{ MHz}}{(12) \times (2400)} = 556 \text{ counts} = 22\text{C Hex}$$

The high and low byte of this value is placed in the variables FULL_BIT_HIGH and FULL_BIT_LOW, respectively. 115H is the value loaded into HALF_BIT_HIGH and HALF_BIT_LOW.



Listing 1. Variables used by the software serial port. Channel 0

```

;
; Receive Routine
;
RCV_START_BIT_0  BIT    20H.0    ; Indicates start bit
; has been received
RCV_DONE_0      BIT    20H.1    ; Indicates data byte
; has been received
RCV_BUF_0       DATA  30H      ; Software Receive
; "SBUF"
RCV_REG_0       DATA  31H      ; Temporary register
; for receive bits
RCV_COUNT_0     DATA  32H      ; Counter for receiving
; bits

; Transmit Routine:
;
TXM_START_BIT_0 BIT    20H.3    ; Indicates start bit
; has been transmitted
TXM_IN_PROGRESS_0 BIT  20H.4    ; Indicates transmit is
; in progress
TXM_BUF_0       DATA  34H      ; Software transmit
; "SBUF"
TXM_REG_0       DATA  35H      ; Temporary register
; for transmitting bits
TXM_COUNT_0     DATA  36H      ; Counter for transmit-
; ting bits
DATA_0          DATA  37H      ; Register used for the
; test program

;
NEG_EDGE        EQU    11H      ; Two modes of operation
S_W_TIMER       EQU    49H      ; for compare/capture
; modules

;
HALF_BIT_HIGH   EQU    01H      ; Half bit time = 115H
HALF_BIT_LOW    EQU    15H
FULL_BIT_HIGH   EQU    02H      ; Full bit time = 22CH
FULL_BIT_LOW    EQU    2CH      ; 2400 Baud at 16 MHz

```

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Initialization

Listing 2 contains the initialization code for the receive and transmit process. Module 0 of the PCA is used as a receiver and is first set up to detect a negative edge from the start bit. Modules 2 and 3 are used for the additional 2 channels (see the Appendix). Module 3 is used as a separate software timer to transmit bits.

Listing 2. Initialization Routine

```

ORG 0000H
LJMP INITIALIZE
ORG 001BH
LJMP RECEIVE_DONE           ; Timer 1 overflow -
                           ; simulates "RI" interrupt

ORG 0033H
LJMP RECEIVE               ; PCA interrupt
;
INITIALIZE: MOV SP, #5FH    ; Initialize stack pointer
                           ; (specific to test program)
INIT_PCA:  MOV CMOD, #00H   ; Increment PCA timer
                           ; @ 1/12 Osc Frequency
                MOV CCON, #00H ; Clear all status flags
                MOV CCAPM0, #NEG_EDGE ; Module 0 in negative-edge
                           ; trigger mode (P1.3)
                MOV CCAPM3, #S_W_TIMER ; Module 3 as software timer
                           ; mode
                MOV CL, #00H
                MOV CH, #00H
                MOV IE, #0D8H ; Init all needed interrupts
                           ; EA, EC, ES, ET1
                SETB CR      ; Turn on PCA Counter

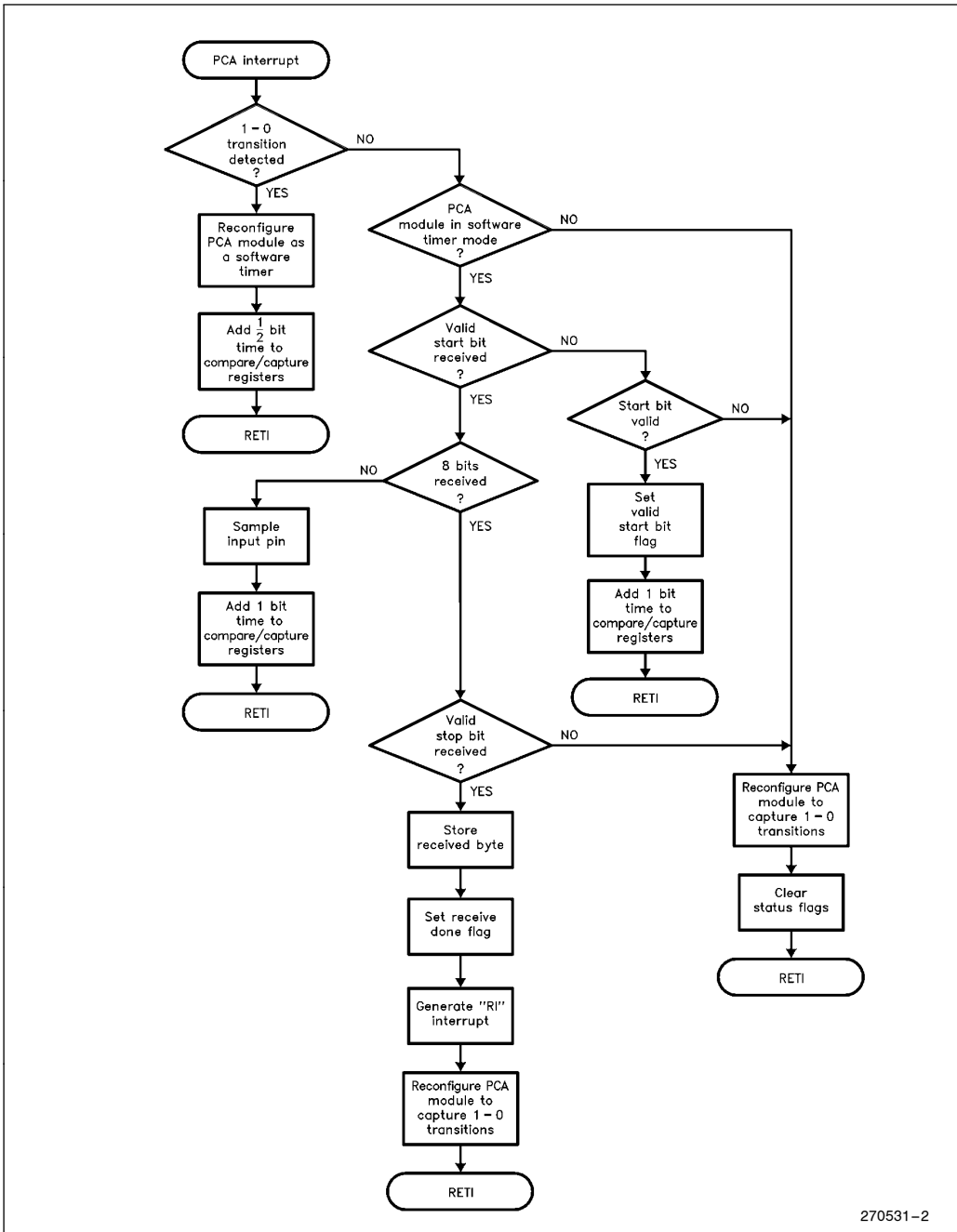
```

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All flags and registers from Listing 1 should be cleared in the initialization process.

Receive Routine

Two operating modes of the PCA are needed to receive bits. The module must first be able to detect the leading edge of a start bit so it is initially set up to capture a 1-to-0 transition (i.e. Negative-Edge Capture mode). The module is then reconfigured as a software timer to cause an interrupt at the center of each bit to deserialize the incoming data. The flowchart for the receive routine is given in Figure 1.



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Figure 1. Flowchart for the Receive Routine

Listing 3.1 shows the code needed to detect a start bit. Notice that the first software timer interrupt will occur one-half bit time after the leading edge of the start bit to check its validity. If it is valid, the RCV_START_BIT is set. The rest of the samples will occur a full bit time later. The RCV_COUNT register is loaded with a value of 9 which indicates the number of bits to be sampled: 8 data bits and 1 stop bit.

Listing 3.1. Receive Interrupt Routine

```

RECEIVE:  PUSH ACC
          PUSH PSW
;
MODULE_0: CLR CCF0                ; Assume reception on
          ; Module 0
          MOV A, CCAPM0           ; Check mode of module. If
          ANL A, #01111111B      ; set up to receive negative
          CJNE A, #NEG_EDGE, RCV_START_0 ; edges, then module
          ; is waiting for a start bit
;
          CLR C                  ; Update compare/capture
          MOV A, #HALF_BIT_LOW   ; registers for half bit time
          ADD A, CCAP0L          ; to sample start bit
          MOV CCAP0L, A         ; Half bit time = 115H
          MOV A, #HALF_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          MOV CCAPM0, #S_W_TIMER ; Reconfigure module 0 as
          POP PSW                ; a software timer to sample
          POP ACC                ; bits
          RETI
;
RCV_START_0: CJNE A, #S_W_TIMER, ERROR_0 ; Check module is
          ; configured as a software
          ; timer, otherwise error.
          JB RCV_START_BIT_0, RCV_BYTE_0 ; Check if start bit
          ; is received yet.
          JB P1.3, ERROR_0         ; Check that start bit = 0,
          ; otherwise error.
          SETB RCV_START_BIT_0    ; Signify valid start bit
          ; was received
          MOV RCV_COUNT_0, #09H  ; Start counting bits sampled
;
          CLR C                  ; Update compare/capture
          MOV A, #FULL_BIT_LOW   ; registers to sample
          ADD A, CCAP0L          ; incoming bits
          MOV CCAP0L, A         ; Full bit time = 22CH
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP0H
          MOV CCAP0H, A
          POP PSW
          POP ACC
          RETI

```

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The next 8 timer interrupts will receive the incoming data bits; the RCV_COUNT register keeps track of how many bits have been sampled. As each bit is sampled, it is shifted through the Carry Flag and saved in RCV_REG. The ninth sample checks the validity of the stop bit. If it is valid, the data byte is moved into RCV_BUF.

The main routine must have a way to know that a byte has been received. With the on-chip UART, the RI (Receive Interrupt) bit is set whenever a byte has been received. For the software serial port, any unimplemented interrupt vector can be used to generate an interrupt when a byte has been received. This routine uses the Timer 1 Overflow interrupt (its selection is arbitrary). A routine to test this interrupt is included in the listing in the Appendix.

Listing 3.2. Receive Interrupt Routine (Continued)

```

RCV_BYTE_0: DJNZ RCV_COUNT_0, RCV_DATA_0 ; On 9th sample,
                                                ; check for valid stop bit
RCV_STOP_0: JNB P1.3, ERROR_0
             MOV RCV_BUF_0, RCV_REG_0 ; Save received byte in
             ; receive "SBUF"
             SETB RCV_DONE_0 ; Flag which module received
             ; a byte
             SETB TF1 ; Generate an interrupt so
             ; main program knows a byte
             ; has been received
             ; (Note: selection of TF1 is
             ; arbitrary)
             MOV CCAPM0, #NEG_EDGE ; Reconfigure module 0 for
             ; Reception of a start bit

             POP PSW
             POP ACC
             RETI

;
RCV_DATA_0: MOV C, P1.3 ; Sampling data bits
             MOV A, RCV_REG_0 ; Shifts bits thru CY into
             RRC A ; ACC
             MOV RCV_REG_0, A ; Save each reception in
             ; temporary register
             CLR C ; Update c/c register for
             MOV A, #FULL_BIT_LOW ; next sample time
             ADD A, CCAP0L
             MOV CCAP0L, A
             MOV A, #FULL_BIT_HIGH
             ADDC A, CCAP0H
             MOV CCAP0H, A
             POP PSW
             POP ACC
             RETI

```

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In addition, an error routine (Listing 3.3) is included for invalid start or stop bits to offer some protection against noise. If an error occurs, the module is re-initialized to look for another start bit.

Listing 3.3 Error Routine for Receive Routine

```

ERROR_0: MOV CCAPM0, #NEG_EDGE ; Reset module to look for
             ; start bit
             CLR RCV_START_BIT_0 ; Clear flags which might
             ; have been set

             POP PSW
             POP ACC
             RETI

```

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Transmit Routine

Another PCA module is configured as a software timer to interrupt the CPU every bit time. With each timer interrupt one or more bits can be transmitted through port pins. In the test program three channels were operated simultaneously, but in the listings below, one channel is shown for simplicity. The selection of port pins is user programmable. The flowchart for the transmit routine is given in Figure 2.

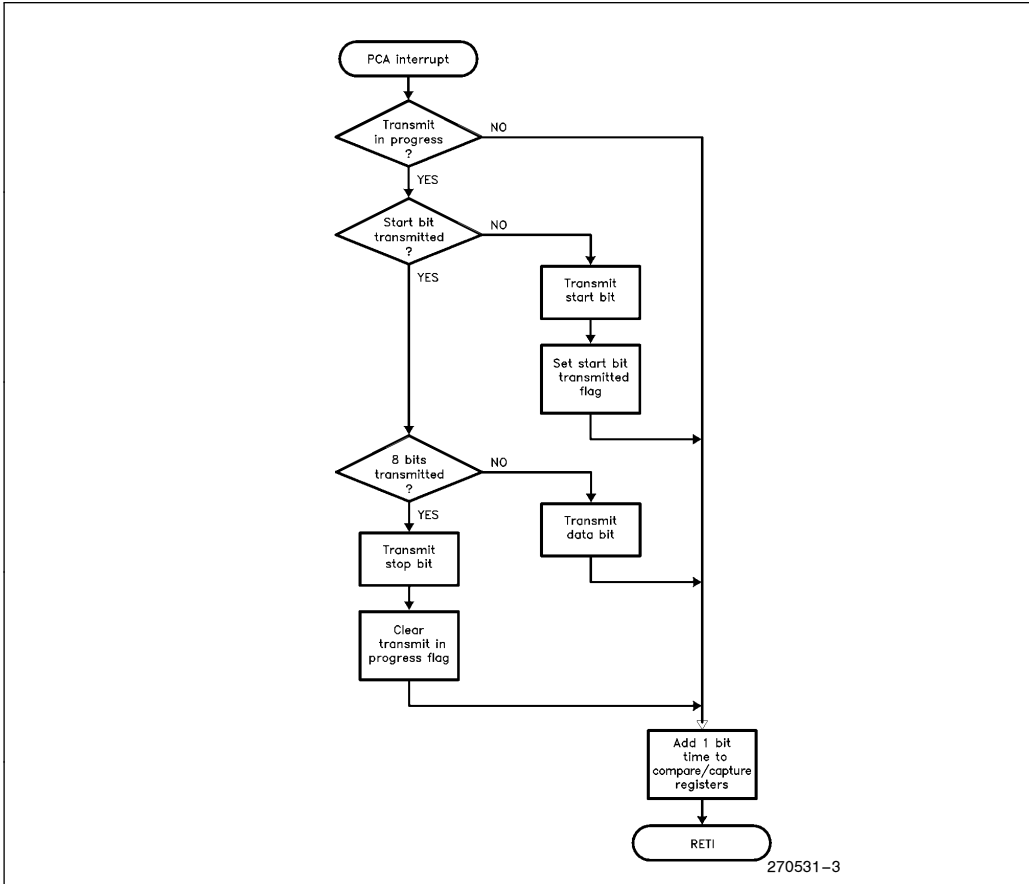


Figure 2. Flowchart for the Transmit Routine

When a byte is ready to be transmitted, the main program moves the data byte into the TXM_BUF register and sets the corresponding TXM_IN_PROGRESS bit. This bit informs the interrupt routine which channel is transmitting. The data byte is then moved in the storage register TXM_REG, and the TXM_COUNT is loaded. This main routine is shown in Listing 4.1.

Listing 4.1 Transmit Set Up Routine. Channel 0.

```

TXM_ON_0: CLR TXM_START_BIT_0    ; Clear status flag from
                                ; previous transmission
          MOV TXM_BUF_0, DATA_0  ; Load "SBUF" with data byte
          MOV TXM_REG_0, TXM_BUF_0
          MOV TXM_COUNT_0, #09    ; 8 data bits + 1 stop bit
          SETB TXM_IN_PROGRESS_0
  
```

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Listing 4.2 shows the transmit interrupt routine. The first time through, the start bit is transmitted. As each successive interrupt outputs a bit, the contents of TXM_REG is shifted right one place into the Carry flag, and the TXM_COUNT is decremented. When TXM_COUNT equals zero, the stop bit is transmitted.

Listing 4.2. Transmit Interrupt Routine

```

TRANSMIT: PUSH ACC
          PUSH PSW
          CLR CCF3                ; Clear s/w timer interrupt
          ; for transmitting bits
          JNB TXM_IN_PROGRESS_0, TRANSMIT_1 ; Check which
          ; channel is transmitting.
          ; "TRANSMIT_1" is listed in
          ; the Appendix
;
TRANSMIT_0: JB TXM_START_BIT_0, TXM_BYTE_0 ; If start bit
          ; has been sent, continue
          ; transmitting bits.
          CLR P3.2                ; Otherwise transmit start
          ; bit
          SETB TXM_START_BIT_0    ; Signify start bit sent
          JMP TXM_EXIT
;
TXM_BYTE_0: DJNZ TXM_COUNT_0, TXM_DATA_0 ; If bit count
          ; equals 1 thru 9, transmit
          ; data bits (8 total)
;
TXM_STOP_0: SETB P3.2            ; When bit count = 0,
          ; transmit stop bit
          CLR TXM_IN_PROGRESS_0  ; Indicate transmission is
          ; finished and ready for
          ; next byte
          JMP TXM_EXIT
;
TXM_DATA_0: MOV A, TXM_REG_0     ; Transmit one bit at a time
          RRC A                  ; through the carry bit
          MOV P3.2, C
          MOV TXM_REG_0, A       ; Save what's not been sent
;
TXM_EXIT: CLR C                 ; Update compare value with
          MOV A, #FULL_BIT_LOW  ; Full bit time = 22CH
          ADD A, CCAP3L
          MOV CCAP3L, A
          MOV A, #FULL_BIT_HIGH
          ADDC A, CCAP3H
          MOV CCAP3H, A
          POP PSW
          POP ACC
          RETI

```

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Conclusion

The software routines in the Appendix can be altered to vary the baud rate and number of channels to fit a particular application. The number of channels which can be implemented is limited by the CPU time required to service the PCA interrupt. At higher baud rates, fewer channels can be run.

The test program verifies the simultaneous operation of three half-duplex channels at 2400 Baud and the on-chip full-duplex channel at 9600 Baud. Thirty-three percent of the CPU time is required to operate all four channels. The test was run for several hours with no apparent malfunctions.

APPENDIX

```
MCS-51 MACRO ASSEMBLER    SWPORT                01/01/80    PAGE    1

DOS_3_20 (038-N) MCS-51 MACRO ASSEMBLER, V2.2
OBJECT MODULE PLACED IN SWPORT.OBJ
ASSEMBLER INVOKED BY: C:\AEDIT\ASMS1.EXE SWPORT.RCV

LOC OBJ      LINE    SOURCE
SWMPD51      1
SWCVS20     2
SWLIST      3
152          ;
153          ;
154          ; This program tests the receive routines of a software serial port.
155          ; Three half-duplex channels are implemented in software to run at
156          ; 2400 baud (16MHz) with the chip serial ports also running full-duplex
157          ; at 9600 baud. It is not necessary to have a baud rate of the percent of the CPU time is required to run
158          ; all four ports simultaneously.
159          ;
160          ;
161          ; To test the receive routines, "dummy" terminals transmit 00 - FF hex
162          ; continually to the PCA. When the first byte is received, it is
163          ; compared with 00. If the comparison is valid, the compare value is
164          ; incremented and the routine waits to receive the next byte. Error
165          ; routines occur if an invalid start bit or stop bit comparison occurs
166          ; or if an invalid start bit or stop bit is received.
167          ;
168          ORG 00H
169          LAMP INITIALIZE
170          ;
171          ORG 01BH
172          LAMP RECEIVE_DONE
173          ;
174          ORG 0223H
175          LAMP SERIAL_PORT
176          ;
177          ORG 0233H
178          LAMP RECEIVE
179          ;
180          ;
181          ;
182          ;
183          ;
184          ;
185          ;
186          ;
187          ;
188          ;
189          ;
190          ;
191          ;
192          ;
193          ;
194          ;
195          ;
196          ;
197          ;
198          ;

VARIABLES USED BY THE SOFTWARE SERIAL PORT
=====
RECEIVE ROUTINE:
=====
RCV_START_BIT_0     BIT
RCV_START_BIT_1     BIT
RCV_START_BIT_2     BIT
RCV_DONE_0         BIT
RCV_DONE_1         BIT
RCV_DONE_2         BIT
RCV_OK_0           BIT
RCV_OK_1           BIT
RCV_OK_2           BIT

20H.0 ; Indicates start bit has been
21H.0 ; received
22H.0
20H.1 ; Indicates data byte has been
21H.1 ; received
22H.1
20H.2 ; Used in main test program to check
21H.2 ; for a received byte
22H.2

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```

```

MCS-51 MACRO ASSEMBLER      SWF0RT      01/01/80      PAGE      2
LOC OBJ      LINE      SOURCE
0030          199      RCV_BUF_0
0040          200      DATA
0050          201      RCV_BUF_1
0050          202      DATA
0041          203      RCV_REC_0
0041          204      DATA
0051          205      RCV_REC_1
0051          206      DATA
0032          207      RCV_COUNT_0
0042          208      DATA
0052          209      RCV_COUNT_1
0052          210      DATA
0033          211      COUNT_0
0043          212      DATA
0053          213      COUNT_1
0053          214      DATA
0011          215      NEG_EDGE
0049          216      S_W_TIMER
0015          217      HALF_BIT_LOW
0001          218      EQU
0001          219      HALF_BIT_HIGH
002C          220      EQU
0002          221      FULL_BIT_LOW
0002          222      FULL_BIT_HIGH
0002          223      EQU
0002          224      EQU
0002          225      EQU
0002          226      EQU
0002          227      EQU
0002          228      EQU
0002          229      EQU
0036 75815F          230      INITIALIZE:
0039 75D900          231      MOV SP, #5FH
003C 75D800          232      MOV CMO0, #00H
003F 75DA11          233      MOV CC0N, #00H
0042 75DB11          234      MOV CCAPM0, #NEG_EDGE
0045 75DC11          235      MOV CCAPM1, #NEG_EDGE
0048 75E900          236      MOV CCAPM2, #NEG_EDGE
0048 75E900          237      MOV CL, #00H
004E 75A800          238      MOV CF, #00H
004E 75A808          239      MOV CF, #0D8H
0051 D2DE          240      SETB CR
0053 759850          241      INIT_SP:
0056 75CBFF          242      MOV SCON, #50H
0059 75CACC          243      MOV RCAP2H, #0FH
005C 75C834          244      MOV RCAP2L, #0CCH
005C 75C834          245      MOV TZCON, #34H
005F C200          246      CLR RCV_START_BIT_0
0061 C208          247      CLR RCV_START_BIT_1
0063 C210          248      CLR RCV_START_BIT_2
0065 C201          249      CLR RCV_DONE_0

```

MCS-51 MACRO ASSEMBLER SWPORT

```

LOC OBJ      LINE      SOURCE
0067 C209    254      CLR RCV_DONE_1
0069 C211    255      CLR RCV_DONE_2
           256      ;
006B C202    257      CLR RCV_ON_0
006D C20A    258      CLR RCV_ON_1
006F C212    259      CLR RCV_ON_2
           260      ;
           261      ; Port 3 pins used in test program for error routines
           262      ;
           263      ; Main program:
0071 D2B2    264      SETB P3.2      ; Error in comparison on module 0
0073 D2B3    265      SETB P3.3      ; Error in comparison on module 1
0075 D2B4    266      SETB P3.4      ; Error in comparison on module 2
           267      ;
           268      ; Interrupt routines:
0077 D2B5    269      SETB P3.5      ; Error in reception on module 0
0079 D2B6    270      SETB P3.6      ; Error in reception on module 1
007B D2B7    271      SETB P3.7      ; Error in reception on module 2
           272      ;
007D 753000  273      MOV RCV_BUF_0, #00H
0080 754000  274      MOV RCV_BUF_1, #00H
0083 755000  275      MOV RCV_BUF_2, #00H
           276      ;
0086 753200  277      MOV RCV_COUNT_0, #00H
0089 754200  278      MOV RCV_COUNT_1, #00H
008C 755200  279      MOV RCV_COUNT_2, #00H
           280      ;
008F 753100  281      MOV RCV_REG_0, #00H
0092 754100  282      MOV RCV_REG_1, #00H
0095 755100  283      MOV RCV_REG_2, #00H
           284      ;
0098 753300  285      MOV COUNT_0, #00H
009B 754300  286      MOV COUNT_1, #00H
009E 755300  287      MOV COUNT_2, #00H
           288      ;
           289      ;
           290      ;
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           292      ;
           293      ;
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LOC	OBJ	MCS-51 MACRO ASSEMBLER	SWPORT	LINE	SOURCE
			01/01/80	PAGE	4
309					CLR RCV_ON_2
310	00C1	C212			INC COUNT_2
311	00C3	0553			JMP CHECK_0
312	00C5	80DA			
313	00C7	C2B2			; Error in comparison on module 0
314	00C9	75DA00			; Discontinue receiving bytes
315	00CC	80DF			
316					CLR P3.2
317	00CE	C2B3			MOV CCAPM0_1, #00H
318	00D0	75DB00			
319	00D3	80E4			CLR P3.3
320					MOV CCAPM1, #00H
321	00D5	C2B4			CLR P3.4
322	00D7	75DC00			MOV CCAPM2, #00H
323	00DA	80C5			JMP CHECK_0
324					
325					
326					
327					
328					PCA INTERRUPT ROUTINE - RECEIVE BITS
329	00DC	C0E0			=====
330	00DE	C0D0			PUSH ACC
331					PUSH PSW
332					
333	00E0	20D811			JB CCF0, MODULE_0
334	00E3	20D808			; Check which module caused
335	00E6	20DA08			; PCA interrupt and jump to
336	00E9	D0D0			; appropriate routine
337	00EB	80E0			POP PSW
338	00ED	32			POP ACC
339					RET
340	00EE	0201E4			
341	00F1	0201E4			LJMP MODULE_1
342					LJMP MODULE_2
343					
344					
345					CHANNEL_0
346					=====
347					
348	00F4	C2D8			CLR CCF0
349	00F6	E5DA			MOV A, CCAPM0
350	00F8	547F			ANL A, #01111111B
351	00FA	B41115			CJNE A, #NEG_EDGE, RCV_START_0
352					; Reception on module 0
353					; Check mode of module. If set up to
354					; receive negative edges, then module
355					; is waiting for a start bit
356					
357					CLR C
358					MOV A, #HALF_BIT_LOW
359					ADD A, CCAP0L
360					MOV CCAP0L, A
361					MOV A, #HALF_BIT_HIGH
362					ADD A, CCAP0H
363					MOV CCAP0H, A
					; Update Compare/Capture registers for
					; module 0
					; No sample start bit
					; Half bit time = 115H
					POP PSW
					POP ACC

MCS-51 MACRO ASSEMBLER	SWPORT	SOURCE	LINE
LOC OBJ			
0111 32		RETI	364
0112 B4494B		CJNE A, #S_M_TIMER, ERROR_0	365
0115 20001A	RCV_START_0:	JB RCV_START_BIT_0, RCV_BYTE_0	366
0118 209345		JB P1.3, ERROR_0	367
011B D200		SETB RCV_START_BIT_0	368
011D 753209		MOV RCV_COUNT_0, #09H	369
0120 C3		CLR C	370
0121 742C		MOV C, #FULL_BIT_LOW	371
0123 25FA		ADD A, CCAPOH	372
0125 F5EA		MOV CCAPOH, A	373
0127 7402		MOV A, #FULL_BIT_HIGH	374
0129 35FA		ADDC A, CCAPOH	375
012B F3FA		MOV CCAPOH, A	376
012D 0BE0		POP RSN	377
012F 0BE0		POP ACC	378
0131 32		RETI	379
0132 D53212	RCV_BYTE_0:	DJNZ RCV_COUNT_0, RCV_DATA_0	380
0135 309328	RCV_STOP_0:	JNB P1.3, ERROR_0	381
0138 D3130		SETB RCV_DONE_0	382
013B D28F		SETB TFI	383
013F 75D411		MOV CCAPMO, #NEG_EDGE	384
0142 D4D0		POP PSW	385
0144 D4E0		POP ACC	386
0146 32		RETI	387
0147 A293	RCV_DATA_0:	MOV C, P1.3	388
0149 E831		MOV A, RCV_REG_0	389
014B 13		RRC A	390
014C F531		MOV RCV_REG_0, A	391
014E C3		CLR C	392
0151 742C		MOV C, #FULL_BIT_LOW	393
0153 F5EA		ADD A, CCAPOH	394
0155 7402		MOV A, #FULL_BIT_HIGH	395
0157 35FA		ADDC A, CCAPOH	396
0159 F3FA		MOV CCAPOH, A	397
015B D4D0		POP PSW	398
015D 0BE0		POP ACC	399
015F 32		RETI	400
0160 C2B5	ERROR_0:	CLR P3.5	401
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MCS-51 MACRO ASSEMBLER	SWPORT	LINE	SOURCE
		418	
		419	
0162 75DA11		420	
0165 C200		421	
0167 D0D0		422	
0169 D0E0		423	
016B 32		424	
		425	
		426	
		427	
		428	
016C C2D9		429	
016E E5DB		430	
0170 547F		431	
0172 B41115		432	
		433	
		434	
0175 C3		435	
0176 7415		436	
0178 25EB		437	
017A F5BB		438	
017C 7401		439	
017E F5EB		440	
0180 75EB		441	
0182 75DB49		442	
0185 D0D0		443	
0187 D0E0		444	
0189 32		445	
018A B4494B		446	
018C 2081		447	
0190 209445		448	
		449	
0193 D208		450	
0195 754209		451	
		452	
0198 C3		453	
0199 242C		454	
019B 25EB		455	
019D F5EB		456	
019F 7402		457	
01A1 35FB		458	
01A3 F5FB		459	
01A5 D0D0		460	
01A7 D0E0		461	
01A9 32		462	
		463	
01AA D54212		464	
		465	
01AD 309428		466	
01B0 854140		467	
01B3 D209		468	
01B7 726E		469	
01B9 726E		470	
01BA D0D0		471	
01BC D0E0		472	

NCS-51 MACRO ASSEMBLER SWF0RT

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LOC OBJ          LINE          SOURCE
01BE 32          473          RETI
01BF A294        474          MOV C, P1.4
01C0 E541        475          MOV A, RCV_REG_1
01C1 13         476          RRC A
01C2 13         477          MOV RCV_REG_1, A
01C3 13         478          ;
01C4 F541        479          ;
01C5 C3         480          CLR C
01C6 742C       481          MOV A, #FULL_BIT_LOW
01C7 25EB       482          ADD A, CCAP1L
01C8 F5EB       483          MOV CCAP1L, A
01C9 7402       484          MOV A, #FULL_BIT_HIGH
01CA 35FB       485          ADDC A, CCAP1H
01CB F5FB       486          MOV CCAP1H, A
01CC D0D0       487          POP FSN
01CD 09E0       488          POP ACC
01CE 32         489          RETI
01CF C2B6       490          CLR P3.6
01D0 75DB11     491          MOV CCAP1L, #NEG_EDGE
01D1 C208       492          CLR RCV_START_BIT_1
01D2 D0D0       493          POP FSN
01D3 D0D0       494          POP ACC
01D4 13         495          RETI
01D5 32         496          ;
01D6 32         497          ;
01D7 32         498          ;
01D8 32         499          ;
01D9 32         500          ;
01DA 32         501          ;
01DB 32         502          ;
01DC 32         503          ;
01DD 32         504          ;
01DE 32         505          ;
01DF 32         506          ;
01E0 32         507          ;
01E1 32         508          ;
01E2 32         509          ;
01E3 32         510          ;
01E4 C2DA       511          CLR CCF2
01E5 E5DC       512          MOV A, CCAP2M
01E6 547F       513          ANL A, #01111111B
01E7 B41115     514          CJNE A, #NEG_EDGE, RCV_START_2
01E8 7315       515          CLR C
01E9 7315       516          MOV A, #HALF_BIT_LOW
01EA 25FC       517          ADD A, CCAP2L
01EB F5FC       518          MOV CCAP2L, A
01EC 7401       519          MOV A, #HALF_BIT_HIGH
01ED 35FC       520          ADDC A, CCAP2H
01EE F5FC       521          MOV CCAP2H, A
01EF 75DC49     522          MOV CCAP2M, #S_W_TIMER
01F0 D0D0       523          POP FSN
01F1 D0D0       524          POP ACC
01F2 32         525          RETI
01F3 32         526          ;
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01F8 32         531          ;
01F9 32         532          ;
01FA 32         533          ;
01FB 32         534          ;
01FC 32         535          ;
01FD 32         536          ;
01FE 32         537          ;
01FF 32         538          ;
0200 32         539          ;
0201 32         540          ;
0202 B4494B     541          CJNE A, #S_W_TIMER, ERROR_2
0203 20101A     542          JB RCV_START_BIT_2, RCV_BYTE_2
0204 203545     543          JB P1.5, ERROR_2
0205 32         544          ;
0206 32         545          ;
0207 32         546          ;
0208 32         547          ;
0209 32         548          ;
020A 32         549          ;
020B D210       550          SETB RCV_START_BIT_2
020C 753209     551          MOV RCV_COUNT_2, #09H
020D 32         552          ;
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02C9 32         740          ;
02CA 32         741          ;
02CB 32         742          ;
02CC 32         743          ;
02CD 32         744          ;
02CE 32         745          ;
02CF 32         746          ;
02D0 32         747          ;
02D1 32         748          ;
02D2 32         749          ;
02D3 32         750          ;
02D4 32         751          ;
02D5 32         752          ;
02D6 32         753          ;
02D7 32         754          ;
02D8 32         755          ;
02D9 32         756          ;
02DA 32         757          ;
02DB 32         758          ;
02DC 32         759          ;
02DD 32         760          ;
02DE 32         761          ;
02DF 32         762          ;
02E0 32         763          ;
02E1 32         764          ;
02E2 32         765          ;
02E3 32         766          ;
02E4 32         767          ;
02E5 32         768          ;
02E6 32         769          ;
02E7 32         770          ;
02E8 32         771          ;
02E9 32         772          ;
02EA 32         773          ;
02EB 32         774          ;
02EC 32         775          ;
02ED 32         776          ;
02EE 32         777          ;
02EF 32         778          ;
02F0 32         779          ;
02F1 32         780          ;
02F2 32         781          ;
02F3 32         782          ;
02F4 32         783          ;
02F5 32         784          ;
02F6 32         785          ;
02F7 32         786          ;
02F8 32         787          ;
02F9 32         788          ;
02FA 32         789          ;
02FB 32         790          ;
02FC 32         791          ;
02FD 32         792          ;
02FE 32         793          ;
02FF 32         794          ;
0300 32         795          ;
0301 32         796          ;
0302 32         797          ;
0303 32         798          ;
0304 32         799          ;
0305 32         800          ;
0306 32         801          ;
0307 32         802          ;
0308 32         803          ;
0309 32         804          ;
030A 32         805          ;
030B 32         806          ;
030C 32         807          ;
030D 32         808          ;
030E 32         809          ;
030F 32         810          ;
0310 32         811          ;
0311 32         812          ;
0312 32         813          ;
0313 32         814          ;
0314 32         815          ;
0315 32         816          ;
0316 32         817          ;
0317 32         818          ;
0318 32         819          ;
0319 32         820          ;
031A 32         821          ;
031B 32         822          ;
031C 32         823          ;
031D 32         824          ;
031E 32         825          ;
031F 32         826          ;
0320 32         827          ;
0321 32         828          ;
0322 32         829          ;
0323 32         830          ;
0324 32         831          ;
0325 32         832          ;
0326 32         833          ;
0327 32         834          ;
0328 32         835          ;
0329 32         836          ;
032A 32         837          ;
032B 32         838          ;
032C 32         839          ;
032D 32         840          ;
032E 32         841          ;
032F 32         842          ;
0330 32         843          ;
0331 32         844          ;
0332 32         845          ;
0333 32         846          ;
0334 32         847          ;
0335 32         848          ;
0336 32         849          ;
0337 32         850          ;
0338 32         851          ;
0339 32         852          ;
033A 32         853          ;
033B 32         854          ;
033C 32         855          ;
033D 32         856          ;
033E 32         857          ;
033F 32         858          ;
0340 32         859          ;
0341 32         860          ;
0342 32         861          ;
0343 32         862          ;
0344 32         863          ;
0345 32         864          ;
0346 32         865          ;
0347 32         866          ;
0348 32         867          ;
0349 32         868          ;
034A 32         869          ;
034B 32         870          ;
034C 32         871          ;
034D 32         872          ;
034E 32         873          ;
034F 32         874          ;
0350 32         875          ;
0351 32         876          ;
0352 32         877          ;
0353 32         878          ;
0354 32         879          ;
0355 32         880          ;
0356 32         881          ;
0357 32         882          ;
0358 32         883          ;
0359 32         884          ;
035A 32         885          ;
035B 32         886          ;
035C 32         887          ;
035D 32         888          ;
035E 32         889          ;
035F 32         890          ;
0360 32         891          ;
0361 32         892          ;
0362 32         893          ;
0363 32         894          ;
0364 32         895          ;
0365 32         896          ;
0366 32         897          ;
0367 32         898          ;
0368 32         899          ;
0369 32         900          ;
036A 32         901          ;
036B 32         902          ;
036C 32         903          ;
036D 32         904          ;
036E 32         905          ;
036F 32         906          ;
0370 32         907          ;
0371 32         908          ;
0372 32         909          ;
0373 32         910          ;
0374 32         911          ;
0375 32         912          ;
0376 32         913          ;
0377 32         914          ;
0378 32         915          ;
0379 32         916          ;
037A 32         917          ;
037B 32         918          ;
037C 32         919          ;
037D 32         920          ;
037E 32         921          ;
037F 32         922          ;
0380 32         923          ;
0381 32         924          ;
0382 32         925          ;
0383 32         926          ;
0384 32         927          ;
0385 32         928          ;
0386 32         929          ;
0387 32         930          ;
0388 32         931          ;
0389 32         932          ;
038A 32         933          ;
038B 32         934          ;
038C 32         935          ;
038D 32         936          ;
038E 32         937          ;
038F 32         938          ;
0390 32         939          ;
0391 32         940          ;
0392 32         941          ;
0393 32         942          ;
0394 32         943          ;
0395 32         944          ;
0396 32         945          ;
0397 32         946          ;
0398 32         947          ;
0399 32         948          ;
039A 32         949          ;
039B 32         950          ;
039C 32         951          ;
039D 32         952          ;
039E 32         953          ;
039F 32         954          ;
03A0 32         955          ;
03A1 32         956          ;
03A2 32         957          ;
03A3 32         958          ;
03A4 32         959          ;
03A5 32         960          ;
03A6 32         961          ;
03A7 32         962          ;
03A8 32         963          ;
03A9 32         964          ;
03AA 32         965          ;
03AB 32         966          ;
03AC 32         967          ;
03AD 32         968          ;
03AE 32         969          ;
03AF 32         970          ;
03B0 32         971          ;
03B1 32         972          ;
03B2 32         973          ;
03B3 32         974          ;
03B4 32         975          ;
03B5 32         976          ;
03B6 32         977          ;
03B7 32         978          ;
03B8 32         979          ;
03B9 32         980          ;
03BA 32         981          ;
03BB 32         982          ;
03BC 32         983          ;
03BD 32         984          ;
03BE 32         985          ;
03BF 32         986          ;
03C0 32         987          ;
03C1 32         988          ;
03C2 32         989          ;
03C3 32         990          ;
03C4 32         991          ;
03C5 32         992          ;
03C6 32         993          ;
03C7 32         994          ;
03C8 32         995          ;
03C9 32         996          ;
03CA 32         997          ;
03CB 32         998          ;
03CC 32         999          ;
03CD 32         1000         ;

```

CHANNEL 2

; Similar to module 0

MCS-51 MACRO ASSEMBLER	SWPORT	LOC OBJ	LINE	SOURCE
			528	CLR C
		0210 C3	529	MOV A, #FULL_BIT_LOW
		0211 742C	530	ADD A, CCAP2I
		0213 256C	531	MOV A, #FULL_BIT_HIGH
		0215 F5EC	532	ADD A, CCAP2H
		0217 7402	533	MOV A, #FULL_BIT_LOW
		0219 35FC	534	ADD A, CCAP2H
		021B 556C	535	POP PSW
		021D 00E0	536	POP ACC
		0221 32	537	RETI
		0222 D55212	538	DJMZ RCV_COUNT_2, RCV_DATA_2
		0225 399528	539	JNB P1_5_ERROR_2
		0228 D21150	540	SETB RCV_DONE_2
		022B D28F	541	SETB RCV_DONE_2
		022D D28F	542	SETB RCV_DONE_2
		022F 75DC11	543	MOV C, #NEG_EDGE
		0232 D0D0	544	POP PSW
		0234 D0E0	545	POP ACC
		0236 32	546	RETI
		0237 2995	547	MOV C, P1_5
		0239 F551	548	MOV A, RCV_REG_2
		023B 13	549	RRC A
		023C F551	550	MOV RCV_REG_2, A
		023E C3	551	CLR C
		023F 742C	552	MOV A, #FULL_BIT_LOW
		0241 256C	553	ADD A, CCAP2I
		0243 7402	554	MOV A, #FULL_BIT_HIGH
		0245 35FC	555	ADD A, CCAP2H
		0247 F5FC	556	MOV A, #FULL_BIT_LOW
		0249 F5FC	557	ADD A, CCAP2I
		024B D0D0	558	POP PSW
		024D D0E0	559	POP ACC
		024F 32	560	RETI
		0250 C2B7	561	CLR P3_7
		0252 75DC11	562	MOV C, #NEG_EDGE
		0255 C210	563	CLR RCV_START_BIT_2
		0257 D0D0	564	POP PSW
		0259 D0E0	565	POP ACC
		025B 32	566	RETI
		025C C0E0	567	PUSH ACC
		025E C0D0	568	PUSH PSW
		0260 C2BF	569	CLR TFI
			570	
			571	
			572	
			573	
			574	
			575	
			576	
			577	
			578	
			579	
			580	
			581	
			582	

This routine simulates the "RI" interrupt. When a byte is received on one of the channels, this interrupt is generated. Bits are set so the main routine knows which channel received a byte.

MCS-51 MACRO ASSEMBLER SWFPORT

```

LOC OBJ          LINE          SOURCE
0262 300106      583          JNB RCV_DONE_0, RCV_1
0265 C201        584          CLR RCV_DONE_0
0267 C200        585          CLR RCV_START_BIT_0
0269 D202,      586          SETB RCV_ON_0
026A          587          ; Check which module received a byte
026B          588          ; Clear flags needed for next reception
026C          589          ; Tell main routine which channel received
026D          590          ; a byte
026E C209        591          JNB RCV_DONE_1, RCV_2
0270 C208        592          CLR RCV_DONE_1
0271 D20A,      593          SETB RCV_ON_1
0272          594          ; RCV_2:
0273          595          JNB RCV_DONE_2, RETURN
0274 301106      596          CLR RCV_DONE_2
0275 C211        597          CLR RCV_START_BIT_2
0276 D212,      598          SETB RCV_ON_2
0277          599          ; RETURN:
0278          600          POP PSW
0279 D0E0        601          POP ACC
0281 32         602          RETI
0282          603          ;
0283          604          ;
0284          605          ;
0285          606          ;
0286          607          ;
0287          608          ; When a byte is received on the full-duplex serial port, it is then
0288          609          ; transmitted back to a "dummy" terminal. This terminal checks that the
0289          610          ; byte it transmitted to the PCA is the same value it receives back.
0290          611          ;
0291          612          ; SERIAL_PORT:
0292 C0E0          613          PUSH ACC
0293 C0D0          614          PUSH PSW
0294 C0D0          615          JNB RI, TXM
0295 C0D0          616          MOV A, SBUF
0296 E359          617          MOV SBUF, A
0297 C0E9          618          POP PSW, A
0298 D0D0          619          POP PSW
0299 D0E0          620          POP ACC
029A 32         621          RETI
029B          622          ;
029C          623          ; TXM:
029D          624          CLR TI
029E D0D0          625          POP PSW
029F D0E0          626          POP ACC
029A 32         627          RETI
029B          628          ; END

```

REGISTER BANK(S) USED: 0
 ASSEMBLY COMPLETE, NO ERRORS FOUND

MCS-51 MACRO ASSEMBLER SWPORT
 DOS 3.20 (038-N) MCS-51 MACRO ASSEMBLER, V2.2
 OBJECT MODULE PLACED IN SWPORT.OBJ
 ASSEMBLER INVOKED BY: C:\AEDIT\ASMS1.EXE SWPORT.TR

```

LOC  OBJ      LINE  SOURCE
1      $NOMOD51
2      $NOSYMBOLS
3      $NOLIST
152    ;
153    ; This program tests the transmit routines for the software serial port.
154    ; It initiates the first transmission, the timer is started, before
155    ; the PCA timer is started. Successive interrupts are generated every bit
156    ; time by the software timer.
157    ;
158    ; For test purposes, the data transmitted increments from 00 to FF hex.
159    ; *Dummy* terminals receive these bytes and display the bytes as they
160    ; are incremented.
161    ;
162    ;
163    ;
164    ORG 00H
165    LAMP INIT_TXM
166    ;
167    ORG 0023H
168    LAMP SERIAL_PORT
169    ;
170    ORG 0033H
171    LAMP TRANSMIT
172    ;
173    ;
174    ;
175    ;
176    ;
177    TXM_START_BIT_0
178    TXM_START_BIT_1
179    TXM_START_BIT_2
180    ;
181    TXM_IN_PROGRESS_0
182    TXM_IN_PROGRESS_1
183    TXM_IN_PROGRESS_2
184    ;
185    TXM_BUF_0
186    TXM_BUF_1
187    TXM_BUF_2
188    ;
189    TXM_REG_0
190    TXM_REG_1
191    TXM_REG_2
192    ;
193    TXM_COUNT_0
194    TXM_COUNT_1
195    TXM_COUNT_2
196    ;
197    DATA_0
198    DATA_1
    
```

VARIABLES USED BY THE SOFTWARE SERIAL PORT

- 20H.3 ; Indicates start bit has been
- 21H.3 ; transmitted
- 22H.3
- 20H.4 ; Indicates transmit is in progress
- 21H.4
- 22H.4
- 34H ; Software transmit "SPUP"
- 44H
- 54H
- 35H ; Temporary register for
- 45H ; transmitting bits
- 55H
- 36H ; Counter for transmitting bits
- 46H
- 56H
- 37H ; Register used for the test
- 47H ; program

```

LOC OBJ          LINE  SOURCE
0057             199  DATA_2
0049             200  EQU          5_W_TIMER
002C             201  EQU          49H
0002             202  EQU          2CH
0002             203  EQU          2CH
0002             204  EQU          02H
0002             205  EQU          2400
0002             206  EQU          16
0002             207  EQU          2400
0002             208  EQU          16
0002             209  EQU          2400
0002             210  EQU          16
0036 75815F     211  INIT_TXM:
0039 75D900     212  MOV CMOD, #00H
003C 75D800     213  MOV CON, #00H
003F 75F900     214  MOV CH, #00H
0042 75E900     215  MOV CL, #00H
0045 75DD49     216  MOV CCAP3, #S_W_TIMER
0048 75A8D8     217  MOV IE, #0D8H
004B 759850     218  MOV SCON, #50H
004E 75C8FE     219  MOV RCAP2H, #0FFH
0051 75C8CC     220  MOV RCAP2L, #2CH
0054 75C834     221  MOV I2CON, #34H
0057 C203       222  CLR TXM_START_BIT_0
0059 C20B       223  CLR TXM_START_BIT_1
005B C213       224  CLR TXM_START_BIT_2
005D C204       225  CLR TXM_IN_PROGRESS_0
005F C20C       226  CLR TXM_IN_PROGRESS_1
0061 C214       227  CLR TXM_IN_PROGRESS_2
0063 753400     228  MOV TXM_BUF_0, #00H
0066 754400     229  MOV TXM_BUF_1, #00H
0069 755400     230  MOV TXM_BUF_2, #00H
006C 753500     231  MOV TXM_REG_0, #00H
006F 754500     232  MOV TXM_REG_1, #00H
0072 755500     233  MOV TXM_REG_2, #00H
0075 753600     234  MOV TXM_COUNT_0, #00H
0078 754600     235  MOV TXM_COUNT_1, #00H
007B 755600     236  MOV TXM_COUNT_2, #00H
007E 7537FF     237  MOV DATA_0, #0FFH
0081 7547FF     238  MOV DATA_1, #0FFH
0084 7557FF     239  MOV DATA_2, #0FFH
0087 75ED2C     240  MOV CCAP3L, #2CH
008A 75FD02     241  MOV CCAP3H, #02H
008D D2DE       242  SETB CR

```

```

; Software timer mode for the
; compare/capture module
; Full bit time = 22CH
; 2400 Baud at 16 Mhz
;
; (Compatible with receive routines)
; Increment PCA timer @ 1/12 osc. freq.
; Clear all status flags
; Module 3 configured as software timer
; Initialize all needed interrupts
; Serial port in mode 1 (8-bit UART)
; Reload values for 9600 Baud @ 16 Mhz
; Timer 2 as a baud-rate generator,
; turn Timer 2 on

```

```

INITIALIZATION
=====
MOV SP, #5FH
MOV CMOD, #00H
MOV CON, #00H
MOV CH, #00H
MOV CL, #00H
MOV CCAP3, #S_W_TIMER
MOV IE, #0D8H
MOV SCON, #50H
MOV RCAP2H, #0FFH
MOV RCAP2L, #2CH
MOV I2CON, #34H
CLR TXM_START_BIT_0
CLR TXM_START_BIT_1
CLR TXM_START_BIT_2
CLR TXM_IN_PROGRESS_0
CLR TXM_IN_PROGRESS_1
CLR TXM_IN_PROGRESS_2
MOV TXM_BUF_0, #00H
MOV TXM_BUF_1, #00H
MOV TXM_BUF_2, #00H
MOV TXM_REG_0, #00H
MOV TXM_REG_1, #00H
MOV TXM_REG_2, #00H
MOV TXM_COUNT_0, #00H
MOV TXM_COUNT_1, #00H
MOV TXM_COUNT_2, #00H
MOV DATA_0, #0FFH
MOV DATA_1, #0FFH
MOV DATA_2, #0FFH
MOV CCAP3L, #2CH
MOV CCAP3H, #02H
SETB CR

```

MCS-51 MACRO ASSEMBLER	SWPORT	LINE	SOURCE
		254	MAIN TEST ROUTINE - TRANSMIT BITS
		255	=====
		256	JMP TXM_ON_0
		257	JMP TXM_ON_0
		258	JMP TXM_ON_0
		259	JMP TXM_ON_0
008F 02009D		260	JMP TXM_ON_0
0092 300408		261	JMP TXM_ON_0
0095 300C16		262	JMP TXM_ON_0
0098 301424		263	JMP TXM_ON_0
009B 80F5		264	JMP TXM_ON_0
		265	JMP TXM_ON_0
009D C203		266	JMP TXM_ON_0
009F 0537		267	JMP TXM_ON_0
00A1 853734		268	JMP TXM_ON_0
00A4 853435		269	JMP TXM_ON_0
00A7 753609		270	JMP TXM_ON_0
00AA 0664		271	JMP TXM_ON_0
00AC 80E4		272	JMP TXM_ON_0
		273	JMP TXM_ON_0
00AE C20B		274	JMP TXM_ON_0
00B0 0547		275	JMP TXM_ON_0
00B2 854744		276	JMP TXM_ON_0
00B5 854445		277	JMP TXM_ON_0
00B8 754609		278	JMP TXM_ON_0
00BB 80D5		279	JMP TXM_ON_0
00BD 80D5		280	JMP TXM_ON_0
		281	JMP TXM_ON_0
00BF C213		282	JMP TXM_ON_0
00C1 0557		283	JMP TXM_ON_0
00C3 855754		284	JMP TXM_ON_0
00C6 954455		285	JMP TXM_ON_0
00C8 821409		286	JMP TXM_ON_0
00CC 8714		287	JMP TXM_ON_0
00CE 80C2		288	JMP TXM_ON_0
		289	JMP TXM_ON_0
		290	JMP TXM_ON_0
		291	JMP TXM_ON_0
		292	JMP TXM_ON_0
		293	JMP TXM_ON_0
		294	JMP TXM_ON_0
00D0 C0E0		295	JMP TXM_ON_0
00D2 C0D0		296	JMP TXM_ON_0
00D4 C2DB		297	JMP TXM_ON_0
00D6 30041E		298	JMP TXM_ON_0
		299	JMP TXM_ON_0
		300	JMP TXM_ON_0
		301	JMP TXM_ON_0
		302	JMP TXM_ON_0
00D9 200307		303	JMP TXM_ON_0
00DC C2B2		304	JMP TXM_ON_0
00DE D203		305	JMP TXM_ON_0
00E0 0200F7		306	JMP TXM_ON_0
		307	JMP TXM_ON_0
		308	JMP TXM_ON_0


```

LOC OBJ          LINE   SOURCE
00E3 D53607      309      DJNZ TXM_COUNT_0, TXM_DATA_0
00E6 D282        310      ; If bit count equals 1 thru 9,
00E8 C204        311      ; transmit data bits (8 total)
00EA 0200F7      312      SETB P3.2
00EB 0200F7      313      CLR TXM_IN_PROGRESS_0
00ED E535        314      JMP TRANSMIT_1
00EE 0200F7      315      ;
00EF 0200F7      316      MOV A, TXM_REG_0
00F0 0200F7      317      RRC A,3
00F1 0200F7      318      MOV TXM_REG_0, A
00F2 F535        319      MOV TXM_REG_0, A
00F4 0200F7      320      JMP TRANSMIT_1
00F5 0200F7      321      ;
00F6 0200F7      322      ;
00F7 0200F7      323      ;
00F8 0200F7      324      ;
00F9 0200F7      325      ;
00FA 0200F7      326      TRANSMIT_1:
00FB 0200F7      327      JB TXM_START_BIT_1, TXM_BYTE_1
00FC D283        328      CLR P3.3
00FD D208        329      SETB TXM_START_BIT_1
00FE 020118      330      JMP TRANSMIT_2
00FF D208        331      ;
0100 D54607      332      TXM_BYTE_1:
0101 020118      333      DJNZ TXM_COUNT_1, TXM_DATA_1
0102 020118      334      ;
0103 D283        335      SETB P3.3
0104 C20C        336      CLR TXM_IN_PROGRESS_1
0105 020118      337      JMP TRANSMIT_2
0106 020118      338      ;
0107 E545        339      MOV A, TXM_REG_1
0108 1200F7      340      RRC A,3
0109 0200F7      341      MOV TXM_REG_1, A
010A 020118      342      JMP TRANSMIT_2
010B 020118      343      ;
010C 020118      344      ;
010D 020118      345      ;
010E 020118      346      ;
010F 020118      347      ;
0110 020118      348      TRANSMIT_2:
0111 020118      349      JB TXM_START_BIT_2, TXM_BYTE_2
0112 C204        350      CLR P3.4
0113 D213        351      SETB TXM_START_BIT_2
0114 020139      352      JMP TXM_EXIT
0115 020139      353      ;
0116 D55607      354      TXM_BYTE_2:
0117 D284        355      DJNZ TXM_COUNT_2, TXM_DATA_2
0118 C204        356      SETB P3.4
0119 020139      357      CLR TXM_IN_PROGRESS_2
011A 020139      358      JMP TXM_EXIT
011B 020139      359      ;
011C E555        360      MOV A, TXM_REG_2
011D 120139      361      RRC A,3
011E 020139      362      MOV TXM_REG_2, A
011F 020139      363      JMP TXM_EXIT
0120 020139      364      ;
0121 020139      365      ;
0122 020139      366      ;
0123 020139      367      ;
0124 020139      368      ;
0125 D55607      369      ;
0126 D284        370      ;
0127 C204        371      ;
0128 020139      372      ;
0129 020139      373      ;
012A 020139      374      ;
012B 020139      375      ;
012C 020139      376      ;
012D 020139      377      ;
012E 020139      378      ;
012F E555        379      ;
0130 120139      380      ;
0131 020139      381      ;
0132 92B4        382      ;
0133 020139      383      ;
0134 A555        384      ;
0135 020139      385      ;
0136 020139      386      ;
0137 020139      387      ;
0138 020139      388      ;
0139 020139      389      ;
013A 020139      390      ;
013B 020139      391      ;
013C 020139      392      ;
013D 020139      393      ;
013E 020139      394      ;
013F 020139      395      ;
0140 020139      396      ;
0141 020139      397      ;
0142 020139      398      ;
0143 020139      399      ;
0144 020139      400      ;
0145 020139      401      ;
0146 020139      402      ;
0147 020139      403      ;
0148 020139      404      ;
0149 020139      405      ;
014A 020139      406      ;
014B 020139      407      ;
014C 020139      408      ;
014D 020139      409      ;
014E 020139      410      ;
014F 020139      411      ;
0150 020139      412      ;
0151 020139      413      ;
0152 020139      414      ;
0153 020139      415      ;
0154 020139      416      ;
0155 020139      417      ;
0156 020139      418      ;
0157 020139      419      ;
0158 020139      420      ;
0159 020139      421      ;
015A 020139      422      ;
015B 020139      423      ;
015C 020139      424      ;
015D 020139      425      ;
015E 020139      426      ;
015F 020139      427      ;
0160 020139      428      ;
0161 020139      429      ;
0162 020139      430      ;
0163 020139      431      ;
0164 020139      432      ;
0165 020139      433      ;
0166 020139      434      ;
0167 020139      435      ;
0168 020139      436      ;
0169 020139      437      ;
016A 020139      438      ;
016B 020139      439      ;
016C 020139      440      ;
016D 020139      441      ;
016E 020139      442      ;
016F 020139      443      ;
0170 020139      444      ;
0171 020139      445      ;
0172 020139      446      ;
0173 020139      447      ;
0174 020139      448      ;
0175 020139      449      ;
0176 020139      450      ;
0177 020139      451      ;
0178 020139      452      ;
0179 020139      453      ;
017A 020139      454      ;
017B 020139      455      ;
017C 020139      456      ;
017D 020139      457      ;
017E 020139      458      ;
017F 020139      459      ;
0180 020139      460      ;
0181 020139      461      ;
0182 020139      462      ;
0183 020139      463      ;
0184 020139      464      ;
0185 020139      465      ;
0186 020139      466      ;
0187 020139      467      ;
0188 020139      468      ;
0189 020139      469      ;
018A 020139      470      ;
018B 020139      471      ;
018C 020139      472      ;
018D 020139      473      ;
018E 020139      474      ;
018F 020139      475      ;
0190 020139      476      ;
0191 020139      477      ;
0192 020139      478      ;
0193 020139      479      ;
0194 020139      480      ;
0195 020139      481      ;
0196 020139      482      ;
0197 020139      483      ;
0198 020139      484      ;
0199 020139      485      ;
019A 020139      486      ;
019B 020139      487      ;
019C 020139      488      ;
019D 020139      489      ;
019E 020139      490      ;
019F 020139      491      ;
01A0 020139      492      ;
01A1 020139      493      ;
01A2 020139      494      ;
01A3 020139      495      ;
01A4 020139      496      ;
01A5 020139      497      ;
01A6 020139      498      ;
01A7 020139      499      ;
01A8 020139      500      ;
01A9 020139      501      ;
01AA 020139      502      ;
01AB 020139      503      ;
01AC 020139      504      ;
01AD 020139      505      ;
01AE 020139      506      ;
01AF 020139      507      ;
01B0 020139      508      ;
01B1 020139      509      ;
01B2 020139      510      ;
01B3 020139      511      ;
01B4 020139      512      ;
01B5 020139      513      ;
01B6 020139      514      ;
01B7 020139      515      ;
01B8 020139      516      ;
01B9 020139      517      ;
01BA 020139      518      ;
01BB 020139      519      ;
01BC 020139      520      ;
01BD 020139      521      ;
01BE 020139      522      ;
01BF 020139      523      ;
01C0 020139      524      ;
01C1 020139      525      ;
01C2 020139      526      ;
01C3 020139      527      ;
01C4 020139      528      ;
01C5 020139      529      ;
01C6 020139      530      ;
01C7 020139      531      ;
01C8 020139      532      ;
01C9 020139      533      ;
01CA 020139      534      ;
01CB 020139      535      ;
01CC 020139      536      ;
01CD 020139      537      ;
01CE 020139      538      ;
01CF 020139      539      ;
01D0 020139      540      ;
01D1 020139      541      ;
01D2 020139      542      ;
01D3 020139      543      ;
01D4 020139      544      ;
01D5 020139      545      ;
01D6 020139      546      ;
01D7 020139      547      ;
01D8 020139      548      ;
01D9 020139      549      ;
01DA 020139      550      ;
01DB 020139      551      ;
01DC 020139      552      ;
01DD 020139      553      ;
01DE 020139      554      ;
01DF 020139      555      ;
01E0 020139      556      ;
01E1 020139      557      ;
01E2 020139      558      ;
01E3 020139      559      ;
01E4 020139      560      ;
01E5 020139      561      ;
01E6 020139      562      ;
01E7 020139      563      ;
01E8 020139      564      ;
01E9 020139      565      ;
01EA 020139      566      ;
01EB 020139      567      ;
01EC 020139      568      ;
01ED 020139      569      ;
01EE 020139      570      ;
01EF 020139      571      ;
01F0 020139      572      ;
01F1 020139      573      ;
01F2 020139      574      ;
01F3 020139      575      ;
01F4 020139      576      ;
01F5 020139      577      ;
01F6 020139      578      ;
01F7 020139      579      ;
01F8 020139      580      ;
01F9 020139      581      ;
01FA 020139      582      ;
01FB 020139      583      ;
01FC 020139      584      ;
01FD 020139      585      ;
01FE 020139      586      ;
01FF 020139      587      ;

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MCS-51 MACRO ASSEMBLER      SNEORT
LOC OBJ      LINE      SOURCE
0139 C3      364      CLR C          ; Update compare value with
013A 742C    365      MOV A, CCAP3L ; full bit time = 22CH
013B 256D    366      ADD A, CCAP3L
013C F56D    367      MOV CCAP3L, A
013D F56D    368      MOV A, #FULL_BIT_HIGH
013E 35FD    369      ADDC A, CCAP3H
013F 35FD    370      MOV CCAP3H, A
0140 F5FD    371      POP PSW
0141 D0D0    372      POP ACC
0142 D0D0    373      RETI
0143 D0D0    374      ;
0144 32      375      ;
0145 32      376      ;
0146 32      377      ;
0147 32      378      ;
0148 32      379      ; When a byte is received on the full-duplex serial port, it is then
0149 32      380      ; transmitted back to a "dummy" terminal. This terminal checks that
014A 32      381      ; the byte it transmitted to the PCA is the same value it receives back.
014B 32      382      ;
014C 32      383      ;
014D C0E0    384      SERIAL_PORT:
014E C0E0    385      PUSH ACC
014F 30980B  386      JNB RI, TXM ; Check whether RI or TI
0150 E599    387      MOV A, SBUF ; caused the interrupt
0151 C298    388      CLR RI
0152 4599    389      MOV SBUF, A
0153 4599    390      POP PSW
0154 D0E0    391      POP ACC
0155 32      392      RETI
0156 32      393      ;
0157 C299    394      TXM:
0158 D0D0    395      POP PSW
0159 D0E0    396      POP ACC
0160 32      397      ;
0161 32      398      ;
0162 32      399      ;
0163 32      400      END

REGISTER BANK(S) USED: 0
ASSEMBLY COMPLETE, NO ERRORS FOUND
    
```