M8085AH
8-BIT HMOS MICROPROCESSOR

Military

- **Single +5V Power Supply with 10% Voltage Margins**
- **Full Military Temperature Range: −55°C to +125°C (T_C)**
- **1.3 μs Instruction Cycle (M8085AH)**
- **100% Compatible with M8085A**
- **100% Software Compatible with M8080A**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is Non-Maskable) Plus an M8080A-Compatible Interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capablity to 64K Bytes of Memory**

The Intel M8085AH is a complete 8 bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the M8080A microprocessor, and it is designed to improve the present M8080A's performance by higher system speed. Its high level of system integration allows a minimum system of four IC's [M8085AH (CPU), M8155 (RAM/IO), M2764A (EPROM), and M8282 (Octal Latch)] while maintaining total system expandability.

The M8085AH incorporates all of the features that the M8224 (clock generator) and M8228 (system controller) provided for the M8080A, thereby offering a high level of system integration.

The M8085AH uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of M8155H/M8755A memory products allow a direct interface with the M8085AH.

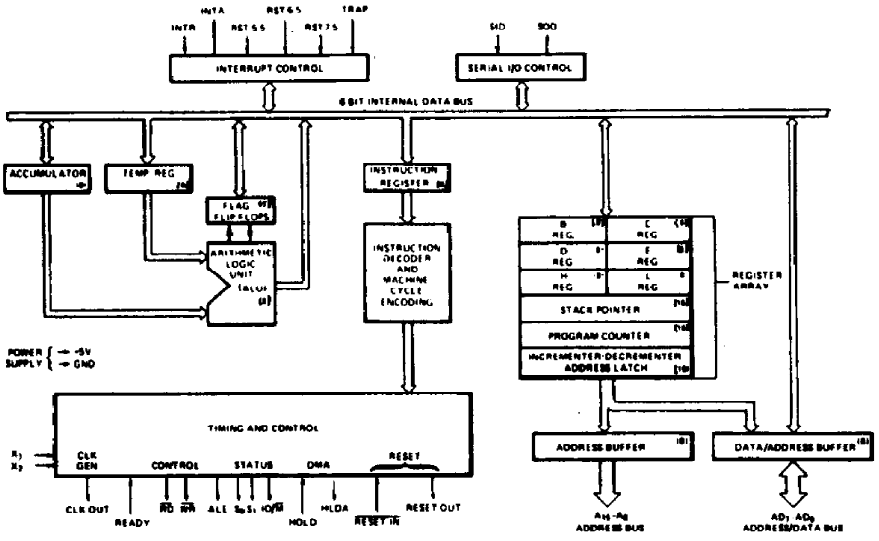

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Figure 1. M8085AH CPU Functional Block Diagram

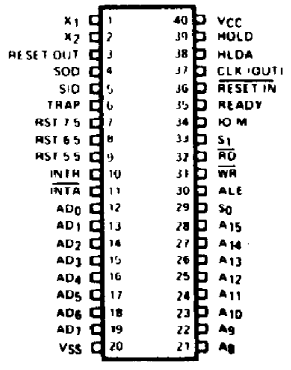

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Figure 2. M8085AH Pin Configuration

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November 1987
Order Number: 271019-002

Table 1. Pin Description

Symbol	Type	Name and Function
A_8–A_{15}	O	**ADDRESS BUS:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7}	I/O	**MULTIPLEXED ADDRESS/DATA BUS:** Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	**ADDRESS LATCH ENABLE:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0, S_1, and IO/$\overline{M}$	O	**MACHINE CYCLE STATUS:** IO/$\overline{M}$ / S_1 / S_0 / Status 0 / 0 / 1 / Memory write 0 / 1 / 0 / Memory read 1 / 0 / 1 / I/O write 1 / 1 / 0 / I/O read 0 / 1 / 1 / Opcode fetch 1 / 1 / 1 / Opcode fetch 1 / 1 / 1 / Interrupt Acknowledge * / 0 / 0 / Halt * / X / X / Hold * / X / X / Reset * = 3-state (high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.
$\overline{RD}$	O	**READ CONTROL:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**WRITE CONTROL:** A low level $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY	I	**READY:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	**HOLD:** Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**HOLD ACKNOWLEDGE:** Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.
INTR	I	**INTERRUPT REQUEST:** Is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
INTA	O	**INTERRUPT ACKNOWLEDGE:** Is used instead of (and has the same timing as) RD during the Instruction cycle after an INTR is accepted. It can be used to activate an M8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**RESTART INTERRUPTS:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.

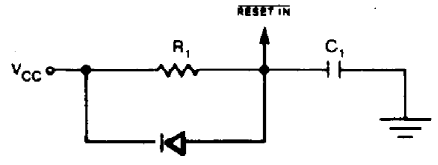
Table 1. Pin Description (Continued)

Symbol	Type	Name and Function
TRAP	I	**TRAP:** Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5–7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{\text{RESET IN}}$	I	**RESET IN:** Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, $\overline{\text{RESET IN}}$ must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration, $\overline{\text{RESET IN}}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT	O	**RESET OUT:** Reset Out indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2	I	**X_1 and X_2:** Are connected to a crystal LC or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	**CLOCK:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**SERIAL INPUT DATA LINE:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**SERIAL OUTPUT DATA LINE:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**POWER:** +5 volt supply.
V_{SS}		**GROUND:** Reference.

Table 2. Interrupt Priority, Restart Address and Sensitivity

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising Edge AND High Level Until Sampled
RST 7.5	2	3CH	Rising Edge Latched
RST 6.5	3	34H	High Level Until Sampled
RST 5.5	4	2CH	High Level Until Sampled
INTR	5	(Note 2)	High Level Until Sampled

NOTES:
1. The processor pushes the PC on the stack before branching to the indicated address.
2. The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.



Typical Power-On Reset RC Values*
R_1 = 75 KΩ
C_1 = 1 μF
*Values may have to vary due to applied power supply ramp up time

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Figure 3. Power-On Reset Circuit

NOTE:
Additional details on the M8085AH's operation are available by referring to the MCS-80/85 Microprocessor section of the **Microsystem Components Handbook.** Topics covered include: a functional description; interrupt and serial I/O operation; how to generate wait states; and driving the X_1 and X_2 (clock) inputs.
Basic system timing and interface techniques are also described.

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ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias(1) . −55°C to +125°C
Storage Temperature . . . . . −65°C to + 150°C
Voltage on Any Pin with
Respect to Ground . . . . . −0.5V to +7V
Power Dissipation 1.5W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_C(1) = −55°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V; unless otherwise specified

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{CC}	Power Supply Current		200	mA	
I_{IL1}	Input Leakage; Except Pin 1		±10	μA	$0 \le V_{IN} \le V_{CC}$
I_{IL2}	Input Leakage Pin 1		±70	μA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage		±10	μA	$0.45 \le V_{OUT} \le V_{CC}$
V_{ILR}	Input Low Level, RESET	−0.5	+0.8	V	
V_{IHR}	Input High Level, RESET	2.4	V_{CC} + 0.5	V	
V_{HY}	Hysteresis, RESET	0.25		V	

A.C. CHARACTERISTICS T_C(1) = −55°C to +125°C, V_{CC} = 5V ±10%, V_{SS} = 0V

Symbol	Parameter	M8085AH(2)		Units
		Min	Max	
t_{CYC}	CLK Clock Period	320	2000	ns
t_1	CLK Low Time (Standard CLK Loading)	80		ns
t_2	CLK High Time (Standard CLK Loading)	120		ns
t_r, t_f	CLK Rise and Fall Time		30	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control(1)	270		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE(1)	90		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	70		ns

NOTE:
1. Case temperatures are "instant on."

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	M8085AH(2)		Units
		Min	Max	
t_{ARY}	READY Valid from Address Valid		220	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		ns
t_{CC}	Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		ns
t_{HABE}	HLDA to Bus Enable		210	ns
t_{HABF}	Bus Float After HLDA		210	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		ns
t_{HDH}	HOLD Hold Time	0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		ns
t_{INH}	INTR Hold Time	0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		ns
t_{LA}	Address Hold Time After ALE	100		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		ns
t_{LCK}	ALE Low During CLK High	100		ns
t_{LDR}	ALE to Valid Data During Read		460	ns
t_{LDW}	ALE to Valid Data During Write		200	ns
t_{LL}	ALE Width	140		ns
t_{LRY}	ALE to READY Stable		110	ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$	0		ns
t_{RYH}	READY Hold Time	0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		ns
t_{WDL}	LEADING Edge of $\overline{WRITE}$ to Data Valid		40	ns

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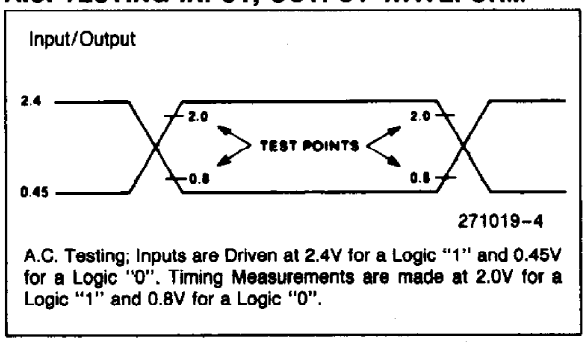
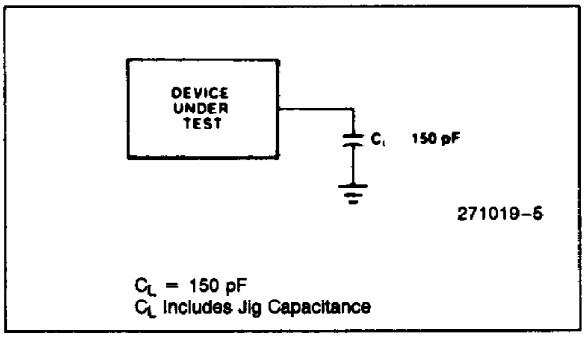
NOTES:
1. A_8–A_{15} address Specs apply IO/$\overline{M}$, S_0, and S_1 except A_8–A_{15} are undefined during T_4–T_6 of OF cycle whereas IO/$\overline{M}$, S_0, and S_1 are stable.
2. *Test Conditions*: t_{CYC} = 320 ns (M8085AH); C_L = 150 pF.
3. For all output timing where $C_L \neq 150$ pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF ≤ C_L ≤ 300 pF; +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. To calculate timing specifications at other values of t_{CYC} use Table 5.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. Testing; Inputs are Driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 150 pF
C_L Includes Jig Capacitance

Table 5. Bus Timing Specification as T_{CYC} Dependent

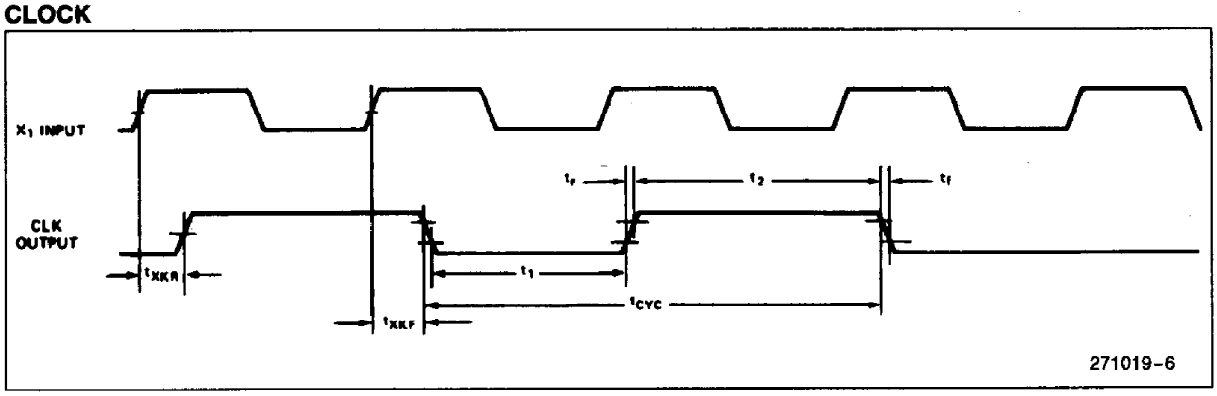
Symbol	M8085AH	
t_{AL}	(1/2) T − 45	Minimum
t_{LA}	(1/2) T − 60	Minimum
t_{LL}	(1/2) T − 20	Minimum
t_{LCK}	(1/2) T − 60	Minimum
t_{LC}	(1/2) T − 30	Minimum
t_{AD}	(5/2 + N) T − 225	Maximum
t_{RD}	(3/2 + N) T − 180	Maximum
t_{RAE}	(1/2) T − 10	Minimum
t_{CA}	(1/2) T − 40	Minimum
t_{DW}	(3/2 + N) T − 60	Minimum
t_{WD}	(1/2) T − 60	Minimum

Symbol	M8085AH	
t_{CC}	(3/2 + N) T − 80	Minimum
t_{CL}	(1/2) T − 110	Minimum
t_{ARY}	(3/2) T − 260	Maximum
t_{HACK}	(1/2) T − 50	Minimum
t_{HABF}	(1/2) T + 50	Maximum
t_{HABE}	(1/2) T − 50	Maximum
t_{AC}	(2/2) T − 50	Minimum
t_1	(1/2) T − 80	Minimum
t_2	(1/2) T − 40	Minimum
t_{RV}	(3/2) T − 80	Minimum
t_{LDR}	(4/2) T − 180	Minimum

NOTE:
N is equal to the total WAIT states. T = t_{CYC}.

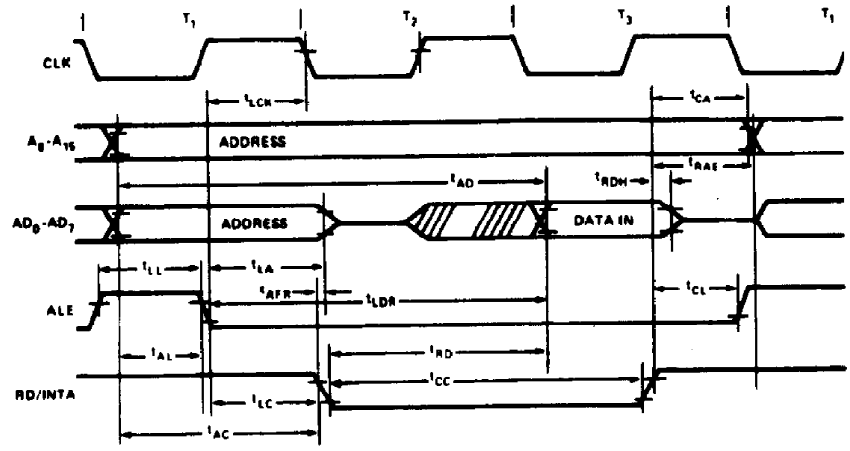
WAVEFORMS

CLOCK

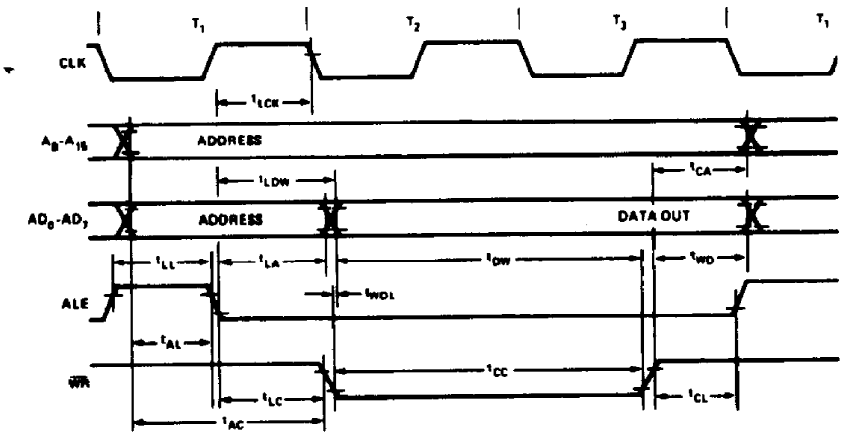


WAVEFORMS (Continued)

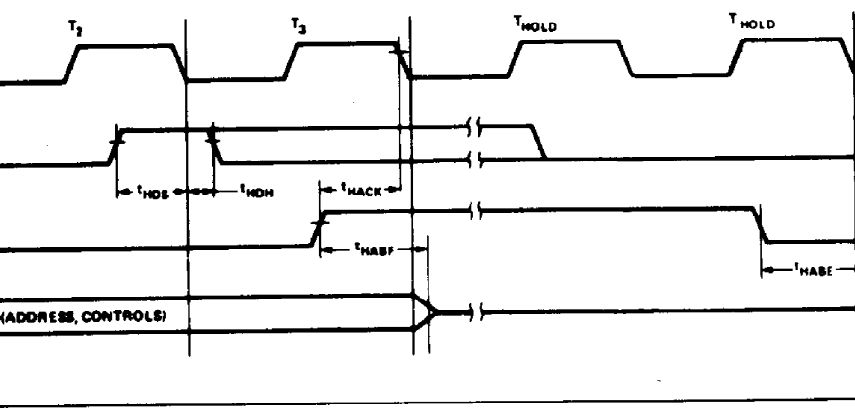
READ



WRITE



HOLD



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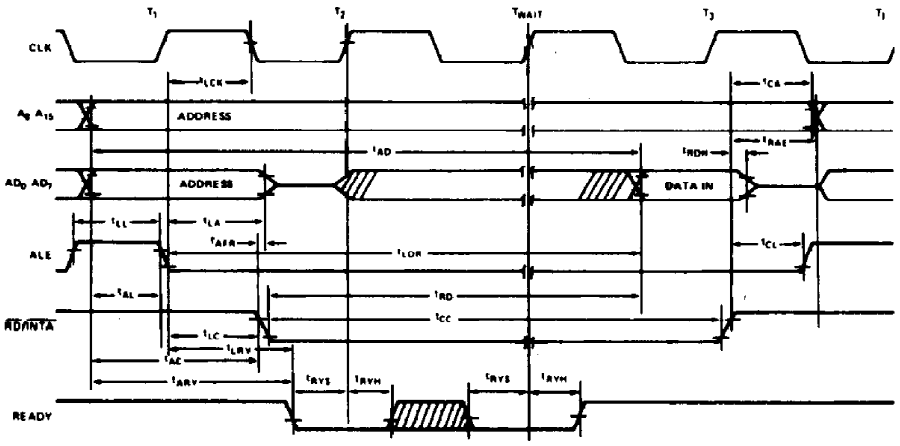
WAVEFORMS (Continued)

READ OPERATION WITH WAIT CYCLE (TYPICAL) — SAME READY TIMING APPLIES TO WRITE



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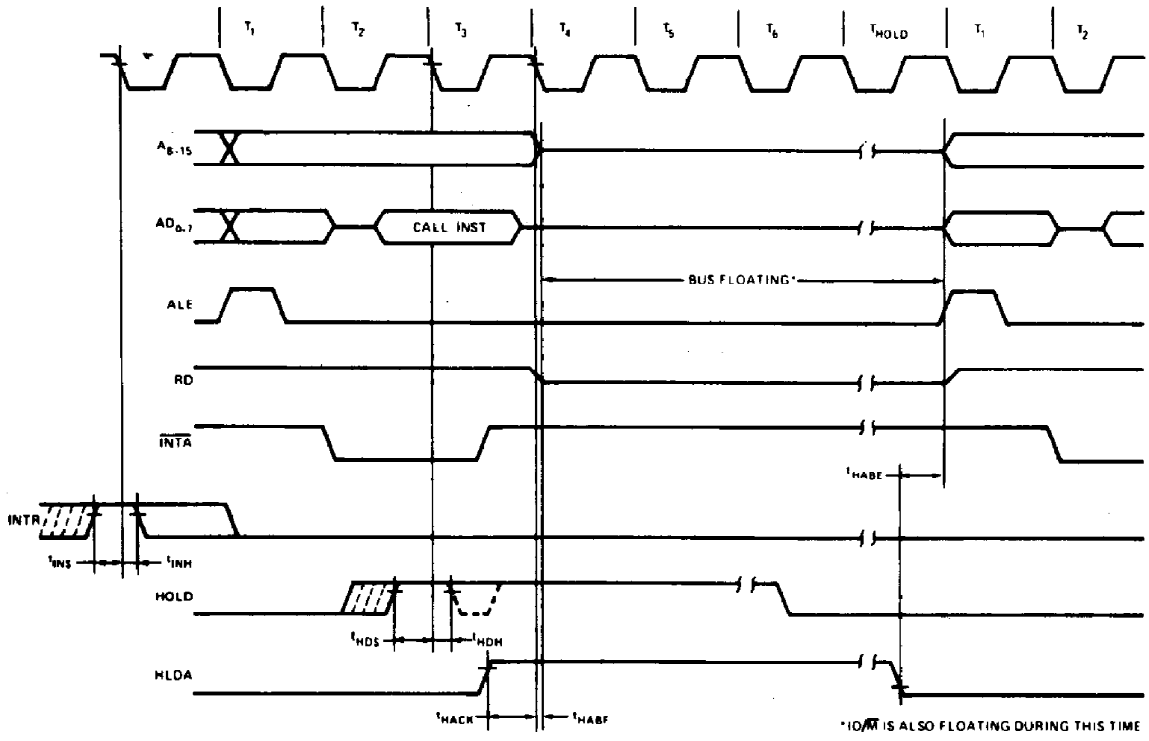
NOTE:
1. Ready must remain stable during setup and hold times.

INTERRUPT AND HOLD



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