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80960MX
SPECIFICATION UPDATE

The 80960MX may contain design defects or errors known as errata which may cause the 80960MX to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Rev. Date	Version	Description
July, 1997	002	Revised Errata #5 and #6. Added Errata #8.
July 20, 1996	001	This is the new Specification Update document. It contains all identified errata published prior to this date.
Mar. 28, 1996	2.00	Arctangent Limitation
Nov. 16, 1994	1.09	New microcode release #P12C19447005 and the deletion of errata #6, #7, and #8.
Nov. 11, 1994	1.08	Further clarification of errata #8.
Sep. 22, 1994	1.07	Deletion of errata #8 (bus queues) and addition of new errata #8.
Aug. 2, 1994	1.06	Addition of errata #8.
June 29, 1994	1.05	Addition of errata #6 and #7.
	1.04	New microcode release #P12C1941004 and deletion of errata #6.
	1.03	Added errata #4 and #5.
	1.02	New microcode release #P12C19349003 and the deletion of errata #3. Errata #4 now becomes errata #3.
	1.01	Added errata #3 and #4.
	1.00	New microcode release #P12C19342002.

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PREFACE

As of July, 1996, Intel has consolidated available historical device and documentation errata into this document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
i960® MM/MX Processor Hardware Reference Manual	271274
Military i960® MM/MX Superscalar Processor	271194

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80960MX product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

❚	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Rev. #	Steppings			Page	Status	ERRATA
	A	B	C			
1			X	8	NoFix	No External IACs when Global Interrupts are Disabled
2			X	8	NoFix	False Arithmetic Status when Using REMR or REMRL
3			X	8	NoFix	Global Stacks and Local Registers Cause Processor Hang
4			X	9	NoFix	ACs Invalidation
5			X	9	NoFix	Flush/Modify Coherency of External Cache IAC issue
6			X	10	NoFix	Arctangent Limitations
7			X	10	NoFix	Trigonometric Calculation Error
8			X	10	NoFix	Incoherent Data between Internal Data Cache and Memory

Specification Changes

Rev. #	Steppings			Page	Status	SPECIFICATION CHANGES
	A	B	C			
						None for this revision of this specification update.

Specification Clarifications

Rev. #	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

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Documentation Changes

Rev. #	Document Revision	Page	Status	DOCUMENTATION CHANGES
				None for this revision of this specification update.

IDENTIFICATION INFORMATION

Markings

This product is sold in Die and Wafer form only. No mark is provided. All products sold with assembly seal date code after 9445 is C-1 stepping.

Mark Specifications:

Mxxxxxxx-xx/B	= Product Marketing Name
FFFFFFFF	= FPO#
(	= ESD Classification Indicator
YYWW	= Assembly Seal Date Code
XX	= Country of Origin
C	= Indication Compliance to MIL-STD-**#
[M] [C] ZZZZ	= Mask Copyright Date

ERRATA

1.   *No External IACs when Global Interrupts are Disabled*

PROBLEM: If the Global Interrupt Disable bit is set in the Interrupt Controls Register or any Process Controls Register, the processor will not accept external (hardware) Inter-Agent Communications (IACs).

With any Global Interrupt Disable bit set, all the external IACs are disabled. The disable function does not affect the internal IACs via instructions such as synmovq and selfiac.

IMPLICATION: Additional IAC control is required.

WORKAROUND: Software must clear the Global Interrupt Disable bit via a MODPC instruction or Set Interrupt Registers software IAC after the original IAC was sent. Hardware should continue to assert external IAC pin until the IAC acknowledge is sent.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

2.   *False Arithmetic Status when Using REMR or REMRL*

PROBLEM: The arithmetic status is set incorrectly in the Arithmetic Controls Register after the execution of REMR or REMRL.

REMR/REMRL instructions sometimes return the wrong value of arithmetic status in the Arithmetic Controls Register (bits 3-6) if bus queues are OFF and NIF (no imprecise faults) mode is ON. Bus queues are OFF if bit 6 in the MX Bus Controls register is reset and NIF mode is ON if bit 15 in the Arithmetic Controls register is set.

IMPLICATION: Could provide false information during execution of REMR and REMRL.

WORKAROUND: Don't use Bus queues OFF and NIF mode ON together.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

3.   *Global Stacks and Local Registers Cause Processor Hang*

PROBLEM: If the lifetime of the stack object is global and the local register contains a local access descriptor (AD), then the processor may hang.

If the stack object is global (with global lifetime) and one of the local register frames contains an AD to a local object (local lifetime), then the processor may hang if processor timing is on.

IMPLICATION: No additional hardware fixes will be implemented.

WORKAROUND: Don't define user processes as global and stacks of user processes as global. If user processes and stacks are defined as global, then turn timing off.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

4. ACs Invalidation

PROBLEM: None of the initialization IACs invalidate Icache.

The following IACs do not invalidate the internal Icache: Restart Processor IAC, Warmstart Processor IAC, Reinitialization IAC, Continue Initialization IAC.

IMPLICATION: Causes the use of additional instructions, increasing program execution time.

WORKAROUND: The user should issue the Purge Instruction Cache IAC before issuing any of the above IACs if it is necessary to invalidate the internal Icache.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

5. Flush/Modify Coherency of External Cache IAC issue

PROBLEM: The Flush/Modify Coherency of External Cache IAC does not work correctly.

When the match bit is set to a logic low in field 2 of this IAC, the processor should check for the address match. If it is a match, the data should be flushed out to memory. If it is not a match, the processor should go to the next address. Currently if it is not a match, the processor will read the data from local memory and put it into the backside cache and report a hit. The processor will modify the state bits in the external cache as specified by bits 6 & 7 of field 2.

IMPLICATION: This could cause false data to be placed into the backside cache.

WORKAROUND: Always set bit 2 of field 2 to a logic high to disable match feature.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

6. Arctangent Limitations

PROBLEM: When performing an ATANRL function (dst:=atanrl(src2/src1)), with the quotient of src1 and src2 larger than ±32K

(32768 < quot < -32768)

the processor may lock up. Hardware reset is required to recover from lockup condition.

IMPLICATION: Limits the range of this function.

WORKAROUND: Limit the numerator (src2) and denominator (src1) variables to provide a quotient within ±32K (±32768).

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

7. Trigonometric Calculation Error

PROBLEM: When performing a trigonometric function with the following conditions, the calculation could produce an incorrect result. Conditions:

1. The Trace Enable bit is set in the Process Controls Register (bit 0).
2. The Instruction Trace Mode bit is set in the Trace Controls Register (bit 1).

IMPLICATION: Could provide false results during trigonometric calculations.

WORKAROUND: Enable both floating-point overflow and underflow masks in the Arithmetic Control Register (bits 24-25) during trace mode OR write a software version of the trigonometric function.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

8. Incoherent Data between Internal Data Cache and Memory

PROBLEM: A complex addressing store instruction creates an opportunity for an incorrect internal data cache entry.

Under certain cases during MEMB addressing store instructions, an internal signal, redo-memory (REDO), is generated. A collision of this signal and a "fill" to internal data cache will cause the store to be canceled, thus canceling internal data cache update. External Memory is updated but incoherent data exists in the cache, which could be accessed by a subsequent load instruction. In addition, a random "invalidate" of a valid internal data cache entry could occurs.

The REDO signal is generated by the following:

If there is a carry out of the addition of the lower 12 bits of the addressing calculation then the guessed 32 bit address is not the same as the actual one. OR if the AND of the upper 20 bits (of the two sources) are non zero (making the added value different from the ORed value) then high else low.

Example:

A case like 777777+888888 would not produce a redo, because the added and ORed values are the same.

IMPLICATION: This creates incoherent data between Internal Data Cache and Memory.

WORKAROUND: Any of the following will prevent the problem from occurring:

1. Avoid complex addressing loads and stores. Reference: Register Indirect with Index Addressing Mode section on page 8-15 in the Programmer's Reference Manual.
2. Replace complex addressing instructions with indirect addressing.

    i.e.

    Replace:

    st r3,INDX+OFFSET(g0)

    With:

    lda INDX+OFFSET(g0),g12
    st r3,(g12)

3. Disable internal data cache.

STATUS: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

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DOCUMENTATION CHANGES

None for this revision of this specification update.