80960KA/KB
SPECIFICATION UPDATE

Release Date: June, 1997
Order Number: 272851-002

The 80960KA/KB may contain design defects or errors known as errata which may cause the 80960KA/KB to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect IL 60056-7641

or call in North America 1-800-879-4683, Europe 44-0-1793-431-155,
France 44-0-1793-421-777, Germany 44-0-1793-421-333, other countries 708-296-9333

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REVISION HISTORY

Intel has manufactured the 80960KA/KB under two series of steppings, known respectively as "Non-Shrink" and "Shrink" to denote manufacturing processes. Intel currently manufactures all 80960KA/KB devices using the "Shrink" Process 648. Therefore, the complete name of the C stepping is "Shrink C" stepping.

The C stepping corrected a number of errata and incorporated other changes to improve manufacturability in plastic packages. Minor changes have since been made via segmentation and metal line organization for manufacturability. There have been no further logic modifications.

Date of Revision	Version	Description
6/30/97	002	Added Errata #4. Added Document Change #1. Added Document Change #2.
07/01/96	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Electrical specifications for these products are found in the following documents:

Title	Order
80960KA Embedded 32-Bit Processor datasheet	270775
80960KB Embedded 32-Bit Processor with Integrated Floating-Point Unit datasheet	270565

Functional descriptions for these products are found in the following documents:

Title	Order
i960® KA/KB Microprocessor Programmer's Reference Manual	270567
80960KB Hardware Designer's Reference Manual	270564

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

SUMMARY TABLE OF CHANGES

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 80960KA/KB product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings				Page	Status	ERRATA
	A	B	C	C-2			
1			X		8	NoFix	ALE# Does Not Function in Secondary Bus Master Mode
2			X		8	NoFix	Problem Using HLDA and ADS# with Asynchronous Logic
3			X		9	NoFix	Breakpoint Register Initialization
4	X	X	X	X	9	NoFix	Undocumented Register Flushes on Interrupt Return for the 80960KA/KB Microprocessors

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	#	#	#			
						None for this revision of this specification update.

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	#	#	#			
						None for this revision of this specification update.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	270775-005 270565-007	13		Page 8, Table 3
2	270775-005 270565-007	13		Page 22, Figure 18

IDENTIFICATION INFORMATION

Markings

As of January 1994, all 80960KA/KB, A80960KA/KB, TA80960KA/KB, and NG80960KA devices will be marked with stepping numbers.

Unless otherwise documented, 80960KA/KB devices marked with other specification numbers belong to different steppings. Be sure you have a correct technical bulletin for the devices at hand.

Stepping register

The following table applies to all C stepping devices:

Part Number	Specification Number	Package	Status
A80960KA	C	PGA-132	Current
A80960KB	C	PGA-132	Current
TA80960KA	C	PGA-132 Extended Temp.	Current
TA80960KB	C	PGA-132 Extended Temp.	Current
NG80960KA	C	PQFP-132	Current
NG80960KB	C	PQFP-132	Current
TG80960KA	C	PQFP-132 Extended Temp	Current
TG80960KB	C	PQFP-132 Extended Temp	Current
A80960KA-10	S V835	PGA-132	Obsolete
TA80960KA-10	S V862	PGA-132 Extended Temp.	Obsolete
A80960KA-16	S V806	PGA-132	Obsolete
TA80960KA-16	S V863	PGA-132 Extended Temp.	Obsolete
A80960KA-20	S V807	PGA-132	Obsolete
TA80960KA-20	S V864	PGA-132 Extended Temp.	Obsolete
A80960KA-25	Q 348	PGA-132 Special	Obsolete
A80960KA-25	S I25	PGA-132 Special	Obsolete
A80960KA-25	S N098	PGA-132 Special	Obsolete
A80960KA-25	S V808	PGA-132	Obsolete
TA80960KA-25	Q 348	PGA-132 Special	Obsolete
TA80960KA-25	S V865	PGA-132 Extended Temp.	Obsolete

QA80960KA-25	Q 348	PGA-132 Extended BI	Obsolete
A80960KB-10	S V836	PGA-132	Obsolete
TA80960KB-10	S V866	PGA-132 Extended Temp.	Obsolete
A80960KB-16	S V809	PGA-132	Obsolete
TA80960KB-16	S V867	PGA-132 Extended Temp.	Obsolete
A80960KB-20	S I25	PGA-132 Special	Obsolete
A80960KB-20	S V810	PGA-132	Obsolete
LA80960KB-20	S W137	PGA-132 Ext. Temp & BI	Obsolete
TA80960KB-20	S V868	PGA-132 Extended Temp.	Obsolete
A80960KB-25	Q 8276	PGA-132	Obsolete
A80960KB-25	S V811	PGA-132	Obsolete
TA80960KB-25	S V869	PGA-132 Extended Temp.	Obsolete
A80960MC-16	S V942	PGA-132 Special	Obsolete
KD80960KA-10	S V777	PQFP-132 Multi-Layer	Obsolete
KD80960KA-10	S V972	PQFP-132 Multi-Layer	Obsolete
KD80960KA-16	S V483	PQFP-132 Multi-Layer	Obsolete
KD80960KA-20	S V484	PQFP-132 Multi-Layer	Obsolete
KD80960KB-10	S V778	PQFP-132 Multi-Layer	Obsolete
KD80960KB-16	S V485	PQFP-132 Multi-Layer	Obsolete
KD80960KB-20	S V486	PQFP-132 Multi-Layer	Obsolete
NG80960KA-10	S V925	PQFP-132	Obsolete
NG80960KA-16	S V926	PQFP-132	Obsolete
NG80960KA-20	S V927	PQFP-132	Obsolete
NG80960KA-20	S W158	PQFP-132 Special	Obsolete
NG80960KA-25	Q 8117	PQFP-132 Special	Obsolete
NG80960KB-10	S V928	PQFP-132	Obsolete
NG80960KB-16	S V929	PQFP-132	Obsolete
NG80960KB-20	S V930	PQFP-132	Obsolete

ERRATA

1. ALE# Does Not Function in Secondary Bus Master Mode

PROBLEM: When two 80960KA/KB processors share the same local bus in a Primary Bus Master (PBM)/Secondary Bus Master (SBM) relationship, ALE# does not work on the Secondary Bus Master.

IMPLICATION: This erratum effectively makes "bus re-enter" operation impossible.

WORKAROUND: None.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

2. Problem Using HLDA and ADS# with Asynchronous Logic

PROBLEM: Asynchronous logic connected to the HLDA and ADS# pins may malfunction due to ground bounce on these outputs. The problem occurs when address/data buffers switch from a high state to a low state.

This problem exists on devices in both the PGA and PQFP packages. On the 80960KA/KB device, the LAD bus buffers share a ground with the buffers for the ADS#, HLDA, DT/R#, W/R#, ALE#, BE2#, BE1#, BE0#, CACHE and INTA pins. In addition to ground bounce on the ADS# and HLDA pins, it may be possible to observe ground bounce, undershoot and overshoot on other pins from this group.

The problem depends on how many outputs switch, proximity to the switching outputs and proximity to ground pads on the die. The worst case situation occurs when all address/data outputs switch simultaneously.

IMPLICATION: None

WORKAROUND: Logic external to the 80960KA/KB processor should sample HLDA synchronously on an "A" or "D" clock edge. ADS# can be sampled synchronously on an "A", "C", or "D" clock edge. Check setup and hold times carefully.

All 80960KA/KB processor designs must consider good power and ground distribution and decoupling techniques. As with all i960 family designs, a multi-layer circuit board is recommended. Use of a multi-layer board will not eliminate this problem, but may lessen its effects.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

3. Breakpoint Register Initialization

PROBLEM: There are two breakpoint registers on the 80960Kx. These registers can be written using the Set Breakpoint Register IAC only, and they cannot be read. Bits 2-31 of the register contain the address on which to break, and bit 1 enables or disables the breakpoint. These registers are not set to a specific value during initialization, and may be enabled upon powerup. This could cause sporadic breakpoints to occur if tracing is enabled in the process controls and breakpoint trace mode is enabled in the trace controls.

IMPLICATION: This errata does not affect the normal function of the breakpoint registers.

WORKAROUND: Disable the breakpoints using the Set Breakpoint Register IAC to set bit 1 of both registers to 1. Alternatively, if breakpoints are not being used, do not set the breakpoint trace mode bit in the trace controls.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

4. Undocumented Register Flushes on Interrupt Return for the 80960KA/KB Microprocessors

PROBLEM: The 80960Kx processors may execute unnecessary local register set flushes on interrupt return. The flushes occur when the working register belongs to an interrupt service routine (isr), and a ***return*** instruction is executed. The interrupt return flushes every register set in the cache excluding the set belonging to the procedure that was interrupted.

Example One: (A) function #1 is the only register set in the cache and is interrupted by isr #1. (B) on the return from interrupt, the function #1 register set is reinstated as the working set with no sets flushed to the stack.

Example Two: (A) function #1 calls function #2, which calls function #3; function #3 is interrupted by isr #1. On the return from interrupt, function #1 and function #2 are flushed to the stack. (B) function #3 is reinstated as the working register set.

Example Three: (A) function #3 is interrupted by isr #1 which is interrupted by an isr of higher priority, isr #2. On return from interrupt, function #3 is flushed to the procedure stack. Isr #1 is reinstated as the working register. (B) On the interrupt return from isr #1, there are no sets in the cache to flush. (C) The processor must perform a register cache fill from the procedure stack.

Notice that on return from the only active isr, the working register set belongs to the first interrupted procedure and the remainder of the cache is invalid.

IMPLICATION: The flushes are transparent to the user; however, they will cause an unexpected increase in interrupt latency.

WORKAROUND: Accommodate the longer interrupt return latency. Otherwise, prevent any combination of nested functions and/or interrupts.

STATUS: Refer to Summary Table of Changes to determine the affected stepping(s).

SPECIFICATION CHANGES

None for this revision of this specification update.

SPECIFICATION CLARIFICATIONS

None for this revision of this specification update.

DOCUMENTATION CHANGES

1. Page 8, Table 3

ISSUE: $\overline{\text{DEN}}$ pin description omitted.

AFFECTED DOCUMENT(S): *80960KA Embedded 32-Bit Microprocessor* Data Sheet, #270775-005 and *80960KB Embedded 32-Bit Microprocessor with Integrated Floating-Point Unit* Data Sheet, #270565-007.

2. Page 22, Figure 18

ISSUE: Pins M2 and M13 are incorrectly shown:

"M2 was NC and M13 was V_{CC}"

The corrected text shows:

"M2 is V_{CC} and M13 is NC"

AFFECTED DOCUMENT(S): *80960KA Embedded 32-Bit Microprocessor* Data Sheet, #270775-005 and *80960KB Embedded 32-Bit Microprocessor with Integrated Floating-Point Unit* Data Sheet, #270565-007.

Table 3. 80960KA Pin Description: L-Bus Signals (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLK2	I	**SYSTEM CLOCK** provides the fundamental timing for 80960KA systems. It is divided by two inside the 80960KA to generate the internal processor clock.
LAD31:0	I/O T.S.	**LOCAL ADDRESS / DATA BUS** carries 32-bit physical addresses and data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, bits 0-31 contain read or write data. These pins float to a high impedance state when not active. Bits 0-1 comprise SIZE during a T_a cycle. SIZE specifies burst transfer size in words. LAD1 LAD0 0 0 1 Word 0 1 2 Words 1 0 3 Words 1 1 4 Words
$\overline{ALE}$	O T.S.	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. $\overline{ALE}$ is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active LOW and floats to a high impedance state during a hold cycle (T_h).
$\overline{ADS}$	O O.D.	**ADDRESS/DATA STATUS** indicates an address state. $\overline{ADS}$ is asserted every T_a state and deasserted during the following T_d state. For a burst transaction, $\overline{ADS}$ is asserted again every T_d state where $\overline{READY}$ was asserted in the previous cycle.
W/$\overline{R}$	O O.D.	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles.
DT/$\overline{R}$	O O.D.	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the L-Bus. It is low during T_a and T_d cycles for a read or interrupt acknowl-edgment; it is high during T_a and T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted.
$\overline{DEN}$	O O.D.	**DATA ENABLE** (active low) enables data transceivers. The processor asserts DEN# during all Td and Tw states. The DEN# line is an open drain-output of the 80960KB-processor.
$\overline{READY}$	I	**READY** indicates that data on LAD lines can be sampled or removed. If $\overline{READY}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w) and $\overline{ADS}$ is not asserted in the next cycle.
$\overline{LOCK}$	I/O O.D.	**BUS LOCK** prevents bus masters from gaining control of the L-Bus during Read/Modify/Write (RMW) cycles. The processor or any bus agent may assert $\overline{LOCK}$. At the start of a RMW operation, the processor examines the $\overline{LOCK}$ pin. If the pin is already asserted, the processor waits until it is not asserted. If the pin is not asserted, the processor asserts $\overline{LOCK}$ during the T_a cycle of the read transaction. The processor deasserts $\overline{LOCK}$ in the T_a cycle of the write transaction. During the time $\overline{LOCK}$ is asserted, a bus agent can perform a normal read or write but not a RMW operation. The processor also asserts $\overline{LOCK}$ during interrupt-acknowledge transactions. Do not leave $\overline{LOCK}$ unconnected. It must be pulled high for the processor to function properly.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

ERRATA - 6/13/97
$\overline{DEN}$ pin description omitted.

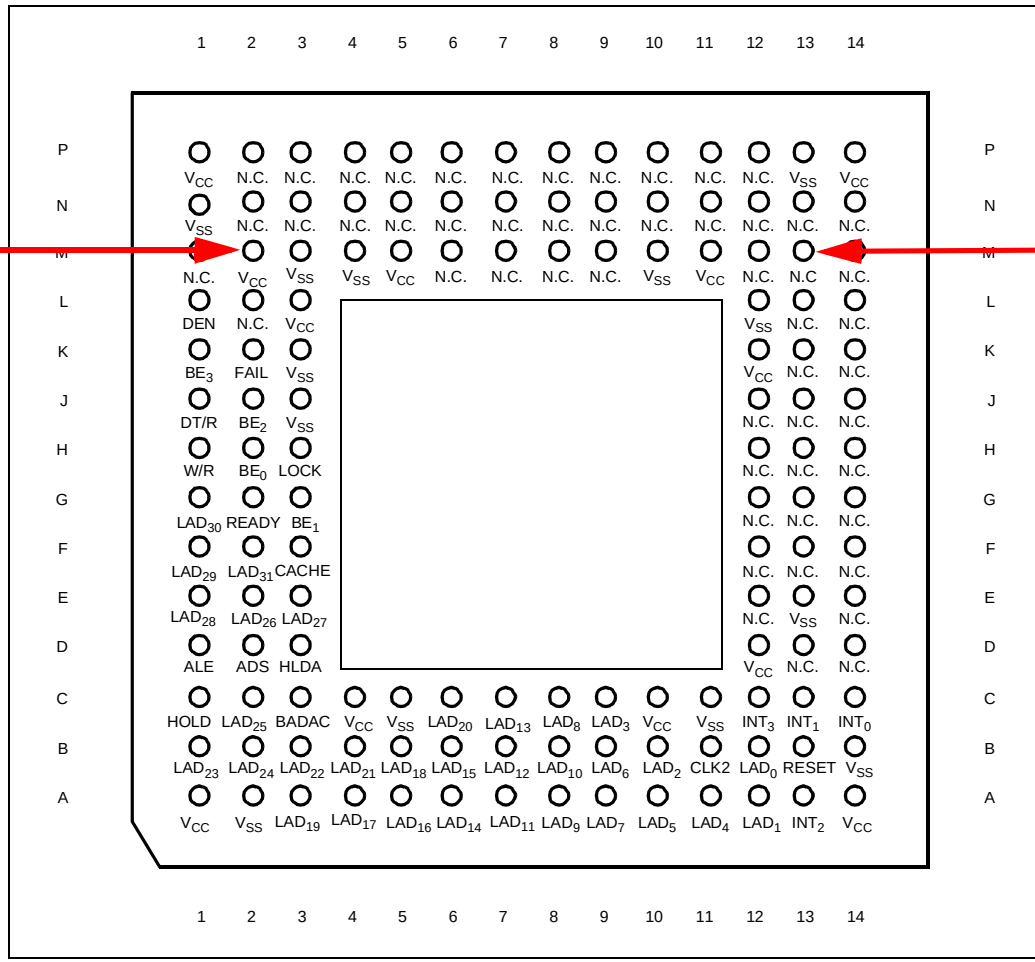

Figure 18. 80960KA PGA Pinout—View from Bottom (Pins Facing Up)

ERRATA: 6-17-97

Pin M2 was N.C.; should be V_{CC}.

Pin M13 was V_{CC}; should be N.C.

This page now shows it correctly.

Table 4. 80960KB Pin Description: L-Bus Signals (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLK2	I	**SYSTEM CLOCK** provides the fundamental timing for 80960KB systems. It is divided by two inside the 80960KB and four 80-bit registers (FP0 through FP3) to generate the internal processor clock.
LAD31:0	I/O T.S.	**LOCAL ADDRESS / DATA BUS** carries 32-bit physical addresses and data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, bits 0-31 contain read or write data. These pins float to a high impedance state when not active. Bits 0-1 comprise SIZE during a T_a cycle. SIZE specifies burst transfer size in words. LAD1 LAD0 0 0 1 Word 0 1 2 Words 1 0 3 Words 1 1 4 Words
$\overline{ALE}$	O T.S.	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. $\overline{ALE}$ is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active LOW and floats to a high impedance state during a hold cycle (T_h).
$\overline{ADS}$	O O.D.	**ADDRESS/DATA STATUS** indicates an address state. $\overline{ADS}$ is asserted every T_a state and deasserted during the following T_d state. For a burst transaction, $\overline{ADS}$ is asserted again every T_d state where $\overline{READY}$ was asserted in the previous cycle.
W/$\overline{R}$	O O.D.	**WRITE/READ** specifies, during a T_a cycle, whether the operation is a write or read. It is latched on-chip and remains valid during T_d cycles.
DT/$\overline{R}$	O O.D.	**DATA TRANSMIT / RECEIVE** indicates the direction of data transfer to and from the L-Bus. It is low during T_a and T_d cycles for a read or interrupt acknowl-edgment; it is high during T_a and T_d cycles for a write. DT/$\overline{R}$ never changes state when $\overline{DEN}$ is asserted.
$\overline{DEN}$	O O.D.	**DATA ENABLE** (active low) enables data transceivers. The processor asserts DEN# during all Td and Tw states. The DEN# line is an open drain-output of the 80960KB-processor.
$\overline{READY}$	I	**READY** indicates that data on LAD lines can be sampled or removed. If $\overline{READY}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w) and $\overline{ADS}$ is not asserted in the next cycle.
$\overline{LOCK}$	I/O O.D.	**BUS LOCK** prevents bus masters from gaining control of the L-Bus during Read/Modify/Write (RMW) cycles. The processor or any bus agent may assert $\overline{LOCK}$. At the start of a RMW operation, the processor examines the $\overline{LOCK}$ pin. If the pin is already asserted, the processor waits until it is not asserted. If the pin is not asserted, the processor asserts $\overline{LOCK}$ during the T_a cycle of the read transaction. The processor deasserts $\overline{LOCK}$ in the T_a cycle of the write transaction. During the time $\overline{LOCK}$ is asserted, a bus agent can perform a normal read or write but not a RMW operation. The processor also asserts $\overline{LOCK}$ during interrupt-acknowledge transactions. Do not leave $\overline{LOCK}$ unconnected. It must be pulled high for the processor to function properly.

I/O = Input/Output, O = Output, I = Input, O.D. = Open Drain, T.S. = Three-state

ERRATA - 6/13/97
$\overline{DEN}$ pin description omitted.

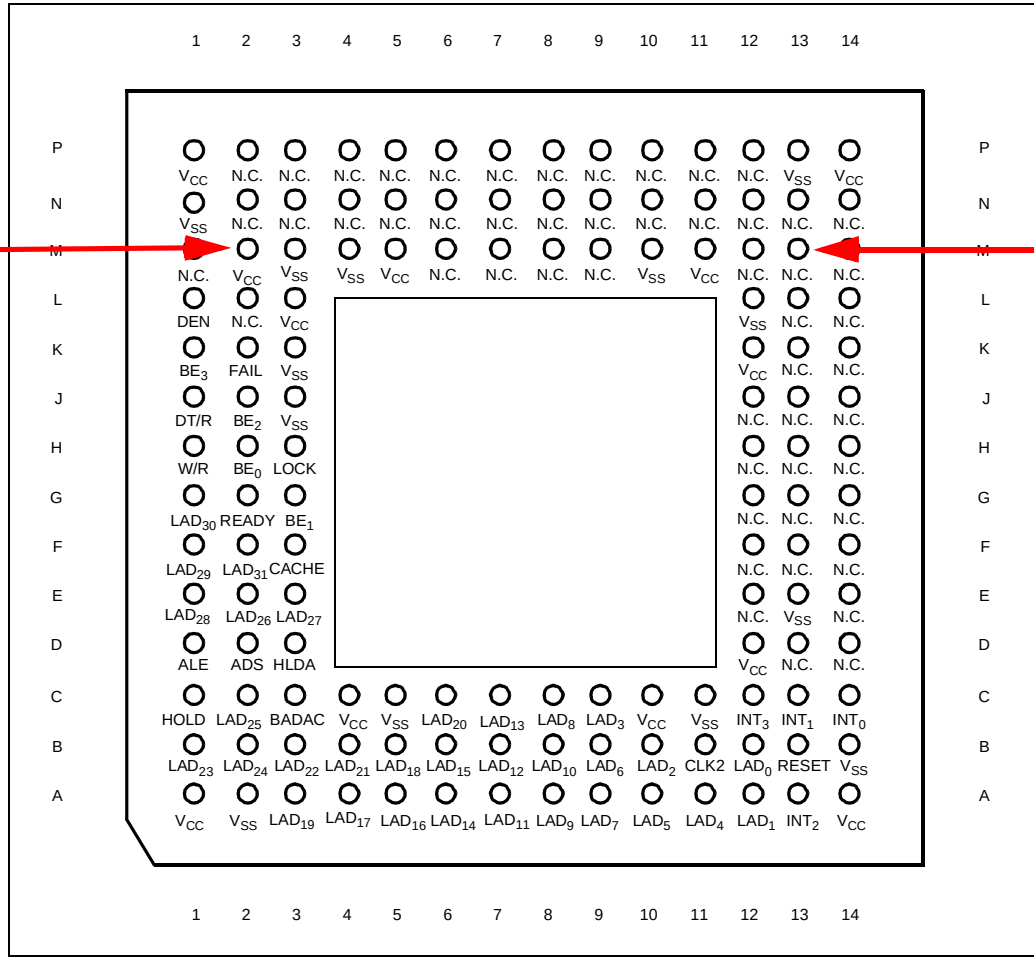

Figure 18. 80960KB PGA Pinout—View from Bottom (Pins Facing Up)

ERRATA

6-17-97:

Pin M2 was N.C.; should be V_{CC}.

Pin M13 was V_{CC}; should be N.C.

This page now shows it correctly.