80L960JA/JF Processor Conversion to 80960Jx 3.3 V, 5 V Tolerant Processor

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1.0 Introduction

This paper addresses the issues that arise when converting an 80L960JA/JF processor design to the new 80960Jx 3.3 V, 5 V I/O tolerant processor. The 80L960JA/JF processors support 3.3 V external logic only and therefore requires the use of translation devices to interface to 5 V external logic. The new 80960Jx 3.3 V, 5 V I/O tolerant processors have built-in support for interface to 3.3 V and 5 V external logic.

Converting to the 80960 3.3 V, 5 V tolerant processor will allow a performance upgrade to the 33 MHz 80960JA/JF, the clock doubled 80960JD and the clock tripled 80960JT processors. All these processors are code and pin compatible.

Areas of concern when converting a 3.3 V 80L960JA/JF design to the 3.3 V, 5 V tolerant 80960JA/JF processor are:

- Package Pin-outs; A PCB layout change is needed to accommodate the VCC5 pin.
- Device ID; Software that recognizes the on-chip device ID must be updated.
- AC Timings; Timings must be re-evaluated in light of new timing specifications.
- Thermals; Thermal performance requires no design change.
- Functional Considerations; Both processors function identically.

The above topics are discussed in detail later in this document.

Refer to the appropriate data sheet corresponding to the particular device and speed grade for specific timing and I_{CC} values. Up-to-date data sheets can be found at Intel's developer web site located at: http://Developer.Intel.com/design/i960 or by calling Intel's literature center at:

1-800-548-4725.

- *80960JA/JF/JD/JT 3.3V Embedded 32-bit Microprocessor* Data Sheet (order # 273159)
- *80L960JA/JF 3.3V Embedded 32-bit Microprocessor* Data Sheet (order # 272744)

2.0 Package Considerations

One package change has been made for the 3.3 V, 5 V tolerant version of the 80960JA/JF processor. An external pin, VCC5 (pin C7 PGA package, pin 20 PQFP package) selects between standard 5 V interface logic or 3.3 V interface logic. Prior 80L960JA/JF processors have this pin defined as NO CONNECT.

See Section 3.0, "VCC5 Pin Requirements (VDIFF)" on page 6 for further information.

3.0 VCC5 Pin Requirements (VDIFF)

The 80960JA/JF processor's 5 V tolerant input buffers and TTL-compatible outputs allow the processor to interface with existing TTL-compatible external logic without voltage translator components. Thus, the processor can operate at 3.3 V while the off-chip peripherals can operate at 5 V.

An external pin on the processor (VCC5, pin C7 PGA package, pin 20 PQFP package) selects between standard 5 V interface levels or 3.3 V interface levels.

In 3.3 V-only systems where the 80960JA/JF input pins are driven from 3.3 V logic, connect the VCC5 pin directly to the 3.3 V V_{CC} plane.

In mixed-voltage systems where the processor is powered by 3.3 V and interfaces with 5 V components, the VCC5 pin must be connected to 5 V. Connecting the VCC5 pin to 5 V allows proper 5 V tolerant I/O buffer operation and prevents damage to the input pins being driven by 5 V external logic.

The voltage differential between the 80960JA/JF VCC5 pin and its 3.3 V V_{CC} pins must not exceed 2.25 V. If this voltage requirement is not met, current flow through the pin may exceed the processor's capabilities and result in damage to the processor.

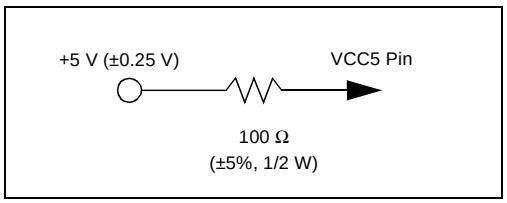
Instances when the voltage can exceed 2.25 V are during power up or power down, where one power supply reaches its level faster than the other, briefly causing an excess voltage differential. Another instance is during steady-state operation, where the differential voltage of the regulator (provided a regulator is used) cannot be maintained within 2.25 V.

Two methods can prevent a differential voltage greater than 2.25 V:

- Use a regulator that is designed to prevent the voltage differential from exceeding 2.25 V, or,
- Insert a 100 Ω series current limiting resistor on the VCC5 pin. The resistor can prevent damage in the case of a power failure, where the 5 V supply remains on and the 3.3 V supply goes to zero.

As shown in Figure 1, place the 100 Ω resistor in series with the VCC5 pin to limit the current through the pin.

Figure 1. VCC5 Current-Limiting Resistor



4.0 Device Considerations

4.1 Device Identification

The 80960JA/JF 3.3 V devices include a new device identification number based on the IEEE 1149.1 specification.

If your application code checks for proper device ID, the code needs to be re-compiled to reflect the new device ID. The device ID's are as follows:

Table 1. Device Identifications

Device	80L960 Device ID	New DeviceID
80960JA	0x00821013	0x30821013
80960JF	0x00820013	0x30820013

4.2 80960JA/JF AC Timings

The following describes the differences in timings between the 80L960JA/JF 3.3 V and 80960JA/JF 3.3 V (5 V tolerant) devices. See the data sheets for specific timing information. Timing changes from the 80L960 to the 80960JA/JF 3.3 V (5 V tolerant) processor are as follows:

- AC timings that get worse:
  - — Minimum CLKIN frequency (T_F minimum)
  - — Maximum CLKIN period (T_C maximum)
  - — Maximum allowable CLKIN rise and fall times (T_{CR} and T_{CF})
  - — Output hold times (T_{OH1} and T_{OF} minimum)
- AC timings that improve:
  - — CLKIN high and low times (T_{CH} and T_{CL})
  - — Output valid and float times (T_{OV1}, T_{OV2} and T_{OF} maximum)
  - — Input setup times (T_{IS1} and T_{IS2})
  - — Output-to-Output times (T_{LXL}, T_{LXA} and T_{DXD})
- One new specification has been added (T_{LX})

Note: It is anticipated that the next release of the 80960JA/JF/JD/JT processor data sheet, will includ longer input hold times (by 0.5 nS to 1 nS) for the 80960JA/JF processor. These timings can include; T_{IH1}, T_{IH3} and T_{IH4}.

Table 2 shows which timings are the same or improved and which timings are worse versus the 809L60JA/JF 3 V device.

Table 2. 80960JA/JF AC Timing Comparisons (Sheet 1 of 2)

Symbol	Parameter	Min	Max
Input Clock Timings			
T_F	CLKIN Frequency		
	80960JA/JF 25	WORSE	SAME
	80960JA/JF 16	WORSE	SAME
T_C	CLKIN Period		
	80960JA/JF 25	SAME	WORSE
	80960JA/JF 16	SAME	WORSE
T_{CS}	CLKIN Period Stability		SAME
T_{CH}	CLKIN High Time	BETTER	
T_{CL}	CLKIN Low Time	BETTER	
T_{CR}	CLKIN Rise Time		
	80960JA/JF 25		SAME
	80960JA/JF 16		WORSE
T_{CF}	CLKIN Fall Time		
	80960JA/JF 25		SAME
	80960JA/JF 16		WORSE
Synchronous Output Timings			
T_{OV1},T_{OH1}	Output Valid Delay and Output Hold for all outputs except ALE/$\overline{ALE}$ inactive and DT/$\overline{R}$ for 3.3 V input signals.		
	80960JA/JF 25	WORSE	BETTER
	80960JA/JF 16	WORSE	BETTER
	Same as above, but for 5.5 V input signals.		
	80960JA/JF 25	NEW	NEW
	80960JA/JF 16	NEW	NEW
T_{OV2},T_{OH2}	Output Valid Delay and Output Hold for DT/$\overline{R}$		
	80960JA/JF 25	SAME	SAME
	80960JA/JF 16	SAME	BETTER
T_{OF}	Output Float Delay		
	80960JA/JF 25	WORSE	BETTER
	80960JA/JF 16	WORSE	BETTER

Table 2. 80960JA/JF AC Timing Comparisons (Sheet 2 of 2)

Symbol	Parameter	Min	Max
Synchronous Input Timings			
T_{IS1}	Input Setup to CLKIN - AD31:0, $\overline{NMI}$, $\overline{XINT7:0}$		
	80960JA/JF 25	SAME	
	80960JA/JF 16	BETTER	
T_{IH1}	Input Hold from CLKIN - AD31:0, $\overline{NMI}$, $\overline{XINT7:0}$	SAME	
T_{IS2}	Input Setup to CLKIN - $\overline{RDYRCV}$ and HOLD		
	80960JA/JF 25	SAME	
	80960JA/JF 16	BETTER	
T_{IH2}	Input Hold from CLKIN - $\overline{RDYRCV}$ and HOLD	SAME	
T_{IS3}	Input Setup to CLKIN - $\overline{RESET}$		
	80960JA/JF 25	SAME	
	80960JA/JF 16	SAME	
T_{IH3}	Input Hold from CLKIN - $\overline{RESET}$	SAME	
T_{IS4}	Input Setup to CLKIN - $\overline{ONCE}$, STEST		
	80960JA/JF 25	SAME	
	80960JA/JF 16	SAME	
T_{IH4}	Input Hold from CLKIN - $\overline{ONCE}$, STEST	SAME	
Relative Output Timings			
T_{LX}	Address Valid to ALE/$\overline{ALE}$ inactive		
	3.3 V I/O	NEW	
	5 V I/O	NEW	
T_{LXL}	ALE/$\overline{ALE}$ Width	BETTER	
T_{LXA}	Address Hold from ALE/$\overline{ALE}$ Inactive		
T_{DXD}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Active		

4.3 Thermal Considerations

If the current 3.3 V design meets the thermal requirements of the original 3.3 V 809L60JA/JF processor, nothing needs to be modified or changed to accept the new 3.3 V, 5 V tolerant processor at the same clock speed. The new processors exhibit lower power consumption and therefore less heat dissipation than the corresponding 80L960JA/JF processors. Please see the specific data sheet for detailed I_{CC} specifications.

4.4 Functional Considerations

Errata that existed on the 80L960JA/JF processors have been fixed on the 80960Jx C0 stepping.

No other functional differences appear on the 80960Jx 3.3 V, 5 V tolerant processor versus the 80L960JA/JF 3.3 V processor.

5.0 Revision History

Revision	Date	Description
001	April, 1998	Initial version.
002	August,1998	Corrected reference to PLCC package. Now refers to PQFP package.