

i960[®] JA/JF/JD/JS/JC/JT Microprocessors

PRODUCT HIGHLIGHTS

- Clock tripling technology
- Large caches for faster performance
- State of the art testability
- i960[®] processor compatible RISC core
- 100 MIPS execution for the i960 - JT-100 processors
- 16-Kbyte 2-way set associative instruction cache
- 4-Kbyte direct mapped data cache
- 1-Kbyte on-chip data RAM
- Built-in interrupt controller
- Low-power features
- Two 32-bit timers



PRODUCT OVERVIEW

The i960[®] JC and JS processors are Intel's newest additions to the i960 Jx-processor family. The JS and JC processors feature larger cache sizes for faster performance and are 100% socket and code compatible with the existing i960 Jx processor family.

The JS and JC feature 16 Kbyte 2-way set associative instruction cache and 4 Kbyte direct mapped data cache. These increased cache sizes enable designers to build high-performance systems with low-cost memory. These features make them ideal for your most cost effective designs in networking applications such as remote access, XDSL, and hubs.

Like the other i960 Jx processors, the JC and JS are available in three different package types — the ceramic pin grid array, the plastic quad flat pack and the new mini plastic ball grid array or Mini-PBGA. The Mini-PBGA package, approximately the size of a U.S. dime, is outstanding wherever high-performance, small form factor requirements are needed. The Mini-PBGA package enables high port densities for space constrained applications such as remote access equipment.

Upgradeability plays a significant role in system cost and time-to-market. The i960 Jx-series is socket and code compatible from 16 MHz to 100 MHz. With the Jx-series, it is possible to have one design that produces 28 different levels of performance. In addition, the Jx processors are object code compatible with the entire i960 processor family.

The i960 processor family is supported by more than 70 vendors with over 200+ tools providing hardware, software and services ranging from real-time operating systems to evaluation boards to compilers. This helps ensure rapid time-to-market for your i960 processor based product.

i960® Jx PROCESSOR FEATURES AND BENEFITS

Features	Benefits
100% Pin for pin compatibility for all versions of the i960 Jx processor series	Rapid, easy design upgrades
High performance embedded architecture <ul style="list-style-type: none"> ■ 45 MIPS per watt execution at 33 MHz 	High performance, low power, low system cost
16-Kbyte on-chip instruction cache <ul style="list-style-type: none"> ■ 2-way set associative ■ Cache lock modes 	Reduce external bus traffic, accelerate execution of standard software and time critical interrupt routines
4-Kbyte data cache <ul style="list-style-type: none"> ■ Direct mapped write through 	Enhance performance to maintain single cycle data manipulation
32-bit multiplexed burst bus <ul style="list-style-type: none"> ■ Bus width is programmable by region, supports 8-, 16- or 32-bits wide peripherals ■ Supports bursts up to four 32-bit words 	Balance bandwidth and cost
Big endian data format <ul style="list-style-type: none"> ■ Supports aligned/unaligned big or little endian accesses ■ Multiword unaligned big endian 	Able to read aligned/unaligned words without significant system degradation of performance losses
Two identical 32-bit timers <ul style="list-style-type: none"> ■ Fully independent with auto reload 	Reduce board level cost with integration and reduce chip count
Local register cache <ul style="list-style-type: none"> ■ 8 local register sets ■ Saves or restores 16 local registers in 4 clock cycles ■ 128-bit wide interface for quick context switches on call returns and interrupts 	Fast context switching for critical routines to reduce the external bus traffic
JTAG <ul style="list-style-type: none"> ■ Supports IEEE 1149.1 standards 	Makes testing and debugging of surface mount systems possible through a common JTAG standard
High speed interrupt controller <ul style="list-style-type: none"> ■ 8 maskable external interrupt pins ■ One non-maskable interrupt pin ■ Two internal timer sources ■ Programmable edge or level detection ■ 240 interrupt vectors 	Improve control prioritization of software interrupts, hardware interrupts and process priority
Low power <ul style="list-style-type: none"> ■ As much as 400% power reduction from i960® CF processor 	Enable more performance with less power consumption
Power management features <ul style="list-style-type: none"> ■ Halt mode ■ 90% power reduction during HALT 	Reduce power use during inactive period to meet office environment

LOW-POWER SUPPORT

Many future designs for imaging, networking and remote access equipment will support low-power operation requiring the system to detect and initiate this mode. The system must reduce power to particular units of the equipment while maintaining the ability to return to normal operation without physically restarting the system. New systems will also be required to use less power in normal operation.

The i960 Jx processors support a power down mode of operation to significantly reduce the power consumption by approximately 90 percent. Execution of the HALT instruction initiates a semi-sleep mode. During this mode, normal on-chip timer operation, support for external bus masters through the HOLD/HOLDA interface, and the ability to detect interrupts remains functional. The interrupt source can be from either an external device or the integrated timers. Once an interrupt occurs, the processor will “wake up” and continue execution, starting with the instruction specified by the interrupt source.

EASE OF DESIGN

The Embedded Applications require both low system costs and excellent performance. This apparent conflict has been resolved with the i960 Jx processors. The i960 Jx processors will offer core clock speeds of 16, 25, 33, 40, 50, 66, and 100 MHz. This flexibility allows a designer to choose from any number of combinations to meet the price/performance requirements of the application.

ADVANCED CACHE ARCHITECTURE

i960 Jx processors contain three independent caches: instruction cache, data cache, and local register cache. Besides the on-chip cache, there is a zero wait-state, on-chip data RAM.

The Jx-series processors provide a 4-Kbyte direct mapped data cache. The inclusion of a data cache is a significant performance enhancement for applications that keep most of their data in RAM.


The on-chip data RAM is a unique feature of the processor. A 1-Kbyte region of zero wait-state memory provides storage for data variables and interrupt vectors. An on-chip data RAM also helps bus-intensive multi-master applications such as internetworking. While the processor accesses data in the on-chip RAM, the memory bus is free for use by external agents such as Ethernet and Token Ring controllers. Unlike a data cache, variables can never be “kicked out” of the data RAM. Intel’s compilers (CTOOLS960 and GNU960) can take advantage of the on-chip data RAM for critical variable storage, providing high speed and deterministic access to data.

INTERRUPT PERFORMANCE

The 80960Jx-series is designed to improve interrupt latency and throughput by supporting two operational modes: dedicated mode and expanded mode. Dedicated mode requires the external device to signal an interrupt request to the processor with a dedicated signal toggling. When the interrupt controller detects an active signal, it figures out the priority and vector of the associated interrupt. The dedicated mode of operation supports either edge or level detection besides fast or debounced sampling. Expanded mode requires the external device to place an interrupt vector on the interrupt pins, requiring the off-chip interrupt controller to read the pins and figure out the priority and vector of the interrupt.

The i960 Jx processor features these additional techniques to improve interrupt performance:

- The processor core determines the address of the first instruction of the interrupt service routine from the priority vector. The 80960Jx-series allows caching the interrupt vector addresses that point to the addresses of the executable instruction. Reserved for this purpose are the first 64 Bytes of on-chip data RAM. Caching these vectors reduce the external bus traffic to provide higher throughput.
- To reduce the time necessary for the processor to fetch the first instruction to be executed, the i960 Jx processors can permanently lock critical sections of code, such as interrupt handlers in the instruction cache. This feature enables faster and more deterministic interrupt response time.

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- The core performs a task switch to the interrupt service routine. This includes allocating a fresh register set, switching to a dedicated stack, and saving the previous internal state for later resumption of the underlying task. The i960 Jx processors can reduce the task switch time by reserving local register set(s) for interrupts priority 28 and higher.
 - These improvements enable the 80960Jx-series to reduce interrupt latency by a factor of five to 10 times the existing i960 Kx microprocessors.

In summary, the new versions of the Jx-series provide OEM's with low-power options, a host of new features to improve performance and testability and new higher performance options for embedded applications. The new Mini-PBGA package is outstanding wherever high performance, small form factor requirements are needed. The new 100 MHz i960 JT CPU features up to 16 Kbytes of instruction cache and 4 Kbytes of data cache and is code compatible with the entire i960 processor family.

The ability to quickly proliferate products at new price/performance points is very important to successful manufacturers. The i960 Jx processors enable customers to quickly modify products to meet new market needs thanks to upward binary code compatibility and a wide variety of pin-compatible products. For this reason, knowledge in one processor can make the move to new processors extremely easy.

In an embedded application with an infinite number of product variations, the design engineer has the difficult task of choosing the best architecture for his or her application. Intel's i960 microprocessor family wants the customer to make an architecture choice for today and for the future.

PRODUCT	SPEED (MHz)	INSTRUCTION CACHE	FPU	PACKAGE	TEMP	KEY FEATURES
80960HA	25, 33, 40	16K	No	A, FC	C	32-bit RISC superscalar CPU with two timers, flexible memory system and 8K Data Cache
80960HD	33/16, 50/25, 66/33, 80/40	16K	No	A, FC	C	Clock-Doubled 32-bit RISC superscalar CPU with two-timers, flexible memory system and 8K Data Cache
80960HT	75/25 60/20	16K	No	A, FC	C	Clock-Tripled 32-bit RISC superscalar CPU with two-timers, flexible memory system and 8K Data Cache
80960CA	16, 25, 33	1K	No	A, KU	C, E, A	32-bit RISC superscalar CPU with on-chip DMA and programmable bus size
80960CF	16, 25, 33, 40	4K	No	A, KU	C, E, A	32-bit RISC superscalar CPU with on-chip DMA and programmable bus size and 1K data cache
80960JA	16, 25, 33	2K	No	A, TG, NG, GD	C	32-bit RISC core that has very low-power consumption with variable programmable bus at 8-, 16-, or 32-bit and 1K data cache, 3.3V
80960JF	16, 25, 33	4K	No	A, NG, GD	C	32-bit RISC core that has very low-power consumption with variable programmable bus at 8-, 16-, or 32-bit and 2K data cache, 3.3V
80960JD	33/16, 50/25 33/66, 20/40	4K	No	A, NG, GD	C	32-bit RISC core that utilizes speed doubler technology. Internal bus runs at twice the speed of external bus and 2K data cache, 3.3V
80960JS	16, 25, 33	16K	No	A, NG, TG, GD	C	32-bit RISC core that has very low-power consumption with variable programmable bus at 8-, 16-, or 32-bit and 4K data cache, 3.3V
80960JC	33/16, 50/25 33/66, 20/40	16K	No	A, NG, GD	C	32-bit RISC core that utilizes speed doubler technology. Internal bus runs at twice the speed of external bus and 4K data cache, 3.3V
80960JT	33/100	16K	No	A, NG	C	32-bit CPU with multiplexed bus clock tripled 32-bit RISC with 4K Data Cache
80960KA	16, 20, 25	512 byte	No	A, NG	C	32-bit RISC CPU with multiplexed bus
80960KB	16, 20, 25	512 byte	Yes	A, NG	C	32-bit RISC CPU with multiplexed bus and IEEE floating-point
80960SA	10, 16, 20	512 byte	No	N, S	C	Low-cost 32-bit RISC CPU with multiplexed 16-bit bus
80960SB	10, 16, 20	512 byte	Yes	N, S	C	Low-cost 32-bit RISC CPU with multiplexed 16-bit bus and IEEE floating-point
80960MC	25	512 byte	No	A	C	

PACKAGES:

A = 168L PGA for i960 CA, CF, HA, HD, and HT processors, A = 132L PGA for i960 Jx series processors and the KA/KB processor, FC = 208L SQFP (also known as PQ2) for i960 HA/HD/HT processors, KU = 196L PQFP for i960 CA/CF processor, no CA 33 MHz, no CF 40 MHz, NG = 132L PQFP for i960 JX processors and the KA/KB processor, no KA 25 MHz, N = 84L PLCC for i960 SA/SB processor, no SB 20 MHz, S = 80L QFP (EIAJ), no SA 20 MHz, no SB 16 MHz, no SB 20 MHz, GD = 196PBG 15 millimeter for i960 JA, JF, JD, JT processors

TEMPERATURE RANGES:

C = Commercial (0 to 70° C), E = Extended (-40 to 100° C), A = Automotive (-40 to 125° C).

Additional product information is always available via the World Wide Web, CompuServe*, and Intel's Bulletin Board System (BBS).

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