Integrated Device Technology, Inc.

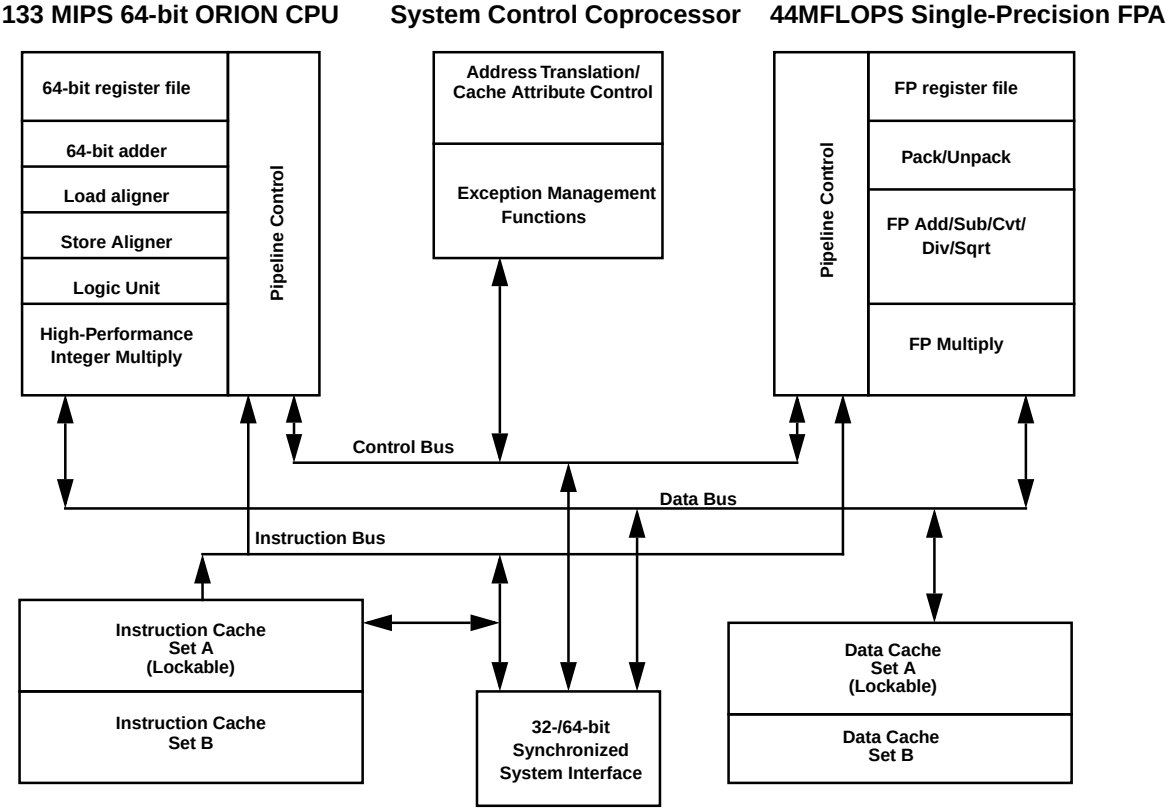
EMBEDDED 64-BIT ORION™ RISC MICROPROCESSOR

ORION
IDT79R4650™
IDT79RV4650™

FEATURES

- High-performance embedded 64-bit microprocessor
  - 64-bit integer operations
  - 64-bit registers
  - 80MHz, 100MHz, 133MHz operation frequency
- High-performance DSP capability
  - 66.7 Million Integer Multiply-Accumulate Operations/ sec @ 133 MHz
  - 44 MFlops floating point operations @133MHz
- High-performance microprocessor
  - 133 MIPS at 133MHz
  - 66.7 M Mul-Add/second at 133MHz
  - 44 MFLOP/s at 133MHz
  - >300,000 dhrystone (2.1)/sec capability at 133MHz (175 dhrystone MIPS)
- High level of integration
  - 64-bit, 133 MIPS integer CPU
  - 44MFlops Single precision floating-point unit
  - 8KB instruction cache; 8KB data cache
  - Integer multiply unit with 66.7M Mul-Add/sec
- Low-power operation
  - Active power management powers-down inactive units
  - Standby mode
- Upward software compatible with IDT RISController Family
- Large, efficient on-chip caches
  - Separate 8kB Instruction and 8kB Data caches
  - Over 1500MB/sec bandwidth from internal caches
  - 2-set associative
  - Write-back and write-through support
  - Cache locking to facilitate deterministic response
- Bus compatible with ORION family
  - System interfaces to 67 MHz, provides bandwidth up to 533 MB/S
  - Direct interface to 32-bit wide or 64-bit wide systems
  - Synchronized to external reference clock for multi-master operation
- Improved real-time support
  - Fast interrupt decode
  - Optional cache locking

BLOCK DIAGRAM:



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DESCRIPTION

The IDT79R4650 is a low-cost member of the IDT ORION family, targeted to a variety of performance hungry embedded applications. The R4650 continues the ORION tradition of high-performance through high-speed pipelines, high-bandwidth caches and bus interface, 64-bit architecture, and careful attention to efficient control. The R4650 reduces the cost of this performance relative to the R4600, by removing functional units that are frequently unneeded for many embedded applications, such as double-precision floating point arithmetic and a TLB.

The R4650 adds features relative to the R4600, reflective of its target applications. These features enable system cost reduction (e.g. optional 32-bit system interface) as well as higher performance for certain types of systems (e.g. cache locking, improved real-time support, integer DSP capability).

The R4650 supports a wide variety of embedded processor-based applications, such as consumer game systems, multi-media functions, internetworking equipment, switching equipment, and printing systems. Upwardly software-compatible with the RISController family, and bus- and upwardly software-compatible with the IDT ORION family, the R4650 will serve in many of the same applications, but, in addition supports other applications such as those requiring integer DSP functions.

The R4650 brings ORION performance levels to lower cost systems. ORION performance is preserved by retaining large on-chip caches that are two-way set associative, a streamlined high-speed pipeline, high-bandwidth, 64-bit execution, and facilities such as early restart for data cache misses. These techniques combine to allow the system designer over 2GB/sec aggregate internal bandwidth, 533 MB/sec bus bandwidth, 175 Dhrystone MIPS, 44MFlops, and 66.7 M Multiply-add/second.

The R4650 provides complete upward application-software compatibility with the IDT79R3000™ and IDT79R4700™ families of microprocessors.An array of development tools facilitates the rapid development of R4650-based systems, enabling a wide variety of customers to take advantage of the high-performance capabilities of the processor while maintaining short time to market goals.

The 64-bit computing capability of the R4650 enables a wide variety of capabilities previously limited by the lower bandwidth and bit-manipulation rates inherent in 32-bit architectures. For example, the R4650 can perform loads and stores from cached memory at the rates of 8-bytes every clock cycle, doubling the bandwidth of an equivalent 32-bit processor. This capability, coupled with the high clock rate for the R4650 pipeline, enables new levels of performance to be obtained from embedded systems.

This data sheet provides an overview of the features and architecture of the R4650 CPU. A more detailed description of the processor is available in the *IDT79R4650 Processor Hardware User's Manual*, available from IDT. Further information on development support, applications notes, and complementary products are also available from your local IDT sales representative.

HARDWARE OVERVIEW

The R4650 family brings a high-level of integration designed for high-performance computing. The key elements of the R4650 are briefly described below. A more detailed description of each of these subsystems is available in the User's Manual.

Pipeline

The R4650 uses a 5-stage pipeline similar to the IDT79R3000 and the IDT79R4600. The simplicity of this pipeline allows the R4650 to be lower cost and lower power than super-scalar or super-pipelined processors. Unlike superscalar processors, applications that have large data dependencies or that require a great deal of load/stores can still achieve performance close to the peak

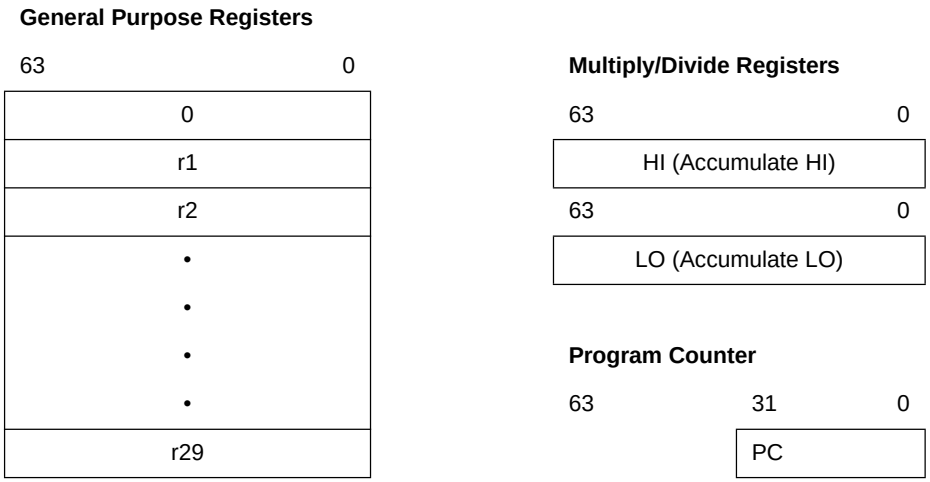
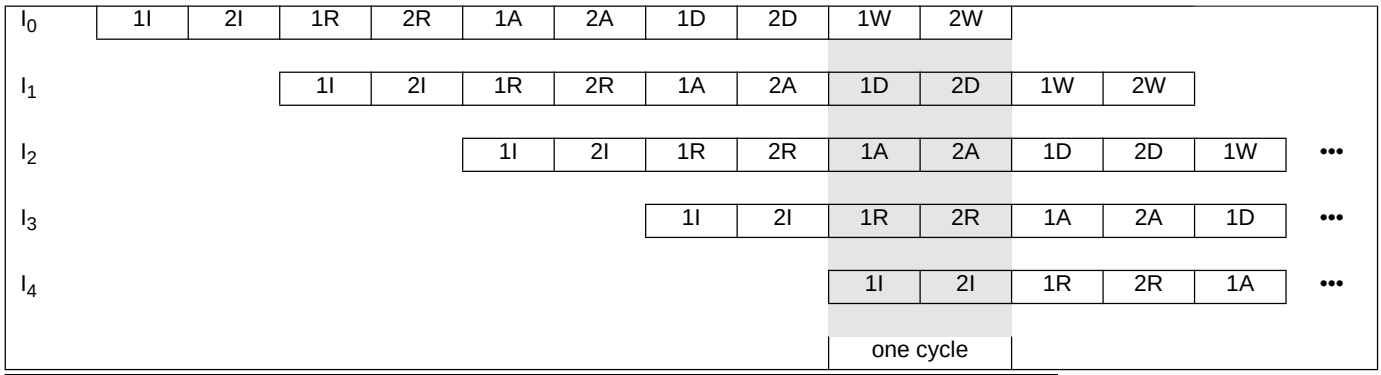


Figure 1: CPU Registers



1I-1R	Instruction cache access
2I	**Instruction virtual to physical address translation**
2A-2D	Data cache access and load align
1D	Data virtual to physical address translation
1D-2D	Virtual to physical address translation
2R	Register file read
2R	Bypass calculation
2R	Instruction decode
2R	Branch address calculation
1A	Issue or slip decision
1A-2A	Integer add, logical, shift
1A	Data virtual address calculation
2A	Store align
1A	Branch decision
2W	Register file write

Figure 2: R4650 Pipeline

performance of the processor. Figure 2 shows the R4650 pipeline.

Integer Execution Engine

The R4650 implements the MIPS-III Instruction Set Architecture, and thus is fully upward compatible with applications running on the earlier generation parts. The R4650 includes the same additions to the instruction set found in the R4600 family of microprocessors, targeted at improving performance and capability while maintaining binary compatibility with earlier R30xx processors. The extensions result in better code density, greater multi-processing support, improved performance for commonly used code sequences in operating system kernels, and faster execution of floating-point intensive applications. All resource dependencies are made transparent to the programmer, insuring transportability among implementations of the MIPS instruction set architecture. In addition, MIPS-III specifies new instructions defined to take advantage of the 64-bit architecture of the processor.

Finally, the R4650 also implements additional instructions, which are considered extensions to the MIPS-III architecture. These instructions improve the multiply and multiply-add throughput of the CPU, making it well suited to a wide variety of imaging and DSP applications. These extensions, which use opcodes allocated by MIPS Technologies for this purpose, are supported by a wide variety of development tools.

The MIPS integer unit implements a load/store architecture with single cycle ALU operations (logical, shift, add, sub) and autonomous multiply/divide unit. The 64-bit register resources include: 32 general-purpose orthogonal integer registers, the HI/LO result registers for the integer multiply/divide unit, and the program counter. In addition, the on-chip floating-point co-processor adds 32 floating-point registers, and a floating-point control/status register.

Register File

The R4650 has thirty-two general-purpose 64-bit registers. These registers are used for scalar integer operations and address calculation. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline. Figure 1 illustrates the R4650 Register File.

ALU

The R4650 ALU consists of the integer adder and logic unit. The adder performs address calculations in addition to arithmetic operations, and the logic unit performs all logical and shift operations. Each of these units is highly optimized and can perform an operation in a single pipeline cycle.

Integer Multiply/Divide

The R4650 uses a dedicated integer multiply/divide unit, optimized for high-speed multiply and multiply-accumulate operation. Table 1 shows the performance, expressed in terms of pipeline clocks, achieved by the R4650 integer multiply unit.

Opcode	Operand Size	Latency	Repeat	Stall
MULT/U, MAD/U	16 bit	3	2	0
	32 bit	4	3	0
MUL	16 bit	3	2	1
	32 bit	4	3	2
DMULT, DMULTU	any	6	5	0
DIV, DIVU	any	36	36	0
DDIV, DDIVU	any	68	68	0

Table 1: R4650 Integer Multiply Operation

The MIPS-III architecture defines that the results of a multiply or divide operation are placed in the HI and LO registers. The values can then be transferred to the general purpose register file using the MFHI/MFLO instructions.

The R4650 adds a new multiply instruction, “MUL”, which can specify that the multiply results bypass the “Lo” register and are placed immediately in the primary register file. By avoiding the explicit “Move-from-Lo” instruction required when using “Lo”, throughput of multiply-intensive operations is increased.

An additional enhancement offered by the R4650 is an atomic “multiply-add” operation, MAD, used to perform multiply-accumulate operations. This instruction multiplies two numbers and adds the product to the current contents of the HI and LO registers. This operation is used in numerous DSP algorithms, and allows the R4650 to cost reduce systems requiring a mix of DSP and control functions.

Finally, aggressive implementation techniques feature low latency for these operations along with pipelining to allow new operations to be issued before a previous one has fully completed. Table 1 also shows the repeat rate (peak issue rate), latency, and number of processor stalls required for the various operations. The R4650 performs automatic operand size detection to determine the size of the operand, and implements hardware interlocks to prevent overrun, allowing this high-performance to be achieved with simple programming.

Floating-Point Co-Processor

The R4650 incorporates an entire single-precision floating-point co-processor on chip, including a floating-point register file and execution units. The floating-point co-processor forms a “seamless” interface with the integer unit, decoding and executing instructions in parallel with the integer unit.

The floating-point unit of the R4650 directly implements single-precision floating point operations. This enables the R4650 to perform functions such as graphics rendering, without requiring extensive die area or power consumption. The single-precision unit of the R4650 is directly compatible with the single-precision operation of the R4600, and features the same latencies and repeat rates.

The R4650 does not directly implement the double-precision operations found in the R4600. However, to maintain software compatibility, the R4650 will signal a trap when a double-precision operation is initiated, allowing the requested function to be emulated in software. Alternatively, the system architect could use a software library emulation of double-precision functions, selected at compile time, to eliminate the overhead associated with trap and emulation.

Floating-Point Units

The R4650 floating-point execution units perform single precision arithmetic, as specified in the IEEE Standard 754. The execution unit is broken into a separate multiply unit and a combined add/convert/divide/square root unit. Overlap of multiplies and add/subtract is supported. The multiplier is partially pipelined, allowing a new multiply to begin every 6 cycles.

As in the IDT79R4600, the R4650 maintains fully precise floating-point exceptions while allowing both overlapped and pipelined operations. Precise exceptions are extremely important in mission-critical environments, such as ADA, and highly desirable for debugging in any environment.

The floating-point unit’s operation set includes floating-point add, subtract, multiply, divide, square root, conversion between fixed-point and floating-point format, conversion among floating-point formats, and floating-point compare. These operations comply with IEEE Standard 754. Double precision operations are not directly supported; attempts to execute double-precision floating point operations, or refer directly to double-precision registers, result in the R4650 signalling a “trap” to the CPU, enabling emulation of the requested function.

Table 2 gives the latencies of some of the floating-point instructions in internal processor cycles.

Operation	Instruction Latency
ADD	4
SUB	4
MUL	8
DIV	32
SQRT	31
CMP	3
FIX	4
FLOAT	6
ABS	1
MOV	1
NEG	1
LWC1	2
SWC1	1

Table 2: Floating-Point Operation

Floating-Point General Register File

The floating-point register file is made up of thirty-two 32-bit registers. These registers are used as source or target registers for the single-precision operations.

References to these registers as 64-bit registers (as supported in the R4600) will cause a trap to be signalled to the integer unit.

The floating-point control register space contains two registers; one for determining configuration and revision information for the coprocessor and one for control and status information. These are primarily involved with diagnostic software, exception handling, state saving and restoring, and control of rounding modes.

System Control Co-processor (CP0)

The system control co-processor in the MIPS architecture is responsible for the virtual to physical address translation and cache protocols, the exception control system, and the diagnostics capability of the processor. In the MIPS architecture, the system control co-processor (and thus the kernel software) is implementation dependent.

In the R4650, significant changes in CP0 relative to the R4600 have been implemented. These changes are designed to simplify memory management, facilitate debug, and speed real-time processing.

System Control Co-Processor Registers

The R4650 incorporates all system control co-processor (CP0) registers on-chip. These registers provide the path through which the virtual memory system's address translation is controlled, exceptions are handled, and operating modes are controlled (kernel vs. user mode, interrupts enabled or disabled, cache features). In addition, the R4650 includes registers to implement a real-time cycle counting facility, which aids in cache diagnostic testing, assists in data error detection, and facilitates software debug. Alternatively, this timer can be used as the operating system reference timer, and can signal a periodic interrupt.

Table 3 shows the CP0 registers of the R4650.

Number	Name	Function
0	IBase	Instruction address space base (new in R4650)
1	IBound	Instruction address space bound (new in R4650)
2	DBase	Data address space base (new in R4650)
3	DBound	Data address space bound (new in R4650)
4-7, 10, 20-25, 29, 31	—	Not used
8	BadVAddr	Virtual address on address exceptions
9	Count	Counts every other cycle
11	Compare	Generate interrupt when `Count = Compare`
12	Status	Miscellaneous control/status
13	Cause	Exception/Interrupt information
14	EPC	Exception PC
15	PRId	Processor ID
16	Config	Cache and system attributes
17	CAlg	Cache attributes for the eight 512MB regions of the virtual address space — new register
18	IWatch	Instruction breakpoint virtual address
19	DWatch	Data breakpoint virtual address
26	ECC	Used in cache diagnostics
27	CacheErr	Cache diagnostics
28	TagLo	Cache index
30	ErrorEPC	CacheError exception PC

Table 3: R4650 CPO Registers

Operation modes

The R4650 supports two modes of operation: user mode and kernel mode.

Kernel mode operation is typically used for exception handling and operating system kernel functions, including CP0 management and access to IO devices. In kernel mode, software has access to the entire address space and all of the co-processor 0 registers, and can select whether to enable co-processor 1 accesses. The processor

enters kernel mode at reset, and whenever an exception is recognized.

User mode is typically used for applications programs. User mode accesses are limited to a subset of the virtual address space, and can be inhibited from accessing CP0 functions.

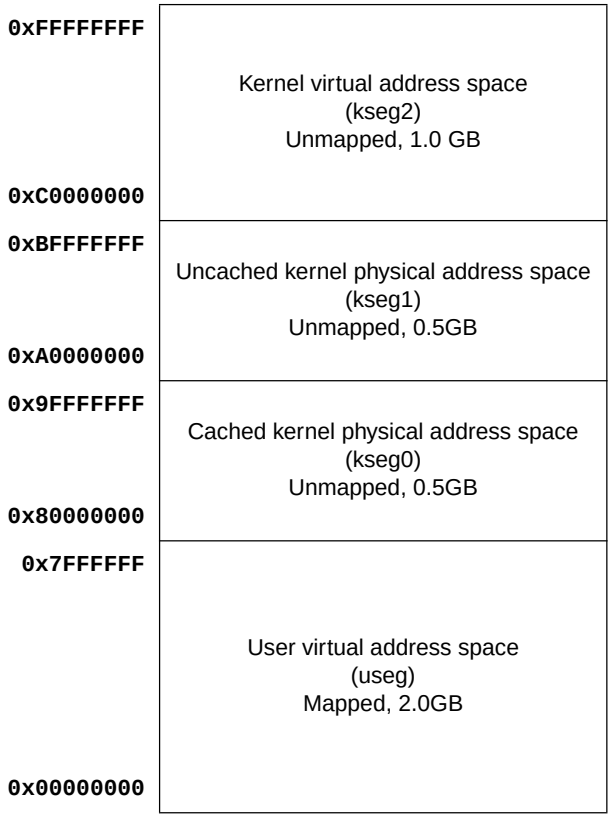


Figure 3: Mode Virtual Addressing (32-bit mode)

Virtual to Physical Address Mapping

The 4GB virtual address space of the R4650 is shown in figure 3. The 4 GB address space is divided into addresses accessible in either kernel or user mode (kuseg), and addresses only accessible in kernel mode (kseg2:0).

The R4650 supports the use of multiple user tasks sharing common virtual addresses, but mapped to separate physical addresses. This facility is implemented via the “base-bounds” registers contained in CP0.

When a user virtual address is asserted (load, store, or instruction fetch), the R4650 compares the virtual address with the contents of the appropriate “bounds” register (instruction or data). If the virtual address is “in bounds”, the value of the corresponding “base” register is added to the virtual address to form the physical address for that reference. If the address is not within bounds, an exception is signalled.

This facility enables multiple user processes in a single physical memory without the use of a TLB. This type of operation is further supported by a number of development tools for the R4650, including real-time operating systems and “position independent code”.

Kernel mode addresses do not use the base-bounds registers, but rather undergo a fixed virtual to physical address translation.

Debug Support

To facilitate software debug, the R4650 adds a pair of “watch” registers to CP0. When enabled, these registers will cause the CPU to take an exception when a “watched” address is appropriately accessed.

Interrupt Vector

The R4650 also adds the capability to speed interrupt exception decoding. Unlike the R4600, which utilizes a single common exception vector for all exception types (including interrupts), the R4650 allows kernel software to enable a separate interrupt exception vector. When enabled, this vector location speeds interrupt processing by allowing software to avoid decoding interrupts from general purpose exceptions.

Cache Memory

In order to keep the R4650’s high-performance pipeline full and operating efficiently, the R4650 incorporates on-chip instruction and data caches that can each be accessed in a single processor cycle. Each cache has its own 64-bit data path and can be accessed in parallel. The cache subsystem provides the integer and floating-point units with an aggregate bandwidth of over 1500 MB per second at a pipeline clock frequency of 133MHz. The cache subsystem is similar in construction to that found in the R4600, although some changes have been implemented. Table 6 is an overview of the caches found on the R4650.

Instruction Cache

The R4650 incorporates a two-way set associative on-chip instruction cache. This virtually indexed, physically tagged cache is 8KB in size and is parity protected.

Because the cache is virtually indexed, the virtual-to-physical address translation occurs in parallel with the cache access, thus further increasing performance by allowing these two operations to occur simultaneously. The tag holds a 20-bit physical address and valid bit, and is parity protected.

The instruction cache is 64-bits wide, and can be refilled or accessed in a single processor cycle. Instruction fetches require only 32 bits per cycle, for a peak instruction bandwidth of 533MB/sec at 133MHz. Sequential accesses take advantage of the 64-bit fetch to reduce power dissipation, and cache miss refill, can write 64 bits-per-cycle to minimize the cache miss penalty. The line size is eight instructions (32 bytes) to maximize performance.

In addition, the contents of one set of the instruction cache (set “A”) can be “locked” by setting a bit in a CP0 register. Locking the set prevents its contents from being overwritten by a subsequent cache miss; refill occurs then only into “set B”.

This operation effectively “locks” time critical code into one 4kB set, while allowing the other set to service other instruction streams in a normal fashion. Thus, the benefits

of cached performance are achieved, while deterministic real-time response is preserved.

Data Cache

For fast, single cycle data access, the R4650 includes an 8KB on-chip data cache that is two-way set associative with a fixed 32-byte (eight words) line size. Table 4 lists the R4650 cache attributes.

Characteristics	Instruction	Data
Size	8KB	8KB
Organization	2-way set associative	2-way set associative
Line size	32B	32B
Index	$vAddr_{11..0}$	$vAddr_{11..0}$
Tag	$pAddr_{31..12}$	$pAddr_{31..12}$
Write policy	n.a.	writeback /writethru
Line transfer order	read sub-block order	read sub-block order
	write sequential	write sequential
Miss restart after transfer of	entire line	first word
Parity	per-word	per-byte
Cache locking	set A	set A

Table 4: R4650 Cache Attributes

The data cache is protected with byte parity and its tag is protected with a single parity bit. It is virtually indexed and physically tagged to allow simultaneous address translation and data cache access

The normal write policy is writeback, which means that a store to a cache line does not immediately cause memory to be updated. This increases system performance by reducing bus traffic and eliminating the bottleneck of waiting for each store operation to finish before issuing a subsequent memory operation. Software can however select write-through for certain address ranges, using the CAlg register in CP0. Cache protocols supported for the data cache are:

- **Uncached**. Addresses in a memory area indicated as uncached will not be read from the cache. Stores to such addresses will be written directly to main memory, without changing cache contents.
- **Writeback**. Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later writeback. If the cache lookup misses, the target line is first brought into the cache before the cache is updated.
- **Write-through with write allocate.** Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated and main memory will also be written; the state of the “writeback” bit of the cache line will be unchanged. If the cache lookup misses, the target line is first brought into the cache before the cache is updated.
- **Write-through without write-allocate.** Loads and instruction fetches will first search the cache, reading main memory only if the desired data is not cache resident. On data store operations, the cache is first searched to see if the target address is cache resident. If it is resident, the cache contents will be updated, and the cache line marked for later writeback. If the cache lookup misses, then only main memory is written.

Associated with the Data Cache is the store buffer. When the R4650 executes a Store instruction, this single-entry buffer gets written with the store data while the tag comparison is performed. If the tag matches, then the data is written into the Data Cache in the next cycle that the Data Cache is not accessed (the next non-load cycle). The store buffer allows the R4650 to execute a store every processor cycle and to perform back-to-back stores without penalty.

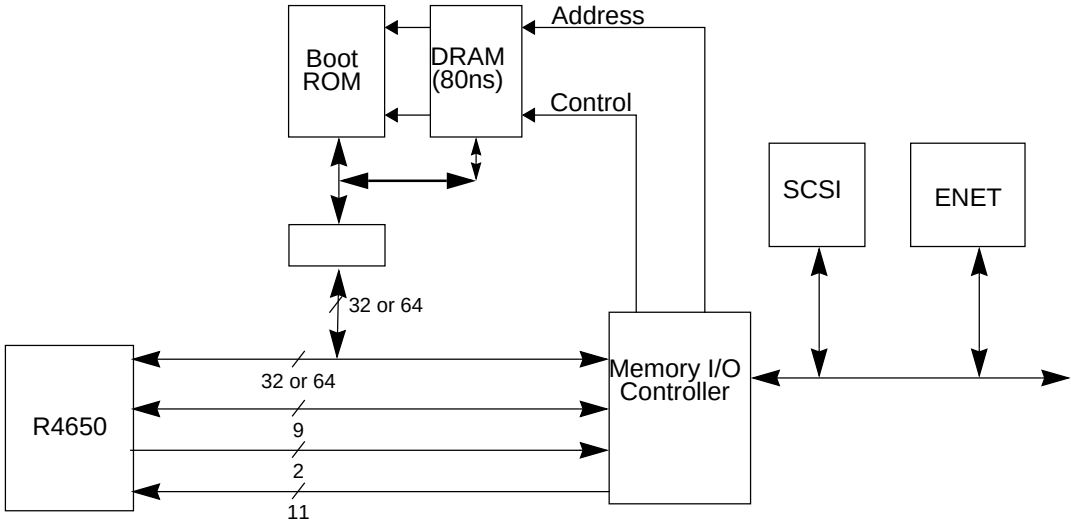


Figure 4: Typical R4650 System Architecture

Write buffer

Writes to external memory, whether cache miss write-backs or stores to uncached or write-through addresses, use the on-chip write buffer. The write buffer holds up to four address and data pairs. The entire buffer is used for a data cache writeback and allows the processor to proceed in parallel with memory update. For uncached and write-through stores, the write buffer significantly increases performance over the R4000 family of processors.

System Interface

The R4650 supports a 64-bit system interface that is bus compatible with the R4600 system interface. In addition, the R4650 supports a 32-bit system interface mode, allowing the CPU to interface directly with a lower cost memory system.

The interface consists of a 64-bit Address/Data bus with 8 check bits and a 9-bit command bus protected with parity. In addition, there are 8 handshake signals and 6 interrupt inputs. The interface has a simple timing specification and is capable of transferring data between the processor and memory at a peak rate of 533MB/sec at 133MHz.

Figure 4 shows a typical system using the R4650. In this example two banks of DRAMs are used to supply and accept data with a DDxxDD data pattern.

The R4650 clocking interface allows the CPU to be easily mated with external reference clocks. The CPU input clock is the bus reference clock, and can be between 25 and 67MHz (somewhat dependent on maximum pipeline speed for the CPU).

An on-chip phase-locked-loop generates the pipeline clock from the system interface clock by multiplying it up an amount selected at system reset. Supported multipliers are values 2 through 8 inclusive, allowing systems to implement pipeline clocks at significantly higher frequency than the system interface clock.

System Address/Data Bus

The 64-bit System Address Data (SysAD) bus is used to transfer addresses and data between the R4650 and the rest of the system. It is protected with an 8-bit parity check bus, SysADC. When initialized for 32-bit operation, SysAD can be viewed as a 32-bit multiplexed bus, with 4 parity check bits.

The system interface is configurable to allow easier interfacing to memory and I/O systems of varying frequencies. The bus frequency and reference timing of the R4650 are taken from the input clock. The rate at which the CPU transmits data to the system interface is programmable via boot time mode control bits. The rate at which the processor receives data is fully controlled by the external device. Therefore, either a low cost interface requiring no read or write buffering or a faster, high performance interface can be designed to communicate with the R4650. Again, the system designer has the flexibility to make these price/performance trade-offs.

System Command Bus

The R4650 interface has a 9-bit System Command (SysCmd) bus. The command bus indicates whether the SysAD bus carries an address or data. If the SysAD carries an address, then the SysCmd bus also indicates what type of transaction is to take place (for example, a read or write). If the SysAD carries data, then the SysCmd bus also gives information about the data (for example, this is the last data word transmitted, or the cache state of this data line is clean exclusive). The SysCmd bus is bidirectional to support both processor requests and external requests to the R4650. Processor requests are initiated by the R4650 and responded to by an external device. External requests are issued by an external device and require the R4650 to respond.

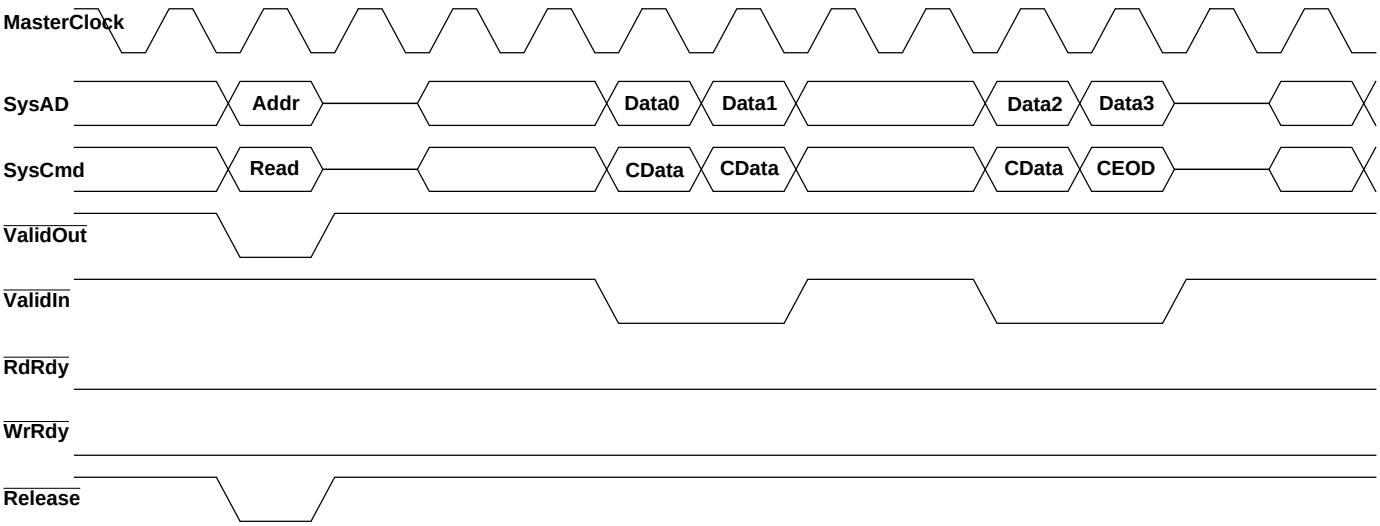


Figure 5: R4650 Block Read Request (64-bit interface option)

The R4650 supports single datum (one to eight byte) and 8-word block transfers on the SysAD bus. In the case of a single-datum transfer, the low-order 3 address bits gives the byte address of the transfer, and the SysCmd bus indicates the number of bytes being transferred. The choice of 32- or 64-bit wide system interface dictates whether a cache line block transaction requires 4 double word data cycles or 8 single word cycles, and whether a single datum transfer larger than 4 bytes needs to be broken into two smaller transfers.

Handshake Signals

There are six handshake signals on the system interface. Two of these, $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ are used by an external device to indicate to the R4650 whether it can accept a new read or write transaction. The R4650 samples these signals before deasserting the address on read and write requests.

$\overline{\text{ExtRqst}}$ and $\overline{\text{Release}}$ are used to transfer control of the SysAD and SysCmd buses between the processor and an external device. When an external device needs to control the interface, it asserts $\overline{\text{ExtRqst}}$. The R4650 responds by asserting $\overline{\text{Release}}$ to release the system interface to slave state.

$\overline{\text{ValidOut}}$ and $\overline{\text{ValidIn}}$ are used by the R4650 and the external device respectively to indicate that there is a valid command or data on the SysAD and SysCmd buses. The R4650 asserts $\overline{\text{ValidOut}}$ when it is driving these buses with a valid command or data, and the external device drives $\overline{\text{ValidIn}}$ when it has control of the buses and is driving a valid command or data.

Non-overlapping System Interface

The R4650 requires a non-overlapping system interface, compatible with the R4600. This means that only one processor request may be outstanding at a time and that the request must be serviced by an external device before the R4650 issues another request. The R4650 can issue read and write requests to an external device, and an external device can issue read and write requests to the R4650.

The R4650 asserts $\overline{\text{ValidOut}}$ and simultaneously drives the address and read command on the SysAD and SysCmd buses. If the system interface has $\overline{\text{RdRdy}}$ or Read transactions asserted, then the processor tristates its drivers and releases the system interface to slave state by asserting $\overline{\text{Release}}$. The external device can then begin sending the data to the R4650.

Figure 5 shows a processor block read request and the external agent read response. The read latency is 4 cycles ($\overline{\text{ValidOut}}$ to $\overline{\text{ValidIn}}$), and the response data pattern is DDxxDD. Figure 6 shows a processor block write.

Write Reissue and Pipeline Write

The R4600 and the R4650 implement additional write protocols designed to improve performance. This implementation doubles the effective write bandwidth. The write re-issue has a high repeat rate of 2 cycles per write. A write issues if WrRdy is asserted 2 cycles earlier and is still asserted at the issue cycle. If it is not still asserted, the last write re-issues again. Pipelined writes have the same 2-cycle per write repeat rate, but can issue one more write after WrRdy de-asserts. They still follow the issue rule as R4x00 mode for other writes.

External Requests

The R4650 responds to requests issued by an external device. The requests can take several forms. An external device may need to supply data in response to an R4650 read request or it may need to gain control over the system interface bus to access other resources which may be on that bus.

The following is a list of the supported external requests:

- Read Response
- Null

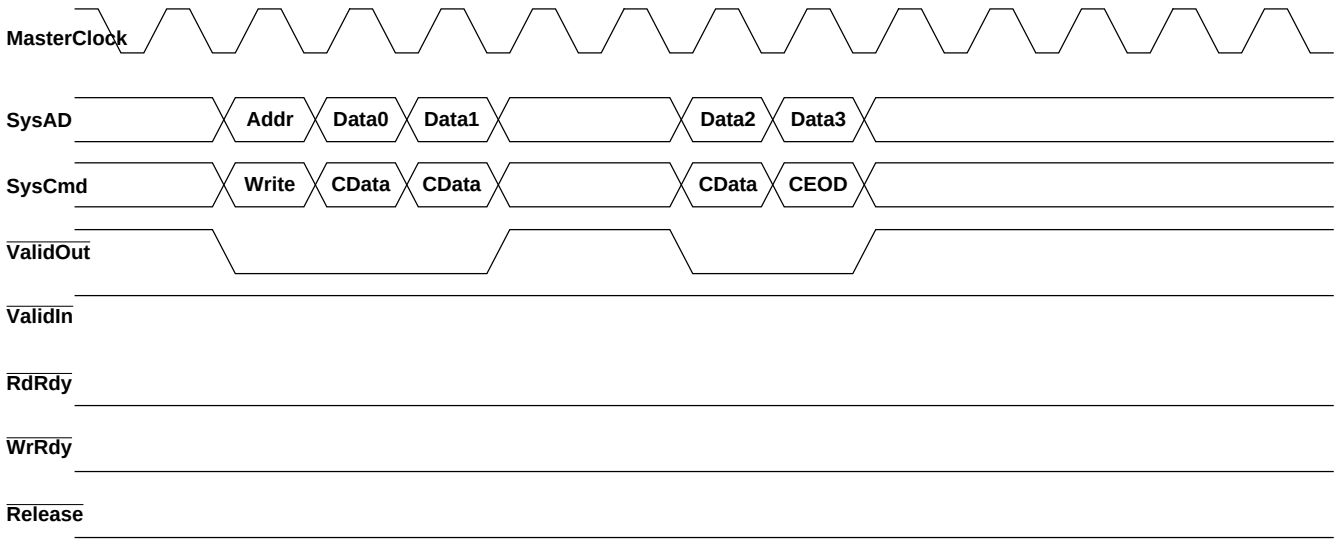


Figure 6: R4650 Block Write Request (64-bit system interface)

Boot Time Options

Fundamental operational modes for the processor are initialized by the boot-time mode control interface. The boot-time mode control interface is a serial interface operating at a very low frequency (MasterClock divided by 256). The low-frequency operation allows the initialization information to be kept in a low-cost EPROM; alternatively the twenty-or-so bits could be generated by the system interface ASIC or a simple PAL.

Immediately after the VCCOK Signal is asserted, the processor reads a serial bit stream of 256 bits to initialize all fundamental operational modes. After initialization is complete, the processor continues to drive the serial clock output, but no further initialization bits are read.

Boot-Time Modes

The boot-time serial mode stream is defined in Table 5. Bit 0 is the bit presented to the processor when VCCOK is asserted; bit 255 is the last.

Power Management

CP0 is also used to control the power management for the R4650. This is the standby mode and it can be used to reduce the power consumption of the internal core of the CPU. The standby mode is entered by executing the WAIT instruction with the SysAD bus idle and is exited by any interrupt.

Standby Mode Operation

The R4650 provides a means to reduce the amount of power consumed by the internal core when the CPU would otherwise not be performing any useful operations. This is known as “Standby Mode”.

Entering Standby Mode

Executing the WAIT instruction enables interrupts and enters Standby mode. When the WAIT instruction finishes the W pipe-stage, if the SysAd bus is currently idle, the internal clocks will shut down, thus freezing the pipeline. The PLL, internal timer, and some of the input pins (Int[5:0]*, NMI*, ExtReq*, Reset*, and ColdReset*) will continue to run. If the conditions are not correct when the WAIT instruction finishes the W pipe-stage (i.e. the SysAd bus is not idle), the WAIT is treated as a NOP.

Once the CPU is in Standby Mode, any interrupt, including the internally generated timer interrupt, will cause the CPU to exit Standby Mode.

Mode bit	Description
0	Reserved (must be zero)
4..1	Writeback data rate: 64-bit / 32-bit 0 → D / 0 → W 1 → DDx / 1 → WWx 2 → DDxx / 2 → WWxx 3 → DxDx / 3 → WxWx 4 → DDxxx / 4 → WWxxx 5 → DDxxxx / 5 → WWxxxx 6 → DxxDxx / 6 → WxxWxx 7 → DDxxxxxx / 7 → WWxxxxxx 8 → DxxxDxxx / 8 → WxxxWxxx 9-15 reserved / 9-15 reserved
7..5	Clock multiplier: 0 → 2 1 → 3 2 → 4 3 → 5 4 → 6 5 → 7 6 → 8 7 reserved
8	0 → Little endian 1 → Big endian
10..9	00 → R4000 compatible 01 → reserved 10 → pipelined writes 11 → write re-issue
11	Disable the timer interrupt on Int[5]
12	0 → 64-bit system interface 1 → 32-bit system interface
14..13	Output driver strength: 10 → 100% strength (fastest) 11 → 83% strength 00 → 67% strength 01 → 50% strength (slowest)
255..15	Must be zero

Table 5: Boot time mode stream

Thermal Considerations

The R4650 utilizes special packaging techniques to improve the thermal properties of high-speed processors. The R4650 is packaged using cavity down packaging in a 208-pin MQUAD.

The R4650 utilizes the MQUAD package (the “MS” package), which is an all-aluminum package with the die attached to a normal copper lead frame mounted to the aluminum casing. Due to the heat-spreading effect of the aluminum, the MQUAD package allows for an efficient thermal transfer between the die and the case. The aluminum offers less internal resistance from one end of the package to the other, reducing the temperature gradient across the package and therefore presenting a greater area for convection and conduction to the PCB for a given temperature. Even nominal amounts of airflow will dramatically reduce the junction temperature of the die, resulting in cooler operation.

The R4650 is guaranteed in a case temperature range of 0° to +85° C. The type of package, speed (power) of the device, and airflow conditions affect the equivalent ambient temperature conditions that will meet this specification.

The equivalent allowable ambient temperature, T_A, can be calculated using the thermal resistance from case to ambient ($\varnothing_{CA}$) of the given package. The following equation relates ambient and case temperatures:

$$T_A = T_C - P * \varnothing_{CA}$$

where P is the maximum power consumption at hot temperature, calculated by using the maximum I_{CC} specification for the device.

Typical values for $\varnothing_{CA}$ at various airflows are shown in Table 6.

Preliminary

	$\varnothing_{CA}$					
Airflow (ft/min)	**0**	**200**	**400**	**600**	**800**	**1000**
208 MQUAD	21	13	10	9	8	7

Table 6: Thermal Resistance ($\varnothing_{CA}$) at Various Airflows

Note that the R4650 implements advanced power management to substantially reduce the average power dissipation of the device. This operation is described in the *IDT79R4640 and IDT79R4650 RISC Processor Hardware User’s Manual*.

DATA SHEET REVISION HISTORY

Changes to version dated September 1995:

AC Electrical Characteristics:

- In System Interface Parameters tables (R4650 and RV4650), Data Setup and Data Hold minimums changed.

PIN DESCRIPTION

The following is a list of interface, interrupt, and miscellaneous pins available on the R4650. Pins marked with one asterisk are active when low.

Pin Name	Type	Description
System interface:		
ExtRqst*	Input	External request Signals that the system interface needs to submit an external request.
Release*	Output	Release interface Signals that the processor is releasing the system interface to slave state
RdRdy*	Input	Read Ready Signals that an external agent can now accept a processor read.
WrRdy*	Input	Write Ready Signals that an external agent can now accept a processor write request.
ValidIn*	Input	Valid Input Signals that an external agent is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	Output	Valid output Signals that the processor is now driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
SysAD(63:0)	Input/Output	System address/data bus A 64-bit address and data bus for communication between the processor and an external agent.
SysADC(7:0)	Input/Output	System address/data check bus An 8-bit bus containing parity check bits for the SysAD bus during data bus cycles.
SysCmd(8:0)	Input/Output	System command/data identifier bus A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmdP	Input/Output	Reserved system command/data identifier bus parity For the R4650 this signal is unused on input and zero on output.
Clock/control interface:		
MasterClock	Input	Master clock Master clock input used as the system interface reference clock. All output timings are relative to this input clock. Pipeline operation frequency is derived by multiplying this clock up by the factor selected during boot initialization.
VccP	Input	Quiet Vcc for PLL Quiet Vcc for the internal phase locked loop.
VssP	Input	Quiet Vss for PLL Quiet Vss for the internal phase locked loop.
Interrupt interface:		
Int*(5:0)	Input	Interrupt Six general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register.
NMI*	Input	Non-maskable interrupt Non-maskable interrupt, ORed with bit 6 of the interrupt register.
Initialization interface:		

Pin Name	Type	Description
Vccok	Input	Vcc is OK When asserted, this signal indicates to the R4650 that the 3.3V (5.0V) power supply has been above 3.0V (4.5V) for more than 100 milliseconds and will remain stable. The assertion of Vccok initiates the reading of the boot-time mode control serial stream.
ColdReset*	Input	Cold reset This signal must be asserted for a power on reset or a cold reset. ColdReset must be de-asserted synchronously with MasterClock.
Reset*	Input	Reset This signal must be asserted for any reset sequence. It may be asserted synchronously or asynchronously for a cold reset, or synchronously to initiate a warm reset. Reset must be de-asserted synchronously with MasterClock.
ModeClock	Output	Boot mode clock Serial boot-mode data clock output at the system clock frequency divided by two hundred and fifty six.
ModeIn	Input	Boot mode data in Serial boot-mode data input.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	R4650 5.0V±5% Commercial	RV4650 3.3V±5% Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5(2) to +7.0	–0.5(2) to +4.6	V
T_C	Operating Temperature (case)	0 to +85	0 to +85	°C
T_{BIAS}	Case Temperature Under Bias	–55 to +125	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	–55 to +125	°C
I_{IN}	DC Input Current	20(3)	20(3)	mA
I_{OUT}	DC Output Current	50(4)	50(4)	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} minimum = –2.0V for pulse width less than 15ns. V_{IN} should not exceed V_{CC} +0.5 Volts.
3. When V_{IN} < 0V or V_{IN} > V_{CC}
4. Not more than one output should be shorted at a time. Duration of the short should not exceed 30 seconds.

RECOMMENDED OPERATION TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	R4650 V_{CC}	RV4650 V_{CC}
Commercial	0°C to +85°C (Case)	0V	5.0V±5%	3.3V±5%

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4650

(V_{CC} = 5.0±5%, T_{CASE} = 0°C to +85°C)

Parameter	R4650 80MHz		R4650 100MHz		R4650 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	3.5V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	0.8V	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	2.0V	V_{CC} + 0.5V	—
I_{IN}	—	±10uA	—	±10uA	—	±10uA	$0 \le V_{IN} \le V_{CC}$
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

POWER CONSUMPTION—R4650

Parameter		R4650 80MHz		R4650 100MHz		R4650 133MHz		Conditions
		Typical[9]	Max	Typical[9]	Max	Typical[9]	Max	
System Condition:		80/40MHz		100/50MHz		133/44MHz		—
I_{CC}	standby	—	50 mA	—	75 mA	—	100 mA	C_L = 0pF[8]
		—	125 mA	—	150 mA	—	200 mA	C_L = 50pF
	active, 64-bit bus option	575 mA	800 mA	700 mA	1200 mA	950 mA	1350 mA	C_L = 0pF No SysAd activity[8]
		675 mA	1200 mA	800 mA	1400 mA	1050 mA	1750 mA	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		675 mA	1400 mA	800 mA	1675 mA	1050 mA	2000 mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[8]
	active, 32-bit bus option	575 mA	800 mA	700 mA	1000 mA	950 mA	1350 mA	C_L = 0pF No SysAd activity[8]
		625 mA	1000 mA	750 mA	1200 mA	1000 mA	1550 mA	C_L = 50pF R4x00 compatible writes, T_C = 25°C
		625 mA	1100 mA	750 mA	1350 mA	1000 mA	1650 mA	C_L = 50pF Pipelined writes or write re-issue, T_C = 25°C[8]

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—R4650

(V_{CC}=5.0V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—R4650

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Pipeline clock frequency	PClk		50	80	50	100	50	133	MHz
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock Frequency(5)	—	—	20	40	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	—	±250	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTES:

5. Operation of the R4650 is only guaranteed with the Phase Lock Loop enabled.
6. Timings are measured from 1.5V of the clock to 1.5V of the signal.
7. Capacitive load for all output timings is 50pF.
8. Guaranteed by Design.
9. Typical integer instruction mix and cache miss rates.

System Interface Parameters—R4650(6)

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	11	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Output Hold	t_{DOH} *	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	7	—	6	—	6	—	ns
Data Hold	t_{DH}		4	—	3	—	3	—	ns

* 25pf loading on external putput signals, fastest settings

Boot Time Interface Parameters—R4650

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle

Parameter	Symbol	Test Conditions	R4650 80MHz		R4650 100MHz		R4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

DC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE RV4650

(V_{CC} = 3.3±5%, T_{CASE} = 0°C to +85°C)

Parameter	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Conditions
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
V_{OL}	—	0.1V	—	0.1V	—	0.1V	$\|I_{OUT}\|$= 20uA
V_{OH}	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	V_{CC} - 0.1V	—	
V_{OL}	—	0.4V	—	0.4V	—	0.4V	$\|I_{OUT}\|$= 4mA
V_{OH}	2.4V	—	2.4V	—	2.4V	—	
V_{IL}	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	–0.5V	$0.2V_{CC}$	—
V_{IH}	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	$0.7V_{CC}$	V_{CC} + 0.5V	—
V_{OHC}	—	—	—	—	—	—	—
V_{ILC}	—	—	—	—	—	—	—
V_{IHC}	—	—	—	—	—	—	—
C_{IN}	—	10pF	—	10pF	—	10pF	—
C_{OUT}	—	10pF	—	10pF	—	10pF	—
I/O_{LEAK}	—	20uA	—	20uA	—	20uA	Input/Output Leakage

POWER CONSUMPTION—RV4650

Parameter		RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Conditions
		Typical[9]	Maximum	Typical[9]	Maximum	Typical[9]	Maximum	
System Condition:		80/40MHz		100/50MHz		133/44MHz		—
I_{CC}	standby	—	40 mA	—	50 mA	—	60 mA	C_L = 0pF[8]
		—	90 mA	—	100 mA	—	110 mA	C_L = 50pF
	active, 64-bit bus option	375 mA	575 mA	475 mA	700 mA	625 mA	925 mA	C_L = 0pF, No SysAd activity[8]
		450 mA	800 mA	550 mA	925 mA	700 mA	1150 mA	C_L = 50pF R4x00 |compatible writes T_C = 25°C
		450 mA	950 mA	550 mA	925 mA	700 mA	1300 mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C[8]
	active, 32-bit bus option	375 mA	575 mA	475 mA	700 mA	625 mA	925 mA	C_L = 0pF, No SysAd activity[8]
		400 mA	700 mA	525 mA	825 mA	650 mA	1050 mA	C_L = 50pF R4x00 compatible writes T_C = 25°C
		400 mA	775 mA	525 mA	825 mA	650 mA	1125 mA	C_L = 50pF Pipelined writes or Write re-issue, T_C = 25°C[8]

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL TEMPERATURE RANGE—RV4650

(V_{CC}=3.3V ± 5%; T_{CASE} = 0°C to +85°C)

Clock Parameters—RV4650

Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Pipeline clock frequency	PClk		50	80	50	100	50	133	MHz
MasterClock HIGH	t_{MCHIGH}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock LOW	t_{MCLOW}	Transition ≤ 5ns	6	—	4	—	3	—	ns
MasterClock Frequency(5)	—	—	20	40	25	50	25	67	MHz
MasterClock Period	t_{MCP}	—	25	40	20	40	15	40	ns
Clock Jitter for MasterClock	$t_{JitterIn}$(8)	—	—	±250	—	±250	—	±250	ps
MasterClock Rise Time	t_{MCRise}(8)	—	—	5	—	5	—	4	ns
MasterClock Fall Time	t_{MCFall}(8)	—	—	5	—	5	—	4	ns
ModeClock Period	$t_{ModeCKP}$	—	—	256* t_{MCP}	—	256* t_{MCP}	—	256* t_{MCP}	ns

NOTES:

10.Operation of the RV4650 is only guaranteed with the Phase Lock Loop enabled.

System Interface Parameters—RV4650(6)

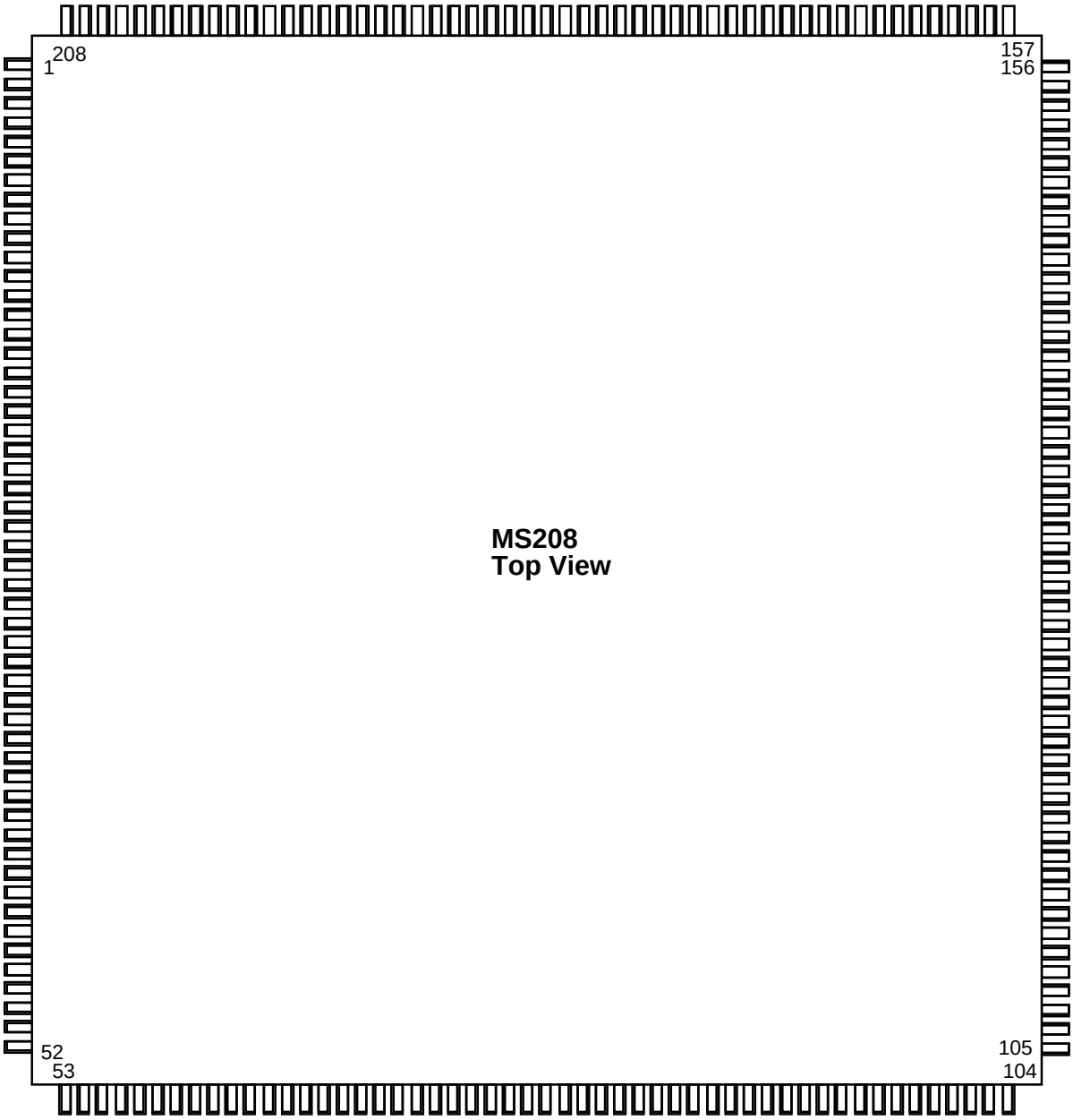
Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Data Output(7)	t_{DM}= Min t_{DO} = Max	$mode_{14..13}$ = 10 (fastest)	1.0	11	1.0	9	1.0	9	ns
		$mode_{14..13}$ = 01 (slowest)	2.0	15	2.0	12	2.0	12	ns
Data Output Hold	t_{DOH} *	$mode_{14..13}$ = 10 (fastest)	1.0	—	1.0	—	1.0	—	ns
Data Setup	t_{DS}	t_{rise} = 5ns t_{fall} = 5ns	7	—	6	—	6	—	ns
Data Hold	t_{DH}		4	—	3	—	3	—	ns

* 25pf loading on external putput signals, fastest settings

Boot Time Interface Parameters—RV4650

Parameter	Symbol	Test Conditions	RV4650 80MHz		RV4650 100MHz		RV4650 133MHz		Units
			Min	Max	Min	Max	Min	Max	
Mode Data Setup	t_{DS}	—	3	—	3	—	3	—	Master Clock Cycle
Mode Data Hold	t_{DH}	—	0	—	0	—	0	—	Master Clock Cycle

PHYSICAL SPECIFICATIONS — 208-PIN MQUAD

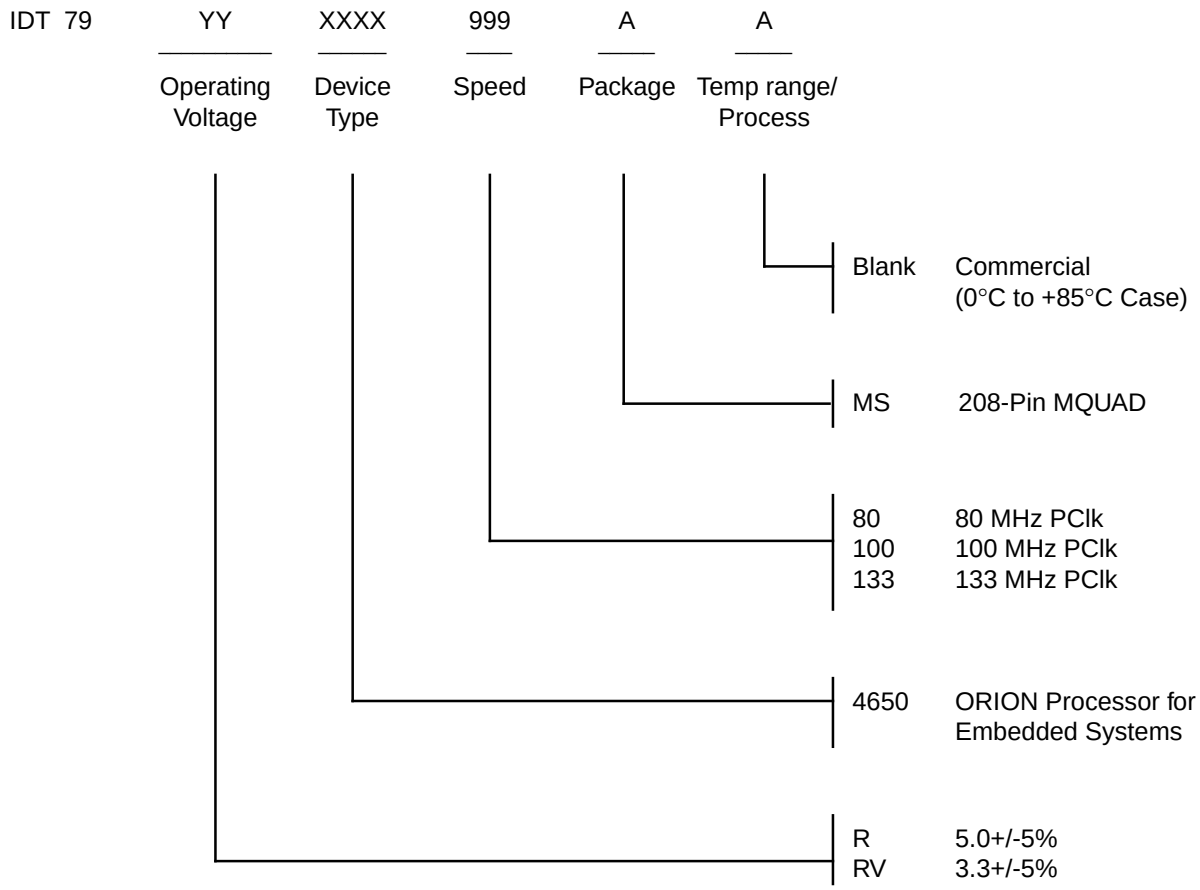


R4650 MQUAD PACKAGE PIN-OUT*

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	N.C.	53	N.C.	105	N.C.	157	N.C.
2	N.C.	54	N.C.	106	N.C.	158	N.C.
3	N.C.	55	N.C.	107	N.C.	159	SysAD59
4	N.C.	56	N.C.	108	N.C.	160	ColdReset*
5	N.C.	57	SysCmd2	109	N.C.	161	SysAD28
6	N.C.	58	SysAD36	110	N.C.	162	Vcc
7	N.C.	59	SysAD4	111	N.C.	163	Vss
8	N.C.	60	SysCmd1	112	N.C.	164	SysAD60
9	N.C.	61	Vss	113	N.C.	165	Reset*
10	SysAD11	62	Vcc	114	SysAD52	166	SysAD29
11	Vss	63	SysAD35	115	ExtRqst*	167	SysAD61
12	Vcc	64	SysAD3	116	Vcc	168	SysAD30
13	SysCmd8	65	SysCmd0	117	Vss	169	Vcc
14	SysAD42	66	SysAD34	118	SysAD21	170	Vss
15	SysAD10	67	Vss	119	SysAD53	171	SysAD62
16	SysCmd7	68	Vcc	120	RdRdy*	172	SysAD31
17	Vss	69	SysAD2	121	Modein	173	SysAD63
18	Vcc	70	Int5*	122	SysAD22	174	Vcc
19	SysAD41	71	SysAD33	123	SysAD54	175	Vss
20	SysAD9	72	SysAD1	124	Vcc	176	VccOK
21	SysCmd6	73	Vss	125	Vss	177	SysADC3
22	SysAD40	74	Vcc	126	Release*	178	SysADC7
23	Vss	75	Int4*	127	SysAD23	179	N.C.
24	Vcc	76	SysAD32	128	SysAD55	180	N.C.
25	SysAD8	77	SysAD0	129	NMI*	181	N.C.
26	SysCmd5	78	Int3*	130	Vcc	182	N.C.
27	SysADC4	79	Vss	131	Vss	183	N.C.
28	SysADC0	80	Vcc	132	SysADC2	184	N.C.
29	Vss	81	Int2*	133	SysADC6	185	VccP
30	Vcc	82	SysAD16	134	SysAD24	186	VssP
31	SysCmd4	83	SysAD48	135	Vcc	187	MasterClock
32	SysAD39	84	Int1*	136	Vss	188	Vcc
33	SysAD7	85	Vss	137	SysAD56	189	Vss
34	SysCmd3	86	Vcc	138	SysAD25	190	SysADC5
35	Vss	87	SysAD17	139	SysAD57	191	SysADC1
36	Vcc	88	SysAD49	140	Vcc	192	Vcc
37	SysAD38	89	Int0*	141	Vss	193	Vss
38	SysAD6	90	SysAD18	142	IOOut	194	SysAD47
39	ModeClock	91	Vss	143	SysAD26	195	SysAD15
40	WrRdy*	92	Vcc	144	SysAD58	196	SysAD46
41	SysAD37	93	SysAD50	145	IOIn	197	Vcc
42	SysAD5	94	ValidIn*	146	Vcc	198	Vss
43	Vss	95	SysAD19	147	Vss	199	SysAD14
44	Vcc	96	SysAD51	148	SysAD27	200	SysAD45
45	N.C.	97	Vss	149	N.C.	201	SysAD13
46	N.C.	98	Vcc	150	N.C.	202	SysAD44
47	N.C.	99	ValidOut*	151	N.C.	203	V_{SS}
48	N.C.	100	SysAD20	152	N.C.	204	V_{CC}
49	N.C.	101	N.C.	153	N.C.	205	SysAD12
50	N.C.	102	N.C.	154	N.C.	206	SysCmdP
51	N.C.	103	N.C.	155	N.C.	207	SysAD43
52	N.C.	104	N.C.	156	N.C.	208	N.C.

*N.C. pins should be left floating for maximum flexibility and compatibility with future designs.

ORDERING INFORMATION



Valid Combinations:

IDT 79R4650 - 80, 100, 133	MQUAD package