RC32364 Document Errata

Notes

Supplemental Information

This Document Errata reflects the errors in the "RC32364 RISController Advanced Architecture 32-bit Embedded Microprocessor Reference Manual" Version 1.0, May 1998.

Revision History

November 19, 1999: First version of document errata - Item #1.

February 15, 2000: Added Item #2.

Errata Items

Item #1 - Move Conditional on Not Zero

Issue: The operation in section Move Conditional on Not Zero on page A-4 of the manual reads:

`if GPR[rt] = 0 then GPR[rd] <-- GPR[rs]`. This is incorrect.

The operation should read: `if GPR[rt] ≠ 0 then GPR[rd] <-- GPR[rs].`

Item #2 - Data Cache Address Range

Issue: The RC32364 includes 2Kb of 2-way set associative data cache that corresponds to an address range between 0x000 and 0x7fc. The address offset for set A is 0x000, while the address offset for set B is 0x1000. To avoid any cache initialization problems, please select one of the following two initialization methods:

1. Initialize index location 0x000-0x3fc for set A and then 0x1000-0x13fc for set B.

or

2. Initialize as if the data cache were at least 8K large.