PowerPC® 750CXr RISC Microprocessor

Data Sheet

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(For DD4.0 Only)

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1. General Information

The PowerPC® 750CXr RISC Microprocessor is an implementation of the PowerPC family of reduced instruction set computer (RISC) microprocessors.

The information in this document is specific to revision DD 4.0 of the 750CXr and may not apply to subsequent revisions.

1.1 Features

This section summarizes the major features of the PowerPC 750CXr implementation of the PowerPC architecture.

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - 4-stage pipeline: fetch, dispatch, execute, and complete
  - Serialization control (predispatch, postdispatch, execution, serialization)
- Fixed-point units
  - Fixed-point unit 1 (FXU1); multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2); shift, rotate, arithmetic, logical
  - Single-cycle arithmetic, shift, rotate, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
  - Thirty-two, 32-bit general purpose registers
  - Secondary FXU executes integer add/compare instructions
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Load/store unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle misaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and little-endian byte addressing supported
  - Misaligned little-endian support in hardware
- Floating-point unit
  - Support for IEEE-754 standard single and double-precision floating-point arithmetic
  - Optimized for single-precision multiply/add
  - Thirty-two, 64-bit floating point registers
  - Enhanced reciprocal estimates
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add

- Floating-point unit (continued)
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- System unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- L1 Cache structure
  - 32KB, 32-byte line, 8-way set associative instruction cache
  - 32KB, 32-byte line, 8-way set associative data cache
  - Single-cycle cache access
  - Pseudo-LRU replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - 3-state (MEI) memory coherency
  - Hardware support for data coherency
  - Non-blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Memory management unit
  - 128-entry, 2-way set associative instruction TLB
  - 128-entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - 4 instruction BATs and 4 data BATs
  - Virtual memory support for up to 4 PB (2^{52}) virtual memory
  - Real memory support for up to 4 GB (2^{32}) of physical memory
  - Support for big/little-endian addressing
- Level 2 (L2) cache
  - Internal L2 cache controller and 4KB-entry tags; 256KB data SRAMs
  - Copy-back or write-through data cache on a page basis, or for all L2
  - 64-byte sectored line size
  - L2 frequency at core speed
  - On-board ECC
- Bus interface
  - Compatible with 60x processor interface (some pin functions removed, see *Table 5-2* on page 31)
  - 32-bit address bus
  - 64-bit data bus (also supports 32-bit mode)
  - Core-to-bus frequency multipliers of 2.5x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, supported
- Power
  - 6W typical @ 400 MHz
- Testability
  - LSSD scan design
  - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

1.2 Special Design Level Considerations/Features

The PowerPC 750CXr supports several unique features including those listed below. Section 6.7 “Operational and Design Considerations,” on page 41 provides a more detailed explanation of these features.

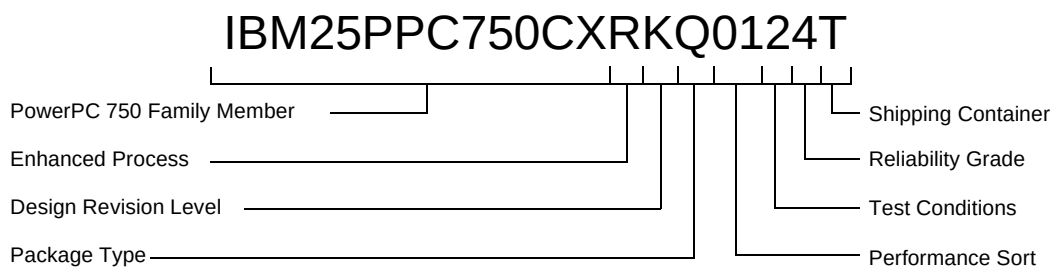
- Provides a 64- or 32-bit Data Bus mode (per setup of $\overline{\text{QACK}}$ pin).
- Supports 1.8V and 2.5V I/O signals.
- Uses a reduced pin list from earlier PowerPC 750 designs (see *Table 5-2* on page 31).
- Data Bus Write Only ($\overline{\text{DBWO}}$) shares a common pin with L2_TESTCLK.
- $\overline{\text{CHKSTP\_OUT}}$ shares a common pin with CLK_OUT.

1.3 Ordering Information

For available devices, contact your local IBM sales office.

Figure 1-1 provides the IBM part numbering nomenclature for the PowerPC 750CXr.

Figure 1-1. IBM Part Number Key



Design Revision Level	K = 4.0
Package Type	Q = Lead Free Plastic/Laminate Ball Grid Array
Performance Sort	01 = 300MHz, 333MHz w/o L2
	03 = 300MHz, 333MHz
	10 = 366 MHz
	20 = 400MHz
	40 = 466 MHz
	50 = 500MHz
	55 = 533MHz
Test Conditions	2 = +1.8V to +1.9V @ 95°C for < 500MHz, +1.85V to +1.95V @ 95°C for 500 MHz and 533MHz
Reliability Grade	4 = Grade 4
Shipping Container	T = Tray

1.4 Processor Version Register (PVR)

The PowerPC 750CXr has the following PVR values for the respective design revision levels.

Table 1-1. Process Version Register (PVR)

Design Revision Level	PVR
DD4.0	00083410

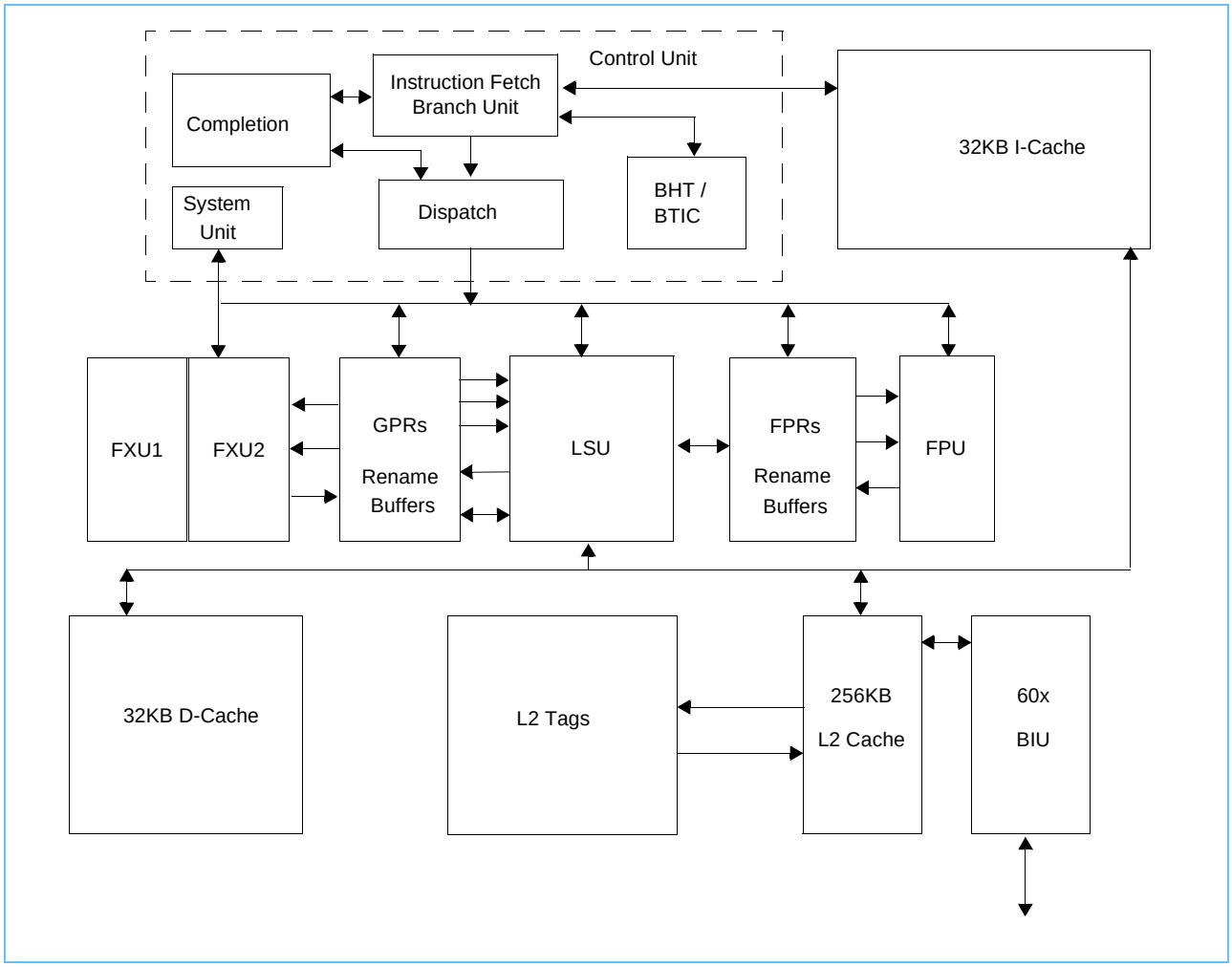
2. Overview

The PowerPC 750CXr is targeted for high performance, low power systems and a 60x bus. The PowerPC 750CXr also includes an internal 256KB L2 cache with on-board Error Correction Circuitry (ECC).

2.1 PowerPC 750CXr Block Diagram

Figure 2-1 shows a block diagram of the PowerPC 750CXr.

Figure 2-1. PowerPC 750CXr Block Diagram



3. General Parameters

Table 3-1 provides a summary of the general parameters of the PowerPC 750CXr.

Table 3-1. General Parameters

Item	Description
Technology	0.18µm CMOS Copper technology, six-layer metallization
Die size	42.7mm^2
Transistor count	20 million (including L2 cache)
Logic design	Fully static
Package	Surface mount 256-lead plastic ball grid array (PBGA), lead free 27mm x 27mm
Core power supply	1.85V for <500MHz, 1.9V for 500MHz and 533MHz
I/O power supply	+1.8V ± 5% +2.5V ± 5%

4. Electrical and Thermal Characteristics

This section provides both AC and DC electrical specifications, and thermal characteristics for the PowerPC 750CXr.

4.1 DC Electrical Characteristics

The tables in this section describe the PowerPC 750CXr's DC electrical characteristics. Table 4-1 provides the absolute maximum ratings.

Table 4-1. Absolute Maximum Ratings

Characteristic	Symbol	Value (BVSEL = 0)	Value (BVSEL = 1)	Unit
Core supply voltage	V_{DD}	-0.3 to +2.0	-0.3 to +2.00	V
PLL supply voltage	AV_{DD}	-0.3 to +2.0	-0.3 to +2.00	V
60x bus supply voltage	OV_{DD}	-0.3 to +2.0	-0.3 to +2.75	V
Input voltage	V_{IN}	-0.3 to +2.0	-0.3 to +2.75	V
Storage temperature range	T_{STG}	-55 to +150	-55 to +150	°C

Notes:

1. Functional and tested operating conditions are given in *Table 4-2* on page 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. **Caution:** V_{IN} must not exceed OV_{DD} by more than 0.6V at any time, including during power-on reset. This is a DC specification only. V_{IN} overshoot transients up to OV_{DD}+0.8v,and undershoots down to GND-0.8v (both measured with the 750CXr in the circuit) are allowed for up to 5ns or 1/3 bus clock cycle, whichever is less.
3. **Caution:** OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.0V, except for up to 20ms during power on/off reset.
4. **Caution:** V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.2V, except for up to 20ms during power up/down.
5. **Caution:** AV_{DD} must not exceed V_{DD} by more than 1.2V, except for up to 20ms during power up/down reset.

Table 4-2 provides the recommended operating conditions for the PowerPC 750CXr.

Table 4-2. Recommended Operating Conditions

Characteristic[1]	Symbol	Value	Unit
Core supply voltage < 500MHz	V_{DD}	+1.8 to +1.9	V
Core supply voltage @ 500 MHz and 533 MHz	V_{DD}	+1.85 to +1.95	V
PLL supply voltage	AV_{DD}	+1.8 to +1.95	V
60x bus supply voltage (1.8V mode)	OV_{DD}	+1.8 to +1.9	V
60x bus supply voltage (2.5V mode)	OV_{DD}	+2.375 to +2.625	V
Input voltage	V_{IN}	GND to OV_{DD}	V
Die-junction temperature (Grade 4)	T_J	0 to +95	°C

Note: These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

1. See performance sort in Section 1.3 on Page 11.

Table 4-3 provides the package thermal characteristics for the PowerPC 750CXr.

Table 4-3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
PBGA package thermal resistance, junction to ambient, thermal resistance, convection only[1]	θ_{JA}	15.9	°C/W
PBGA package thermal resistance, junction-to-ambient thermal resistance, 100 linear ft. per minute	θ_{JA}	13.9	°C/W
PBGA package thermal resistance, junction-to-board thermal resistance	θ_{JB}	7.4	°C/W
PBGA package thermal resistance, junction-to-case thermal resistance	θ_{JC}	0.7	°C/W

Note:
1. Assumes that the package is soldered to a 2S2P board.

Table 4-4 provides DC electrical characteristics for the PowerPC 750CXr.

Table 4-4. DC Electrical Specifications See Table 4-2 on page 15 for recommended operating conditions.

Characteristic	Symbol	Voltage		Unit	Notes
		Min	Max		
Input high voltage (all inputs except SYSCLK)	$V_{IH\ (1.8V)}$	+1.3	+1.9	V	2, 4
	$V_{IH(2.5V)}$	+1.9	+2.625	V	2
Input low voltage (all inputs except SYSCLK)	$V_{IL(1.8V)}$	GND	+0.66	V	4
	$V_{IL(2.5V)}$	GND	+0.7	V	
SYSCLK input high voltage	$CV_{IH(1.8V)}$	+1.3	+1.9	V	
	$CV_{IH(2.5V)}$	+1.95	+2.625	V	
SYSCLK input low voltage	$CV_{IL(1.8V/2.5V)}$	GND	+0.4	V	
Input leakage current, V_{IN} = OV_{DD} = 2.5V	I_{IN}	–	20	µA	3
Input leakage current, V_{IN} = OV_{DD} = 1.8V	I_{IN}	–	20	µA	3
Hi-Z (off state) leakage current, V_{IN} = OV_{DD} = 2.5V	I_{TSI}	–	20	µA	3
Hi-Z (off state) leakage current, V_{IN} = OV_{DD} = 1.8V	I_{TSI}	–	20	µA	3
Output high voltage, I_{OH} = –4mA	$V_{OH(1.8V)}$	+1.4	–	V	
	$V_{OH(2.5V)}$	+2.1	–	V	
Output low voltage, I_{OL} = 4mA	$V_{OL(1.8V, 2.5V)}$	–	+0.4	V	
Capacitance, V_{IN} =0 V, f = 1MHz	C_{IN}	–	+5.0	pF	1

Notes:
1. Capacitance values are guaranteed by design and characterization, and are not tested.
2. Maximum input high voltage for short duration (not continuous operation).
3. Additional input current may be attributed to the Level Protection Keeper Lock circuity. For details, see Section 6.7 on Page 41.
4. V_{IH} and V_{IL} minimum levels are set as a percentage of V_{DD}. V_{IH} is 65% and V_{IL} is 35% respectively.

Table 4-5 provides the power consumption for the PowerPC 750CXr.

Table 4-5. Power Consumption See Table 4-2 on page 15 for recommended operating conditions.

Power Mode	V_{DD}	T_j	Representative Processor Frequency							Unit	Notes
			300/333 MHz (No L2)	300/333 MHz (With L2)	366MHz	400MHz	466 MHz	500MHz	533MHz		
Full-On Mode											
Maximum	1.95V	95°C						9.2	9.8	W	1, 2, 4
	1.9V	95°C	6.8	6.8	7.0	7.5	8.2			W	
Typical	1.9V	65°C						7.3	7.8	W	1, 3, 4
	1.85V	65°C	5.2	5.2	5.6	6.0	6.7			W	
Doze Mode											
Maximum	1.95V	95°C						5.9	6.4	W	1, 2, 4
	1.9V	95°C	4.4	4.4	4.8	5.05	5.4			W	
Typical	1.9V	65°C						4.3	4.8	W	1, 3, 4
	1.85V	65°C	3.1	3.1	3.4	3.6	3.9			W	
Nap Mode											
Maximum	1.95V	95°C						3.05	3.3	W	1, 2, 4
	1.9V	95°C	2.5	2.5	2.7	2.85	2.85			W	
Typical	1.9V	65°C						1.65	1.65	W	1, 3, 4
	1.85V	65°C	1.5	1.5	1.5	1.5	1.55			W	
Sleep Mode											
Maximum	1.95V	95°C						3.0	32	W	1, 2, 4
	1.9V	95°C	2.5	2.5	26	2.8	2.85			W	
Typical	1.9V	50°C						1.22	1.28	W	1, 3, 4
	1.85V	50°C	1.08	1.08	1.1	1.12	1.12			W	

Notes:

1. These values apply for all valid 60x buses. The values do not include I/O Supply Power (OV_{DD}) or PLL/DLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically < 5% of V_{DD} power. AV_{DD} current is less tha 25mA.
2. Maximum power is specified for a mix of parts (both fast and slow process) running RC5 at the indicated core voltage, junction temperature, and core frequency.
3. Typical power is specified for a mix of parts (both fast and slow process) running RC5 at the indicated core voltage, junction temperature, and core frequency.
4. Guaranteed by design and characterization, and is not tested.

4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PowerPC 750CXr. After fabrication, parts are sorted by maximum processor core frequency as shown in the Section 4.2.1 on Page 18, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG(0-3) signals.

4.2.1 Clock AC Specifications

Table 4-6 provides the clock AC timing specifications as defined in Figure 4-1.

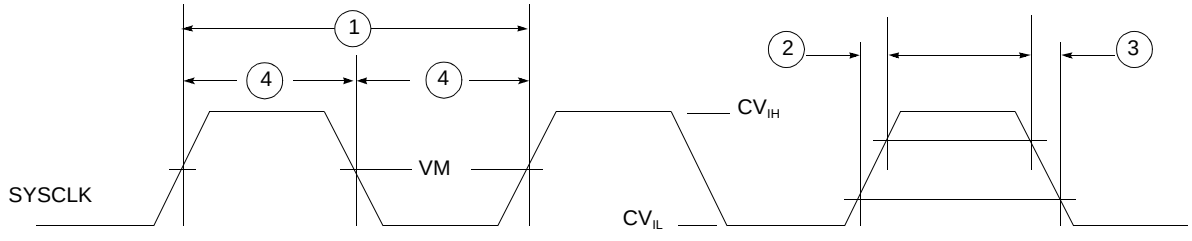
Table 4-6. Clock AC Timing Specifications[1,6] See Table 4-2 on page 15, for recommended operating conditions.

Num	Characteristic	Value		Unit	Notes
		Min	Max		
	Processor frequency	300	533	MHz	
	SYSCLK frequency	66	133	MHz	1
1	SYSCLK cycle time	7.5	15	ns	
2, 3	SYSCLK rise and fall time (slew rate)	1.0	4.0	V/ns	2, 3
4	SYSCLK duty cycle measured at 0.8V	25	75	%	3
	SYSCLK jitter	–	±150	ps	4, 3
	Internal PLL relock time	–	100	µs	5

Notes:

1. Caution: The SYSCLK frequency and the PLL_CFG[0:3] settings must be chosen such that the resulting SYSCLK (bus) frequency and CPU (core) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:3] signal description in Section 6.1 “PLL Configuration,” on page 34 for valid PLL_CFG[0:3] settings.
2. Rise and fall times for the SYSCLK input are measured from +0.4 to +1.2 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. The total input jitter (short term and long term combined) must be under ±150 ps. Contact IBM for use with spread-spectrum clocks or clocks with jitter in excess of ±150 ps.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 4-1. SYSCLK Input Timing Diagram



VM - Midpoint Voltage (+0.85V)

4.3 Spread Spectrum Clock Generator (SSCG)

When designing with an SSCG, there are a number of issues that must be taken into account.

An SSCG creates a controlled amount of long-term jitter. In order for a receiving PLL in the 750CXr to function correctly in this environment, it must be able to accurately track the SSCG clock jitter.

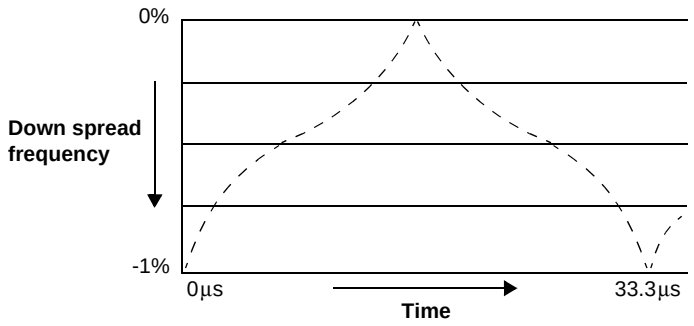
The accuracy with which the 750CXr PLL can track the SSCG is referred to as tracking skew. When performing system timing analysis, the tracking skew must be added to or subtracted from the I/O timing specifications, because the skew appears as a static phase error between the internal PLL and the SSCG clock.

To minimize the impact on I/O timing, the following SSCG configuration is recommended:

- Down-spread mode ≤ 1% of the maximum frequency
- Modulation frequency of 30 kHz
- Linear sweep modulation or a modulation profile (Hershey Kiss™) as shown in Figure 4-2.

In this configuration, the tracking skew is less than 100 ps.

Figure 4-2. Linear Sweep Modulation Profile



4.4 60x Bus Input AC Specifications

Table 4-7 provides the 60x bus input AC timing specifications for the PowerPC 750CXr as defined in Figure 4-3 and Figure 4-4.

Table 4-7. 60x Bus Input Timing Specifications[1,6] See Table 4-2 on page 15 for operating conditions.

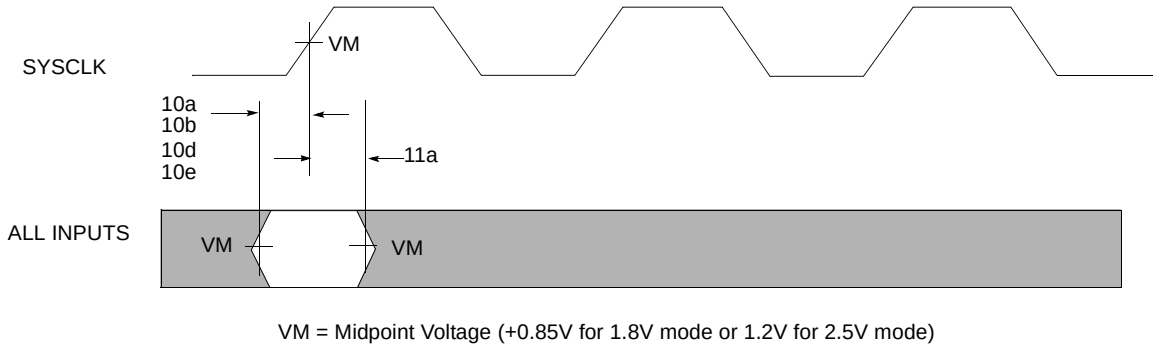
Num	Characteristic	1.8V Mode		2.5V Mode		Unit	Notes
		Min	Max	Min	Max		
10a	Address/Data/Transfer attribute inputs valid to SYSCLK (input setup)	1.15	—	1.25	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	1.15	—	1.25	—	ns	3
10c	Mode select input setup to HRESET (QACK)	8	—	8	—	t_{sysclk}	4, 5, 7
10d	TS to SYSCLK (input setup)	1.35	—	1.4	—	ns	—
10e	DBWO to SYSCLK (input setup)	1.5	—	1.6	—	ns	—
11a	SYSCLK to inputs invalid (input hold)	0.65	—	0.3	—	ns	2
11b	HRESET to mode select input hold (QACK)	0	—	0	—	ns	4, 7

Notes:

1. Input specifications are measured from the midpoint voltage of the signal in question to the midpoint voltage of the rising edge of the input SYSCLK. Input and output timings are measured at the pin (see Figure 4-3). The midpoint voltage used for all pins is 0.85V for 1.8V mode and 1.2V for 2.5V mode.
2. Address/Data Transfer Attribute inputs are composed of all bidirectional and input signals except those listed in Note 3.
3. All other signal inputs are composed of the following: TA, QACK, and ARTRY.
4. The setup and hold time is with respect to the rising edge of HRESET (see Figure 4-4 on page 21).
5. t_{SYSCLK}, is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
6. These values are guaranteed by design and characterization, and are not tested.
7. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a *minimum of 255 bus clocks* after the PLL relock time during the power-on reset sequence.

Figure 4-3 provides the input timing diagram for the PowerPC 750CXr.

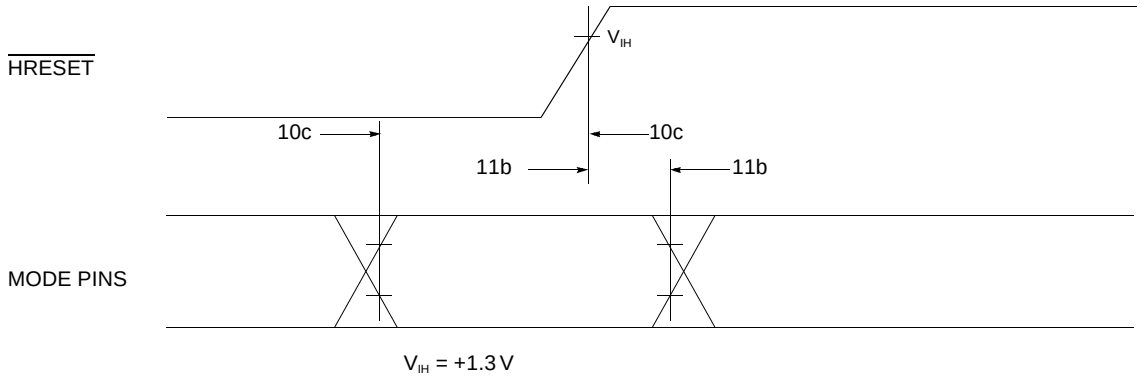
Figure 4-3. Input Timing Diagram



VM = Midpoint Voltage (+0.85V for 1.8V mode or 1.2V for 2.5V mode)

Figure 4-4 provides the mode select input timing diagram for the PowerPC 750CXr.

Figure 4-4. Mode Select Input Timing Diagram



4.5 60x Bus Output AC Specifications

Table 4-8 provides the 60x bus output AC timing specifications for the PowerPC 750CXr as defined in Figure 4-7 on page 24.

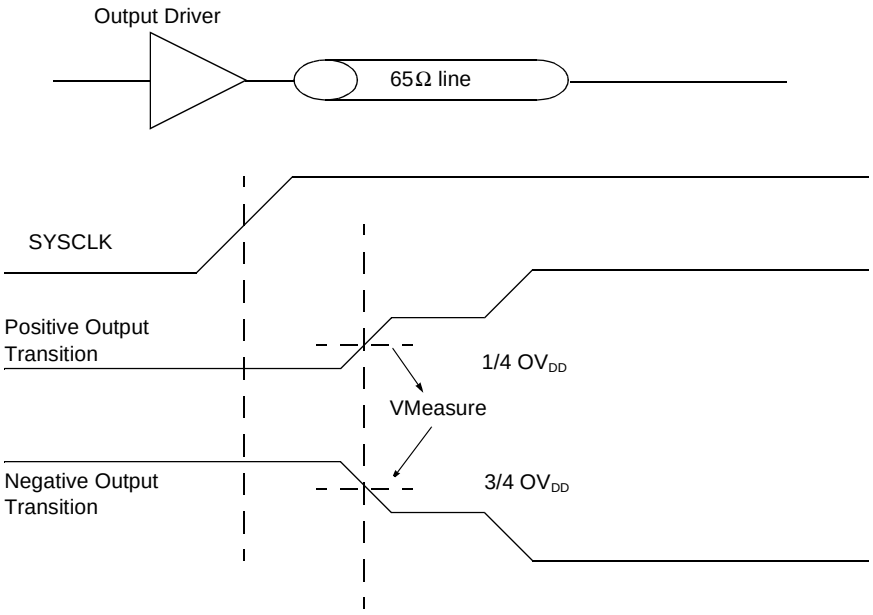
Table 4-8. 60x Bus Output AC Timing Specifications[1,4,6] See Table 4-2 on page 15 for operating conditions.

Num	Characteristic	1.8V Mode		2.5V Mode		Unit	Notes
		Min.	Max.	Min.	Max.		
12	SYSCLK to Output Driven (Output Enable Time)	0.3		0.3		ns	
13	SYSCLK to Output Valid	–	2.31	–	2.2	ns	
14	SYSCLK to Output Invalid (Output Hold)	0.4		0.4		ns	2
15	SYSCLK to Output High Impedance (all signals except ARTRY)	–	2.5	–	2.5	ns	
16	SYSCLK to ARTRY high impedance before precharge	–	3.0	–	3.0	ns	
17	SYSCLK to ARTRY precharge enable	$0.2t_{SYSCLK}$+1.0		$0.2t_{SYSCLK}$+1.0		ns	2, 3, 5
18	Maximum delay to ARTRY precharge		1		1	t_{SYSCLK}	3, 5
19	SYSCLK to ARTRY high impedance after precharge		2		2	t_{SYSCLK}	3, 5

Notes:

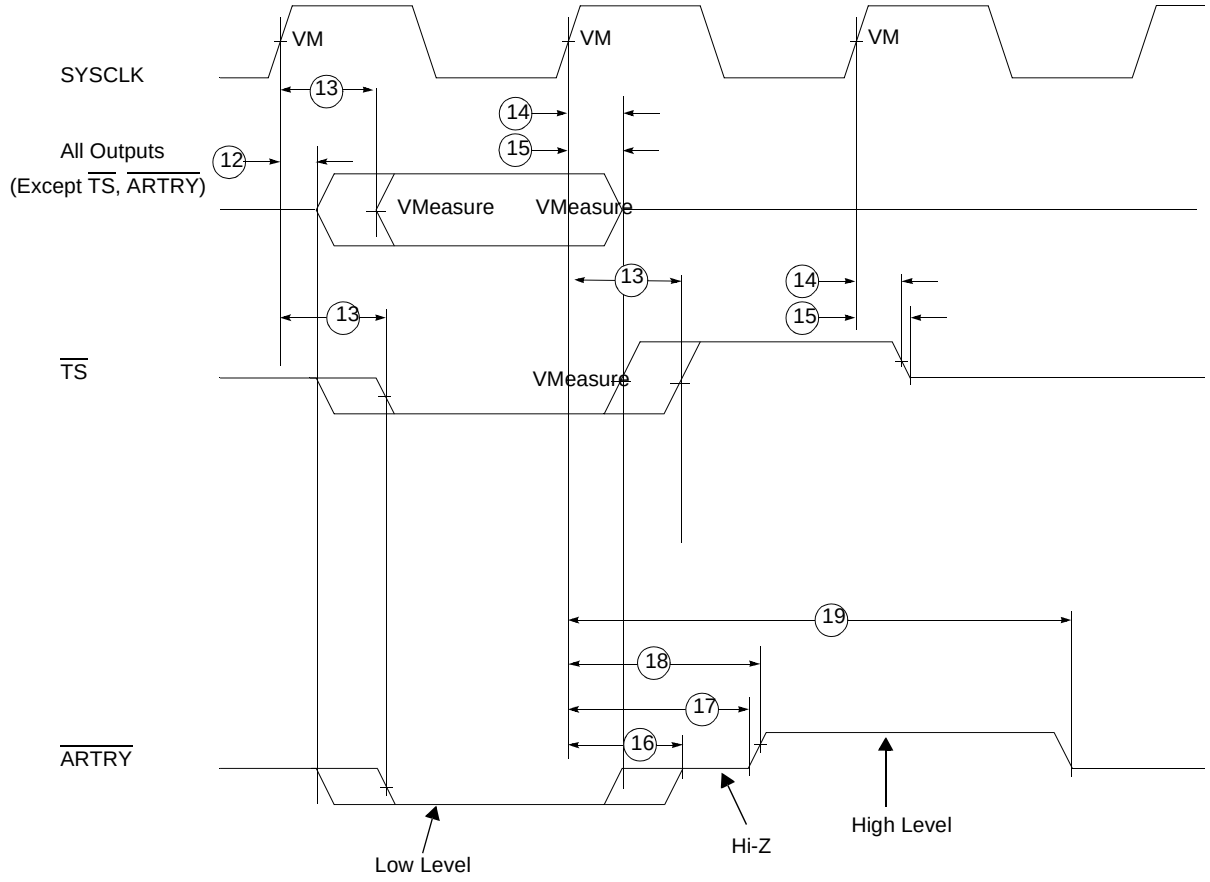
1. All output specifications are measured from the midpoint voltage of the rising edge of SYSCLK to the midpoint voltage of the signal in question defined in figure 4-5. Both input and output timings are measured at the pin. Timings are determined by design. The midpoint voltage used for all pins is 0.85V for 1.8V mode and 1.2V for 2.5V mode.
2. This minimum parameter assumes CL = 0pF.
3. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
4. Output signal transitions are defined in figure 4-5.
5. Nominal precharge width for ARTRY is 1.0 t_{SYSCLK}.
6. Guaranteed by design and characterization, and not tested.

Figure 4-5. Output Valid Timing Definition



Output Transition defined between SYSCLK @ +0.85 V and the respective transition level.
(**Note:** The timing definition uses an infinitely long transmission line model.)

Figure 4-6. Output Timing Diagram for PowerPC 750CXr



VMeasure is defined with reference to Figure 4-5 as 1/4 of the transition of OV_{DD}.

4.5.1 IEEE 1149.1 AC Timing Specifications

Table 4-9 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 4-7, Figure 4-8, Figure 4-9, and Figure 4-10. The five JTAG signals are; TDI, TDO, TMS, TCK, and $\overline{\text{TRST}}$.

Table 4-9. JTAG AC Timing Specifications (Independent of SYSCLK)
See Table 4-2 on page 15 for operating conditions.

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	20	MHz	
1	TCK cycle time	50	—	ns	
2	TCK clock pulse width measured at +1.1V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	Specification obsolete, intentionally omitted				
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	0	—	ns	2
7	Boundary-scan input data hold time	13	—	ns	2
8	TCK to output data valid	–	8	ns	3, 5
9	TCK to output high impedance	3	19	ns	3, 4
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	2.5	12	ns	5
13	TCK to TDO high impedance	3	9	ns	4
14	TCK to output data invalid (output hold)	0	–	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 4-7 provides the JTAG clock input timing diagram.

Figure 4-7. JTAG Clock Input Timing Diagram

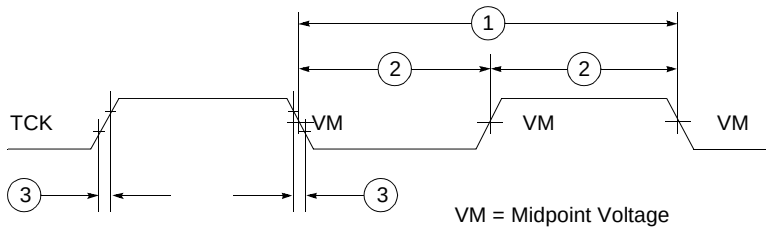


Figure 4-8 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 4-8. $\overline{TRST}$ Timing Diagram

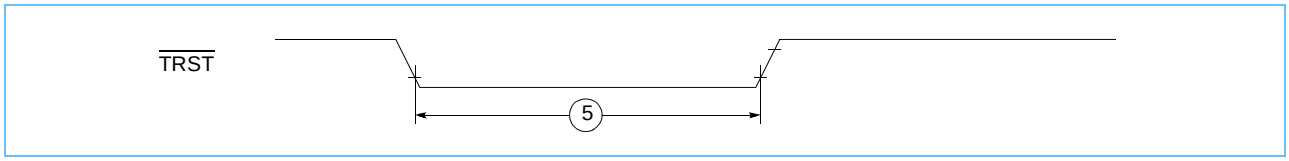


Figure 4-9 provides the boundary-scan timing diagram.

Figure 4-9. Boundary-Scan Timing Diagram

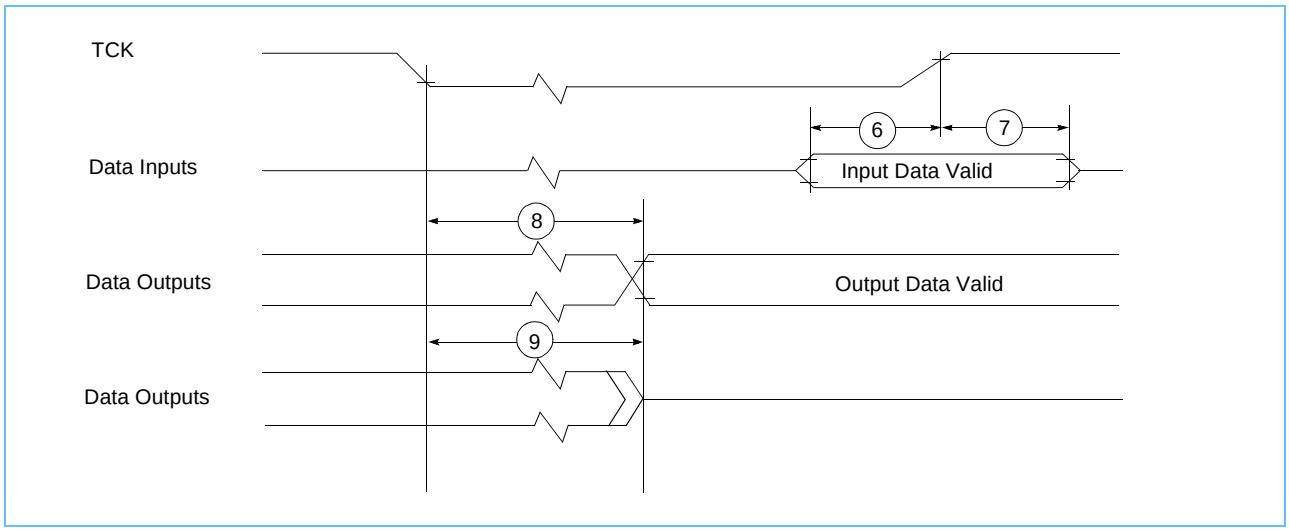
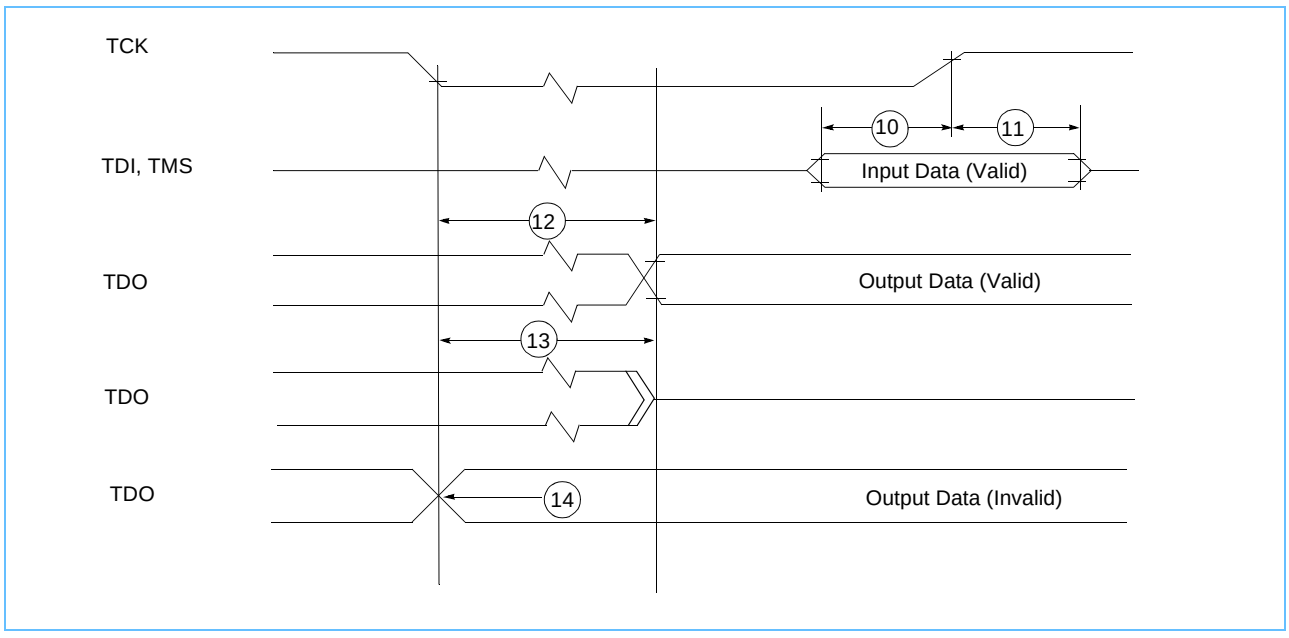


Figure 4-10 provides the test access port timing diagram.

Figure 4-10. Test Access Port Timing Diagram



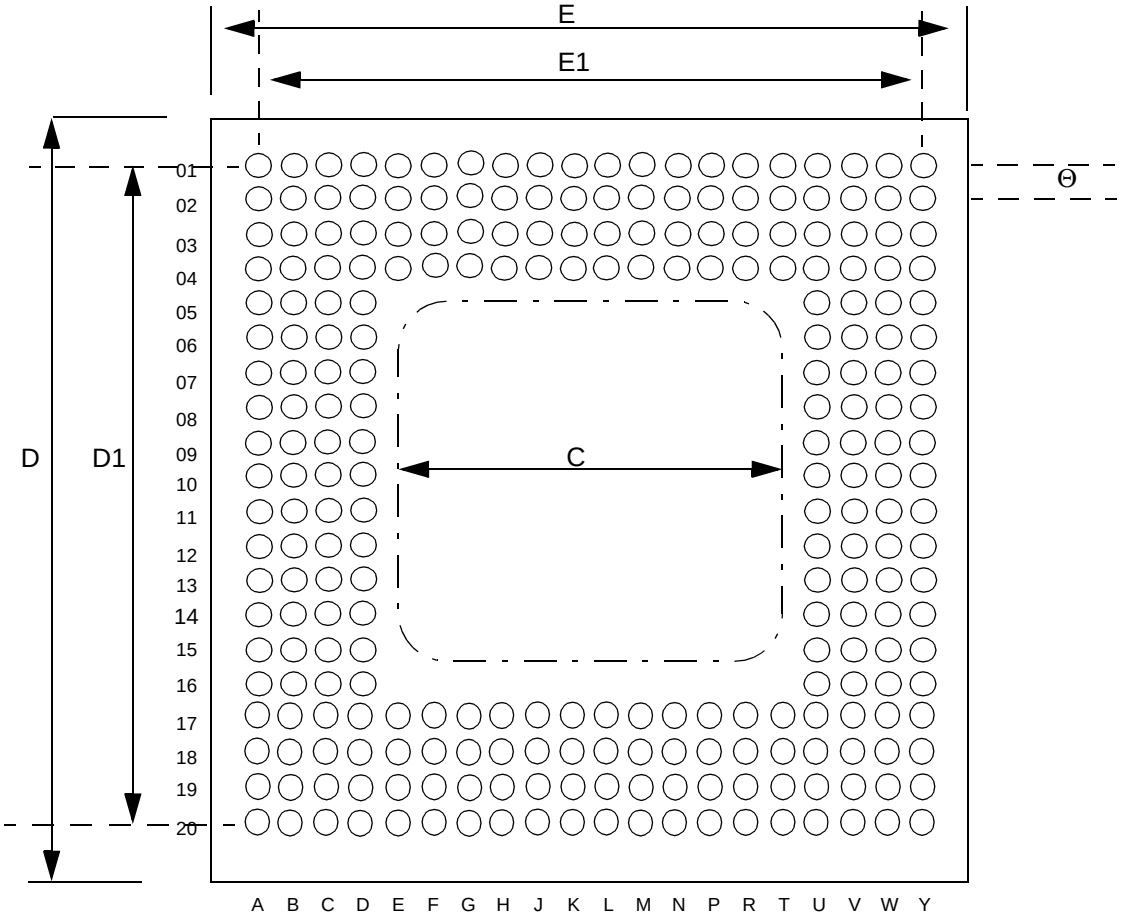
5. PowerPC 750CXr Dimension and Physical Signal Assignments

IBM offers a plastic ball grid array, PBGA, which supports 256 balls as the PowerPC 750CXr lead free package. This package is JEDEC MSL-3 and should be handled accordingly.

The following sections contain several views of the package, pin information, and a pin listing.

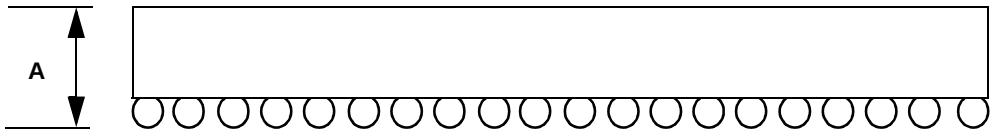
Figure Description	Figure Number and Page
Shows the pinout of the 256 PBGA package as viewed from the solder ball surface.	*Figure 5-1* on page 27
Shows a side profile of the 256 PBGA package including the height from the top of the copper heat spreader to the bottom of the solder balls.	*Figure 5-2* on page 28
Provides a more detailed side profile including the encapsulant (glob) referenced.	*Figure 5-3* on page 28

Figure 5-1. Pinout of the 256 PBGA Package as Viewed from Solder Ball side



Dimension	Nominal Length (mm)
C	15.1 max
D	27.00
D1	24.13
E	27.00
E1	24.13
Θ	1.27

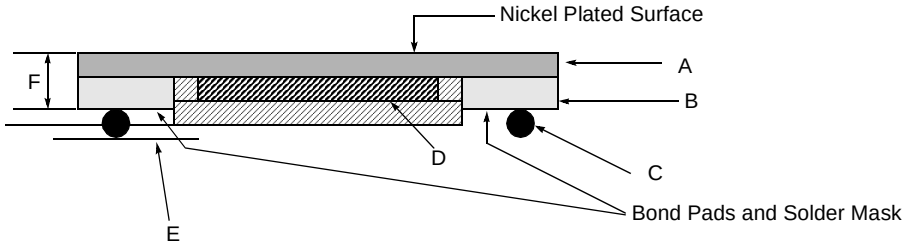
Figure 5-2. Side Profile View of PBGA



Dimension	Total Package Height (mm)
A	1.539 +/-0.127

Note: Dimension A consists of the entire package with solder balls before reflow.

Figure 5-3. Side Profile View Showing Exposed Cavity



Item	Description	Length (mm)	Height (mm)
A	Cu Heat Spreader	27	0.356 nominal
B	Laminate including plating	27	0.585 +/-0.076
C	Solder ball	N/A	0.58 +/- 0.08
D	Chip Cavity	15.1 max	0.47 max
E	Minimum Glop to Solder Ball Height	N/A	0.03
F	Cu Heat Spreader, Laminate, Bond Pads, and Plating	N/A	0.955 +/-0.1

Figure 5-4. PowerPC 750CXr Microprocessor Ball Placement

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	g	g	dh3	g	dh9	dh11	dh13	dh15	dh16	dh19	dh20	dh23	dh24	dh26	dh28	dh30	g	a4	g	g
B	g	g	vdd	dh4	dh6	dh8	dh12	g	dh18	g	g	dh21	g	dh27	dh31	a1	a3	vdd	g	g
C	dh2	vdd	g	vdd	ovdd	dh7	dh10	dh14	dh17	g	g	dh22	dh25	dh29	a0	ovdd	vdd	g	vdd	a5
D	ovdd	dh1	vdd	g	vdd	dh5	ovdd	vdd	ovdd	vdd	vdd	ovdd	vdd	ovdd	a2	vdd	g	vdd	a6	g
E	$\overline{\text{hreset}}$	dh0	$\overline{\text{dbwo}}$[1]	vdd													vdd	ovdd	a8	a11
F	pllcfg0	$\overline{\text{lssd\_mode}}$	$\overline{\text{mcp}}$	l1_tstclk													a7	a9	a10	a13
G	pllcfg2	pllcfg1	sysclk	ovdd													ovdd	a12	a14	a15
H	bvsel	pllcfg3	avdd	vdd													vdd	tt_0	g	tt_1
J	g	$\overline{\text{int}}$	$\overline{\text{ckstp\_in}}$	ovdd													ovdd	tt_3	ts	tt_2
K	$\overline{\text{sreset}}$	$\overline{\text{qack}}$	g	vdd													vdd	g	g	tt_4
L	$\overline{\text{qreq}}$	g	g	vdd													vdd	g	g	tsiz0
M	$\overline{\text{dbg}}$	$\overline{\text{tea}}$	$\overline{\text{artry}}$	ovdd													ovdd	tsiz2	tsiz1	$\overline{\text{ta}}$
N	$\overline{\text{br}}$	g	tdo	vdd													vdd	$\overline{\text{aack}}$	g	$\overline{\text{tbst}}$
P	$\overline{\text{bg}}$	$\overline{\text{ckstp\_out}}$	tdi	ovdd													ovdd	a19	a17	a16
R	$\overline{\text{wt}}$	$\overline{\text{gbl}}$	tms	$\overline{\text{trst}}$													a24	a22	a21	a18
T	dl31	$\overline{\text{ci}}$	tck	vdd													vdd	ovdd	a23	a20
U	ovdd	dl30	vdd	g	vdd	dl26	ovdd	vdd	ovdd	vdd	vdd	ovdd	vdd	ovdd	a29	vdd	g	vdd	a25	g
V	dl29	vdd	g	vdd	ovdd	dl24	dl21	dl17	dl14	g	g	dl9	dl6	dl2	a31	ovdd	vdd	g	vdd	a26
W	g	g	vdd	dl27	dl25	dl23	dl19	g	dl13	g	g	dl10	g	dl4	dl0	a30	a28	vdd	g	g
Y	g	g	dl28	g	dl22	dl20	dl18	dl16	dl15	dl12	dl11	dl8	dl7	dl5	dl3	dl1	g	a27	g	g

Note: This view is looking down from above the PowerPC 750CXr placed and soldered on the system board.

1. $\overline{\text{DBWO}}$ multiplexed with L2_TSTCLK function, see Section 6.7.4 on Page 42 for details.

Table 5-1. Signal Listing for the 256 PBGA Package

Signal Name	Pin Count	Active	I/O	Notes
A0–A31	32	High	I/O	
AACK	1	Low	Input	
ARTRY	1	Low	I/O	
BG	1	Low	Input	
BR	1	Low	Output	
CI	1	Low	Output	
CKSTP_IN	1	Low	Input	
CKSTP_OUT[2]	1	Low	Output	
DBG	1	Low	Input	
DH0-DH31	32	High	I/O	
DL0-DL31	32	High	I/O	
GBL	1	Low	I/O	
HRESET	1	Low	Input	
INT	1	Low	Input	
L1_TSTCLK[1]	1	High	Input	
DBWO/L2_TSTCLK[1,2,3]	1	High	Input	
LSSD_MODE[1]	1	Low	Input	
MCP	1	Low	Input	
PLL_CFG[0-3]	4	High	Input	
QACK[2]	1	Low	Input	OPTIONAL: 64/32-Bit Data Bus mode select. This function will be set when HRESET transitions (low to high). QACK: low = 64-bit mode, high = 32-bit mode.
QREQ	1	Low	Output	
SRESET	1	Low	Input	
SYSCLK	1	—	Input	
TA	1	Low	Input	
TBST	1	Low	I/O	
TCK	1	High	Input	
TDI	1	High	Input	
TDO	1	High	Output	
TEA	1	Low	Input	
TMS	1	High	Input	
TRST	1	Low	Input	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. The CKSTP_OUT signal in test mode allows viewing the PowerPC 750CXr internal clocks.
   The QACK signal allows selection of 32-bit mode.(See the *PowerPC 750CXr* User's Manual for more information.)
3. L2-TSTCLK in normal mode is DBWO, for details, see Section 6.7.4 on Page 42.

Table 5-1. Signal Listing for the 256 PBGA Package (Continued)

Signal Name	Pin Count	Active	I/O	Notes
$\overline{TS}$	1	Low	I/O	
TSIZ0–TSIZ2	3	High	Output	
TT0–TT4	5	High	I/O	
$\overline{WT}$	1	Low	Output	
BVSEL	1	High	Input	Pin set LOW = +1.8 V, pin set HIGH = +2.5 V
AV_{DD}	1			Supply for PLL
OV_{DD}	24			Supply for Receiver/Drivers
V_{DD}	40			Supply for Core
Ground	53			Common Ground

Notes:
1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. The $\overline{CKSTP\_OUT}$ signal in test mode allows viewing the PowerPC 750CXr internal clocks.
   The QACK signal allows selection of 32-bit mode.(See the *PowerPC 750CXr* User's Manual for more information.)
3. L2-TSTCLK in normal mode is DBWO, for details, see Section 6.7.4 on Page 42.

Table 5-2. PPC750 Signals Not Supported in the 750CXr

Signal Name	Pin Count	Active	I/O
$\overline{ABB}$	1	Low	I/O
$\overline{DBB}$	1	Low	I/O
$\overline{DBDIS}$	1	Low	Input
$\overline{RSRV}$	1	Low	Output
$\overline{SMI}$	1	Low	Input
TBEN	1	High	Input
VOLTDET	1	High	Output
AP0–3	4	High	I/O
DP0–7	8	High	I/O
$\overline{DRTRY}$	1	Low	Input
$\overline{TLBISYNC}$	1	Low	Input

Table 5-3. Signal Locations

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
A0	C15	DH0	E2	DL0	W15	AACK	N18
A1	B16	DH1	D2	DL1	Y16	ARTRY	M3
A2	D15	DH2	C1	DL2	V14	BG	P1
A3	B17	DH3	A3	DL3	Y15	BR	N1
A4	A18	DH4	B4	DL4	W14	BVSEL	H1
A5	C20	DH5	D6	DL5	Y14	CI	T2
A6	D19	DH6	B5	DL6	V13	CKSTP_IN	J3
A7	F17	DH7	C6	DL7	Y13	CKSTP_OUT	P2
A8	E19	DH8	B6	DL8	Y12	DBG	M1
A9	F18	DH9	A5	DL9	V12	GBL	R2
A10	F19	DH10	C7	DL10	W12	HRESET	E1
A11	E20	DH11	A6	DL11	Y11	INT	J2
A12	G18	DH12	B7	DL12	Y10	L1_TSTCLK	F4
A13	F20	DH13	A7	DL13	W9	DBWO/L2_TSTCLK[1]	E3
A14	G19	DH14	C8	DL14	V9	LSSD_MODE	F2
A15	G20	DH15	A8	DL15	Y9	MCP	F3
A16	P20	DH16	A9	DL16	Y8	PLL_CFG0	F1
A17	P19	DH17	C9	DL17	V8	PLL_CFG1	G2
A18	R20	DH18	B9	DL18	Y7	PLL_CFG2	G1
A19	P18	DH19	A10	DL19	W7	PLL_CFG3	H2
A20	T20	DH20	A11	DL20	Y6	QACK (Also used for 64/32-bit DB select.)	K2
A21	R19	DH21	B12	DL21	V7	QREQ	L1
A22	R18	DH22	C12	DL22	Y5	SRESET	K1
A23	T19	DH23	A12	DL23	W6	SYSCLK	G3
A24	R17	DH24	A13	DL24	V6	TA	M20
A25	U19	DH25	C13	DL25	W5	TBST	N20
A26	V20	DH26	A14	DL26	U6	TCK	T3
A27	Y18	DH27	B14	DL27	W4	TDI	P3
A28	W17	DH28	A15	DL28	Y3	TDO	N3
A29	U15	DH29	C14	DL29	V1	TEA	M2
A30	W16	DH30	A16	DL30	U2	TMS	R3
A31	V15	DH31	B15	DL31	T1	TRST	R4
						TS	J19
						TSIZ0	L20
						TSIZ1	M19
						TSIZ2	M18
						TT0	H18
						TT1	H20
						TT2	J20
						TT3	J18
						TT4	K20
						WT	R1

Note:

1. See Section 6.7.4 on Page 42 for a detailed discussion.

Table 5-4. Voltage and Ground Assignments

AV_{DD}	OV_{DD}	V_{DD}	V_{DD}	GND	GND
H3	M4	B3	L4	A1	L3
	M17	B18	L17	A2	L18
	P4	C2	N4	A4	L19
	P17	C4	N17	A17	N2
	T18	C17	T4	A19	N19
	U1	C19	T17	A20	U4
	U7	D3	U3	B1	U17
	U9	D5	U5	B2	U20
	U12	D8	U8	B8	V3
	U14	D10	U10	B10	V10
	V5	D11	U11	B11	V11
	V16	D13	U13	B13	V18
	C5	D16	U16	B19	W1
	C16	D18	U18	B20	W2
	D1	E4	V2	C3	W8
	D7	E17	V4	C10	W10
	D9	H4	V17	C11	W11
	D12	H17	V19	C18	W13
	D14	K4	W3	D4	W19
	E18	K17	W18	D17	W20
	G4			D20	Y1
	G17			H19	Y2
	J4			J1	Y4
	J17			K3	Y17
				K18	Y19
				K19	Y20
				L2	

6. System Design Information

This section provides electrical and thermal design recommendations for successful application of the PowerPC 750CXr.

6.1 PLL Configuration

PLL-CFG (Table 6-1) must be set so that both SYSCLK and the core frequency are within the Clock AC Timing Specifications shown in *Table 4-6* on page 18. In addition, the core frequency must not exceed the limit specified in the part number, and the system must meet the required specifications.

Table 6-1. PowerPC 750CXr Microprocessor PLL Configuration

PLL_CFG (0:3)		Processor to Bus Frequency Ratio (r)
Bin	Dec	
0000	0	2.5x
0001	1	7.5x[1]
0010	2	7x
0011	3	PLL Bypass[2]
0100	4	2x[1]
0101	5	6.5x
0110	6	9x[1]
		10x[1]
0111	7	4.5x
1000	8	3x
1001	9	5.5x
1010	10	4x
1011	11	5x
1100	12	8x[1]
1101	13	6x
1110	14	3.5x
1111	15	Off[3]

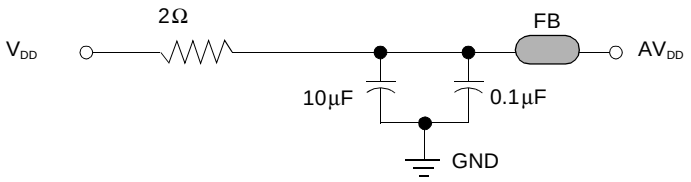
Notes:
1. The 2x,7.5x, 8x 9x, and 10x Processor to Bus Ratios are currently not supported.
2. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note:** The AC timing specifications given in the document do not apply in PLL-bypass mode.
3. In Clock - off mode, no clocking occurs inside the PowerPC 750CXr regardless of the SYSCLK input.

6.2 PLL Power Supply Filtering

The AV_{DD} power signal is provided on the PowerPC 750CXr to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered using a circuit similar to the one shown in Figure 6-1. The circuit should be placed as close as

possible to the AV_{DD} pin to ensure it filters out as much noise as possible. The referenced ferrite bead, FB, shown in *Figure 6-1* should supply an impedance of approximately 30Ω in the 100MHz region (Murata BLM21P300S or similar).

Figure 6-1. PLL Power Supply Filter Circuit



6.3 Decoupling Recommendations

Due to the PowerPC 750CXr's feature large address and data buses, and high operating frequencies, the PowerPC 750CXr can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerPC 750CXr system, and the PowerPC 750CXr itself requires a clean, tightly regulated source of power.

Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor with a low ESR (effective series resistance) rating at each VDD and OVDD pin of the PowerPC 750CXr. It is also recommended that these decoupling capacitors receive their power from separate VDD, OVDD, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should range in value from 220pF to 10µF to provide both high and low-frequency filtering, and should be placed as close as possible to their associated VDD or OVDD pins. Suggested values for the VDD pins: 220pF (ceramic X7R), 0.01µF (ceramic X7R), and 0.1µf (ceramic X7R). Suggested values for the OVDD pins: 0.01µF (ceramic X7R), 0.1µf (ceramic X7R), and 10µF (tantalum). Only SMT (surface-mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD and OVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance.

- Suggested bulk capacitors: 100µF (AVX TPS tantalum) or 330µF (AVX TPS tantalum).

6.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, and GND pins of the PowerPC 750CXr.

6.5 Output Buffer DC Impedance

The PowerPC 750CXr 60x drivers were characterized over various process, voltage, and temperature conditions. To measure Z_0, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of the resistor is varied until the pad voltage is $OV_{DD}/2$; see *Figure 6-2* below.

The output impedance is actually the average of two resistances: the resistance of the pull-up and the resistance of pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until Pad = $OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until Pad = $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. With a properly designed driver R_P and R_N are close to each other in value, then $Z_0 = (R_P + R_N)/2$.

Figure 6-2. Driver Impedance Measurement

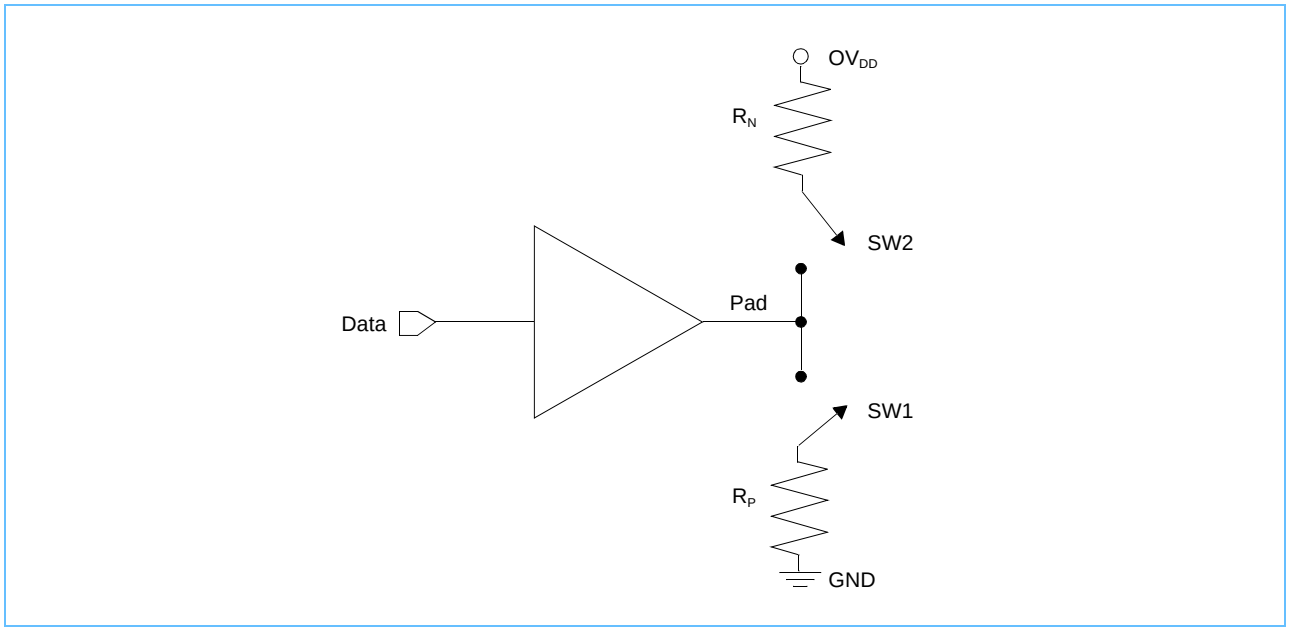


Table 6-2 on page 37 summarizes the impedance a board designer would design to for a typical process.

Table 6-2. Driver Impedance Characteristics

Process	60x Impedance (Ω)	V_{DD}, OV_{DD} (V)	Temperature (°C)
Worst	65	1.8, 1.8	95
Typical	50	1.85, 1.85	65
Best	40	1.90, 1.90	0
Worst	65	1.8, 2.38	95
Typical	50	1.85, 2.5	65
Best	40	1.90, 2.62	0

6.5.1 Input-Output Usage

Table 6-3 provides details on the input-output usage of the PowerPC 750CXr signals. The column titled Usage Group refers to the general functional category of the signal.

In the PowerPC 750CXr, certain input-output signals have pull-ups and pull-downs, which may or may not be enabled. The column titled I/O with Internal Resistors defines which signals have these pull-ups or pull-downs, and their active or inactive state.

The column titled “Level Protect” defines which signals have the designated function added to their I/O cell. For more information, see Section 6.7.1 “Level Protection,” on page 41.

Table 6-3. Input-Output Usage

PowerPC 750CXr Signal Name	Active Level	Input/ Output	Usage Group	I/O with Internal Resistors	Level Protect	Required External Resistor	Comments
A0-31	N/A	BIDI	Address Bus		Keeper		See Notes 1, 3, and 4.
$\overline{\text{AACK}}$	Low	IN	Address Termination		Keeper		Must be actively driven. See Notes 3 and 4.
$\overline{\text{ARTRY}}$	Low	BIDI	Address Termination		Keeper	5kΩ	Pull-up to OV_{DD} required. See Notes 3 and 4.
$\overline{\text{BG}}$	Low	IN	Address Arbitration		Keeper		Active driver or pull-down. See Notes 3 and 4.
$\overline{\text{BR}}$	Low	OUT	Address Arbitration		Keeper		Chip actively drives. See Notes 3 and 4.
BVSEL	N/A	IN	I/O Level		Keeper	5kΩ	Set high or low as design. See Notes 3 and 4.
$\overline{\text{CI}}$	Low	OUT	Transfer Attributes		Keeper		See Note 1. See Notes 3 and 4.
$\overline{\text{CKSTP\_IN}}$	Low	IN	Interrupt/Resets		Keeper		Must be actively driven. See Notes 3 and 4.
$\overline{\text{CKSTP\_OUT}}$	Low	OUT	Interrupt/Resets		Keeper		See Notes 3 and 4.
$\overline{\text{DBG}}$	Low	IN	Data Arbitration		Keeper		Active driver or tie low. See Notes 3 and 4.
DH0-31	N/A	BIDI	Data Bus		Keeper		See Notes 1, 3, and 4.
DL0-31	N/A	BIDI	Data Bus		Keeper		See Notes 1, 3, and 4.
$\overline{\text{GBL}}$	Low	BIDI	Transfer Attributes		Keeper		See Notes 1, 3, and 4.
$\overline{\text{HRESET}}$	Low	IN	Interrupt/Resets		Keeper		Active driver. See Notes 2, 3, and 4.
$\overline{\text{INT}}$	Low	IN	Interrupt/Resets		Keeper		Active driver or pull-up. See Notes 3 and 4.
L1_TSTCLK	N/A	IN	LSSD	Not enabled		5kΩ	Pull-up to OV_{DD} required.
L2_TSTCLK/$\overline{\text{DBWO}}$	Low	IN	LSSD	Not enabled		5kΩ	Pull-up to OV_{DD} required.
$\overline{\text{LSSD\_MODE}}$	Low	IN	LSSD	Not enabled		5kΩ	Pull-up to OV_{DD} required.
$\overline{\text{MCP}}$	Low	IN	Interrupt/Resets		Keeper		Active driver or pull-up. See Notes 3 and 4.
$\overline{\text{PLL\_CFG}}$ (0-3)	N/A	IN	Clock Control		Keeper	As required	Pull-up/pull-down, as required. See Notes 3 and 4.
$\overline{\text{QACK}}$	Low	IN	Status/Control		Keeper		Must be actively driven. See Notes 3 and 4.
$\overline{\text{QREQ}}$	Low	OUT	Status/Control		Keeper		Chip actively drives. See Notes 3 and 4.

Notes:

1. Depends on the system design
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for ESP and RISCWatch™ to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the PowerPC 750CXr. See Figure 6-3 on page 40.
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on the 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or equivalent) must be used. Do not rely on the keepers.

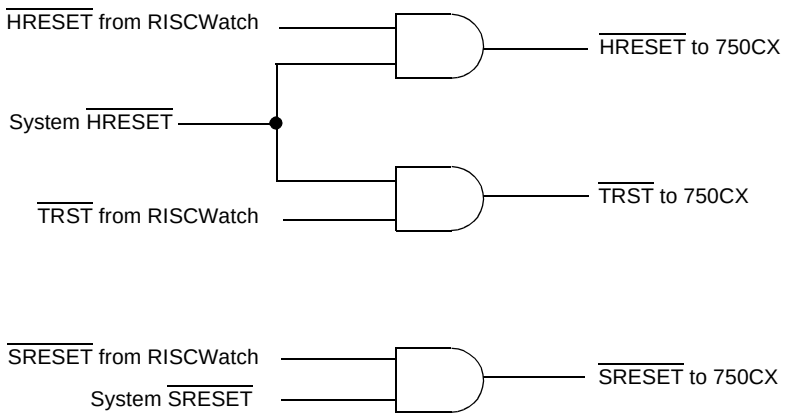
Table 6-3. Input-Output Usage (Continued)

PowerPC 750CXr Signal Name	Active Level	Input/ Output	Usage Group	I/O with Internal Resistors	Level Protect	Required External Resistor	Comments
$\overline{\text{SRESET}}$	Low	IN	Interrupt/Resets		Keeper		Active driver or pull-up. See Notes 2, 3, and 4.
SYSCLK	Low	IN	Clock Control		Keeper	No resistor by design	Active driver. See Notes 3 and 4.
$\overline{\text{TA}}$	Low	IN	Data Termination		Keeper		Active driver. See Notes 3 and 4.
$\overline{\text{TBST}}$	Low	BIDI	Transfer Attributes		Keeper	5kΩ	Pull-up to OV_{DD} required. See Notes 3 and 4.
$\overline{\text{TCK}}$	High	IN	JTAG	Not enabled		External. pulldown	
$\overline{\text{TDI}}$	High	IN	JTAG	Enabled high	Internal-Enabled		50µa @ 2.5V, 25µa@1.8V is the pull-up current for the internal resistor.
$\overline{\text{TDO}}$	High	OUT	JTAG		Keeper		See Notes 3 and 4.
$\overline{\text{TEA}}$	Low	IN	Data Termination		Keeper		Active driver or pull-up. See Notes 3 and 4.
$\overline{\text{TMS}}$	High	IN	JTAG	Enabled high	Internal-Enabled		50µa @ 2.5V, 25µa@1.8V is the pull-up current for the internal resistor.
$\overline{\text{TRST}}$	Low	IN	JTAG	Enabled high	Internal-Enabled		50µa @ 2.5V, 25µa@1.8V is the pull-up current for the internal resistor. See Note 2.
$\overline{\text{TS}}$	Low	BIDI	Address Start		Keeper	5kΩ	Pull-up to OV_{DD} required.
$\overline{\text{TSIZ0\_TSIZ2}}$	N/A	OUT	Transfer Attributes		Keeper		See Notes 1, 3, and 4.
TT0-4	N/A	IN	Transfer Attributes		Keeper		See Notes 1, 3, and 4.
$\overline{\text{WT}}$	Low	OUT	Transfer Attributes		Keeper		See Notes 1, 3, and 4.

Notes:

1. Depends on the system design
2. HRESET, SRESET, and TRST are signals used for ESP and RISCWatch™ to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the PowerPC 750CXr. See Figure 6-3 on page 40.
3. Keepers prevent floating nets from entering the forbidden zone and causing a slight amount of additional current flow in the input circuits.
4. If other components on the 60x bus call for a signal to maintain a particular level while it is not being actively driven, then an external resistor (or equivalent) must be used. Do not rely on the keepers.

Figure 6-3. IBM RISCWatch JTAG to HRESET, TRST, and SRESET Signal Connector



Note: See notes for *Table 6-3* on page 38.

6.6 Thermal Management Information

This section provides thermal management information for the PBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design and air flow.

6.6.1 Thermal Assist Unit

The thermal sensor in the Thermal Assist Unit (TAU) has not been characterized to determine the basic uncalibrated accuracy. The relationship between the actual junction temperature and the temperature indicated by THRM1 and THRM2 is not well known.

IBM recommends calibration of the TAU in these devices before use. Calibration methods are discussed in the IBM Application Note *Calibrating the Thermal Assist Unit in the IBM25PPC750L Processors*. Although this note was written for the 750L, the calibration methods discussed in this document also apply to the 750CXr.

6.6.2 Heat Sink Considerations

The PowerPC 750CXr package will support a maximum normal load of 2.2kg. This load includes the heat sink and any forces used to position or fasten the heat sink.

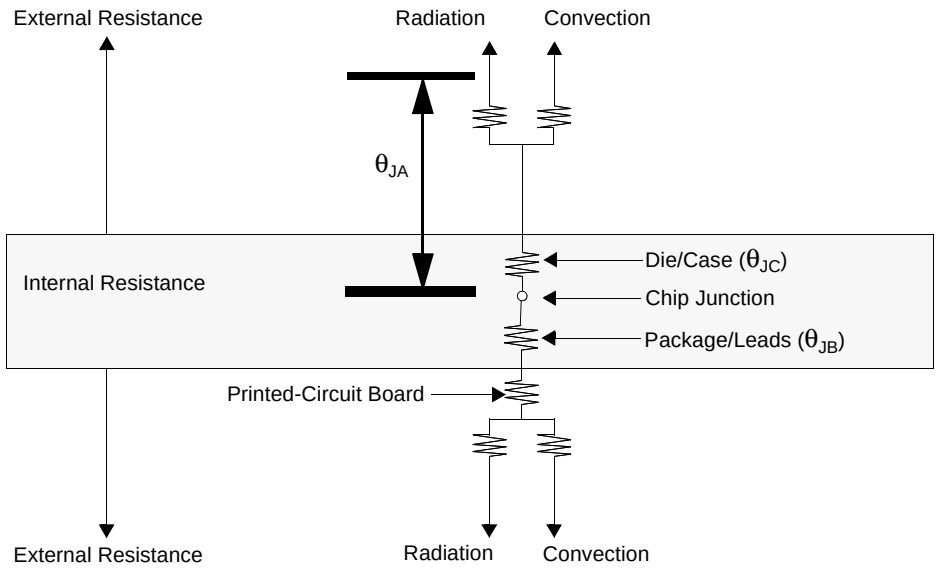
6.6.3 Internal Package Conduction Resistance

For the PBGA, described in Table 4-3 on page 16, the primary intrinsic conduction thermal resistance paths are as follows.

- Die junction-to-case thermal resistance θ_{JC}
- Die junction-to-lead thermal resistance θ_{JB}
- Die junction-to-ambient thermal resistance θ_{JA}

Figure 6-4 depicts the primary heat transfer path for this package.

Figure 6-4. PBGA Package Thermal Model



(Note the internal versus external package resistance.)

6.7 Operational and Design Considerations

6.7.1 Level Protection

A level protection feature is included in the PowerPC 750CXr. The level protection feature is available only in the 1.8V bus mode. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the I/O voltage level is closer to OV_{DD}, the circuit pulls the I/O level to OV_{DD}; if the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry “keeps” the floating inputs defined and avoids meta-stability. In Table 6-3, these signals are defined as “Keeper” in the Level Protect column.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the “keeper” node to overcome the level protection latch. This current is process dependent, but in no case is the current required over 100µA.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

6.7.2 64- or 32-Bit Data Bus Mode

Typical operation is considered to be in 64-bit Data Bus mode. Mode setting is determined by the state of the mode signal ($\overline{\text{QACK}}$) at the transition of $\overline{\text{HRESET}}$ from its active to inactive state (low to high). If $\overline{\text{QACK}}$ is *low* when $\overline{\text{HRESET}}$ transitions from active to inactive, 64-bit mode is selected. If $\overline{\text{QACK}}$ is *high* when $\overline{\text{HRESET}}$ transitions from active to inactive, 32-bit mode is selected.

6.7.3 60x Bus Operation

Selection between 1.8V and 2.5V I/O is accomplished using the BVSEL pin. If BVSEL is set low then the 1.8V mode is enabled. If BVSEL is set high, then the 2.5V mode is enabled.

6.7.4 $\overline{\text{DBWO}}$/L2_TSTCLK

One pin has two functions: $\overline{\text{DBWO}}$ and L2_TSTCLK dependent upon the $\overline{\text{LSSD\_MODE}}$ pin. When the $\overline{\text{LSSD\_MODE}}$ pin is low, the $\overline{\text{DBWO}}$/L2_TSTCLK pin is set to L2_TSTCLK function which is used during the manufacturing process for testing.

When the $\overline{\text{LSSD\_MODE}}$ pin is pulled to the high state, the $\overline{\text{DBWO}}$/L2_TSTCLK pin is set to $\overline{\text{DBWO}}$ which is identical to those descriptions given in earlier versions of the *PowerPC® 750CXr RISC Microprocessor User’s Manuals*.

6.7.5 $\overline{\text{CHKSTP\_OUT}}$/CLKOUT

$\overline{\text{CHKSTP\_OUT}}$/CLKOUT share a common pin. $\overline{\text{CHKSTP\_OUT}}$ is the normal function of this pin. The system clock or processor clock may be viewed by setting the appropriate bits in Hardware Implementation-Dependent Register 0.

Revision Log

Rev	Contents of Modification
Apr. 14, 2003	Version 0.1 Initial preliminary, advanced release.
May 23, 2003	Version 0.2 Modified the following: Changed 750CXe to 750CXR throughout document Figure 1-1 Part Number Key Table 3-1 General Parameters Table 4-5 Power Consumption (also added a note with initial guidelines for power numbers) Table 4-7 60x Bus Input Timing Specifications Figure 4-3 Input Timing Diagram Table 4-8 60x Bus Output AC Timing Specifications Figure 4-7 JTAG Clock Input Timing Diagram
July 11, 2003	Version 0.2 Modified the following: Changed CXR to CXr throughout the document Updated supported frequency range information Added information to Table 4-5 Power Consumption Changed Table 6-1 PowerPC 750CXr Microprocessor PLL Configuration
July 15, 2003	Version 0.2 Made changes based on review comments. Changed Table 6-1 PowerPC 750CXr PLL Configuration
July 17, 2003	Version 0.2 Made changes based on review comments.
July 18, 2003	Version 0.2 Made changes based on review comments.
September 11, 2003	Version 1.0 Release version.
November 24, 2003	Version 1.0 Added 500 and 533 MHz information.
January 12, 2004	Version 1.0 corrected formatting problem. No technical changes.
February 13, 2004	Version 1.1 In Section 1. General Information, changed reference to revision 4.0 of the 750CXr. In Figure 1-1. IBM Part Number Key, added “P = Plastic/Laminate ball Grid Array“ to Package Type. Changed Max voltage to 1.9 for SYSCLK input low voltage in Table 4-4 DC Electrical Specifications. Added columns for 500 and 533 MHz in Table 4-5. Power Consumption. Changed Max processor frequency to 533 MHz in Table 4-6 Clock AC Timing Specifications.
March 2, 2004	Removed Plastic/Laminate BGA in Figure 1-1 Part Number Key Added 466 MHz to Performance Sort in Figure 1-1 Part Number Key Added “< 500 MHz“ to first line of Table 4-2 Recommended Operating Conditions Revised Table 4-5. Power Consumption
February 28, 2005	Removed “Preliminary” from page headers. Updated legal page.