EPSON

E0C37109/E0C37109W

32-bit Single Chip RISC Microcomputer

Preliminary

■ DESCRIPTION

The E0C37109 and E0C37109W are Application-Specific Standard Products (ASSP) that contain Hitachi 32-bit RISC SH7709-compatible chip as the CPU. In addition to the existing peripheral functions of the SH7709, they have a built-in LCD controller compatible with SEIKO EPSON SED1354 and incorporate various interface functions as companion functions such as PCMCIA, compact flash, keyboard and mouse, and ISA bus subset.
These peripheral functions make it possible to configure an application system for portable information equipment using LCD or POS and other terminal equipment by adding only a few external circuits (e.g., memory and buffer). Furthermore, the low-power design of these devices helps to maximize the battery life of portable and mobile equipment.
With all the functions necessary for embedded systems in portable information equipment, multi-media equipment, etc. integrated on a single chip, the E0C37109 and E0C37109W are superior 32-bit, single-chip RISC microcomputers with an excellent cost-performance ratio.
Note that the E0C37109W is a version guaranteed to run under Windows CE.

■ FEATURES

[CPU functions]

- CPU: 32-bit RISC processor SH7709
  - Maximum operating frequency: 80 MHz
  - 32-bit internal data bus
  - 32-bit general-purpose register × 16
  - RISC instruction set
  - Instruction execution rate: One instruction per cycle (for basic instructions)
  - 4G-byte logical address space
  - 372M-byte physical memory space
  - Space identification ASID
  - Built-in multiplier
  - Five-stage pipelining
- Memory management unit (MMU)
  - 4G-byte address space, 256 address space (ASID 8 bits)
  - Paging method
  - Supports multiple page sizes: 1K or 4K bytes
  - 128-entry, 4-way set associative TLB
  - Supports specification of replacement ways by software and random replacement algorithm
  - Can directly access TLB contents by address mapping
- Cache memory
  - Instructions and data coexist 8K-byte cache
  - 128-entry, 4-way set-associative (8K-byte cache), 16 bytes/line
  - Write-back/write-through selectable LRU replacement algorithm
  - One-stage write-back buffer
  - Dividable cache (4K-byte/2-way cache memory + 4K-byte memory)
- Interrupt controller
  - Six external interrupt pins (NMI, IRQ5–IRQ1)
  - Internal interrupts: Interrupt priorities set for each module
- User break control
  - Break channel × 2
  - Allows address, data value, access type, and data size to be set as break conditions
  - Supports successive break
- Bus state controller
  - Physical address space divided into six areas of up to 64M bytes, with the following functions selectable for each
    - – Bus size (8, 16, or 32 bits)
    - – Number of wait cycles
    - – SRAM, DRAM, synchronous DRAM, and burst ROM mapping into directly accessible area
    - – Supports PCMCIA interface
    - – Chip-select signal output for each area
  - DRAM and synchronous DRAM refresh function
    - – Programmable refresh intervals
    - – Supports CAS-before-RAS refresh and self-refresh
    - – Supports power-down DRAM
  - DRAM and synchronous DRAM burst-access function
  - Little endian

- Timer
  - Auto reload-type 32-bit timer × 3 channels
  - Input capture function
  - Six selectable types of counter input clock
  - Maximum resolution: 2 MHz
- Real-time clock
  - Built-in clock, calendar function, and alarm function
  - Built-in 32-kHz crystal oscillator circuit, maximum resolution (interrupt cycle) = 1/256 seconds
- Serial communication interface (SCI0–SCI2)
  - Selectable asynchronous and clock-synchronized modes (SCI0)
  - Full-duplex transmission/reception (SCI0)
  - Supports smart-card interface (SCI0)
  - Transmit/receive 16-byte FIFO (SCI1-SCI2)
  - DMA transfer possible (SCI1–SCI2)
  - IrDA: 1.0-based interface (SCI1)
  - Hardware flow control (SCI2)
- DMA controller
  - Four channels
  - Cycle steal mode/burst mode
- I/O port
  - 16 bits (16 bits on external bus)
- A/D converter
  - 10-bit±4 LSB, 8 channels
  - Conversion time: 10 µs
  - Input range: 0 to AVCC (maximum 3.6V)
- D/A converter
  - 8-bit±4 LSB, 2 channels
  - Conversion time: Maximum 10 µs
  - Input range: 0 to AVCC (maximum 3.6V)
- Power management function
  - Low-power design tailored to minimize reduction in performance
  - Sleep mode, standby mode, module standby mode

[LCD controller functions]

Incorporates SEIKO EPSON SED1354

- Memory interface
  - 16-bit EDO-DRAM or FPM-DRAM
  - 512K bytes (256K × 16 bit DRAM, 1 pc.)
  - 2M bytes (1M × 16 bit DRAM, 1 pc.)
- Usable display
  - 4/8-bit monochrome STN LCD panel
  - 4/8/16-bit color STN LCD panel
  - 9/12-bit TFT panel
  - 18/24-bit TFT panel (maximum 65,536 colors)
- Display mode
  - 1/2/4/8/16-bit/pixel support
  - Monochrome STN panel: Maximum 16 gray levels
  - Color STN panel: Maximum 4,096 colors
  - TFT panel: Maximum 65,536 colors
  - Capable of displaying two different images on the same screen
- Clock source
  - Maximum 40 MHz input clock frequency
  - Memory clock = 1/1 or 1/2 input clock
  - Pixel clock = 1/1, 1/2, or 1/4 memory clock
- Power-down mode
  - Supports two power-down modes
  - Hardware suspend, software suspend

[Companion functions]

- PCMCIA interface (1 slot)
  - 5-V interface possible

  ∗ To support hot insertion/removal, SEIKO EPSON recommends using the separately available E0C37120, an address/data buffer IC.
- Compact flash interface
- Serial interface (16550 equivalent × 2 channels)
- Baud rate generator
- Timer (8254 equivalent)
- Interrupt controller
- PS/2 keyboard interface
- PS/2 mouse interface
- Parallel interface
  - Extended parallel support: EPP mode
- ISA bus subset interface
  - 8/16-bit memory device
  - 8/16-bit I/O device
- Programmable chip select (4 bits)
- Real-time clock (backup possible)
- Power-down mode

[Windows CE function]

- The E0C37109W supports Windows CE

■ PHYSICAL SPECIFICATIONS

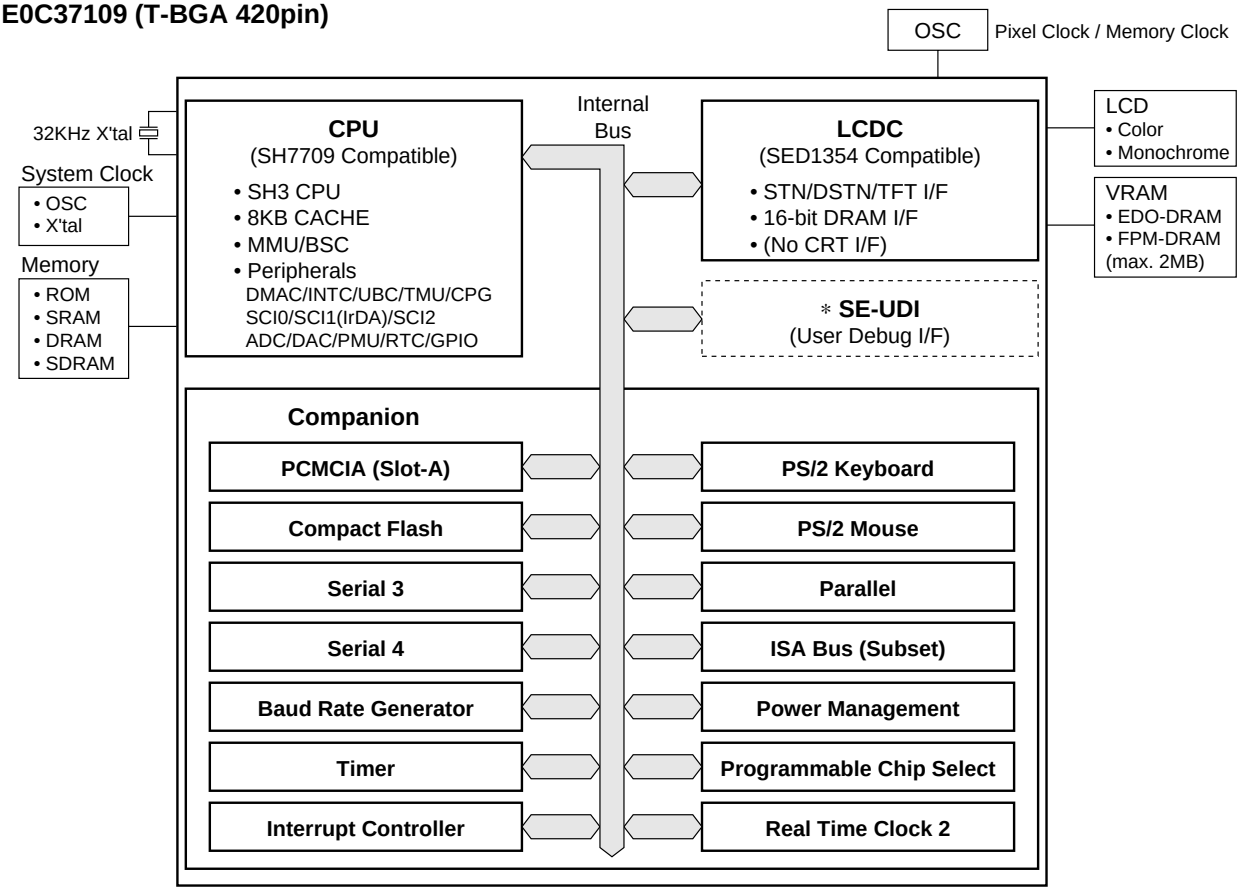
- Power supply voltage ..... 3.3V±0.3V (5V interface possible for PCMCIA function)
- Operating frequency ..... CPU: maximum 80 MHz; Internal peripheral/external bus clock: maximum 40 MHz
- Number of pins ..... 420 (number of pins used: 376)
- Package ..... T-BGA 420pin (outside dimensions 35(W) × 35(H) × 1.7(D) mm, 1.27-mm pitch)
- Process ..... 0.35-µm CMOS/3-layer metallization

■ MEMORY MAP

Physical address		Memory type
00000000h	Area 0	SRAM/ROM (8/16/32 bits) Burst ROM (8/16/32 bits)
04000000h	Area 1	Internal I/O Cannot be used
08000000h	Area 2	SDRAM (32 bits) DRAM (16 bits) SRAM/ROM (8/16/32 bits)
0C000000h	Area 3	SDRAM (32 bits) DRAM (16 bits) SRAM/ROM (8/16/32 bits)
10000000h	Area 4	Companion function (16 bits)
14000000h	Area 5	LCD controller (16 bits)
18000000h	Area 6	PCMCIA/ISA (16 bits)
1C000000h	Area 7	Cannot be used Reserved area

■ BLOCK DIAGRAM

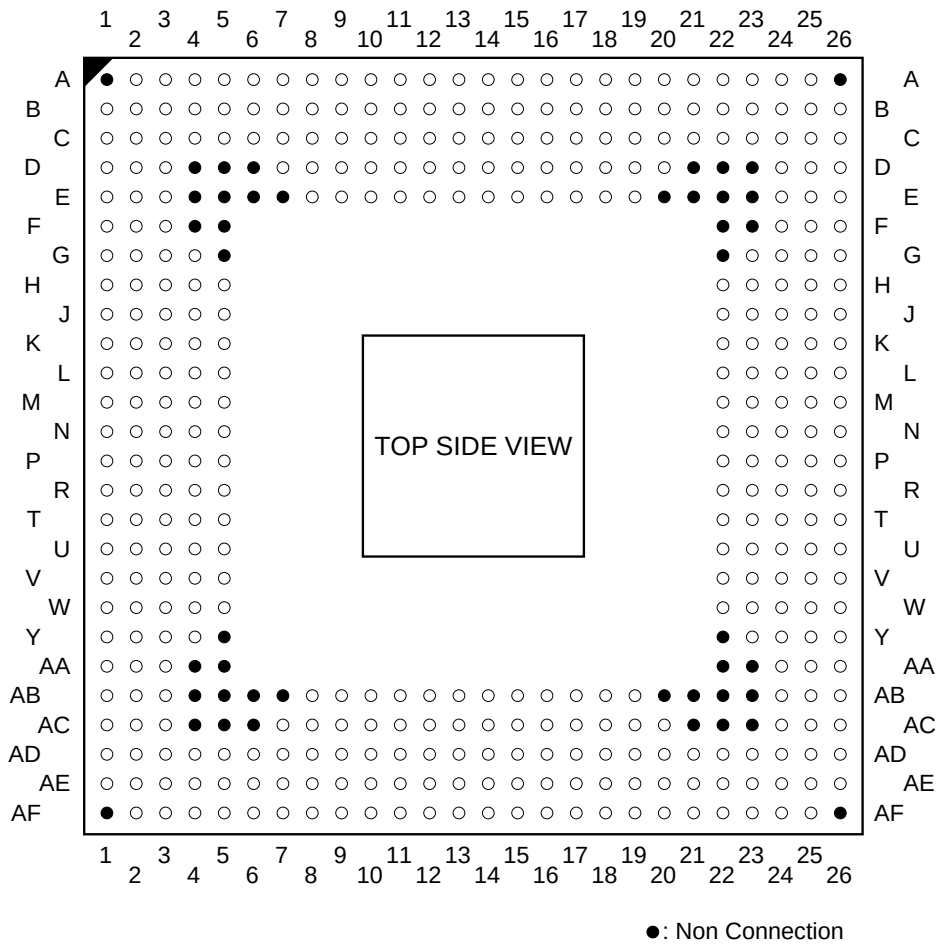
E0C37109 (T-BGA 420pin)



∗ SE-UDI: To be added in the future ... JTAG-compliant user debugging interface

■ PIN DESCRIPTION

● Pin Assignment



● Pin Functions

Notes: • Symbols representing the types of pins mean the following:

I : Input port
O : Output port
I/O : Bi-directional port
P : Power port
PU : with pull-up resistance
PD : with pull-down resistance
BH : with bus hold circuit
OD : with open drain (5V tolerant)

• The pin names with the suffix # are those of active-low pins.

[CPU functions]

Function	Pin name	Description	Type	No. of pins	Power
Data bus	D[15:0]	Data bus D[15:0]	I/O PU	16	Vcc
	D[23:16]/PTA[7:0]	Data bus D[23:16]; I/O port A[7:0]	I/O PU	8	Vcc
	D[31:24]/PTB[7:0]	Data bus D[31:24]; I/O port B[7:0]	I/O PU	8	Vcc
Address bus	A[21:0]	Address bus A[21:0]	O BH	22	Vcc
	A[25:22]/CA[25:22]	Address bus A[25:22]; PC card address [25:22]	O	4	Vcc
Bus control	CS0#	Chip select 0	O	1	Vcc
	CS2#	Chip select 2	O	1	Vcc
	CS3#	Chip select 3	O	1	Vcc
	CS4#	Chip select 4	O	1	Vcc
	CS5#	Chip select 5	O	1	Vcc
	CE1B#	CE1(area 6 PCMCIA)	O	1	Vcc
	BS#	Bus cycle start signal	O	1	Vcc
	RAS3U#/PTE[2]	RAS (area 3 DRAM, area 2, 3 SDRAM upper 32MB); I/O port E[2]	I/O PU	1	Vcc
	RAS3L#/PTJ[0]	RAS (area 3 DRAM, area 2, 3 SDRAM lower 32MB); I/O port J[0]	I/O PU	1	Vcc
	RAS2U#/PTE[1]	RAS (area 2 DRAM upper 32MB); I/O port E[1]	I/O PU	1	Vcc
	RAS2L#/PTJ[1]	RAS (area 2 DRAM lower 32MB); I/O port J[1]	I/O PU	1	Vcc
	CASLL#/CAS#/PTJ[2]	CAS (DRAM) for D[7:0]; CAS (SDRAM); I/O port J[2]	I/O PU	1	Vcc
	CASLH#/PTJ[3]	CAS (DRAM) for D[15:8]; I/O port J[3]	I/O PU	1	Vcc
	CASHL#/PTJ[4]	CAS (DRAM) for D[23:16]; I/O port J[4]	I/O PU	1	Vcc
	CASHH#/PTJ[5]	CAS (DRAM) for D[31:24]; I/O port J[5]	I/O PU	1	Vcc
	CAS2L#/PTE[6]	CAS(area 2 DRAM) for D[7:0]; I/O port E[6]	I/O PU	1	Vcc
	CAS2H#/PTE[3]	CAS(area 2 DRAM) for D[15:8]; I/O port E[3]	I/O PU	1	Vcc
	WE0#/DQMLL	D[7:0] select signal; DQM (SDRAM)	O	1	Vcc
	WE1#/DQMLU	D[15:8] select signal; DQM (SDRAM)	O	1	Vcc
	WE2#/DQMUL	D[23:16] select signal; DQM (SDRAM)	O	1	Vcc
	WE3#/DQMUU	D[31:24] select signal; DQM (SDRAM)	O	1	Vcc
	RD/WR#	Read/write select signal	O	1	Vcc
	RD#	Read strobe	O	1	Vcc
	CKE	CK enable (for SDRAM only)	O	1	Vcc
	WAIT#	Hardware wait request	I/O	1	Vcc
Interrupt	IRQ[3:1]/PTH[3:1]	External interrupt request; I/O port H[3:1]	I PU	3	Vcc
	IRQ4/PTH[4]	External interrupt request; I/O port H[4]	I PU	1	Vcc
	NMI	Nonmaskable interrupt request	I	1	Vcc
	IRQOUT#	Interrupt request output	O	1	Vcc
	WAKEUP#/PTD[3]	Interrupt request output during standby mode; I/O port D[3]	I/O PU	1	Vcc
Timer	TCLK/PTH[7]	Clock input/output for TMU/RTC; I/O port H[7]	I/O PU	1	Vcc
DMAC	DREQ0#/PTD[4]	DMA request 0; I/O port D[4]	I PU	1	Vcc
	DACK0/PTD[5]	DMA acknowledge 0; I/O port D[5]	I/O PU	1	Vcc
	DREQ1#/PTD[6]	DMA request 1; I/O port D[6]	I PU	1	Vcc
	DACK1/PTD[7]	DMA acknowledge 1; I/O port D[7]	I/O PU	1	Vcc
	DRAK0/PTD[1]	DMA request acknowledge 0; I/O port D[1]	I/O PU	1	Vcc
	DRAK1/PTD[0]	DMA request acknowledge 1; I/O port D[0]	I/O PU	1	Vcc
Smart-card I/F without SCI/FIFO	RXD0/SCPT[0]	Receive data 0; SCI input port [0]	I PU	1	Vcc
	TXD0/SCPT[0]	Transfer data 0; SCI output port [0]	O	1	Vcc
	SCK0/SCPT[1]	Serial clock 0; SCI I/O port [1]	I/O PU	1	Vcc
IrDA with SCIF/FIFO	RXD1/SCPT[2]	Receive data 1; SCI input port [2]	I PU	1	Vcc
	TXD1/SCPT[2]	Transfer data 1; SCI output port [2]	O	1	Vcc
	SCK1/SCPT[3]	Serial clock 1; SCI I/O port [3]	I/O PU	1	Vcc
SCIF with FIFO	RXD2/SCPT[4]	Receive data 2; SCI input port [4]	I PU	1	Vcc
	TXD2/SCPT[4]	Transfer data 2; SCI output port [4]	O	1	Vcc
	SCK2/SCPT[5]	Serial clock 2; SCI I/O port [5]	I/O PU	1	Vcc
	RTS2/SCPT[6]	Request to send 2; SCI I/Oport [6]	I/O PU	1	Vcc
	CTS2/IRQ5/SCPT[7]	Clear to send 2; External interrupt request; SCI input port [7]	I PU	1	Vcc
PCMCIA control	CE2B#	Chip enable 2 for PC card 0	O	1	Vcc
	PTE[4]	I/O port E[4]	I/O PU	1	Vcc
Clock	CAP[1:2]	External capacitance pin for PLL [1:2]	–	2	Vcc
	EXTAL	External clock/crystal oscillator pin	I	1	Vcc
	XTAL	Crystal oscillator pin	O	1	Vcc
	EXCKIO	System clock output	O	1	Vcc
	EXTAL2	Crystal oscillator pin for RTC	I	1	Vbak
	XTAL2	Crystal oscillator pin for RTC	O	1	Vbak
System clock	RESETP#	Power-on reset request	I	1	Vcc
	RESETM#	Manual reset request	I	1	Vcc
	BREQ#	Bus request	I	1	Vcc
	BACK#	Bus acknowledge	O	1	Vcc

Function	Pin name	Description	Type	No. of pins	Power
System clock	SHMD[2:0]	CPU clock-mode setting	I	3	Vcc
	SHMD[4:3]	Area 0 bus-width setting	I	2	Vcc
	SHMD5	Endian setting (fixed to little endian)	I	1	Vcc
	CA#	Chip active	I	1	Vcc
	STATUS[1:0]	Processor status [1:0]	O	2	Vcc
Analog	AN[5:0]/PTL[5:0]	ADC input [5:0]; Input port L[5:0]	I	6	AVcc
	AN[6:7]/DA[1:0]/PTL[6:7]	ADC input [6:7]; DAC output [1:0]; Input port L[6:7]	I/O	2	AVcc
Port	PTC[7:0]/PINT[7:0]	I/O port C[7:0]; Port interrupt [7:0]	I/O PU	8	Vcc
	PTD[2]/RESETOUT#	I/O port D[2]; Reset output	I/O PU	1	Vcc
	PTE[0]	I/O port E[0]	I/O PU	1	Vcc
	PTF[7:0]/PINT[15:8]	I/O port F[7:0]; Port interrupt [15:8]	I PU	8	Vcc
	PTG[6:0]	I/O port G[6:0]	I PU	7	Vcc
	PTH[5]/ADTRG#	I/O port H[5]; Analog trigger	I PU	1	Vcc
	PTH[6]	I/O port H[6]	I PU	1	Vcc

[LCD controller functions]

Function	Pin name	Description	Type	No. of pins	Power
Image memory control (DRAM)	LCAS#	Image memory control (LCAS#/CAS#)	O	1	Vcc
	UCAS#	Image memory control (UCAS#/UWE#)	O	1	Vcc
	WE#	Image memory control (WE#/LWE#)	O	1	Vcc
	RAS#	Image memory control (RAS#)	O	1	Vcc
	MD[15:0]	Image memory data bus	I/O PD	16	Vcc
	MA[11:0]	Image memory address bus	O	12	Vcc
LCD panel control	FPDAT[8:0]	Panel display data	O	9	Vcc
	FPDAT[15:9]	16-bit panel display data (7 high-order bits)	O	7	Vcc
	FPFRAME	Frame pulse	O	1	Vcc
	FPLINE	Line pulse	O	1	Vcc
	FPSHIFT	Shift clock pulse	O	1	Vcc
	FPLCDPWR	LCD power supply control	O	1	Vcc
	FPDRDY	Panel control (DRDY/FPSHIFT2/MOD)	O	1	Vcc
	VCLK	Clock input (pixel clock/memory clock)	I	1	Vcc

[Companion functions]

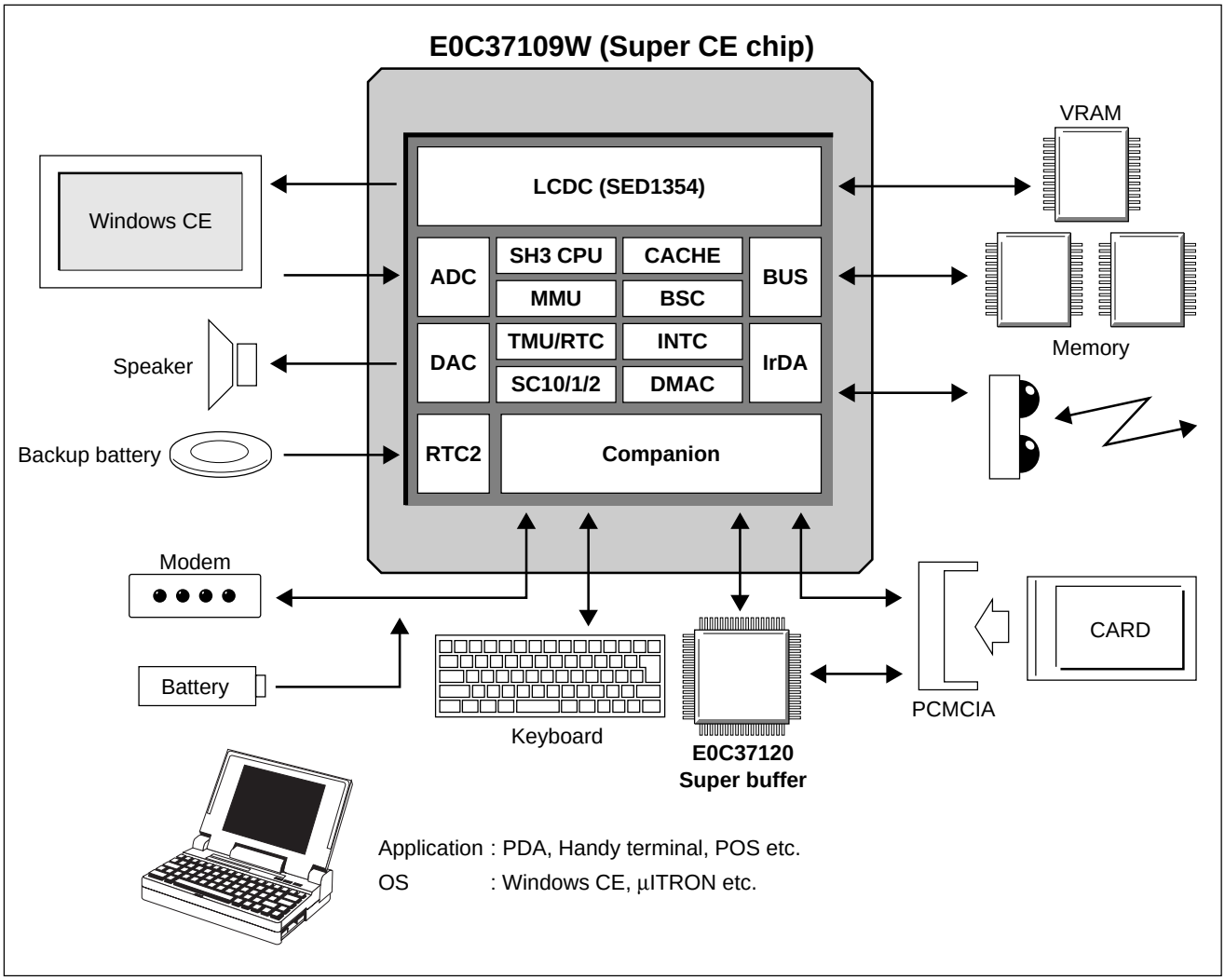
Function	Pin name	Description	Type	No. of pins	Power
PCMCIA I/F	ACE1#	Card select 1	O	1	SlotAVcc
	ACE2#	Card select 2	O	1	SlotAVcc
	AOE#	Memory-card read strobe	O	1	SlotAVcc
	AWE#	Memory-card write strobe	O	1	SlotAVcc
	AIORD#	I/O-card read strobe	O	1	SlotAVcc
	AIOWR#	I/O-card write strobe	O	1	SlotAVcc
	AREG#	Attribute memory/common memory select	O	1	SlotAVcc
	ARDY_IREQ#	Ready/interrupt request	I PU	1	SlotAVcc
	AWAIT#	Card wait request	I PU	1	SlotAVcc
	ACD1#	Card detection 1	I PU	1	Vcc
	ACD2#	Card detection 2	I PU	1	Vcc
	AWP_IOIS16#	Write protect/16-bit access detection	I PU	1	SlotAVcc
	ARESET	Card reset	O	1	SlotAVcc
	ABVD1_STSCHG#	Battery voltage detection/card status change	I PU	1	SlotAVcc
	ABVD2_SPKR	Battery voltage detection/digital sound	I PU	1	SlotAVcc
	AVS1	Supply voltage detection 1	I PU	1	Vcc
	AVS2	Supply voltage detection 2	I PU	1	Vcc
	AVPPPGM	Program power supply control	O	1	Vcc
	AVPPVCC	Program power supply control	O	1	Vcc
	AVCC5#	5V power supply control	O	1	Vcc
	AVCC3#	3.3V power supply control	O	1	Vcc
	AADRENA#	Card address enable	O	1	Vcc
	ADATAENA#	Card data enable	O	1	Vcc
Compact flash I/F	COE#	Memory-card read strobe	O	1	Vcc
	CWE#	Memory-card write strobe	O	1	Vcc
	CREG#	Attribute memory/common memory select	O	1	Vcc
	CCE1#	Card select 1	O	1	Vcc
	CCE2#	Card select 2	O	1	Vcc
	CIORD#	I/O-card read strobe	O	1	Vcc
	CIOWR#	I/O-card write strobe	O	1	Vcc
	CRDY_IREQ#	Ready/interrupt request	I PU	1	Vcc

Function	Pin name	Description	Type	No. of pins	Power
Compact flash I/F	CWAIT#	Card wait request	I PU	1	Vcc
	CWP_IOIS16#	Write protect/16-bit access detection	I PU	1	Vcc
	CRESET	Card resetv	O	1	Vcc
	CBVD1_STSCHG#	Battery voltage detection/card status change	I PU	1	Vcc
Keyboard I/F	KBCLK	Keyboard clock	I/O OD	1	Vcc
	KBDATA	Keyboard data	I/O OD	1	Vcc
Mouse I/F	MSCLK	Mouse clock	I/O OD	1	Vcc
	MSDATA	Mouse data	I/O OD	1	Vcc
Parallel I/F	STROBE#	Strobe	I/O OD	1	Vcc
	AFD#	Auto feed	I/O OD	1	Vcc
	INIT#	Initialize	I/O OD	1	Vcc
	SLCTIN#	Select in	I/O OD	1	Vcc
	SLCT	Select	I	1	Vcc
	PE	Paper end	I	1	Vcc
	ERROR#	Error	I	1	Vcc
	ACK#	Acknowledge	I	1	Vcc
	BUSY	Busy	I	1	Vcc
	LPTD[7:0]	Data bus [7:0]	I/O OD	8	Vcc
Serial I/F (SCI3)	DCD3#	Data carrier detection 3	I PU	1	Vcc
	DTR3#	Data terminal ready 3	O	1	Vcc
	DSR3#	Data set ready 3	I PU	1	Vcc
	RTS3#	Request to send 3	O	1	Vcc
	CTS3#	Clear to send 3	I PU	1	Vcc
	RI3#	Incoming call indication 3	I PU	1	Vcc
	TXD3	Serial-transmit data 3	O	1	Vcc
	RXD3	Serial-receive data 3	I PU	1	Vcc
Serial I/F (SCI4)	DCD4#	Data carrier detection 4	I PU	1	Vcc
	DTR4#	Data terminal ready 4	O	1	Vcc
	DSR4#	Data set ready 4	I PU	1	Vcc
	RTS4#	Request to send 4	O	1	Vcc
	CTS4#	Clear to send 4	I PU	1	Vcc
	RI4#	Incoming call indication 4	I PU	1	Vcc
	TXD4	Serial-transmit data 4	O	1	Vcc
	RXD4	Serial-receive data 4	I PU	1	Vcc
ISA bus I/F (subset)	SBHE#	System byte high enable	O	1	Vcc
	MEMR#	Memory read	O	1	Vcc
	MEMW#	Memory write	O	1	Vcc
	IOR#	I/O read	O	1	Vcc
	IOW#	I/O write	O	1	Vcc
	IOCHRDY	I/O channel ready	I OD	1	Vcc
	IOCS16#	I/O chip select 16	I OD	1	Vcc
	MEMCS16#	Memory chip select 16	I OD	1	Vcc
	ISAENA#	ISA-device data enable	O	1	Vcc
	RSTDRV	ISA-device reset request	O	1	Vcc
ROM I/F	CSROM0#	External ROM chip select (area 0)	O	1	Vcc
	ROMDIS#	CSROM0 disable	I	1	Vcc
Misc.	STANDBY#	CPU standby status	O	1	Vcc
	PCS0#	Programmable chip select 0	O	1	Vcc
	PCS1#	Programmable chip select 1	O	1	Vcc
	PCS2#	Programmable chip select 2	O	1	Vcc
	PCS3#	Programmable chip select 3	O	1	Vcc
	RTC2DIS#	RTC2 disable	I	1	Vbak
	RTC2PS	RTC2 power status	I	1	Vbak

[Other]

Function	Pin name	Description	Type	No. of pins	Power
Test-only pins	TEST0	Test-mode input pin (Use prohibited: Connect to GND)	I PD	1	AVcc
	TEST1	Test-mode input pin (Use prohibited: Connect to GND)	I PD	1	AVcc
	TEST2	Test-mode input pin (Use prohibited: Connect to GND)	I	1	Vbak
Vcc	Vcc	Power supply (3.3V)	P	24	–
	Vcc(PLL)	Power supply (3.3V)	P	2	–
	SlotAVcc	PCMCIA power supply (3.3V/5V/Hi-Z)	P	2	–
	Vbak(RTC2)	RTC2 backup power supply (2.0V to 3.6V/3.3V)	P	1	–
	AVcc	Analog (ADC/DAC) power supply (3.3V)	P	1	–
GND	Vss	Power supply (0V)	P	24	–
	Vss(PLL)	Power supply (0V)	P	2	–
	Vss(RTC2)	Power supply (0V)	P	1	–
	AVss	Analog power supply (0V)	P	2	–

■ EXAMPLE OF APPLICATION



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Issue MAY 1999, Printed in Japan Ⓜ