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8 0-8-1110KMI 2 1

LEGEND

NUMBER	DESCRIPTION
KDFII-BA	M8189-00 PLUS KTFII-AA & BOOT/DIAG. ROMS
KDFII-BB	M8189-00 PLUS KTFII-AA, KEFII-AA & BOOT/DIAG. ROMS
KDFII-BC	M8189-00 PLUS BOOT/DIAG. ROMS
KDFII-BD	M8189-00 PLUS KTFII-AA, KEFII-BB & BOOT/DIAG. ROMS

- NOTES:
1. WHEN INSTALLING ITEMS 2,3,8&9 MAKE SURE THAT PIN 1 IS LOCATED AS SHOWN.
  2. WHEN ITEMS 8 & 9 ARE MASKED ROMS CONNECT J23 TO J24 WITH J22 NOT CONNECTED. WHEN ITEMS 8 & 9 ARE EPROMS CONNECT J22 TO J23 WITH J24 NOT CONNECTED.
  3. BAUD RATE SELECTION. SEE D-CS-M8189-0-K11. SETTINGS SHOWN PRODUCE 9600 BAUD EACH LINE.
  4. KEFII-BB=CIS MICROCODE HYBRID. CONTAINS CIS MICROCODE TO IMPLEMENT THE COMMERCIAL INSTRUCTION SET.

TABLE 1. BOOT/DIAG. SELECTION GUIDE FOR SWITCH PACK E102

SWITCH	ON	OFF
S1	EXECUTE CPU TEST	SKIP CPU TEST
S2	EXECUTE MEMORY TEST	SKIP MEMORY TEST
S3	EXECUTE DECNET BOOT PROGRAM SELECTED BY S4-S7 PER TABLE 2.	EXECUTE STANDARD BOOT PROGRAM PER SWITCH S4
S4	EXECUTE DIALOGUE ROOT PROGRAM. OPERATOR RESPONDS WITH MNEMONIC PER TABLE 3.	EXECUTE AUTOMATIC (TURNKEY) BOOT PROGRAM SELECTED BY S5-S8 PER TABLE 3.

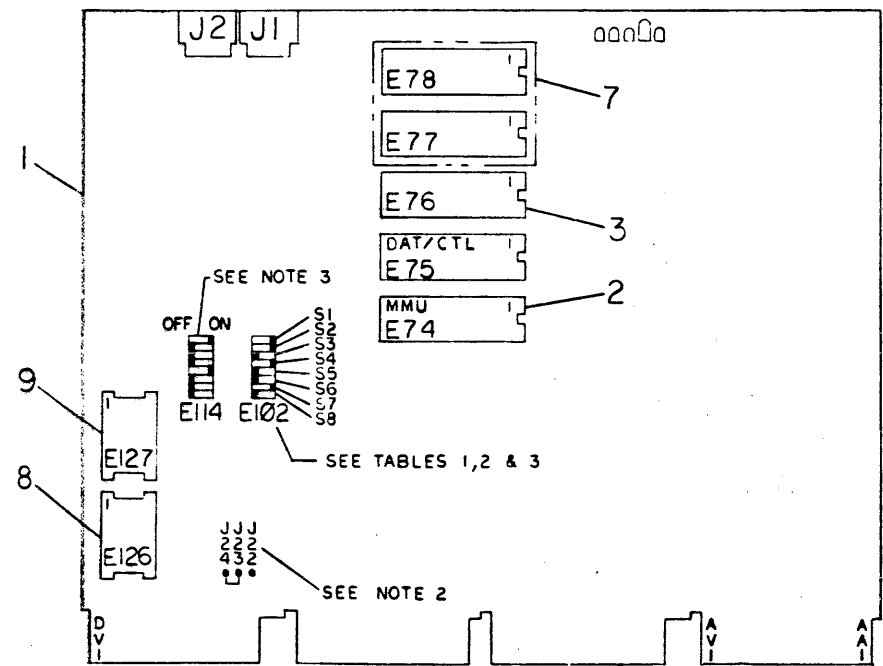
TABLE 2. DECNET BOOT DEVICE SELECTION (S3 ON)

S4	S5	S6	S7	DEVICE
ON	X	X	X	DUVII
OFF	ON	X	OFF	DLVII-E
OFF	ON	X	ON	DLVII-F

NOTE: X = DON'T CARE

TABLE 3. STANDARD BOOT DEVICE SELECTION (S3 OFF)

MNEMONIC	S5	S6	S7	S8	DEVICE
DKn; n<8	OFF	OFF	OFF	ON	RK05
DLn; n<4	OFF	OFF	ON	OFF	RLO1/RLO2
DDn; n<2	OFF	OFF	ON	ON	TU58
DXn; n<2	OFF	ON	OFF	OFF	RX01
DYn; n<2	OFF	ON	ON	OFF	RX02



CAUTION: OFF SHEET PARTS LIST EXISTS, SEE K-PL-KDFII-B-DBP

REVISIONS

REV.	INITIAL	DATE
1	A	12-APR-82
2	B	12-APR-82
3	C	5-13-82

CHEK: C. VALENTINE

DESCRIPTION	DWG PART NO	ITEM NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES		
ANGLES	CLASS OF ACCURACY	NOMINAL DIMENSION RANGE INCHES
10° 30'	CHECK ONE:	0.000 - 0.009
SURFACE QUALITY	MEDIUM	0.012 - 0.018
QUALITY IN	PREFERRED	0.024 - 0.04
QUANTITY & VARIATION	MICRONCHES	0.012 - 0.018 - 0.025 - 0.04 - 0.063 - 0.1
THIRD ANGLE PROJECTION	DRN: H. Cullison	FIRST USED ON: 11/23-8 digital
REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D: [Signature]	TITLE: KDFII-B CPU UNIT ASSEMBLY
DO NOT SCALE DWG	PROJ ENG: [Signature]	SIZE CODE: D
MATERIAL: B 00 KDFII B	PROD: [Signature]	NUMBER: 2
FINISH: [Signature]	SCALE: NONE	REV: 6
	SHEET: 1 OF 1	DIST: [Signature]

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QUANTITY PER VARIATION		
					BA	BB	BC
1	1		M8189-00	KDF11-B QUAD HT CPU,0 AND 0-22 B	1	1	1
2	2		2115542-01	DC 304 F11 MMU,FLOAT PT REG	1	1	-
3	3		5700001-00	HYBRID ASSY FLOATING POINT	-	1	-
4	4		23244E2-00	E2-04	1	1	1
5	5		23245E2-00	E2-04	1	1	1
6	6		H3270-00	TEST CONNECTOR	1	1	1

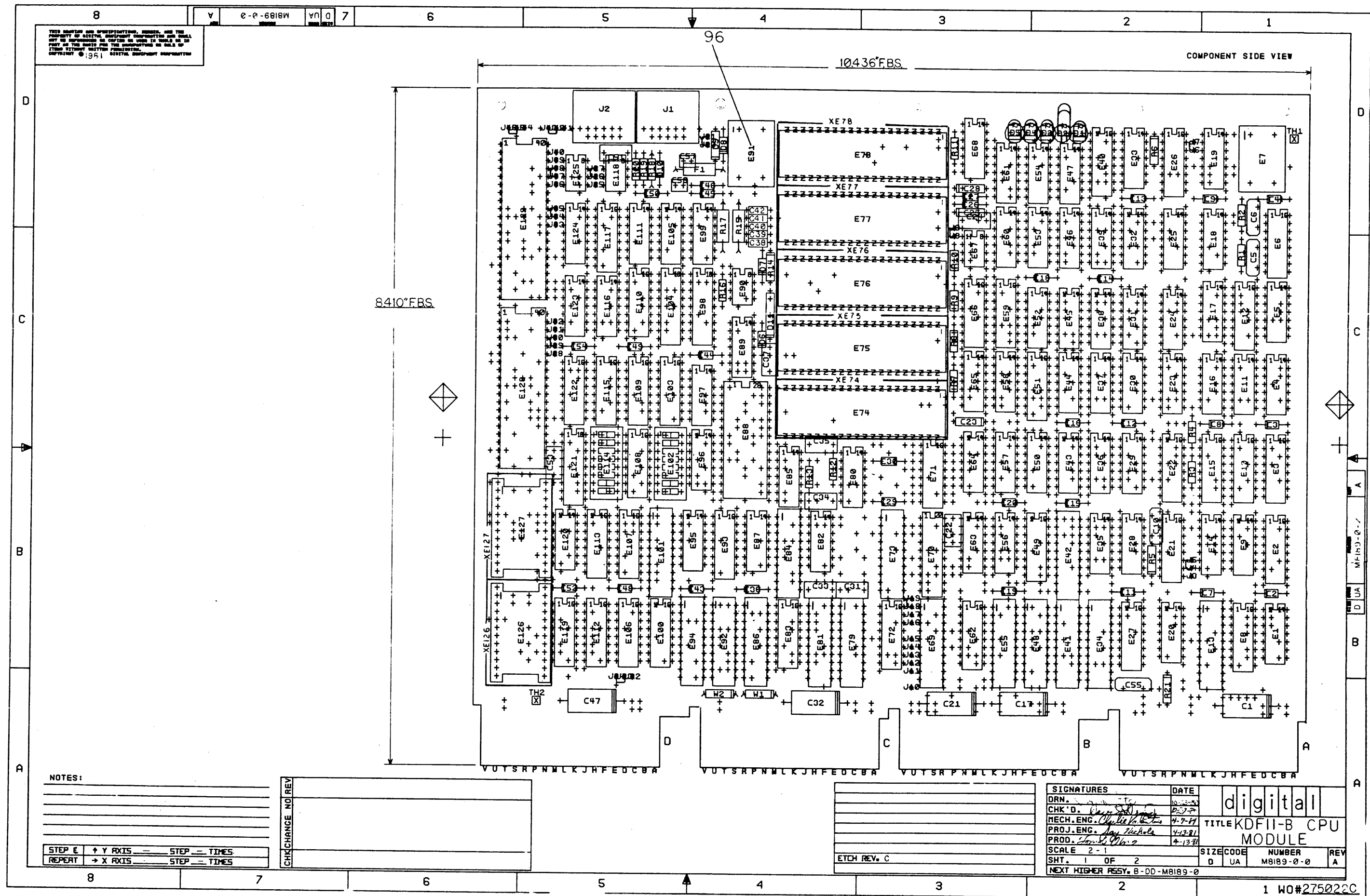
7 NOTE: ITEM #6, THE WRAP-AROUND-TEST JUMPER FOR CONNECTOR J2, IS NOT SHOWN ON UA DWG.  
 8 NOTE: FOR BULK INTERPLANT SHIPMENT OF MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700053-0-0  
 9 NOTE: FOR SHIPMENT OF INDIVIDUAL MODULES REFER TO PACKAGING INSTRUCTION A-SP-3700069-0-0

REVISION HISTORY		BASIC PART NO: KDF11		DRN: P. GROSNIHAN		DATE: 21-JAN-81		D I G I T A L	
ENG	ECO NUMBER	REV	SECTION A OF A	CHK'D:	G. MARINI	DATE:	27-MAY-81	TITLE	PARTS LIST
	INITIAL	A	SECTION. VARIATION INDEX:					KDF11-B CPU UNIT ASSEMBLY	
			(A) BA, BB, BC						
			(B)	DES.ENG.:	C. VALENTINE	DATE:	21-JAN-81		
			(C)	RESP.ENG.:	C. VALENTINE	DATE:	21-JAN-81		DOCUMENT NUMBER
			(D)					SIZE:CODE:	NUMBER
			(E)	MFG.ENG.:	T. OLMO	DATE:	27-APR-81	K	PL
			(F)	ASSEMBLY NUMBER:	C-UA-KDF11-B-0	TOP DOCUMENT NUMBER:	#B-DD-KDF11-B	FILE NAME:	EDIT #
								22423A.PLS	4

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NOTES:

STEP E	↑ Y AXIS	— STEP	— TIMES
REPEAT	→ X AXIS	— STEP	— TIMES

CHK	CHANGE	NO	REV

ETCH REV. C

SIGNATURES		DATE
DRN.		
CHK'D.		
MECH. ENG.		
PROJ. ENG.		
PROD.		
SCALE 2-1		SIZE CODE
SHT. 1 OF 2		NUMBER
NEXT HIGHER REV. B-DD-M8189-0		REV

digital  
 TITLE KDFII-B CPU  
 MODULE



LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY	PER VARIATION	REFERENCE DESIGNATOR
					00		
1	1	D-MD-5014313-0-0	5014313-00	DRILL AND ETCH BD.	1		
2	2		1000022-00	270.0 MMF 100V 5%200PPM MICA	1		C10
3	3		1000024-00	470.0 MMF 100V 5%200PPM MICA	3		C5,C6,C53
4	4		1001610-00	.01 MFD 50V +80-20% 25U CER	3		C26,C27,C30
5	5		1012784-00	.047 MFD 50V +80-20% CER	29		C2-C4,C7-C9,C11-C16,C18-C20,C23, CONT C25,C28,C29,C36,C43-C46,C48-C50, CONT C52,C54
6	6		1016681-00	.47 MFD 50V +80-20% CER	14		C22,C24,C31,C33-C35,C37-C42,C51, CONT C53
7	7		1017472-00	10 MFD 35V +50-10% AL EL	5		C1,C17,C21,C32,C47
8	8		1011740-02	1800.0 MMF 50V 10% CER	2		C56,C57
9	9		1109977-00	1N 749A VZ= 4.3 5%	1		D9
10	10		1112689-00	LED .8MCD@16MA VF=5V	4		D1,D3-D5
11	11		1114384-00	LED 105MW 35MA GREEN	1		D2
12	12		1100114-00	D 664 QS\75PCB PIV= 25V SP	3		D6-D8
13	13		1110967-00	1N 4005 PIV=600 I= 1A D041 SI	1		D10
14	14		1105508-00	1N 823 VZ= 6.2 5% .40W Y	1		D11
15	15		1213506-04	HEADER 10POS RT ANGLE W/3 SI	2		J1,J2
16	16		1215006-06	SOCKET 24PIN IC LOW PROFILE	2		XE126,XE127
17	17		1216116-00	SOCKET 40PIN	5		XE74-XE78
18	18		1210929-02	FUSE, SUB-MINI 1.000A, 125V, A	1		F1
19	19		1211164-04	SW,DIP 1P 1A 8POS	2		E102,E114
20	20		1213113-01	HANDLE,MODULE,	1		
21	21		1300229-00	100.0 .25 W 5.0 % CC	1		R7
22	22		1300318-00	470.0 .25 W 5.0 % CC	3		R6,R12,R16
23	23		1300365-00	1.0 K .25 W 5.0 % CC	4		R3,R4,R8,R11
24	24		1300488-00	12.0 K .25 W 5.0 % CC	2		R19,R20
25	25		1301322-00	180.0 .25 W 5.0 % CC	1		R13
26	26		1301808-00	22.0 K .25 W 5.0 % CC	1		R18
27	27		1302177-00	47.0 K .25 W 5.0 % CC	2		R1,R2

REVISION HISTORY		BASIC PART NO: M8189		DRN:	R. BUREAU	DATE: 11-JUL-80	D I G I T A L			
ENGI	ECO NUMBER	REV	SECTION A OF A	CHK'D:	BOB BARILONE	DATE: 11-JUL-80	TITLE PARTS LIST			
	INITIAL	A	SECTION.VARIATION INDEX	CHK'D:	BOB BARILONE <td>DATE: 11-JUL-80</td> <td colspan="4">KDF11-B CPU MODULE</td>	DATE: 11-JUL-80	KDF11-B CPU MODULE			
			[A] 00	DES.ENG:	C.A. VALENTINE <td>DATE: 14-APR-81</td> <td colspan="4">DOCUMENT NUMBER</td>	DATE: 14-APR-81	DOCUMENT NUMBER			
			[B]	RESP.ENG.:	JAY NICHOLS <td>DATE: 14-APR-81</td> <td>SIZE</td> <td>CODE</td> <td>NUMBER</td> <td>REV</td>	DATE: 14-APR-81	SIZE	CODE	NUMBER	REV
			[C]	MFG.ENG.:	TOMAS OLMO <td>DATE: 14-APR-81</td> <td>K</td> <td>PL</td> <td>M8189-0-DBP</td> <td>A</td>	DATE: 14-APR-81	K	PL	M8189-0-DBP	A
			[D]	ASSEMBLY NUMBER:		TOP DOCUMENT NUMBER:	FILE NAME:		EDIT #	
			[E]	D-UA-M8189-0-0		B-DD-M8189-0-0	Z1037A.PLS		17	
			[F]	"THIS DRAWING AND SPECIFICATIONS HEREIN, ARE THE PROPERTY OF DIGITAL EQUIPMENT CORPORATION AND SHALL NOT BE REPRODUCED OR COPIED OR USED IN WHOLE OR IN PART AS THE BASIS FOR THE MANUFACTURE OR SALE OF ITEMS WITHOUT WRITTEN PERMISSION. COPYRIGHT (C) 1981. DIGITAL EQUIPMENT CORPORATION"						
			[G]							
			[H]							
			[I]							
			[J]							
			[K]							
			[L]							
			[M]							
			[N]							

LINE	ITEM	DOCUMENT NUMBER	PART NUMBER	DESCRIPTION	QTY	PER VARIATION	REFERENCE DESIGNATOR
					00		
28	28		1302602-00	56.0			
29	29		1309422-00	5.10			R5
30	30		1311003-01	R NETWORK 14-180			R9,R10
31	31		1301320-00	1.20 K			E8,E27,E62
32	32		1300005-03	R NETWORK 13-10K			R21
33	33		1300005-07	R NETWORK 15-4.7K			E123
34	34		1300228-00	100.0			E72,E108,E122
35	35		1303178-00	620.0			R15,R17
36	36		1811660-02	OSCILLATOR, XTAL			R14
37	37		1811660-20	OSCILLATOR, XTAL			E91
38	38		1910544-00	74S74			E7
39	39		1910548-00	74S157			E17,E19,E29,E30,E36,E38,E43,E50
40	40		1910550-00	74S174			E15
41	41		1910957-00	74S175			E3,E10,E21,E26,E51
42	42		1911117-00	DEC 8838			E12,E22,E40,E59
43	43		1911469-00	DEC 8640			E2
44	44		1909705-00	DEC 8881			E1,E20,E63
45	45		1911675-00	74S138			E9
46	46		1911712-00	74S51			E66
47	47		1912098-00	0026			E45
48	48		1912388-00	74S02			E90
49	49		1912389-00	74S08			E37,E52,E56
50	50		1912647-00	LS257			E11,E28,E39,E96
51	51		1912649-00	LS75			E83,E100,E106,E110,E113,E119
52	52		1912697-00	LS174			E49
53	53		1912730-00	DC 003			E93,E107,E112
54	54		1912746-00	DEC 74S37			E98,E104
55	55		1912801-00	LS02			E61
56	56		1912803-00	74LS04			E85
57	57		1912804-00	LS05			E89
58	58		1912805-00	LS08			E82,E87
59	59		1912807-00	LS10			E65
60	60		1912808-00	LS11			E25,E95
61	61		1912810-00	LS20			E14
62	62		1912816-00	LS32			E53,E60
63	63		1912824-00	LS74			E120,E124
64	64		1912846-00	LS155			E5,E80,E111,E64
65	65		1912853-00	LS175			E103,E109,E115
66	66		1912857-00	LS197			E117
67	67		1912858-00	LS221			E105
68	68		1912863-00	LS273			E6
69	69		1912868-00	LS299			E86
70	70		1913340-00	74S32			E92,E101
71	71		1913462-00	74S240			E4,E44,E97,E116
72	72		1913671-00	74S374			E42,E73,E79
73	73		1913777-00	LS240			E70
74	74		1914085-00	74S260			E94
75	75		1915218-00	LS245			E23
							E81,E84

D	I	G	I	T	A	L	TITLE	SECTION A	OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							KDF11-B CPU MODULE			K	PL	M8189-0-DBP	A



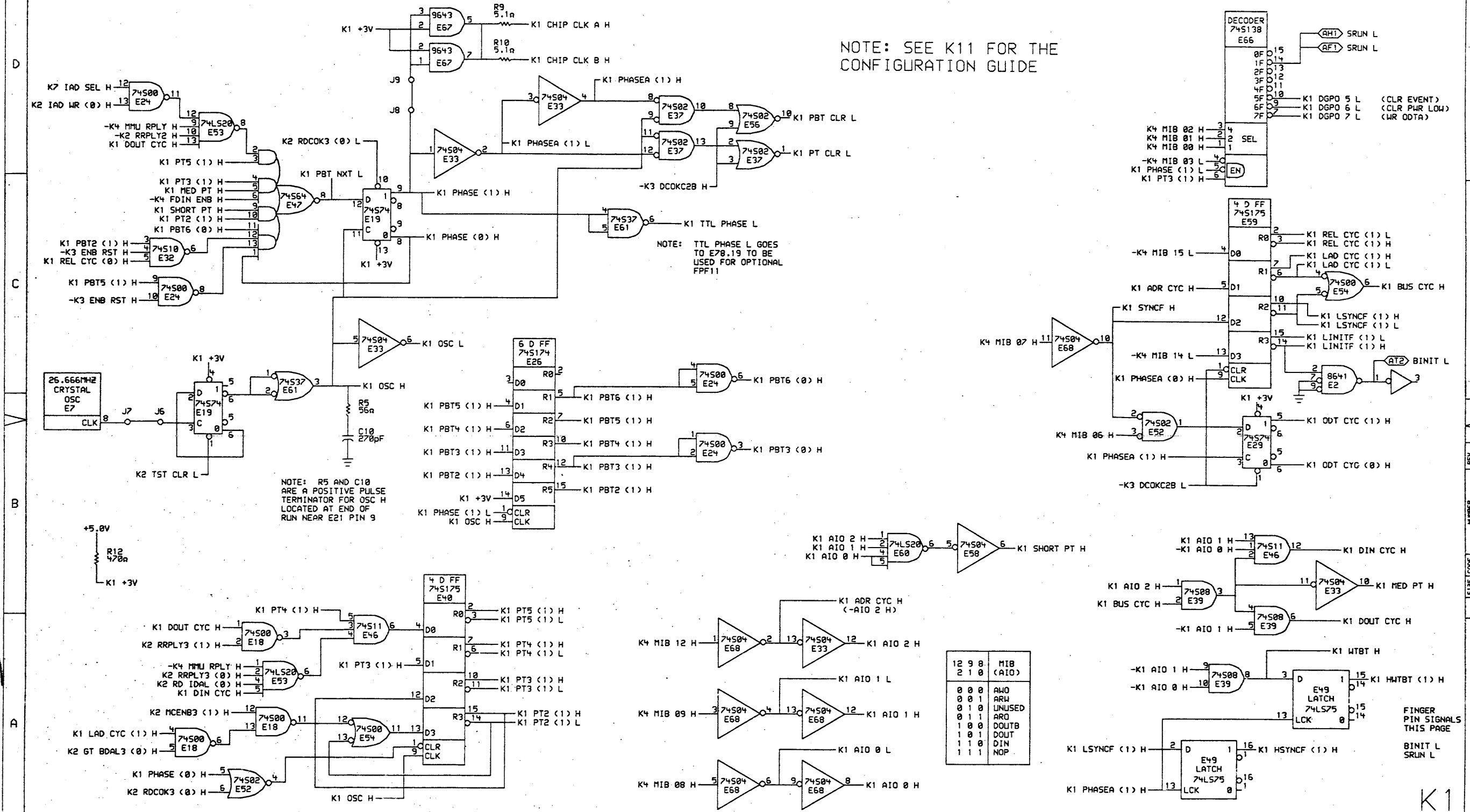
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77	77		1915415-00	9636 DRIVER,DUAL,EIA RS-	1	E118
78	78		1915416-00	9637 RECEIVER,DUAL,RS-42	1	E125
79	79		1916028-01	9643 DRIVER,TTL TO MOS,D	1	E67
80	80		1910532-00	74500 NAND GATE-QUAD 2IN	6	E16,E18,E24,E31,E35,E54
81	81		1910534-00	74504 INVERTER GATE-HEX 1I	4	E33,E58,E68,E99
82	82		1910535-00	74505 INVERTER GATE-HEX 1	1	E57
83	83		1910536-00	74510 NAND GATE-TRIPLE 3IN	1	E32
84	84		1910537-00	74511 AND GATE-TRIPLE 3INP	1	E46
85	85		1910542-00	74564 A-O-I GATE 4-2-3-2	1	E47
86	87		2112623-00	DUAL BAUD RATE GEN/PROG DIVIDER,	1	E121
87	88		2113937-01	6402-1 UART,UNIV.,ASYNCHRO	2	E128,E129
88	91		23061C6-00	C6-01	1	E88
89	92		5700000-01	DAT/CTL HYBRID ASSY W/FP,DCF11-A	1	E75
90	93		9009149-00	PIN, STAKING, P.C. BOARD, .025 X	44	J3-J46
91	94		9009185-00	JUMPER, WIRE, INSULATED, BLACK B	2	W1,W2
92	95		9000024-01	EYELET,ROLL FLANGE .1210DX .192	6	
93	96		9010213-01	SPACER,14 PIN BLK/NYL .060THK.	1	
94	97		1218783-00	CONN .100 2POS JUMPER	12	

D	I	G	I	T	A	L	TITLE		SECTION A OF A	SIZE	CODE	DOCUMENT NUMBER	REV
							KDF11-B CPU MODULE			K	PL	M8189-0-DBP	A

# BASE TIMING - MCLK CTL

# MIB DECODE LOGIC

NOTE: SEE K11 FOR THE CONFIGURATION GUIDE



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REVISIONS	
CHK	CHANGE NO. REV

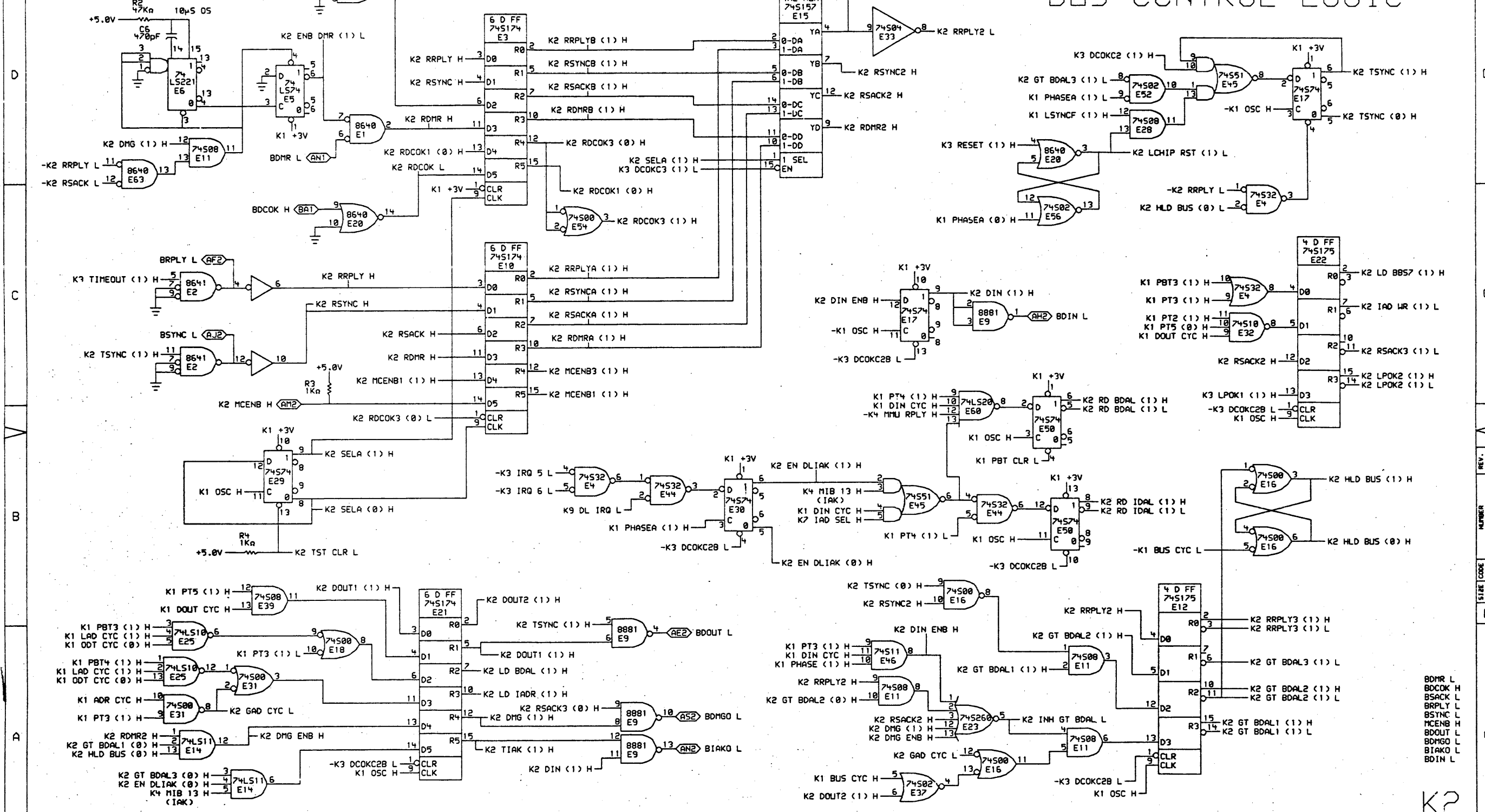
digital	DRN: <i>Hullison</i>	DATE: 05-MAR-81	EMF: <i>Ami Michale</i>	DATE: 4-13-81
	CHK: <i>Hullison</i>	DATE: 9-13-81	BOARD LOCATION: <i>Charlie Valente</i>	DATE: 4-7-81
FIRST USED ON OPTION/MODEL: KDF11-B		NEXT HIGHER ASSEMBLY: B-DD-M8189-0		SIZE CODE: D CS

TITLE: TIMING LOGIC & MIB DECODE  
 DRAWING 1 OF 11  
 NUMBER: M8189-0-K1  
 REV. A

REV. A  
 NUMBER M8189-0-K1  
 SIZE CODE CS  
 FINGER PIN SIGNALS THIS PAGE  
 BINIT L  
 SRUN L

QBUS SYNCHRONIZER

BUS CONTROL LOGIC



K2

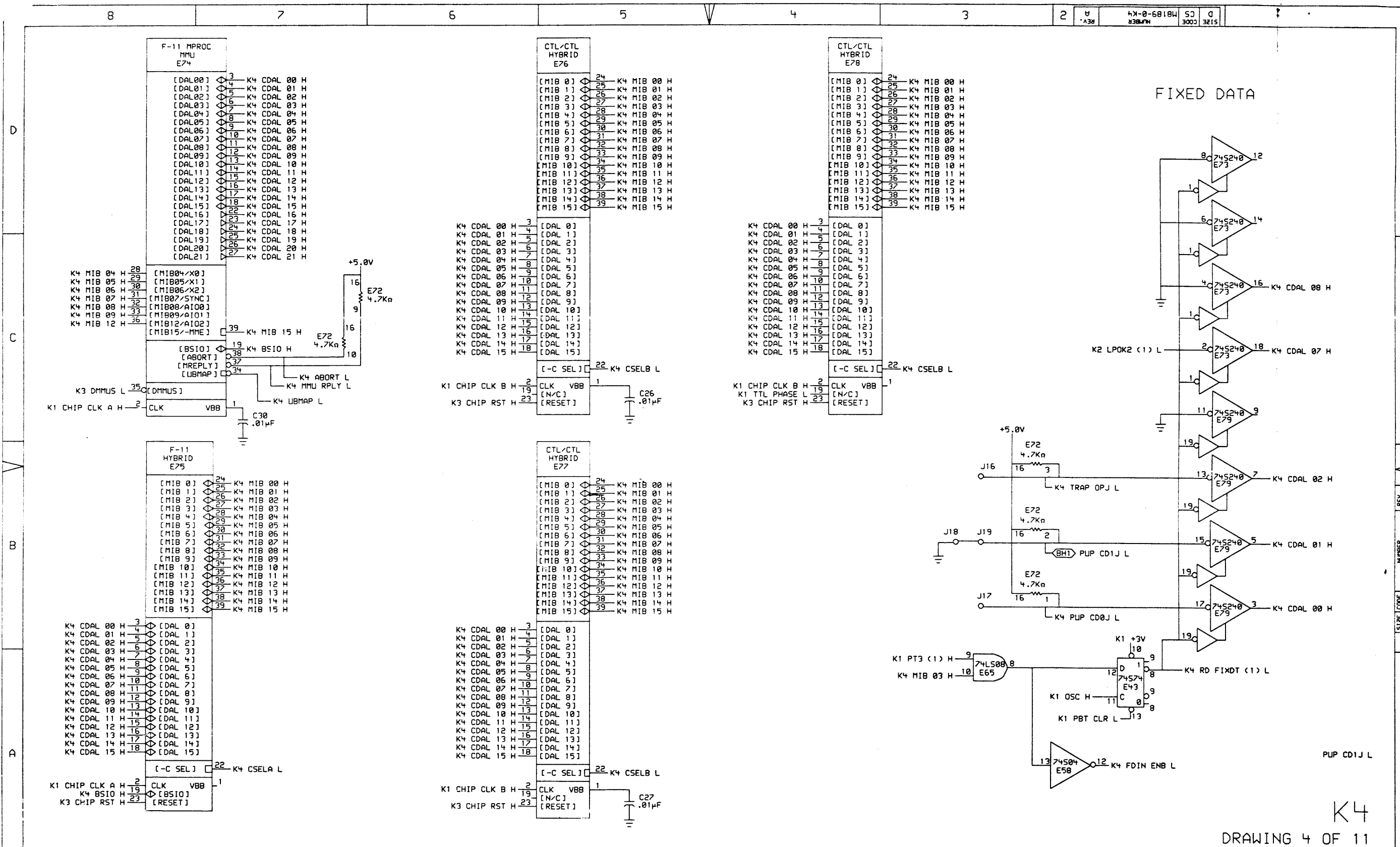
DRAWING 2 OF 11.

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REVISIONS	
CHK	CHANGE NO. REV

digit@l	DRN: H Callison	DATE: 02-MAR-81	ENG: P. K. K. K.	DATE: 4-10-81	TITLE: BUS CONTROL LOGIC
	CHK: D. Callison	DATE: 4-13-81	BOARD LOCATION:	SHEET: 1 OF 1	
FIRST USED ON OPTION/MODEL: KDF11-B		NEXT HIGHER ASSEMBLY: B-DD-M8189-0		SIZE CODE: D CS	NUMBER: M8189-0-K2
				REV: A	





FIXED DATA

K4  
 DRAWING 4 OF 11

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REVISIONS	
CHK	CHANGE NO. REV.

digital	DRN. <i>H. Plummer</i>	DATE 05-MAR-81	ENG. <i>Charles V...</i>	DATE 4-2-81	TITLE: F11 CHIPS & FIXED DATA
	CHK'D. <i>H. Plummer</i>	DATE 4-2-81	BOARD LOCATION: 4-2-81	SHEET 4 OF 11	NUMBER M8189-0-K4
FIRST USED ON OPTION/MODEL: KDF11-B B-DD-M8189-0					REV. A



BDAL 00 L  
 TO  
 BDAL 21 L  
 BCTRL L  
 BBS7 L  
 BWTBT L

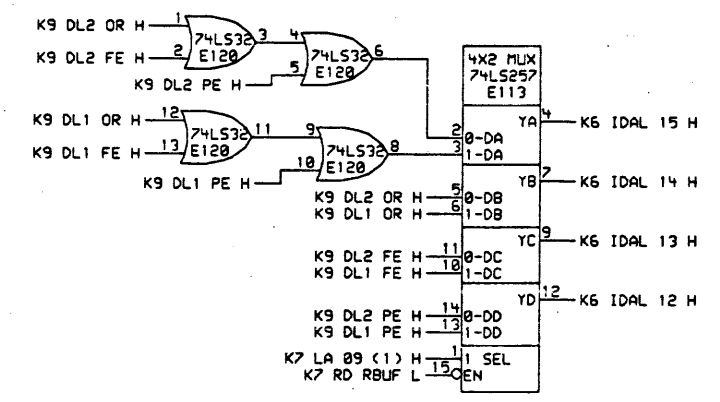
**K5**

DRAWING 5 OF 11

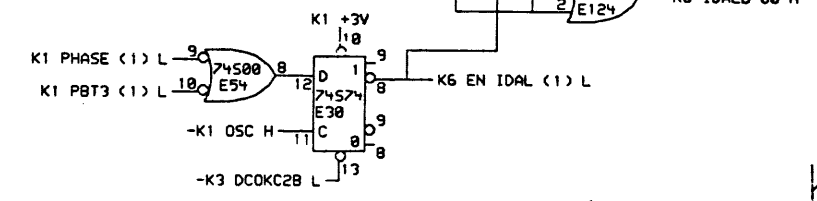
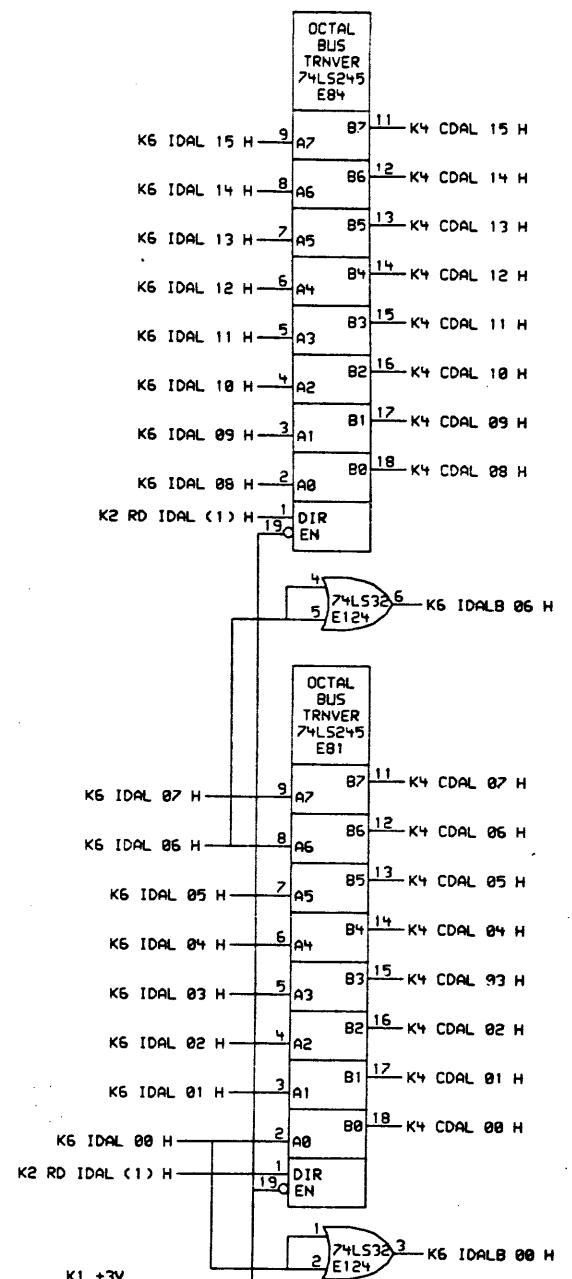
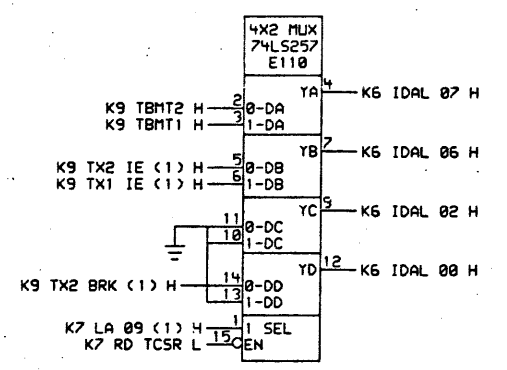
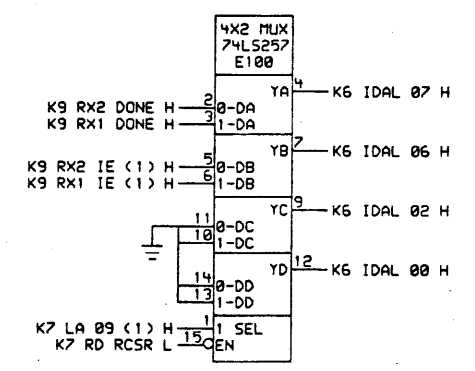
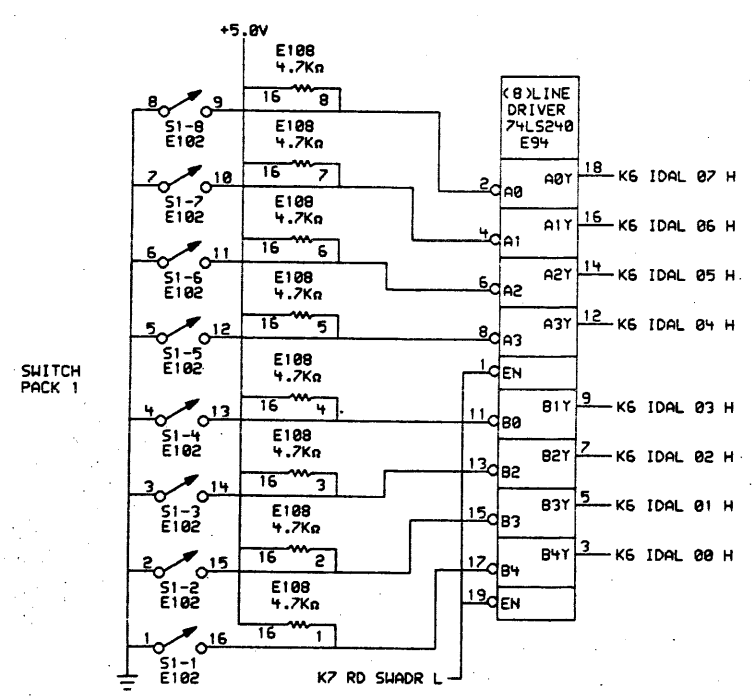
REV. A
SIZE CODE CS M8189-0-K5
B
A

CDAL/IDAL TRANSCEIVERS

SLU's READ STATUS



BOOT SWITCHES



K6  
 DRAWING 6 OF 11

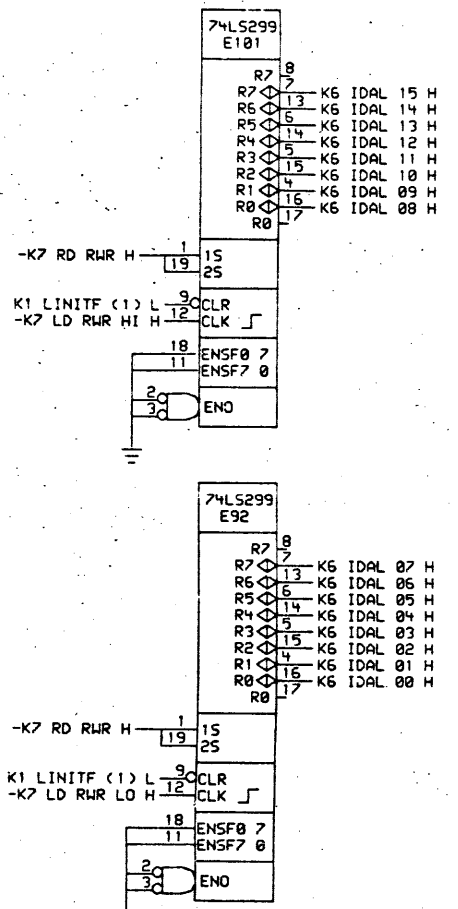
REV.	CHG	NO.	REV.

digital	DRN: <i>Hallinan</i>	DATE: 05-MAR-81	ENG: <i>Charles Valenti</i>	DATE: 4-2-81	TITLE: CDAL/IDAL INTERFACE
	CHK: <i>R. Callahan</i>	DATE: 4-11-81	BOARD LOCATION: 1	SHEET: 1	OF: 1
FIRST USED ON OPTION MODEL: KDF11-B					8-DD-M8189-0
SIZE	CODE	NUMBER	REV.		
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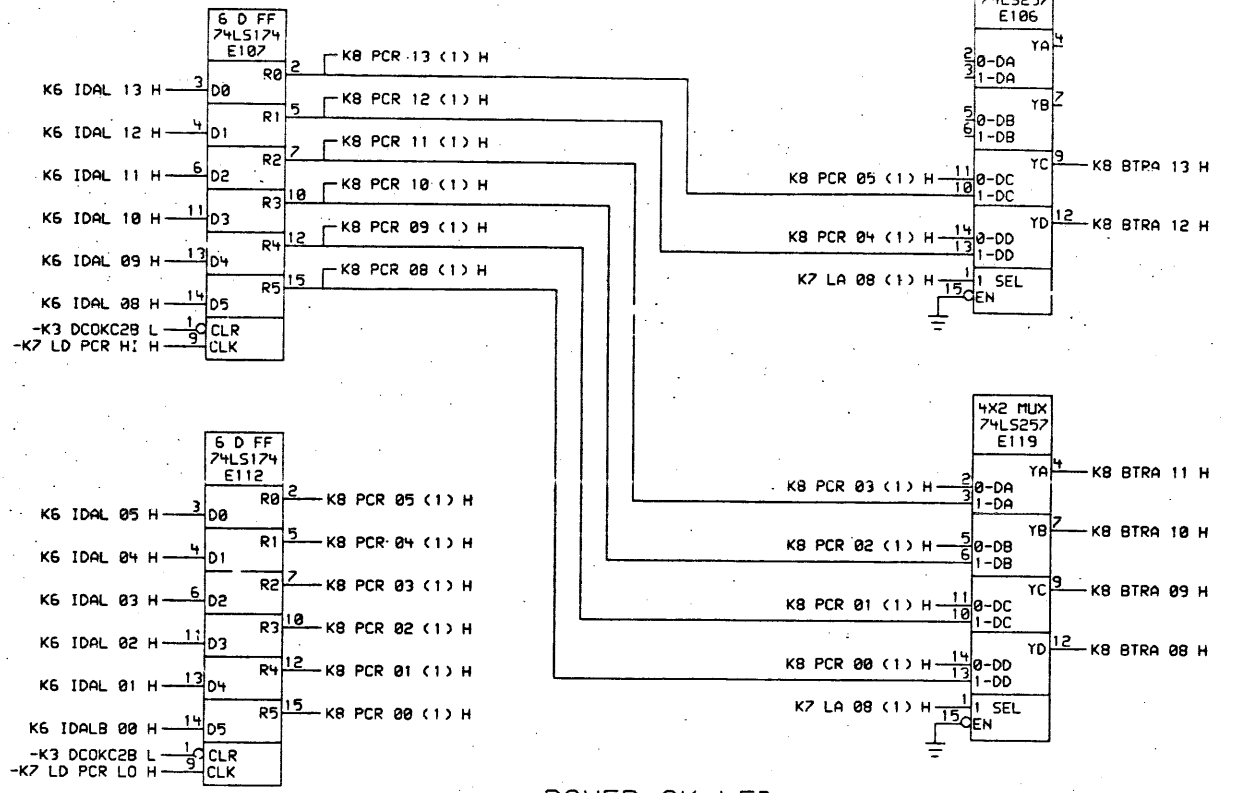




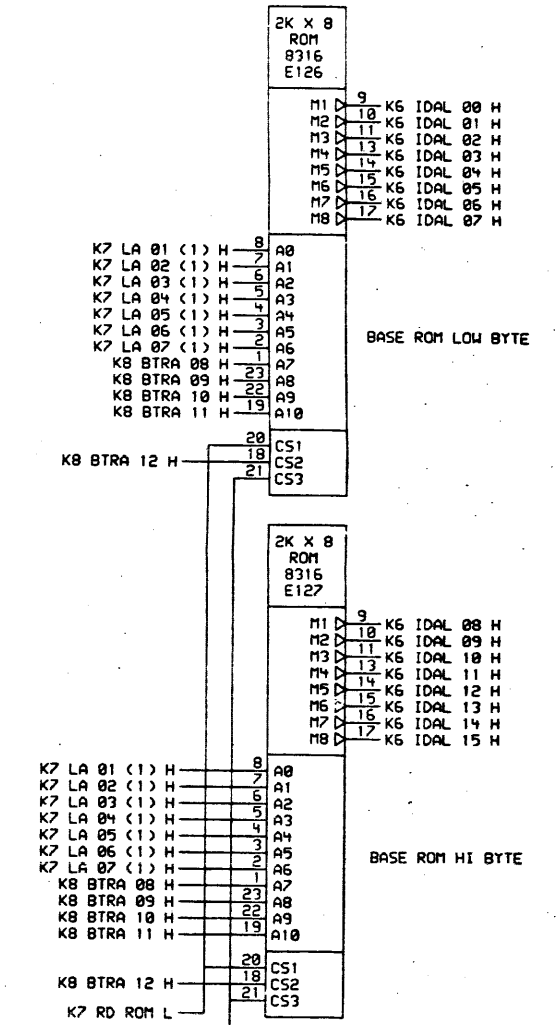
RDWR REG



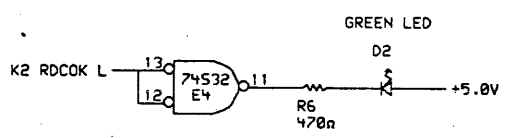
PAGE CTL REG & MUX



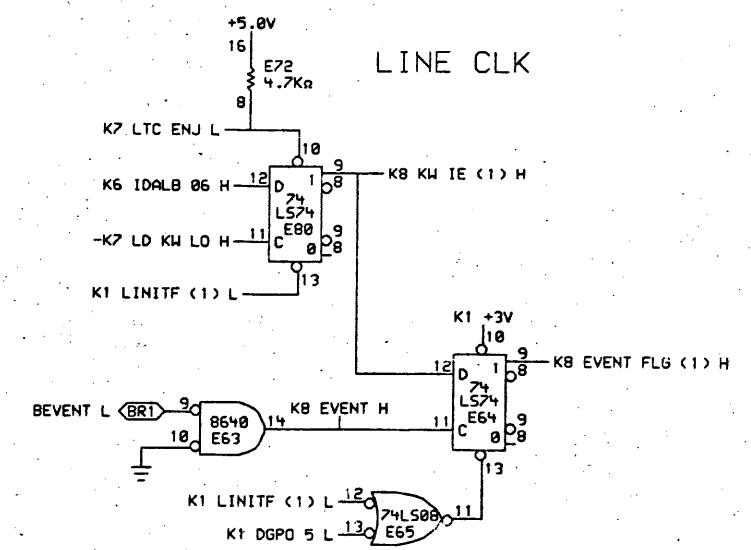
BOOT ROMS



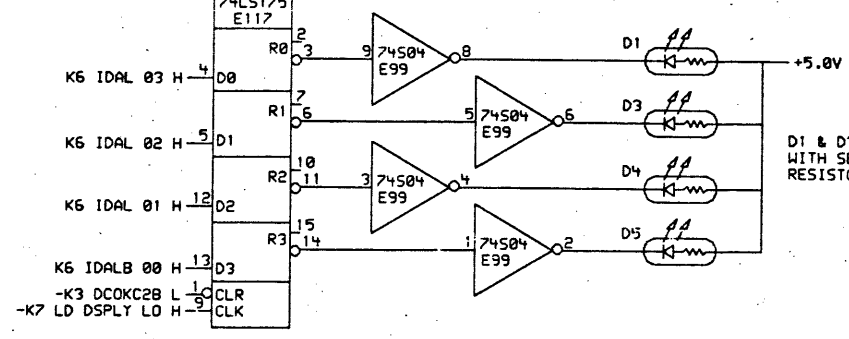
POWER OK LED



LINE CLK



DISPLAY

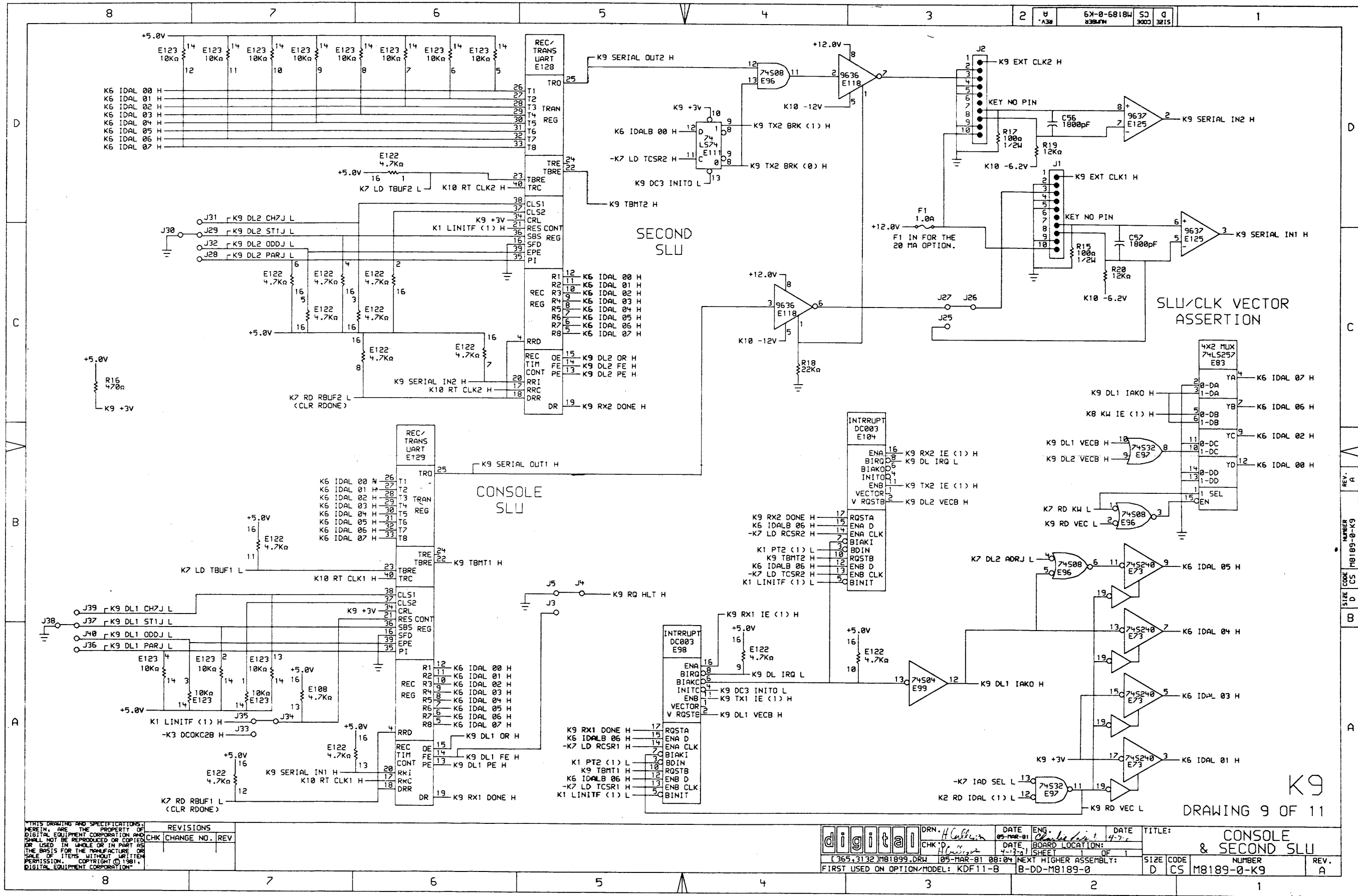


K8  
 DRAWING 8 OF 11

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REVISIONS	CHK	CHANGE NO.	REV

digital	DRN: H. Callison	DATE: 03-APR-81	ENG: H. Callison	DATE: 4-13-81	TITLE: BOOT & CLOCK LOGIC
L 365,3132 M81898.DRW	CHK'D: H. Callison	DATE: 02-APR-81	DATE: 4-13-81	BOARD LOCATION: 1 OF 1	SIZE CODE: D CS
FIRST USED ON OPTION/MODEL: KDF11-B					NUMBER: M8189-0-K8
					REV. A



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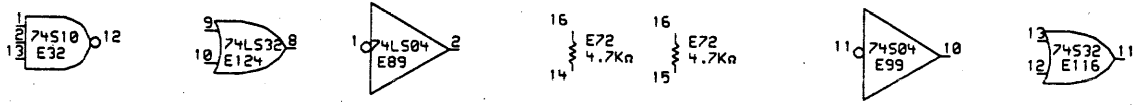
CHK	CHANGE NO.	REV

REVISIONS

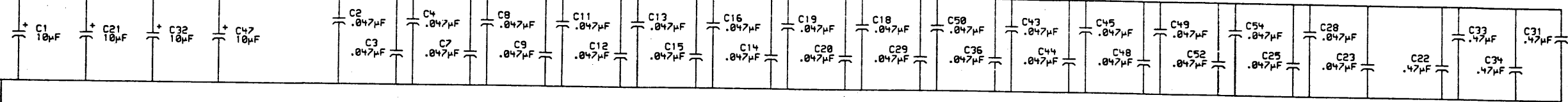
	DRN: H. Colburn	DATE: 05-1981	ENG: Charles...	DATE: 4-7-	TITLE: CONSOLE & SECOND SLU
	CHK: D. ...	DATE: 4-7-81	BOARD LOCATION: 4-7-81	SHEET: OF 1	
L365,3132 M81899-DRW 05-MAR-81 08:04 NEXT HIGHER ASSEMBLY: B-DD-M8189-0		SIZE: D	CODE: CS	NUMBER: M8189-0-K9	REV: A

K9 DRAWING 9 OF 11

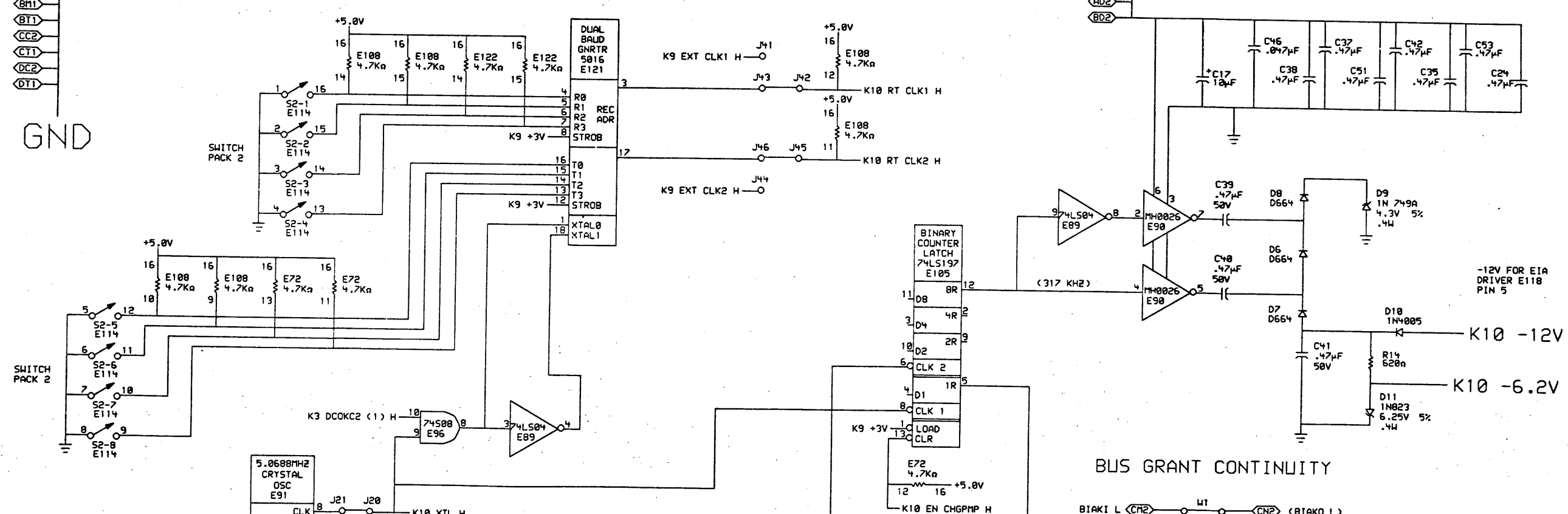
SPARE GATES



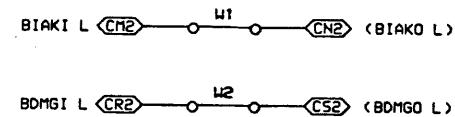
DECOUPLING CAPS



BAUD RATE GENERATOR



BUS GRANT CONTINUITY



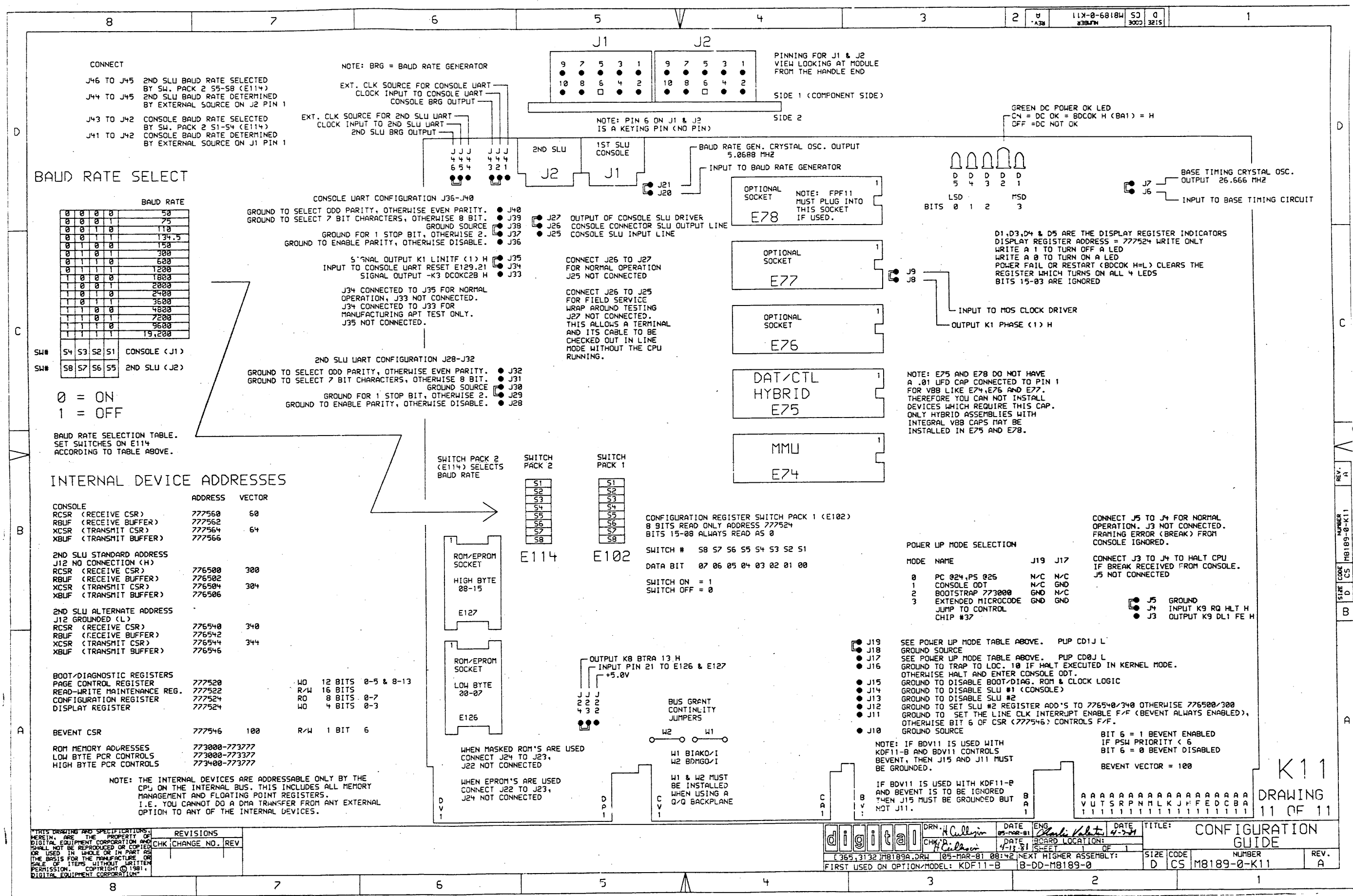
K10

DRAWING 10 OF 11

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REVISIONS	CHK	CHANGE NO.	REV.

digital	DRN: H. Collins	DATE: 05-03-81	ENG: H. Collins	DATE: 4-7-81	TITLE: BAUD RATE & -12V
	CHK: H. Collins	DATE: 4-13-81	SCHEMATIC LOCATION: 1 OF 1		
FIRST USED ON OPTION/MODEL: KDF11-B					
SIZE	CODE	NUMBER	REV.		
D	C5	M8189-0-K10	A		



CONNECT

J46 TO J45 2ND SLU BAUD RATE SELECTED BY SW. PACK 2 55-58 (E114)

J44 TO J45 2ND SLU BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J2 PIN 1

J43 TO J42 CONSOLE BAUD RATE SELECTED BY SW. PACK 2 51-54 (E114)

J41 TO J42 CONSOLE BAUD RATE DETERMINED BY EXTERNAL SOURCE ON J1 PIN 1

BAUD RATE SELECT

BAUD RATE				
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1200
1	0	0	0	1800
1	0	0	1	2000
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19200

SW# 54 53 52 51 CONSOLE (J1)

SW# 58 57 56 55 2ND SLU (J2)

0 = ON

1 = OFF

BAUD RATE SELECTION TABLE. SET SWITCHES ON E114 ACCORDING TO TABLE ABOVE.

INTERNAL DEVICE ADDRESSES

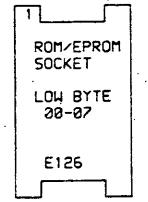
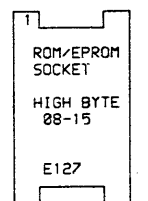
CONSOLE	ADDRESS	VECTOR
RCSR (RECEIVE CSR)	777560	60
RBUF (RECEIVE BUFFER)	777562	
XCSR (TRANSMIT CSR)	777564	64
XBUF (TRANSMIT BUFFER)	777566	
2ND SLU STANDARD ADDRESS		
J12 NO CONNECTION (H)		
RCSR (RECEIVE CSR)	776500	300
RBUF (RECEIVE BUFFER)	776502	
XCSR (TRANSMIT CSR)	776504	304
XBUF (TRANSMIT BUFFER)	776506	
2ND SLU ALTERNATE ADDRESS		
J12 GROUNDED (L)		
RCSR (RECEIVE CSR)	776540	340
RBUF (RECEIVE BUFFER)	776542	
XCSR (TRANSMIT CSR)	776544	344
XBUF (TRANSMIT BUFFER)	776546	
BOOT/DIAGNOSTIC REGISTERS		
PAGE CONTROL REGISTER	777520	W/O 12 BITS 0-5 & 8-13
READ-WRITE MAINTENANCE REG.	777522	R/W 16 BITS
CONFIGURATION REGISTER	777524	RO 8 BITS 0-7
DISPLAY REGISTER	777524	W/O 4 BITS 0-3
BEVENT CSR		
	777546	100 R/W 1 BIT 6
ROM MEMORY ADDRESSES		
LOW BYTE PCR CONTROLS	773000-773777	
HIGH BYTE PCR CONTROLS	773400-773777	

NOTE: THE INTERNAL DEVICES ARE ADDRESSABLE ONLY BY THE CPU ON THE INTERNAL BUS. THIS INCLUDES ALL MEMORY MANAGEMENT AND FLOATING POINT REGISTERS. I.E. YOU CANNOT DO A DMA TRANSFER FROM ANY EXTERNAL OPTION TO ANY OF THE INTERNAL DEVICES.

REVISIONS	CHK	CHANGE NO.	REV

SWITCH PACK 2 (E114) SELECTS BAUD RATE

SWITCH PACK 2	SWITCH PACK 1
S1	S1
S2	S2
S3	S3
S4	S4
S5	S5
S6	S6
S7	S7
S8	S8



WHEN MASKED ROM'S ARE USED CONNECT J24 TO J23, J22 NOT CONNECTED

WHEN EPROM'S ARE USED CONNECT J22 TO J23, J24 NOT CONNECTED

CONFIGURATION REGISTER SWITCH PACK 1 (E102) 8 BITS READ ONLY ADDRESS 777524 BITS 15-08 ALWAYS READ AS 0

SWITCH # 58 57 56 55 54 53 52 51

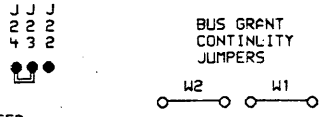
DATA BIT 07 06 05 04 03 02 01 00

SWITCH ON = 1

SWITCH OFF = 0

OUTPUT K8 BTRA 13 H

INPUT PIN 21 TO E126 & E127 +5.0V



W1 BIAKO/I

W2 BDMGO/I

W1 & W2 MUST BE INSTALLED WHEN USING A Q/Q BACKPLANE

POWER UP MODE SELECTION

MODE	NAME	J19	J17
0	PC 024.PS 025	N/C	N/C
1	CONSOLE ODT	N/C	GND
2	BOOTSTRAP 773000	GND	N/C
3	EXTENDED MICROCODE JUMP TO CONTROL CHIP #37	GND	GND

- J19 SEE POWER UP MODE TABLE ABOVE. PUP CD1J L
- J18 GROUND SOURCE
- J17 SEE POWER UP MODE TABLE ABOVE. PUP CD0J L
- J16 GROUND TO TRAP TO LOC. 10 IF HALT EXECUTED IN KERNEL MODE. OTHERWISE HALT AND ENTER CONSOLE ODT.
- J15 GROUND TO DISABLE BOOT/DIAG. ROM & CLOCK LOGIC
- J14 GROUND TO DISABLE SLU #1 (CONSOLE)
- J13 GROUND TO DISABLE SLU #2
- J12 GROUND TO SET SLU #2 REGISTER ADD'S TO 776540/340 OTHERWISE 776500/300
- J11 GROUND TO SET THE LINE CLK INTERRUPT ENABLE F/F (BEVENT ALWAYS ENABLED), OTHERWISE BIT 6 OF CSR (777546) CONTROLS F/F.
- J10 GROUND SOURCE

NOTE: IF BDV11 IS USED WITH KDF11-B AND BDV11 CONTROLS BEVENT, THEN J15 AND J11 MUST BE GROUNDED.

IF BDV11 IS USED WITH KDF11-B AND BEVENT 15 TO BE IGNORED THEN J15 MUST BE GROUNDED BUT NOT J11.

CONNECT J5 TO J4 FOR NORMAL OPERATION. J3 NOT CONNECTED. FRAMING ERROR (BREAK) FROM CONSOLE IGNORED.

CONNECT J3 TO J4 TO HALT CPU IF BREAK RECEIVED FROM CONSOLE. J5 NOT CONNECTED

- J5 GROUND
- J4 INPUT K9 RQ HLT H
- J3 OUTPUT K9 DL1 FE H

BIT 6 = 1 BEVENT ENABLED

IF PSW PRIORITY < 6

BIT 6 = 0 BEVENT DISABLED

BEVENT VECTOR = 100

AAAAAAAAAAAAAAAAAAAAA

VUTSRPNMLKJH FEDCBA

111111111111111111111

K11

DRAWING 11 OF 11

digital	DRN: H. Callan	DATE: 05-02-81	ENG: Charlie Keltner	DATE: 4-2-81	TITLE: CONFIGURATION GUIDE
	CHK: H. Callan	DATE: 4-13-81	BOARD LOCATION: 1	SHEET: 1	OF: 1
FIRST USED ON OPTION/MODEL: KDF11-B					SIZE CODE: D CS
NEXT HIGHER ASSEMBLY: 105-MAR-81 08:42					NUMBER: M8189-0-K11
REV. A					REV. A



