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Data Book Addendum

Product Name: MediaGX™ MMX™ - Enhanced Processor Data Book, Revision 2.0 Addendum

Date: May 14, 1999

Scope

This document details known errors in the Cyrix MediaGX™ MMX™ Enhanced Processor Data Book, Revision 2.0, dated October 1998.

Discussion

Table 1 provides a description of the error, the correction, and denotes the page(s) of the data book that are affected. Following the table are the affected pages with the corrections in bold italics.

These changes will be incorporated into the next released version of the data book.

Note: The change between versions 1.0 and 2.0 of this addendum is the addition of item #11.

Table 1 Addendum Summary

Item	Error	Correction	Affected Text
			Data Book (Rev 2.0)
1	Bit 6 of CCR2 is listed as Reserved.	This is a test bit that must be set to 1.	Table 3-11 on page 52
2	Bit 7 of CCR2 - If equal to 0, SUSP# input is ignored and SUSPA# output floats.	Delete “and SUSPA# output floats”.	Table 3-11 on page 52
3	SUSPA# floats following RESET# and is enabled by setting the SUSP bit in CCR2.	Deleted "floats following reset and".	Section 2.2.1, System Interface Signals on page 23
4	Index C3h[3] of CCR3 is listed as Reserved-Set to 0.	Changed description of bit 3.	Table 3-11 on page 53
5	Index E8h[5] of CCR4 is listed as Reserved-Set to 0.	Changed description of bit 5.	Table 3-11 on page 54
6	Index EBh[5] of PCR is listed as Reserved-Set to 0.	This is a test bit that must be set to 0.	Table 3-11 on page 54
7	Figure 3-2 illustrates the CPU cache architecture.	Figure 3-1 illustrates the CPU cache architecture - not Figure 3-2.	Page 61
8	GX_BASE+8004h[13] - SMIB: All I/O accesses for address range 3C0h-3CFh generate an SMI. This address range is wrong.	Address range is 3B0h-3BFh.	Table 4-10 on page 114

Table 1 Addendum Summary (cont.)

Item	Error	Correction	Affected Text Data Book (Rev 2.0)
9	Change the description of BC_XMAP bits to preclude confusion about what they do and how they work (writes to ROM area are not blocked if in the cache)	Added note to Table 4-11.	Table 4-11 on page 115.
10	Description of required protocol for changing cache operation (WT, WB or Disable)	Changed description of CR0 Register bit 30 and added third paragraph in Section 4.1.4.	Table 3-7 on page 48 and Section 4.1.4, L1 Cache Controller on page 107.
11	Wrong description for bit 2 of CCR7 register.	If set to 1, an NMI is generated - not acknowledged.	Table 3-11 on page 54.

Items #1 and #2

Table 3-11 Configuration Registers

Bit	Name	Description
Index C1h		**CCR1 — Configuration Control Register 1 (R/W)** **Default Value = 00h**
7:3	RSVD	**Reserved:** Set to 0.
2	SMAC	**System Management Memory Access:** If = 1: SMINT instruction can be recognized (see Table 3-33 on page 88). If = 0: SMINT instruction has no affect. **Note:** SMI_LOCK (CCR3[0]) must = 0, or the CPU must be in SMI mode, to write this bit.
1	USE_SMI	**Enable SMM Pins:** If = 1: SMI# input pin is enabled (see Table 3-33 0n page 88). SMINT instruction can be recognized. If = 0: SMI# pin is ignored. **Note:** SMI_LOCK (CCR3[0]) must = 0, or the CPU must be in SMI mode, to write this bit.
0	RSVD	**Reserved** — Set to 0.
Note: Bits 1 and 2 are cleared to zero at reset.		
Index C2h		**CCR2 — Configuration Control Register 2 (R/W)** **Default Value = 00h**
7	USE_SUSP	**Enable Suspend Pins:** If = 1: SUSP# input and SUSPA# output are enabled. If = 0: SUSP# input is ignored and ~~SUSPA# output floats~~.
6	***RSVD***	***Reserved: This is a test bit that must be set to 1.***
5	RSVD	**Reserved:** Set to 0.
4	WT1	**Write-Through Region 1**: If = 1: Forces all writes to the address region between 640KB to 1MB that hit in the on-chip cache to be issued on the external bus.
3	SUSP_HLT	**Suspend on HALT:** If = 1: CPU enters suspend mode following execution of a HALT instruction.
2	LOCK_NW	**Lock NW Bit:** If = 1: Prohibits changing the state of the NW bit (CR0[29]) (refer to on page 11). Set to 1 after setting NW.
1:0	RSVD	**Reserved:** Set to 0.
Note: All bits are cleared to zero at reset.		

Item #3

2.2.1 System Interface Signals

Signal Name	BGA Pin No.	SPGA Pin No.	Type	Description
SUSP#	H2 (PU)	M4 (PU)	I	**Suspend Request** This signal is used to request that the MediaGX processor enter Suspend mode. After recognition of an active SUSP# input, the processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. SUSP# is ignored following RESET# and is enabled by setting the SUSP bit in CCR2. (See Table 3-11 "Configuration Registers" on page 52 for CCR2 bit definitions.) Since the MediaGX processor includes system logic functions as well as the CPU core, there are special modes designed to support the different power management states associated with APM, ACPI, and portable designs. The part can be configured to stop only the CPU core clocks, or all clocks. When all clocks are stopped, the external clock can also be stopped. (See Section 6 “Power Management” on page 201 for more details regarding power management states.) This pin is internally connected to a 20-kohm pull-up resistor. SUSP# is pulled up when not active.
SUSPA#	E2	H4	O	**Suspend Acknowledge** Suspend Acknowledge indicates that the MediaGX processor has entered low-power Suspend mode as a result of SUSP# assertion or execution of a HALT instruction. SUSPA# ~~floats following RESET# and~~ is enabled by setting the SUSP bit in CCR2. (See Table 3-11 "Configuration Registers" on page 52 for CCR2 bit definitions.) The SYSCLK input may be stopped after SUSPA# has been asserted to further reduce power consumption if the system is configured for 3V Suspend mode. (Section 6.4 “3-Volt Suspend Mode” on page 203 for details regarding this mode.)
SERIALP	L3	Q1	O	**Serial Packet** Serial Packet is the single wire serial-transmission signal to the Cx5520 chip. The clock used for this interface is the PCI clock (SYSCLK). This interface carries packets of miscellaneous information to the chipset to be used by the VSA software handlers.

Item #4

Table 3-11 Configuration Registers (cont.)

Bit	Name	Description
Index C3h		**CCR3 — Configuration Control Register 3 (R/W)** **Default Value = 00h**
7	LSS_34	**Load/Store Serialize 3 GBytes to 4 GBytes:** If = 1: Strong R/W ordering imposed in address range C000 0000h to FFFF FFFFh:
6	LSS_23	**Load/Store Serialize 2 GBytes to 3 GBytes:** If = 1: Strong R/W ordering imposed in address range 8000 0000h to BFFF FFFFh:
5	LSS_12	**Load/Store Serialize 1 GByte to 2 GBytes**: If = 1: Strong R/W ordering imposed in address range 4000 0000h to 7FFF FFFFh
4	MAPEN	**Map Enable:** If = 1: All configuration registers are accessible. All accesses to Port 22h are trapped. If = 0: Only configuration registers Index C1h through CFh, FEh, FFh (CCRn, SMAR, DIRn) are accessible. Other configuration registers (including PCR, SMHRn, GCR, VGACTL, VGAM0) are not accessible.
3	***SUSP_SMM_EN***	***Enable Suspend in SMM Mode:*** ***0 = SUSP# ignored in SMM mode.*** ***1 = SUSP# recognized in SMM mode.***
2	RSVD	**Reserved:** Set to 0.
1	NMI_EN	**NMI Enable:** If = 1: NMI is enabled during SMM. If = 0: NMI is not recognized during SMM. **Note:** SMI_LOCK (CCR3[0]) must = 0 or the CPU must be in SMI mode to write to this bit.
Note: All bits are cleared to zero at reset.		

Item #5

Table 3-11 Configuration Registers (cont.)

Bit	Name	Description
Index E8h		**CCR4 — Configuration Control Register 4 (R/W)** **Default Value = 85h**
7	CPUID	**Enable CPUID Instruction:** If = 1: The ID bit in the EFLAGS register to be modified and execution of the CPUID instruction occurs as documented in Table 9-2 "Instruction Fields" on page 234. If = 0: The ID bit can not be modified and execution of the CPUID instruction causes an invalid opcode exception.
6	SMI_NEST	**SMI Nest:** If = 1: SMI interrupts can occur during SMM mode. SMI handlers can optionally set SMI_NEST high to allow higher-priority SMI interrupts while handling the current event
5	***FPU_FAST_EN***	***FPU Fast Mode Enable:*** ***0 = Disable FPU Fast Mode*** ***I1 = Enable FPU Fast Mode***
4	DTE_EN	**Directory Table Entry Cache:** If = 1: Enables directory table entry to be cached. Cleared to 0 at reset.
3	MEM_BYP	**Memory Read Bypassing:** If = 1: Enables memory read bypassing. Cleared to 0 at reset.
2:0	IORT(2:0)	**I/O Recovery Time**: Specifies the minimum number of bus clocks between I/O accesses: 000 = No clock delay 001 = 2-clock delay 010 = 4-clock delay 011 = 8-clock delay 100 = 16-clock delay 101 = 32-clock delay (default value after reset) 110 = 64-clock delay 111 = 128-clock delay Cleared to 0 at reset.
Note: MAPEN (CCR3[4]) must = 1 to read or write to this register.		
Index EBh		**CCR7 — Configuration Control Register 7 (R/W)** **Default Value = 00h**
7:3	RSVD	**Reserved:** Set to 0.
2	NMI	**Generate NMI:** ***0 = Do nothing*** ***1 = Generate NMI*** ***In order to generate multiple NMIs, this bit must be set to zero between each setting of 1.***
1	RSVD	**Reserved:** Set to 0.
0	EMMX	**Cyrix Extended MMX Instructions Enable:** If = 1: Cyrix extended MMX instructions are enabled

Item # 6

Table 3-11 Configuration Registers (cont.)

Bit	Name	Description
Index 20h		**PCR — Performance Control Register (R/W)** **Default Value = 07h**
7	LSSER	**Load/Store Serialize Enable (Reorder Disable):** LSSER should be set to ensure that memory-mapped I/O devices operating outside of the address range 640K to 1M will operate correctly. For memory accesses above 1 GByte, refer to CCR3[7:5] (LSS_34, LSS_23, LSS_12.) If =1: All memory read and write operations will occur in execution order (load/store serializing enabled, reordering disabled). If =0: Memory reads and write can be reordered for optimum performance (load/store serializing disabled, reordering enabled). Memory accesses in the address range 640K to 1M will always be issued in execution order.
6	RSVD	**Reserved —** Set to 0.
5	***RSVD***	***Reserved: This is a test bit that must be set to 0.***
4:0	RSVD	**Reserved —** Set to 0.
Note: MAPEN (CCR3[4]) must = 1 to read or write to this register.		

Item #7

Cache Test Registers

The CPU's 16KB on-chip cache is a four-way set associative memory that is configured as write-back cache. Each cache set contains 256 entries. Each entry consists of a 20-bit tag address, a 16-byte data field, a valid bit, and four dirty bits.

The 20-bit tag represents the high-order 20 bits of the physical address. The 16-byte data represents the 16 bytes of data currently in memory at the physical address represented by the tag. The valid bit indicates whether the data bytes in the cache actually contain valid data. The four dirty bits indicate if the data bytes in the cache have been modified internally without updating external memory (write-back configuration). Each dirty bit indicates the status for one double-word (4 bytes) within the 16-byte data field.

For each line in the cache, there are three LRU bits that indicate which of the four sets was most recently accessed. A line is selected using bits [11:4] of the physical address. ***Figure 3-1 illustrates the CPU cache architecture and how it works.***

The CPU contains three test registers (TR5-TR3) that allow testing of its internal cache. Bit definitions for the cache test registers are shown in Table 3-16. Using a 16-byte cache fill buffer and a 16-byte cache flush buffer, cache reads and writes may be performed.

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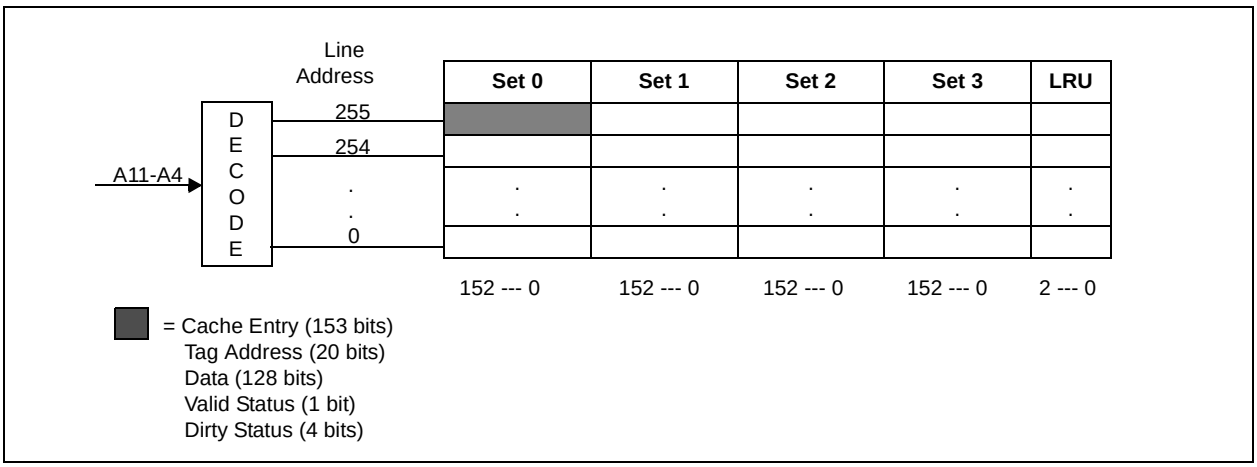

Figure 3-1 CPU Cache Architecture

Item #8

Table 4-10 Internal Bus Interface Unit Registers Internal Bus Interface Unit Registers

Bit	Name	Description
GX_BASE+8000h-8003h	**BC_DRAM_TOP Register (R/W)**	**Default Value = 3FFFFFFFh**
31:30	RSVD	**Reserved:** Set to 0.
29:17	TOP OF DRAM	**Top of DRAM:** Maximum value is FFFh.
16:0	1FFFF	**Granularity:** Must be set to 1FFFFh (128KB).
GX_BASE+8004h-8007h	**BC_XMAP_1 Register (R/W)**	**Default Value = 00000000h**
31:29	RSVD	**Reserved:** Set to 0.
28	GEB8	**Graphics Enable for B8 Region:** — Allow memory R/W operations for address range B8000h-BFFFFh be directed to the graphics pipeline: 0 = Disable; 1 = Enable. (Used for VGA emulation.)
27:24	B8	**B8 Region:** Region control field for address range B8000h-BFFFFh. **Note:** Refer to for decode.
23	RSVD	**Reserved:** Set to 0.
22	PRAE	**PCI Register Access Enable:** Allow PCI Slave to access internal registers on the X-Bus: 0 = Disable; 1 = Enable.
21	A20M	**Address Bit 20 Mask:** Address bit 20 is always forced to a zero except for SMI accesses: 0 = Disable; 1 = Enable.
20	GEB0	**Graphics Enable for B0 Region:** Allow memory R/W operations for address range B0000h-B7FFFh be directed to the graphics pipeline: 0 = Disable; 1 = Enable. (Used for VGA emulation.)
19:16	B0	**B0 Region:** Region control field for address range B0000h-B7FFFh. **Note:** Refer to for decode.
15	SMID	**SMID:** All I/O accesses for address range 3D0h-3DFh generate an SMI: 0 = Disable; 1 = Enable. (Used for VGA virtualization.)
14	SMIC	**SMIC:** All I/O accesses for address range 3C0h-3CFh generate an SMI: 0 = Disable; 1 = Enable. (Used for VGA virtualization.)
13	SMIB	**SMIB:** All I/O accesses for address range ***3B0h-3BFh*** generate an SMI: 0 = Disable; 1 = Enable (Used for VGA virtualization.)
12:8	RSVD	**Reserved** — Set to 0.
7	XPD	**X-Bus Pipeline Disable:** When cleared, the address for the next cycle can be driven on the internal X-Bus before the completion of the data phase of the current cycle.
6	GNWS	**X-Bus Graphics Pipe No Wait State:** Data driven on X-Bus from graphics pipeline: 0 = 1 full clock before X_DSX is asserted 1 = On the same clock in which X_RDY is asserted
5	XNWS	**X-Bus No Wait State:**— Data driven on X-Bus from Internal Bus Interface Unit: 0 = 1 full clock before X_DSX is asserted 1 = On the same clock in which X_RDY is asserted
4	GEA	**Graphics Enable for A Region:** Memory R/W operations for address range A0000h-AFFFFh are directed to the graphics pipeline: 0 = Disable; 1 = Enable. (Used for VGA emulation.)
3:0	A0	**A0 Region:** Region control field for address range A0000h-AFFFFh. **Note:** Refer to for decode.

Item #9

Table 4-10 Internal Bus Interface Unit Registers

Bit	Name	Description
GX_BASE+8008h-800Bh		**BC_XMAP_2 Register (R/W)** **Default Value = 00000000h**
31:28	DC	**DC Region:** Region control field for address range DC000h to DFFFFh.
27:24	D8	**D8 Region:** Region control field for address range D8000h to DBFFFh.
23:20	D4	**D4 Region:** Region control field for address range D4000h to D7FFFh.
19:16	D0	**D0 Region:** Region control field for address range D0000h to D3FFFh.
15:12	CC	**CC Region:** Region control field for address range CC000h to CFFFFh.
11:8	C8	**C8 Region:** Region control field for address range C8000h to CBFFF.
7:4	C4	**C4 Region:** Region control field for address range C4000h to C7FFFh.
3:0	C0	**C0 Region:** Region control field for address range C0000h to C3FFFh.
Note: Refer to Table 4-11 for decode.		
GX_BASE+800Ch-800Fh		**BC_XMAP_3 Register (R/W)** **Default Value = 00000000h**
31:28	FC	**FC Region:** Region control field for address range FC000h to FFFFFh.
27:24	F8	**F8 Region:** Region control field for address range F8000h to FBFFFh.
23:20	F4	**F4 Region:** Region control field for address range F4000h to F7FFFh.
19:16	F0	**F0 Region:** Region control field for address range F0000h to F3FFFh.
15:12	EC	**EC Region:** Region control field for address range EC000h to EFFFFh.
11:8	E8	**E8 Region:** Region control field for address range E8000h to EBFFFh.
7:4	E4	**E4 Region:** Region control field for address range E4000h to E7FFFh.
3:0	E0	**E0 Region:** Region control field for address range E0000h to E3FFFh.
Note: Refer to Table 4-11 for decode.		

Table 4-11 Region-Control-Field Bit Definitions

Bit Position	Function
3	**PCI Accessible:**— The PCI slave can access this memory if this bit is set high and if the appropriate Read or Write Enable bit is also set high.
2	**Cache Enable:** Caching this region of memory is inhibited if this bit is cleared.
1	**Write Enable:** Write operations to this region of memory are allowed if this bit is set high. If this bit is cleared, then write operations in this region are directed to the PCI master.
0	**Read Enable:** Read operations to this region of memory are allowed if this bit is set high. If this bit is cleared then read operations in this region are directed to the PCI master.
Note:	***If Cache Enable = 1 and Write Enable = 1, the Write Enable determination occurs after the data has passed the cache. Since the cache does write update, write data will change the cache if the address is cached. If a read then occurs to that address. the data will come from the written data that is in the cache even though the address is not writable. If this must be avoided then do not make the region cacheable.***

Item #10

Table 3-7 CR4-CR0 Bit Definitions

Bit	Name	Description
CR4 Register		
31:3	RSVD	**Reserved:** Set to 0 (always returns 0 when read).
2	TSC	**Time Stamp Counter Instruction:** If = 1 RDTSC instruction enabled for CPL = 0 only; reset state. If = 0 RDTSC instruction enabled for all CPL states.
1:0	RSVD	**Reserved** — Set to 0 (always returns 0 when read).
CR3 Register		
31:12	PDBR	**Page Directory Base Register:** Identifies page directory base address on a 4KB page boundary.
11:0	RSVD	**Reserved:** Set to 0.
CR2 Register		
31:0	PFLA	**Page Fault Linear Address:** With paging enabled and after a page fault, PFLA contains the linear address of the address that caused the page fault.
CR0 Register		
31	PG	**Paging Enable Bit:** If PG = 1 and protected mode is enabled (PE = 1), paging is enabled. After changing the state of PG, software must execute an unconditional branch instruction (e.g., JMP, CALL) to have the change take effect.
30	CD	**Cache Disable:** If CD = 1, no further cache line fills occur. However, data already present in the cache continues to be used if the requested address hits in the cache. Writes continue to update the cache and cache invalidations due to inquiry cycles occur normally. The cache must also be invalidated ***with a WBINVD instruction*** to completely disable any cache activity.
29	NW	**Not Write-Through:** If NW = 1, the on-chip cache operates in write-back mode. In write-back mode, writes are issued to the external bus only for a cache miss, a line replacement of a modified line, execution of a locked instruction, or a line eviction as the result of a flush cycle. If NW = 0, the on-chip cache operates in write-through mode. In write-through mode, all writes (including cache hits) are issued to the external bus. This bit cannot be changed if LOCK_NW = 1 in CCR2.
18	AM	**Alignment Check Mask:** If AM = 1, the AC bit in the EFLAGS register is unmasked and allowed to enable alignment check faults. Setting AM = 0 prevents AC faults from occurring.
16	WP	**Write Protect:** Protects read-only pages from supervisor write access. WP = 0 allows a read-only page to be written from privilege level 0-2. WP = 1 forces a fault on a write to a read-only page from any privilege level.
5	NE	**Numerics Exception:** NE = 1 to allow FPU exceptions to be handled by interrupt 16. NE = 0 if FPU exceptions are to be handled by external interrupts.
4	1	**Reserved:** Do not attempt to modify.
3	TS	**Task Switched:** Set whenever a task switch operation is performed. Execution of a floating point instruction with TS = 1 causes a DNA fault. If MP = 1 and TS = 1, a WAIT instruction also causes a DNA fault.
2	EM	**Emulate Processor Extension:** If EM = 1, all floating point instructions cause a DNA fault 7.
1	MP	**Monitor Processor Extension:** If MP = 1 and TS = 1, a WAIT instruction causes Device Not Available (DNA) fault 7. The TS bit is set to 1 on task switches by the CPU. Floating point instructions are not affected by the state of the MP bit. The MP bit should be set to one during normal operations.
0	PE	**Protected Mode Enable:** Enables the segment based protection mechanism. If PE = 1, protected mode is enabled. If PE = 0, the CPU operates in real mode and addresses are formed as in an 8086-style CPU. Refer to Section 3.13 "Protection" on page 97.

Item #10 (cont.)

4.1.4 L1 Cache Controller

The MediaGX processor contains an on-board 16KB unified data/instruction L1 cache. It operates in write-back mode. Since the memory controller is also on-board, the L1 cache requires no external logic to maintain coherency. All DMA cycles automatically snoop the L1 cache. For improved graphics performance, part of the L1 cache operates as a scratchpad RAM to be used by the graphics pipeline as a BLT Buffer.

The CD bit (Cache Disable, bit 30) in CR0 globally controls the operating mode of the L1 cache. LCD and LWT, Local Cache Disable and Local Write-through bits in the Translation Lookaside Buffer, control the mode on a page-by-page basis. Additionally, memory configuration control can specify certain memory regions as non-cacheable.

If the cache is disabled, no further cache line fills occur. However, data already present in the cache continues to be used. For the cache to be completely disabled, the cache must be invalidated with a WBINVD instruction after the cache has been disabled.

Write-back caching improves performance by relieving congestion on slower external buses. With four dirty bits, the cache marks dirty locations on a double-word basis. This further reduces the number of double-word bus write operations needed during a replacement or flush operation.

The MediaGX processor will cache SMM regions. This speeds up system management overhead to allow for hardware emulation such as VGA.

The cache of the MediaGX processor provides the ability to redefine 2KB, 3KB, or 4KB of the L1 cache to be scratchpad memory. The scratchpad area is memory mapped to the upper memory region defined by the GCR register (Index B8h). The valid bits for the scratchpad RAM will always be true and the scratchpad RAM locations will never be flushed to memory. The scratchpad RAM serves as a general purpose high speed RAM and as a BLT buffer for the graphics pipeline. Incrementing BLT buffer address registers have been added to enable the graphics pipeline to access this memory as a BLT buffer. A 16-byte line buffer dedicated to the graphics pipeline accesses has been added to minimize graphics interference with normal CPU operation.

Table 4-3 summarizes the registers contained in the L1 cache. These registers do not have default values and must be initialized before use. Table 4-4 gives the register/bit formats.

Table 4-3 L1 Cache BitBLT Register Summary

Mnemonic Name	Function
L1_BB0_BASE L1 Cache BitBLT 0 Base Address	Contains the address offset to the first byte of BLT Buffer 0 in the scratchpad memory.
L1_BB0_POINTER L1 Cache BitBLT 0 Pointer	Contains the address offset to the current line of BLT Buffer 0 in the scratchpad memory.
L1_BB1_BASE L1 Cache BitBLT 1 Base Address	Contains the offset to the first byte of BLT Buffer 1 in the scratchpad memory.
L1_BB1_POINTER L1 Cache BitBLT 1 Pointer	Contains the address offset to the current line of BLT Buffer 1 in the scratchpad memory.

Note: For information on accessing these registers, refer to Section 4.1.6 “CPU_READ/CPU_WRITE Instructions” on page 111.

Item #11

Table 3-11 Configuration Registers (cont.)

Bit	Name	Description
Index E8h		**CCR4 — Configuration Control Register 4 (R/W)** **Default Value = 85h**
7	CPUID	**Enable CPUID Instruction:** If = 1: The ID bit in the EFLAGS register to be modified and execution of the CPUID instruction occurs as documented in Table 9-2 "Instruction Fields" on page 234. If = 0: The ID bit can not be modified and execution of the CPUID instruction causes an invalid opcode exception.
6	SMI_NEST	**SMI Nest:** If = 1: SMI interrupts can occur during SMM mode. SMI handlers can optionally set SMI_NEST high to allow higher-priority SMI interrupts while handling the current event
5	***FPU_FAST_EN***	***FPU Fast Mode Enable:*** ***0 = Disable FPU Fast Mode*** ***1 = Enable FPU Fast Mode***
4	DTE_EN	**Directory Table Entry Cache:** If = 1: Enables directory table entry to be cached. Cleared to 0 at reset.
3	MEM_BYP	**Memory Read Bypassing:** If = 1: Enables memory read bypassing. Cleared to 0 at reset.
2:0	IORT(2:0)	**I/O Recovery Time**: Specifies the minimum number of bus clocks between I/O accesses: 000 = No clock delay 001 = 2-clock delay 010 = 4-clock delay 011 = 8-clock delay 100 = 16-clock delay 101 = 32-clock delay (default value after reset) 110 = 64-clock delay 111 = 128-clock delay Cleared to 0 at reset.
Note: MAPEN (CCR3[4]) must = 1 to read or write to this register.		
Index EBh		**CCR7 — Configuration Control Register 7 (R/W)** **Default Value = 00h**
7:3	RSVD	**Reserved:** Set to 0.
2	NMI	**Generate NMI:** ***0 = Do nothing*** ***1 = Generate NMI*** ***In order to generate multiple NMIs, this bit must be set to zero between each setting of 1.***
1	RSVD	**Reserved:** Set to 0.
0	EMMX	**Cyrix Extended MMX Instructions Enable:** If = 1: Cyrix extended MMX instructions are enabled