AMI 7300 MICROPROCESSOR
ELECTRICAL CHARACTERISTICS

4/10/73

MIR + RALU

0.0 MINIMUMS NOT SPECIFIED ARE 0 (ZERO)

0.0.1 All specifications, unless otherwise specified, are total values for both chips, and are specified over the total operating temperature range.

1.0 ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	-55°C to 150°C
Operating Temperature:	0°C to +70°C
Maximum Voltage on any Pin to Substrate:	+0.3 volts to -20 volts
Power Dissipation @ T = 0°C	1.9 watts

2.0 POWER SUPPLIES FOR BOTH CHIPS:

V_{CC}	+5.0 ± 5% volts
Ground	0.0 volts
V_{GG}	-12.0 ± 5% volts
I_{CC}	-170 mA maximum
I_{GG}	80 mA maximum

3.0 CLOCKS

3.1 CLOCK TIMING (SEE FIGURE 1)

Symbol	Name	MIN	MAX	Units
$V_{'0'}$	Logic '0'	-12 ± 5%		volts
$V_{'1'}$	Logic '1'	V_{CC}-1.0	V_{CC}+0.3	volts
V_{0V}	Logic '0' Overshoot to -20V	20		ns
t_{DL}	Deadtime @ -1V	70	*	ns
t_R, t_F	Rise, Fall Times Logic '1' to -10 V	10	150	ns
t_S	Time State duration	500		ns
t_W	Pulsewidth @ -10 V	350		ns
t_T	Period	1000	2500	ns

* No circuit design technique shall require a max t_{DL}

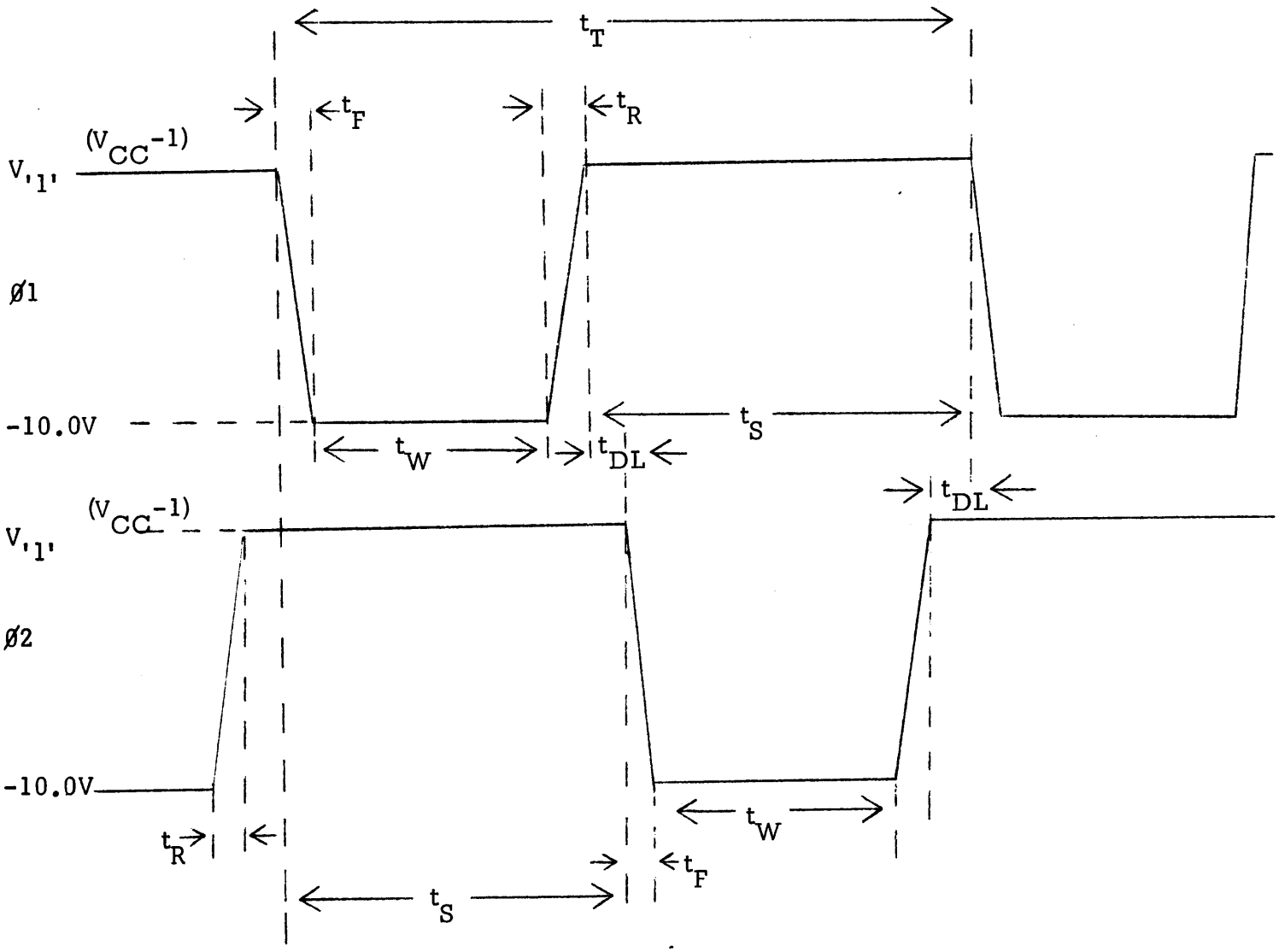


FIGURE 1: CLOCKS

3.2 CLOCK LOADING, BOTH CHIPS COMBINED

ø1:	C_L = 200 pF maximum 25 pF minimum	I = 1 mA DC max to Gnd
ø2:	C_L = 200 pF maximum 25 pF minimum	I = 1 mA DC max to Gnd
	C_{CK} = 25 pf maximum	I_{CK} = 0 mA DC

C_{CK} = Clock to clock capacitance

I_{CK} = Clock to clock current

4.0 INPUT LEVELS

4.1 CHIP TO CHIP SIGNALS (K, BC, CI, MBUS0 to MBUS10)

These signals are all driven from one chip to the other

	MIN	MAX	Units
$V_{'1'}$	V_{CC}-1.2	V_{CC}+0.3	volts
$V_{'0'}$	-10.0	+1.1	volts

4.2 TWO WAY LINES (DE0 - DE7)

When the DE lines are in the Input Mode, the required levels are:

	MIN	MAX	Units
$V_{'1'}$	V_{CC}-1.2	V_{CC}+0.3	volts
$V_{'0'}$	-10.0	+1.1	volts

4.3 I/O HANDSHAKE LINES (*I1, *I2, *I3, *RUN, *AK, & *DR)

	MIN	MAX	Units
$V_{'1'}$	V_{CC}-1.2	V_{CC}+0.3	volts
$V_{'0'}$	-10.0	+11	volts

4.4 RESET

	MIN	MAX	Units
$V_{'1'}$	V_{CC}-1.2	V_{CC}+0.3	volts
$V_{'0'}$	-10.0	+1.1	volts

4.4.1 RESET INPUT PULSEWIDTH

10.0 μsec minimum @ $V_{'0'}$

4.4.2 RESET PULSE RISE AND FALL TIMES

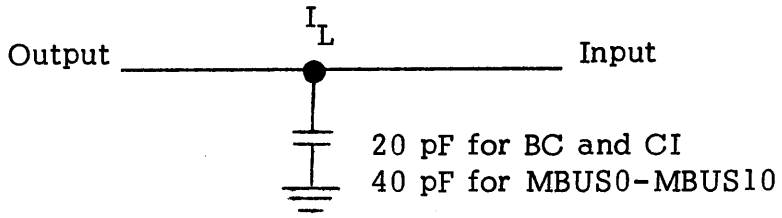
T_f = 1.0 μsec maximum from $V_{'0'}$ to $V_{'1'}$

T_r = not critical

5.0 OUTPUT DRIVE REQUIREMENTS

5.1 BC, CI, MBUS0 to MBUS10

5.1.1 MAXIMUM EXTERNAL LOAD



5.1.2 OUTPUT LEVELS

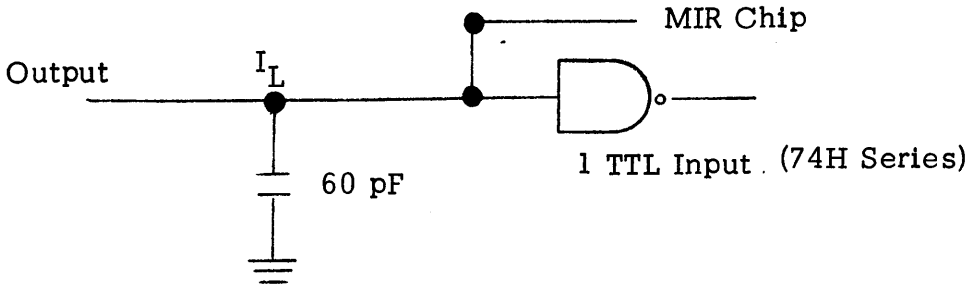
	MIN	MAX	Condition
$V_{'1'}$	V_{CC}-0.4V	V_{CC}+0.3V	I_L = -400 μa
$V_{'0'}$	0.0	+0.4	I_L = 300 μa

5.1.3 DELAY TIMES

(same as 5.2.3)

5.2 DATA EXCHANGE (DE0 - DE7)

5.2.1 MAXIMUM EXTERNAL LOAD



5.2.2 OUTPUT LEVELS

	MIN	MAX	Conditions
$V_{'1'}$	V_{CC}-0.4V	V_{CC}+0.3V	I_L= -400 μa
$V_{'0'}$	0.0	+0.6	I_L= 1.65 ma
$V_{'0'}$			
$V_{'0'}$			

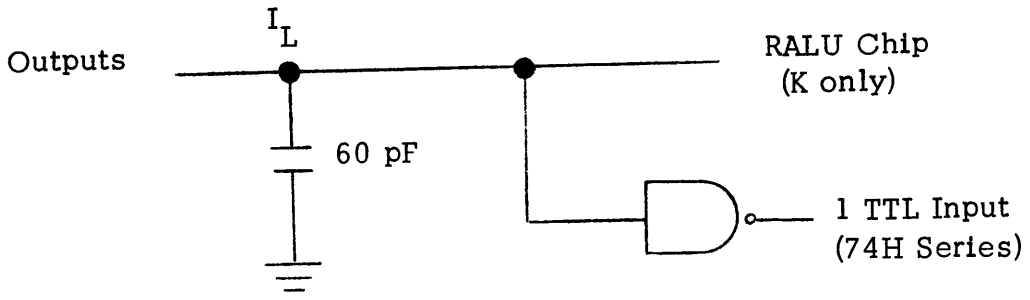
5.2.3 DELAY TIMES

Specified from 90% of negative going edge of Ø1 or Ø2:

750 ns maximum

5.4 I/O HANDSHAKE LINES (*FRUN, *SF, *DR, K)

5.4.1 MAXIMUM EXTERNAL LOADS



5.4.2 OUTPUT LEVELS

	MIN	MAX	Conditions
$V_{'1'}$	V_{CC}-0.4V	V_{CC}+0.3V	I_L = -400 μA
$V_{'0'}$	0.0V	+0.6V	I_L = 1.65 ma

5.4.3 DELAY TIMES

Specified from 90% of negative going edge of Ø1 or Ø2 450ns maximum

6.0 INPUT LEAKAGE

6.1 For the Tri-State Drivers (*SF, DE0 - DE7, MBUS0 - MBUS10) in the Tri-State mode and all other inputs except RESET

I_L = 10 μA maximum at V_{IN} = -5.25V

6.2 For the RESET input:

I_L = 25 μA maximum at V_{IN} = -17.85V

7.0 RESET INPUT CAPACITANCE (MIR CHIP):

10 pF maximum