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Am96/4016
AmZ8000 Evaluation Board

User's Manual

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Address comments concerning this manual to:

ADVANCED MICRO COMPUTERS
Publications Department
3340 Scott Boulevard
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PREFACE

This manual is written for people who are thoroughly versed in the use of microcomputers. Many sections will contain more information than you need, and we encourage you to use the table of contents as a guide for your reading.

The information in this manual is believed to be accurate and complete at the time it was printed. However, AMC reserves the right to change specifications without notice. No responsibility is assumed for errors that might appear in this manual. No part of this manual may be copied or reproduced in any form without prior written permission from AMC.

Publications related to this manual include:

AmZ8002 CPU Data Sheet
AmZ8000 Family Interface Manual
AmZ8000 Data Book
AmZ8001/2 Processor Instruction Set
Am96/4016-ASM Assembler Manual

TABLE OF CONTENTS

Appendixes

Figures

Tables

CHAPTER 1
INTRODUCTION

1-1. DESCRIPTION

The Am96/4016 Evaluation Board is a complete single-board microcomputer built around the new 16-bit AmZ8000 microprocessor. Used with a standard CRT or the low-cost keyboard/display console available as an option, it provides an excellent means of testing the advanced capabilities of this remarkably versatile CPU. Used with Advanced Micro Computer's new AmSYS 8/8 Development System, the entire AmZ8000 instruction set can be macroassembled to create very powerful programs for execution on the Evaluation Board.

The fully assembled and tested board has the following features:

Standard Features

- AmZ8002 CPU (non-segmented)
- 8 kilobytes of dynamic RAM, expandable off-board
- Up to 12 kilobytes of ROM or E-PROM, expandable off-board
- 4-kilobyte ROM Monitor, with breakpoint, single-step and up/down-load commands
- Buffered CPU bus available at edge of board
- Two programmable serial I/O ports (RS232C and 20mA)
- A programmable counter/timer channel associated with one serial port
- 24 programmable parallel I/O lines (three 8-bit ports)
- Fits in Multibus† or iSBC† card cage

†Trademarks of Intel Corporation

Optional Features

- One-pass Assembler in ROM
- Keyboard/Display console
- CRT terminal
- Universal prototyping board
- CPU-bus backplane (2 or 3 slots)
- Six-board card cage
- 64-kilobyte memory expansion
- Complete AmSYS 8/8 Development System, with diskette storage, interface utilities and PASCAL-like macroassembler for the AmZ8000 series

Programs can be entered and executed in either the stand-alone or Development System configuration. Specialized circuits or external expansion boards can also be attached in either mode. The entire CPU bus is buffered and brought to the edge of the board for interconnection, as are extra I/O ports for serial and parallel transfers on the data bus.

Figure 1-1 illustrates the board layout. The lower two edge connectors are physically compatible with the Multibus standard, although the P1 edge connector uses only power and ground in the standard Multibus card cage.

All four top edge connectors on the board are used for I/O. The P3 connector has 24 programmable lines divided into three 8-bit ports for data and handshaking. The P4 connector is also parallel but designed specifically for the optional keyboard/display console that can be attached to the Evaluation Board. The P5 and P6 connectors both carry programmable lines for asynchronous or synchronous serial data. The P5 connector also carries control I/O for an on-board programmable counter/timer channel.

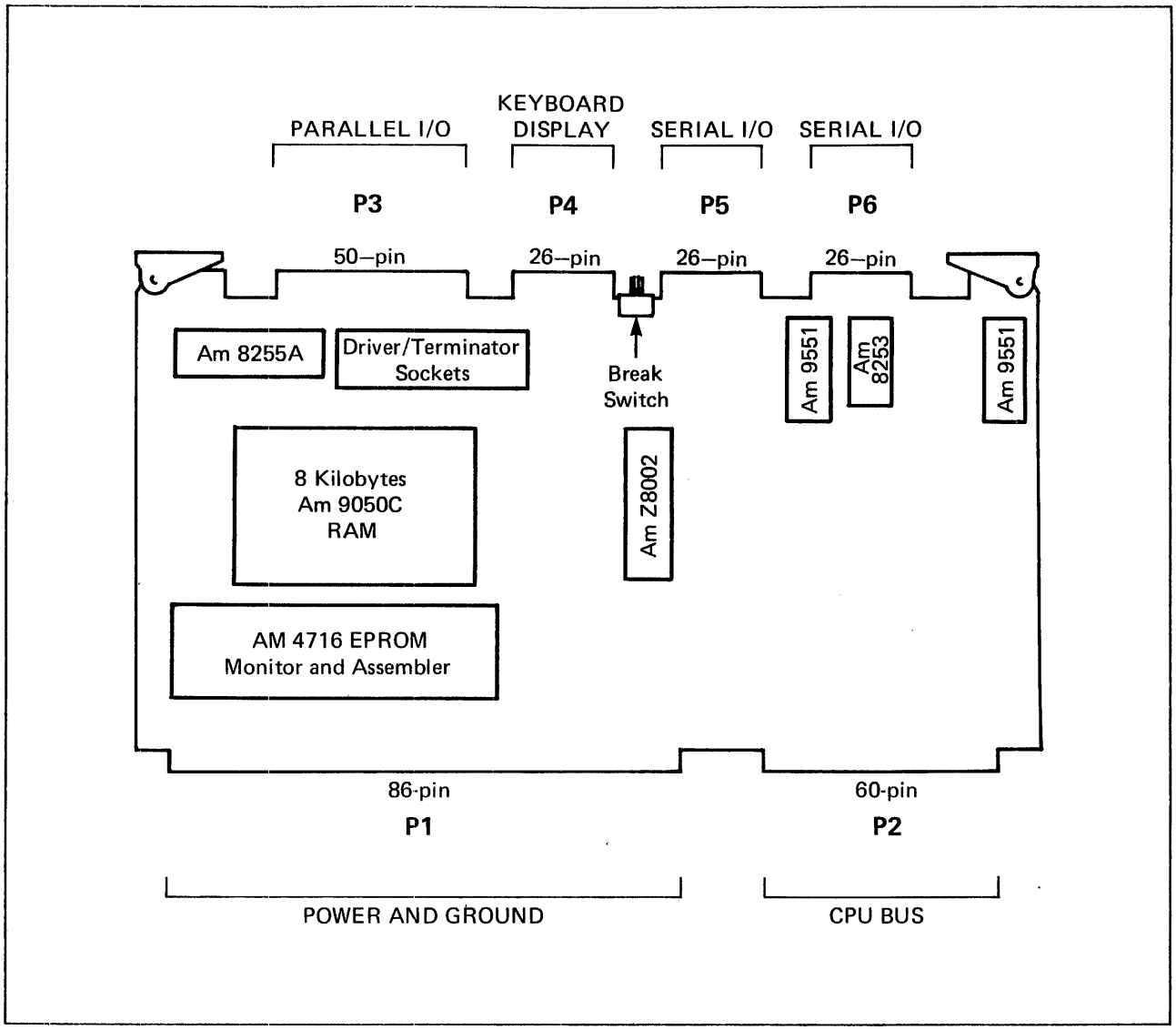


Figure 1-1. Board Layout

The AmZ8002 CPU is in the center of the board. At the upper right are the two Am9551 USARTs for serial I/O, surrounding the Am8253 counter/timer circuit which clocks them. The Am8255A parallel I/O circuit is in the upper left, next to six sockets for driver/terminators on the parallel port lines. Sixteen Am9050C dynamic RAM circuits provide the 8 kilobytes of user memory. The Monitor and optional Assembler programs are contained in six Am4716 E-PROMs.

Figure 1-2 shows a block diagram of the board. The system buses (address, data and control) emerge from the CPU and service all circuits, terminating at the P2. The address and data buses, which are multiplexed in the CPU, are separated into two separate 16-bit buses on the board. The diagram shows more clearly the difference between the P5 and P6 serial I/O ports; one has a counter/timer channel available and the other can be changed from RS232C to 20mA current-loop (TTY) interfacing.

Memory-expansion boards and prototyping boards carrying any AmZ8002-compatible circuits (such as DMAs or even multiple CPUs) can be attached at P2. Specialized circuits can also be attached at P3, P5 and P6. P5 is particularly useful for event-counting process control circuits or foreign host computers.

Figure 1-3 illustrates the range of standard plug-in configurations supported by the board's Monitor program. If attachments to the board are limited to any one or more of these three choices, application programming and execution can begin immediately without having to program the I/O circuits.

When the AmSYS 8/8 is attached for up/down loading of programs, the Development System's console can communicate with the Evaluation Board to control all functions.

The Development System contains a comprehensive set of hardware and software resources to fully utilize AmZ8000 capabilities. The system includes dual diskette drives, 64K bytes of RAM, serial and parallel ports, and a multimaster bus. Existing programming support includes a CPM-compatible operating system with linking loader, editor and debugger and a PASCAL-like AmZ8000 macroassembler, 8080 macroassembler and AmZ8000 translator. High-level languages, including PASCAL, are available. See the AmSYS 8/8 brochure for more details.

Table 1-1 gives a summary list of specifications for the Evaluation Board

1-2. THE CPU

The AmZ8002 microprocessor is a register-oriented CPU with exceedingly well organized minicomputer-like architecture. Sixteen general-purpose registers, each of them two-bytes (one 16-bit word) wide, are available to the user. Over 100 instructions, and 400 combinations of instructions, can be used to manipulate data between the CPU registers, memory and I/O.

The CPU can operate in two modes--system and normal--with separate relocatable stacks for each mode. This allows a distinction between privileged and protected instructions, as well as great flexibility in allocating the system's use of memory. In either mode, ten status conditions are continuously reported:

1. Internal operation
2. Instruction fetch, first word
3. Instruction fetch, subsequent word
4. Memory request, data
5. Memory request, stack
6. Memory refresh cycle
7. I/O cycle
8. Interrupt acknowledge, non-maskable
9. Interrupt acknowledge, non-vectored
10. Interrupt acknowledge, vectored

TABLE 1-1. SPECIFICATIONS

CPU	AmZ8002 (non-segmented)
Time Base	4MHz crystal oscillator
Serial I/O	Two RS232C serial ports with software-programmable baud rates. One port jumper-selectable for 20mA current-loop (TTY) operation.
Parallel I/O	24 parallel I/O lines (three 8-bit ports). Also provides interconnection to AmSYS 8/8 Development System.
RAM Memory	8K bytes of on-board dynamic memory; CPU refreshed (transparent).
ROM Space	12K bytes of ROM/EPROM space provided in six sockets; ROM monitor occupies two sockets.
Counter/Timer	Three 16-bit programmable interval counter; two counters used for serial I/O baud rate control; third counter available to user.
Power	-12VDC @ .085A, +12VDC @ .06A, +5VDC @ 1.65A (without optional keyboard/display console), or +5VDC @ 2.0A (with optional keyboard/display console).
Dimensions	12.0" (305 mm) x 6.75" (172 mm); MULTIBUS form factor with six edge connectors (P1 through P6).
Memory Addressing	ROM space: 0-2FFF(H) RAM space: 4000-5FFF(H)
Environmental Conditions	0 to 55°C ambient in free-air space with relative humidity to 90% without condensation.
Edge-of-Card Connectors	P1: 86-Pin for power, ground, and initialize. P2: 60-Pin CPU bus P3: 50-Pin parallel I/O for up/down-load from AmSYS 8/8 Development System. P4: 26-Pin interface for optional keyboard/display board. P5: 26-Pin RS232 and counter/timer interface. P6: 26-Pin RS232 or 20mA current loop for CRT or TTY console.
Monitor	4K ROM monitor included at addresses 0-0FFF(H)

Assembler	Optional ASCII, one-pass, line assembler in ROM
Up/Down-Load Capability	Can be plugged into AmSYS 8/8 Development System to provide up-load and down-load capability. Can also by used with other computer systems to execute AmZ8000 code.
Optional Keyboard/ Display	56-key keyboard with 20-character alphanumeric LED display. Same physical form as Am96/4016 Evaluation Board with attaching standoff connectors and interconnection ribbon cable.

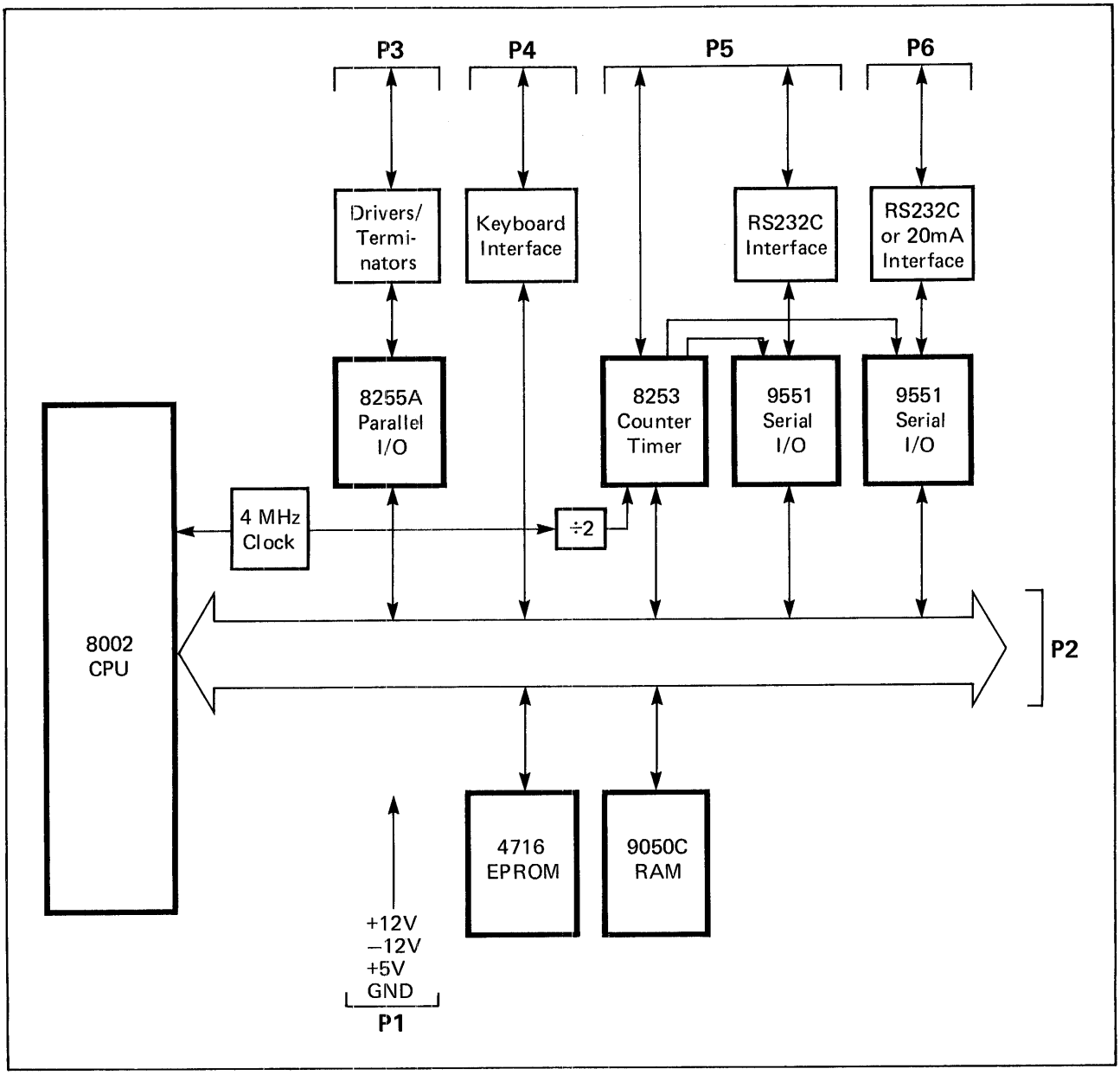


Figure 1-2. Block Diagram

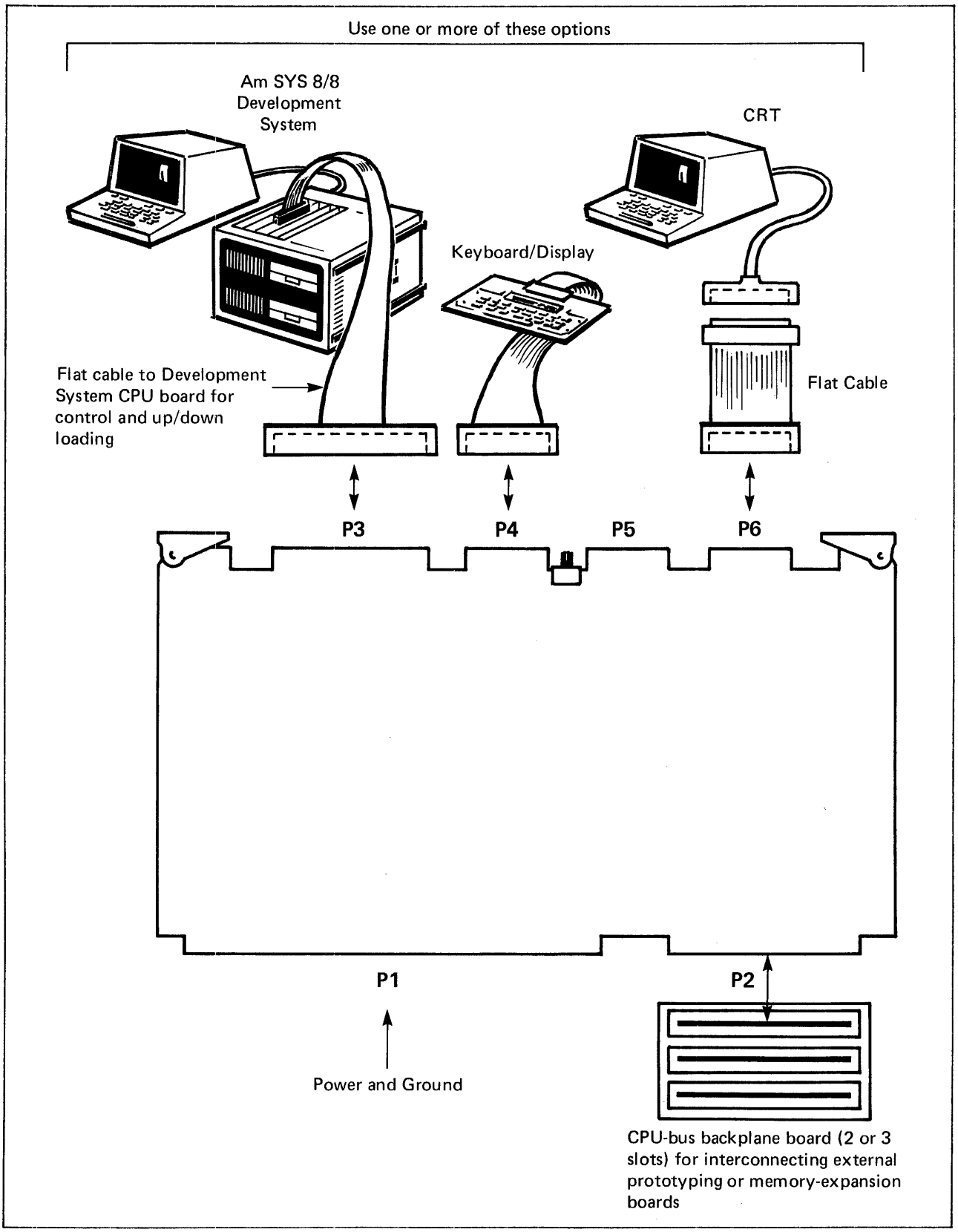


Figure 1-3. Standard Configurations

Only three of these status outputs (2, 6 and 7) are needed by the Evaluation Board's internal functions, but all are available at the P2 edge connector.

The interrupt and trap structure is particularly powerful, with very fast response to external devices and illegal conditions.

Special instructions and hardware features support multiprogramming and multiprocessing. In an asynchronous chain of CPUs, critical resources can be shared without sacrificing throughput.

1-3. MEMORY

The Evaluation Board's dynamic RAM is refreshed by the CPU. Additional memory, either dynamic or static, can be added off-board through the P2 edge connector. AMC will supply a 64-kilobyte memory-expansion board for this purpose which has self-contained refreshing. There is a provision for substituting off-board memory during accesses to the on-board memory's address space.

Depending on your use of CPU functions, a very large amount of memory can be used. The CPU's 16 address lines can directly access 64 kilobytes. However, if the various distinctions between operating mode (system and normal) and memory-access status (instruction, data and stack) are used to differentiate memory resources, up to 384 kilobytes can be addressed as illustrated in figure 1-4.

1-4. INPUT/OUTPUT

Memory space and I/O space are differentiated by a memory-request line and other status outputs from the CPU. The CPU can use 16-bit I/O port addresses, allowing up to 64K ports, although in the Evaluation board implementation the upper four address bits are not decoded and often the lower one or two address bits are used for sub-addressing within peripheral circuits.

The Evaluation Board also implements only 8-bit I/O transfers on the four top edge connectors (P3 through P6). These are the lower 8 bits on the data bus.

The 24 parallel I/O lines of the Am8255A circuit at P3 can be configured to transfer data in a variety of ways, with or without handshaking. In the standard configuration, this edge connector is used for up/down loading between the AmSYS 8/8 Development System and the Evaluation Board. The circuit has a bit set/reset function that increases the efficiency of handshake software. The sockets provided for driver or terminator circuits allow further characterization of these ports for special applications. Ground lines are interleaved with signal lines for better noise immunity at this edge connector.

The two Am9551 USART (universal synchronous/asynchronous receiver/transmitter) circuits attached to the P5 and P6 edge connectors can be programmed for a broad range of full-duplex, doubly-buffered communication protocols, with many automatic overhead features. The baud rate is controlled by two of the three programmable channels in the Am8253 counter/timer circuit.

As mentioned above, no programming of I/O circuits is necessary when the Evaluation Board is used in one of the standard configurations illustrated in figure 1-3. The Monitor program will initialize these circuits for you.

1-5. SOFTWARE

The Evaluation Board's ROM-based Monitor program provides complete system-initialization functions and over two dozen user commands for access to CPU registers and memory. It features breakpoint, single-step and trace functions, as well as up-load and down-load functions for use with the AmSYS 8/8 Development System. Any AmZ8000 instruction whether privileged (system mode) or protected (normal mode) can be entered in hex format using only the Monitor.

The optional ROM-based mnemonic Assembler simplifies instruction entry. Most of the full AmZ8000 instruction set can be used with this one-pass line-by-line Assembler, which also supports forward symbolic references. It is an excellent tool for gaining a feel of AmZ8000 instructions without the need for a complete macroassembler, which is available on the AmSYS 8/8.

The full CPU instruction set can be used to create very powerful application programs. The 110 basic instructions have permutations around operand addressing modes, plus autoincrement and autodecrement facilities. Code written for the AmZ8002 is source-compatible with the AmZ8001 microprocessor

Most instructions are between one and three 16-bit words in length. Instructions and hardware are available to operate on bits, 4-bit digits (BCD), 8-bit bytes, 16-bit words, 32-bit long words, 64-bit quad words, byte strings and word strings.

String instructions are auto-incrementing or auto-decrementing block transfers. The strings can be up to 64 kilobytes in length, the entire directly-addressable memory, and the transfers are interruptible. It is this facility that gives the CPU an intrinsic DMA capability.

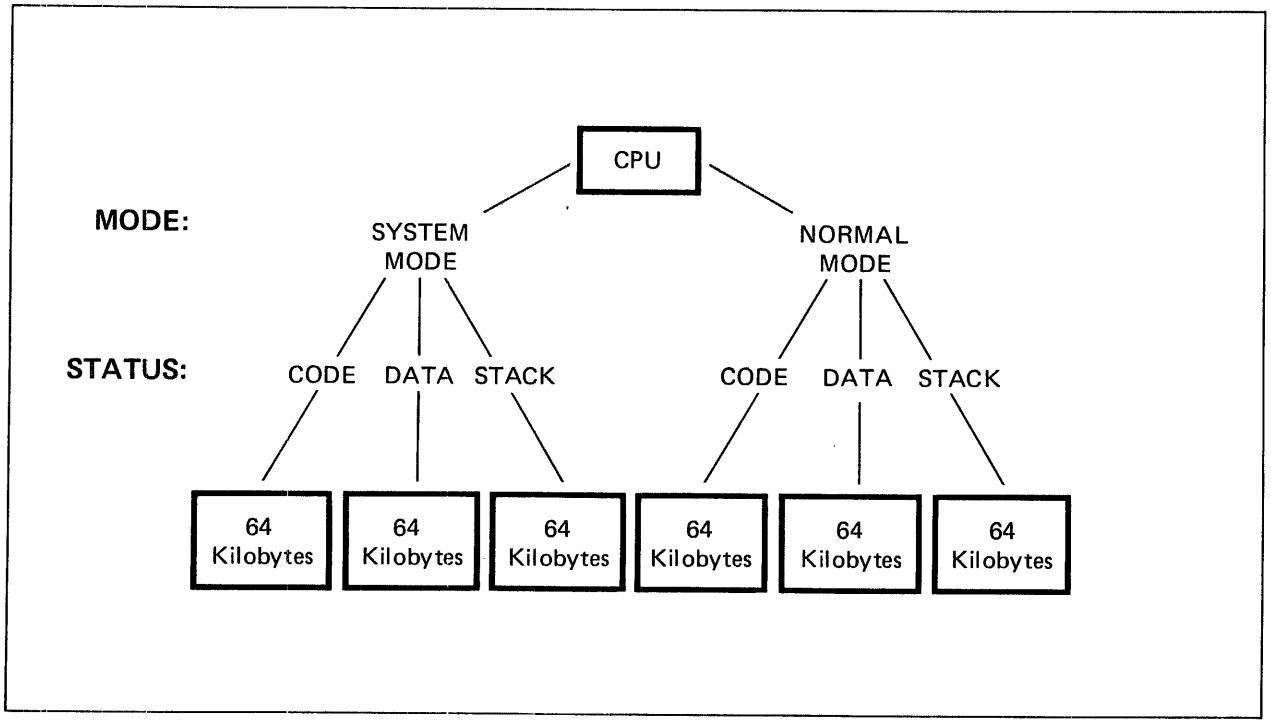


Figure 1-4. Memory-Addressing Potential

CHAPTER 2
HARDWARE INSTALLATION AND INTERFACING

2-1. UNPACKING AND INSPECTION

Upon receipt of this equipment, inspect both the equipment and the shipping carton immediately for evidence of damage during transit. If the shipping carton is damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, save the carton and packing material for the agent's inspection. Shipping damages should be reported immediately to the carrier. Do not attempt to service the board yourself as this will void the warranty.

2-2. SYMBOLS

A special symbolism is used in this and subsequent sections to denote active-low signal levels. An asterisk (*) following a signal name, rather than a bar over the name, means that the signal is active-low (negative-true). For example, WAIT* is active when its voltage potential is low.

2-3. INSTALLATION OVERVIEW

Figure 2-1 illustrates the hardware connectors and sockets that may require setup before the board can be used. These are the six edge connectors, P1 through P6, plus sockets for ROM or E-PROM and the sockets for parallel-I/O driver or terminator circuits. Each of these groups is discussed individually below.

NOTE

When one of the standard configurations illustrated in Figure 1-3 has been ordered from AMC, only the following installation connections need be considered:

Edge Connection	External Connection
P3	AmSYS 8/8 Development System CPU board (P3), as illustrated in figure 2-2.
P4	Keyboard/LED Display Board (Am96/4016-KBD), as illustrated in figure 2-3.
P6	CRT or other RS232C terminal.

2-4. ROM/E-PROM SOCKETS

The board contains six sockets for fixed-address ROM or E-PROM. All boards are shipped with at least two E-PROMs installed, which contain the 4-kilobyte Monitor program. If you ordered the optional line-by-line 8-kilobyte Assembler, the remaining four E-PROM sockets will also be filled. Table 2-1 is therefore only advisory and will not require installation of additional ICs unless you intend to alter the use of ROM space or install the Assembler circuits later.

2-5. PARALLEL I/O DRIVER/TERMINATORS

When the board is ordered, the driver and terminator circuits listed in table 2-2 are provided.

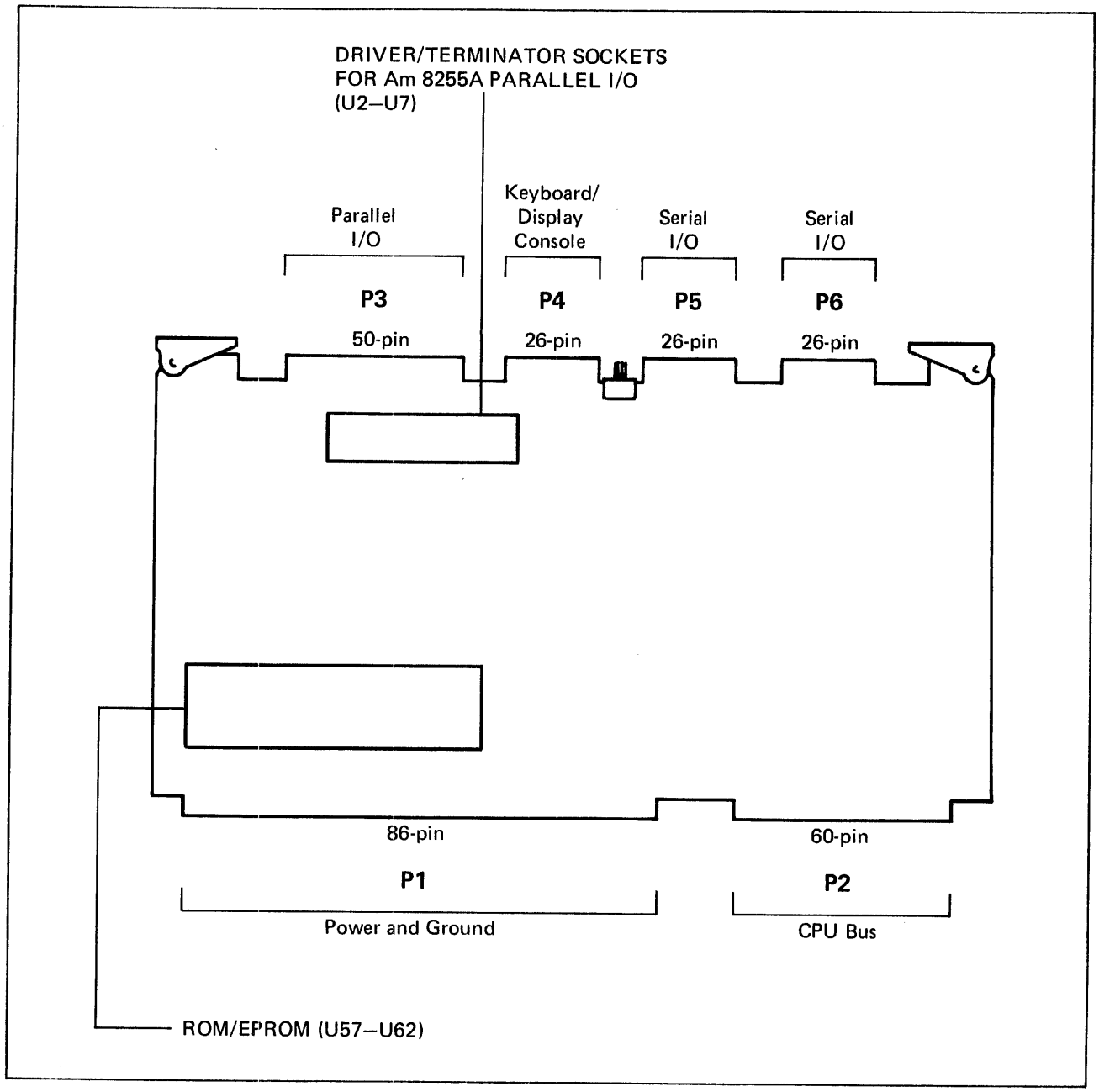


Figure 2-1. Edge Connectors and IC Sockets

TABLE 2-1. ROM/EPROM ADDRESSES AND SOCKETS

Program	Addresses	Socket #
Monitor	0 - 0FFF (even) 0 - 0FFF (odd)	U57 U60
Assembler	1000 - 1FFF (even) 1000 - 1FFF (odd) 2000 - 2FFF (even) 2000 - 2FFF (odd)	U58 U61 U59 U62

TABLE 2-2. DRIVER/TERMINATORS FOR PARALLEL PORT

Device	Function	Socket #
74LS37	Driver	U2
74LS37	Driver	U3
74LS37	Driver	U4
iSBC902	Terminator	U5
iSBC902	Terminator	U6
iSBC902	Terminator	U7

TABLE 2-3. OTHER DRIVER/TERMINATOR CIRCUITS FOR P3

Drivers	Terminators
7438,74LS38	Intel iSBC 901
7437,74LS37	Intel iSBC 902
7432,74LS32	National BLC 901
7426,74LS26	National BLC 902
7409,74LS09	National BLC 903
7408,74LS08	
7403,74LS03	
7400,74LS00	

Non-standard uses of the P3 edge connector may require different devices for these sockets. Some of the possible devices are listed in table 2-3. Alternatively, the sockets can be jumpered for direct connection to the Am8255A pins.

2-6. EDGE CONNECTORS

A minimum of two edge connectors must be used to operate the board. Power (+12V, -12V, +5V) and ground must be supplied through the P1 connector. A system console must also be connected on one of the remaining connectors: either P4 for the AMC-supplied keyboard/display console or P6 for a user-supplied terminal.

Many additions to these required connections are possible, as indicated in the list of edge-connector characteristics and applications below. This list is normally not needed if you are installing a standard configuration illustrated in figure 1-3.

Note that connectors P1 and P2 have their odd-numbered pins on the component side of the board, whereas the remaining connectors have them on the solder side. The abbreviation N/C in the pin-connection lists means no connection.

P1 - an 86-pin connector physically (but not electrically) compatible to the Multibus and iSBC-80 formats. It is used only for power and ground, except that pin 14 can be used for external initializing (reset) when jumpered for this function (see figure 2-4). The pin connections are shown in table 2-4.

P2 - a 60-pin connector physically compatible with the Multibus and iSBC-80 formats. It carries buffered signals from all CPU lines except +5V, which is on the P1 connector, and DECOUPLE which is not used on the AmZ8002. The address/data bus from the CPU is demultiplexed into separate address and data buses. The CPU's RESET* line is connected directly to the RST* line on P2, although RST* also resets the Am9551 USARTs and the Am8255A PIO. One additional line, INH* is used to control addressing of on/off-board memory.

This connector is used to interface a prototyping board and/or external memory boards. An optional backplane is available for this purpose.

If the CPU is disabled via the BUSRQ* input, an off-board device can take control over most of the signals on this connector to access memory and peripherals on the Evaluation Board. The pin connections are shown in table 2-5.

P3 - a 50-pin connector to the six driver/terminator sockets of the Am8255A parallel I/O circuit. The 24 active lines are divided into three 8-bit ports (addresses FF0, FF1 and FF2, where the upper four address bits are not decoded). Each port can be programmed independently for input or output to match the functions of the driver or terminator ICs that you insert in sockets U2 through U7.

TABLE 2-4. P1 CONNECTOR PINS

Component Side	Solder Side
1 GND	2 GND
3 +5V	4 +5V
5 +5V	6 +5V
7 +12V	8 +12V
9 N/C	10 N/C
11 GND	12 GND
13 N/C	14 INIT*
15 N/C	16 N/C
. .	. .
. .	. .
. .	. .
73 N/C	74 N/C
75 GND	76 GND
77 N/C	78 N/C
79 -12V	80 -12V
81 +5V	82 +5V
83 +5V	84 +5V
85 GND	86 GND

TABLE 2-5. P2 CONNECTOR PINS

Component Side	Solder Side
1 GND	2 GND
3 N/C	4 N/C
5 VI*	6 NVI*
7 N/C	8 INH*
9 AS*	10 DS*
11 R/W*	12 MREQ*
13 N/S*	14 B/W*
15 BUSRQ*	16 BUSAK*
17 MI*	18 MO*
19 RST*	20 WAIT*
21 PHI (clock)	22 STOP*
23 NMI*	24 N/C
25 ST0	26 ST1
27 ST2	28 ST3
29 A0	30 A1
31 A2	32 A3
33 A4	34 A5
35 A6	36 A7
37 A8	38 A9
39 A10	40 A11
41 A12	42 A13
43 A14	44 A15
45 D0	46 D1
47 D2	48 D3
49 D4	50 D5
51 D6	52 D7
53 D8	54 D9
55 D10	56 D11
57 D12	58 D13
59 D14	60 D15

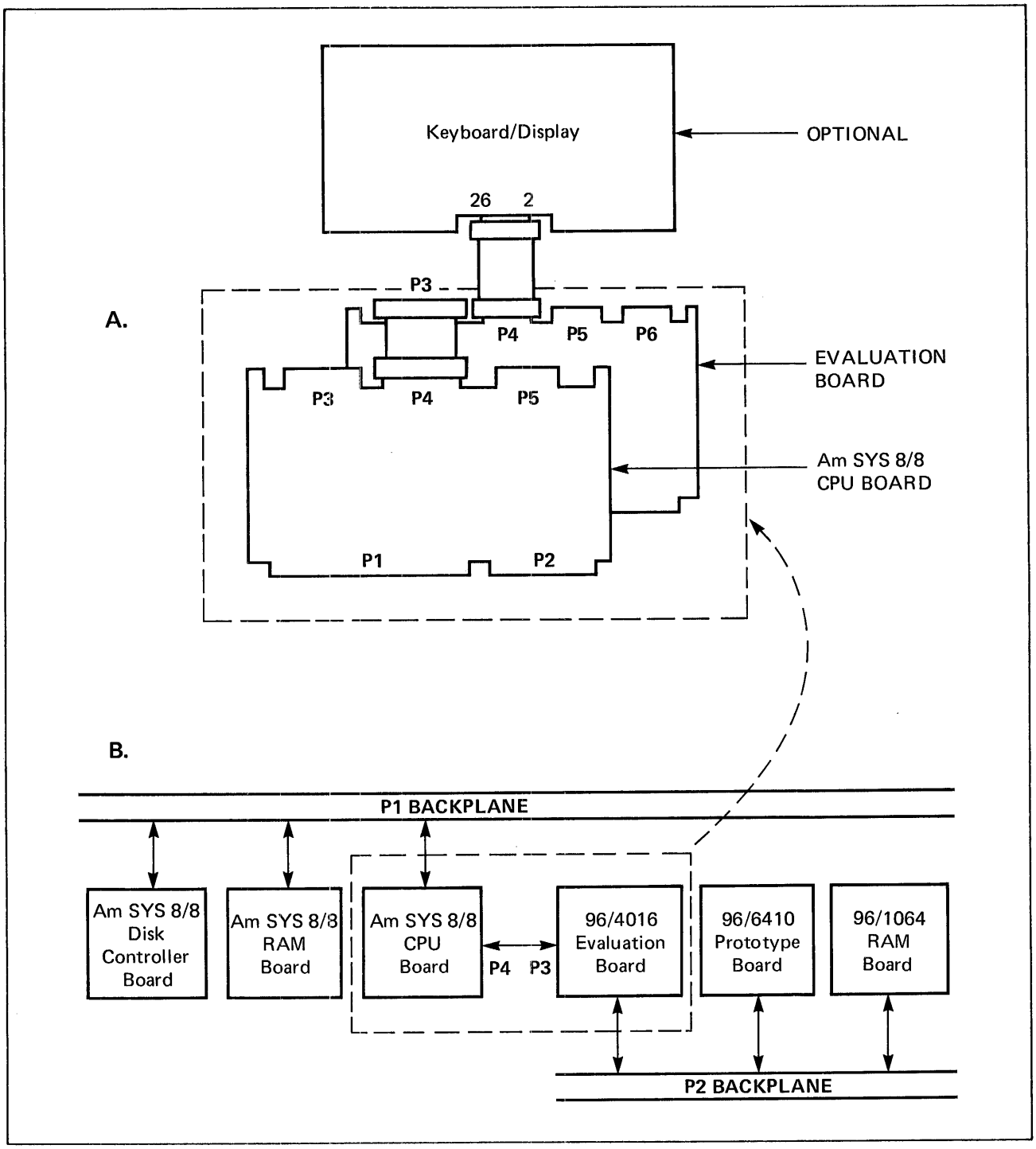


Figure 2-2. Connecting to the AmSYS 8/8

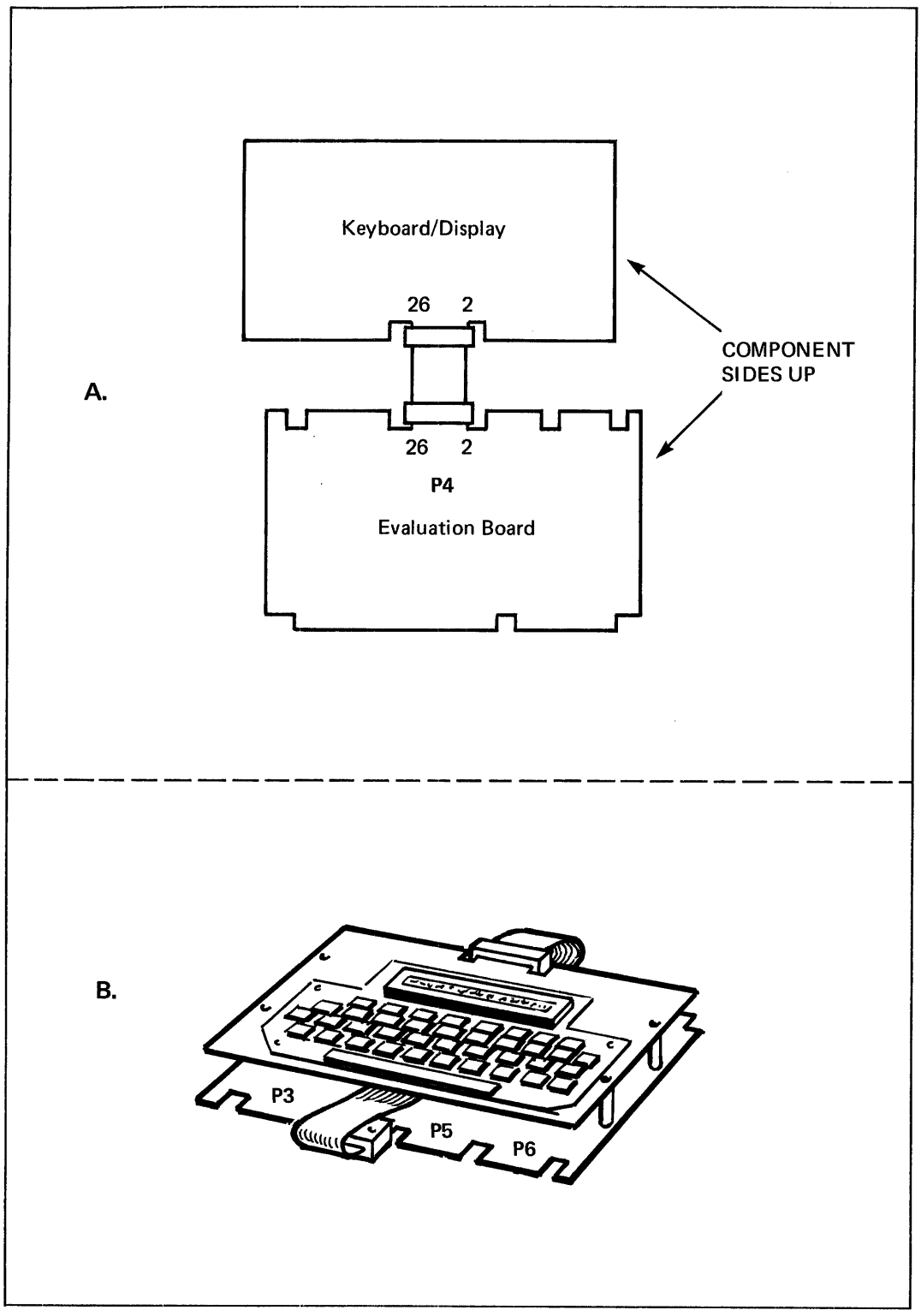


Figure 2-3. Connecting the Keyboard/Display Console

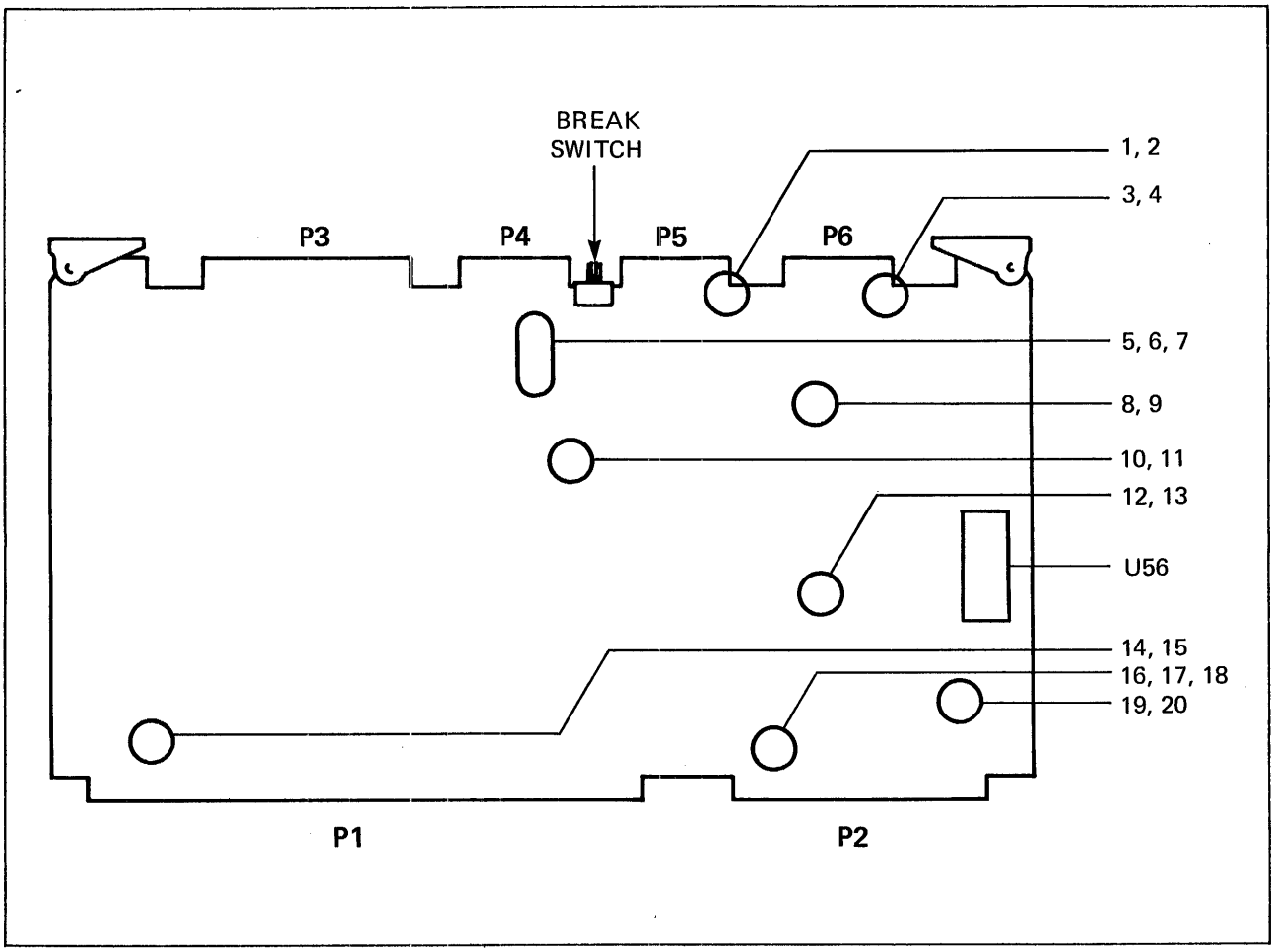


Figure 2-4. Jumper Option

When the AmSYS 8/8 Development System is used, P3 of the Evaluation Board is connected to P4 of the Development System's CPU board (Am95/4005) for up/down loading and control from the Development System's console. This is illustrated in figure 2-2b.

The pin connections are shown in table 2-6. See the Am8255A Data Sheet for more details.

P4 - 26-pin connector used to attach the optional keyboard/display console (Am96/4016-KBD), or for general-purpose parallel I/O.

The cable-connection method for the keyboard/display console is illustrated in figure 2-3.

The pin connections listed in table 2-7 include keyboard return and scan lines (R0-R2, S0-S2) and port addresses for LED characters (Ports FC0 through FD0).

P5 - 26-pin connector to the RS232C interface of one of the two Am9551 serial I/O circuits, plus three pins connected to channel 0 of the Am8253 counter/timer circuit.

This connector can be used for time-controlled serial I/O (e.g., process controllers), a host computer other than the AmSYS 8/8 Development System, or any other RS232C serial device.

The I/O port address for data through this connector is FEF or FED (they are equivalent).

The pin connections are given in table 2-8. Parenthesized numbers are the corresponding EIA pin numbers for RS232C. See the Am9551 and Am8253 Data Sheets for more details.

P6 - 26-pin connector to the RS232C or 20mA current-loop (TTY) interface of one of the two Am9551 serial I/O circuits.

The RS232C interface is factory-set. To obtain a 20mA current-loop interface, turn the jumper at U56 180 degrees (see figure 2-4), and reprogram for baud rate.

This connector can be used for a system console (terminal) or any other serial I/O device. When using an RS232 type CRT Terminal, it is usually necessary to connect the Clear To Send signal to the Request To Send signal. This connection can sometimes be made on the CRT Terminal. Alternatively, the Clear To Send line can be grounded on the Evaluation board by removing the jumper between U56 pins 3 and 14 and connecting an insulated jumper between U56 pins 3 and 6.

The I/O port address for data through this connector is FEB or FE9 (they are equivalent).

The pin connections are given in table 2-9. Parenthesized numbers are the corresponding EIA pin numbers for RS232C. See the Am9551 Data Sheet for more details.

TABLE 2-6. P3 CONNECTOR PINS

Solder Side	Component Side
1 PB7 (Port FF1)	2 GND
3 PB6	4 GND
5 PB5	6 GND
7 PB4	8 GND
9 PB3	10 GND
11 PB2	12 GND
13 PB1	14 GND
15 PB0	16 GND
17 PC3 (Port FF2)	18 GND
19 PC2	20 GND
21 PC1	22 GND
23 PC0	24 GND
25 PC4	26 GND
27 PC5	28 GND
29 PC6	30 GND
31 PC7	32 GND
33 PA7 (Port FF0)	34 GND
35 PA6	36 GND
37 PA5	38 GND
39 PA4	40 GND
41 PA3	42 GND
43 PA2	44 GND
45 PA1	46 GND
47 PA0	48 GND
49 N/C	50 GND

TABLE 2-7. P4 CONNECTOR PINS

Solder Side	Component Side
1 GND	2 KEYBOARD DETECT
3 CTL	4 SHIFT
5 R0	6 R1
7 R2	8 S0
9 S1	10 S2
11 PFC0*	12 PFC4*
13 PFC8*	14 PFCC*
15 PFD0*	16 A0
17 A1	18 ID0
19 ID1	20 ID2
21 ID3	22 ID4
23 ID5	24 ID6
25 GND	26 +5V

TABLE 2-8. P5 CONNECTOR PINS

Solder Side (RS232)	Component Side (RS232)
1 CHASSIS GND	2 N/C
3 TRANSMITTED DATA (2)	4 N/C
5 RECEIVED DATA (3)	6 N/C
7 REQUEST TO SEND (4)	8 N/C
9 CLEAR TO SEND (5)	10 N/C
11 DATA SET READY (6)	12 N/C
13 SIGNAL GND (7)	14 DATA TERM RDY (20)
15 N/C	16 N/C
17 N/C	18 N/C
19 N/C	20 N/C
21 N/C	22 N/C
23 CLK0	24 GATE0
25 OUT0	26 SIGNAL GND

TABLE 2-9. P6 CONNECTOR PINS

Solder Side		(RS232)	Component Side		(RS232)
1	CHASSIS GND	(1)	2	N/C	
3	TRANSMITTED DATA	(2)	4	N/C	
5	RECEIVED DATA	(3)	6	TTY RDR CONTROL	(16)
7	REQUEST TO SEND	(4)	8	N/C	
9	CLEAR TO SEND	(5)	10	N/C	
11	DATA SET READY	(6)	12	N/C	
13	SIGNAL GND	(7)	14	DATA TERM RDY	(20)
15	DATA CARRIER RTN	(8)	16	TTY RDR CONTROL RTN	(21)
17	N/C		18	N/C	
19	N/C		20	N/C	
21	N/C		22	TTY RX TRN	(24)
23	TTY RX	(12)	24	TTY TX RN	(25)
25	TTY TX	(13)	26	SIGNAL GND	

2-7. KEYBOARD/DISPLAY INSTALLATION

When using the optional keyboard/display console, the following installation method should be used.

Orient the Evaluation Board and the keyboard/display board so that their component sides are facing up and the P4 connector of the Evaluation Board faces the only edge connector of the keyboard/display board. Place the flat cable between the two connectors so that the even pins of the Evaluation Board connect to the even pins of the keyboard/display board, as shown in figure 2-3a. Fold the cable between the boards so that the board spacers lock into the holes on the boards, as shown in figure 2-3b. Both boards will then have their component sides facing down.

2-8. PROTOTYPING AND MEMORY-EXPANSION BOARDS

Prototyping and memory-expansion boards can be connected to the CPU bus via P2. AMC offers the following optional products to accomodate these functions:

- Universal Prototyping Board for Multibus (Am96/9410)
- 64-kilobyte dynamic RAM board for standard Multibus and Evaluation Board (Am96/1064).
- Two- and three-board backplane for P2 edge connector (Am96/4016-2S and Am96/4016-3S)
- Six-board Multibus-compatible card cage with cooling fan (Am95/6440). A card cage with power supplies is also available (Am95/6448)

Prototyping boards can contain any type of circuitry, including circuits that capture the system buses. The AmZ8002 bus is described further in the section entitled Principles of Operations.

Expansion memory can be of any type compatible with the available pins and the buffered electrical characteristics at P2 (see appendix A). Dynamic-memory refresh may be done on the external board or it may use the CPU refresh cycle, as does the on-board RAM.

The 64K RAM board supplied by AMC is compatible with both the Evaluation Board (through P2) and with standard Multibus slave applications (through P1). In either configuration, only one of the two Multibus edge connectors is enabled. Due to this dual use, dynamic refresh is handled on the memory board itself rather than relying on the AmZ8002. The P2 connector of the memory board supports 16 address bits whereas its P1 connector supports 20 bits.

2-9. AmSYS 8/8 INTERCONNECTION

When an AmSYS 8/8 Development System is used, P3 of the Evaluation Board is connected to P4 of the Development System's CPU board as illustrated in figure 2-2. A cable (Am96/4016-PCBL) for connecting P3 to P4 is available from AMC. Alternatively, a cable can be fabricated by using two Scotchflex card edge connectors (3M part #3415-0001) and one foot of Scotchflex flat cable (3M part #3306/50).

A diskette-based program named HOST is supplied with the Development System for communication between the Development System and the Evaluation Board. Execution of this utility on the Development System allows Evaluation Board operations to be controled through the Development-system console. However, if the Am96/4016-KBD keyboard/display console is attached, it takes priority over all other consoles as the monitor console.

The Development System can be used for programming work simultaneously with execution of programs on the Evaluation Board. The P1 but serves the AmSYS 8/8 while the P2 bus serves the Evaluation Board. In this case, separate consoles may be needed. However, communication or transfers between the Evaluation Board and the Development System require the HOST program to be in execution.

2-10. JUMPER OPTIONS

Several jumpers, illustrated in figure 2-4, can be connected to modify the standard functions of the Evaluation Board. There is a Break switch for regaining CPU control, two jumpers for grounding external I/O devices to the board, one for timing an external device, one for selecting RS232C or TTY serial interface, one for enabling an initialization line, one for enabling an inhibit line, and one for disabling the memory-cycle Wait state.

All jumpers are unconnected when the board is shipped; the jumpers (12, 13) associated with the Break switch are connected, but the Break switch itself is normally open. Wire-wrapping between the jumper posts will affect the board's functions as described below.

BREAK SWITCH - When pressed, it asynchronously generates a non-maskable interrupt (NMI*) to the CPU, which forces control back to the Monitor program. This circuit is connected via a trace between jumpers 12 and 13. If the NMI* line on P2 is to be used, the Break switch must be disabled by cutting the trace connecting jumpers 12 and 13. The wire-wrap pins at 12 and 13 can be used to reconnect the Break switch at a later time.

Jumper 1,2 - When jumpered, it connects the chassis ground of the external serial I/O device at P5 to the Evaluation-Board ground.

Jumper 3,4 - When jumpered, it connects the chassis ground of the external serial I/O device at P6 to the Evaluation-Board ground.

Jumper 5,6,7 - Used by the Monitor to determine baud rate at P6 as follows:

ALL OPEN

9600 baud - all open
2400 baud - connect 6 to 5
300 baud - connect 7 to 5
110 baud - connect 6 to 5 and 7 to 5

Jumper 8,9 - When jumpered, it connects the 2MHz clock (4MHz ÷ 2) to counter 0 of the Am8253 counter/timer circuit, which is available externally through P5.

Jumper 10,11 - When jumpered, it connects the OUTØ output of the Am8253 at P5 to the NVI* line, thereby generating periodic non-vectored interrupts. OPEN

Jumper 12,13 - These jumpers are factory-connected by a trace to enable the Break switch. If NMI* is used at P2, the trace must be cut. The jumpers can be reconnected later by wire wrapping.

Jumper U56 - Unplugging and rotating this jumper 180 degrees changes the P6 interface from RS232C to 20mA current loop (TTY). The Am9551 must be reprogrammed for baud rate if 20mA is used.

Jumper 14,15 - When jumpered, it enables pin 14 on the P1 Multibus connector to be an INIT* input. When the INIT* line is low, it resets the CPU, USARTs and parallel I/O circuit.

INSTALLED

Jumper 16,17,18 - When jumpered 16-to-17, the INH* line on the P2 connector becomes an active-low output whenever on-board memory space (0000-5FFF) is addressed, thereby disabling off-board memory. When jumpered 17-to-18, the INH* line becomes an input for all memory accesses, thereby disabling on-board memory when the line is low.

Jumper 19,20 - When jumpered, it disables the Wait cycle normally inserted between the T2 and T3 cycles of on-board memory cycles.

CHAPTER 3
OPERATION WITH THE MONITOR

3-1. OVERVIEW OF OPERATIONS

When the Evaluation Board is powered up, the ROM-based Monitor program initailizes the standard board configurations illustrated in figure 1-3. It then displays an asterisk (*) prompt.

Immediately thereafter, any Monitor command described in the following pages can be entered, including the commands that invoke the Assembler or up/down-loads from the AmSYS 8/8 Development System.

The Monitor will communicate with any console in the standard configuration (figure 1-3), although precedence is always given to the keyboard/display console attached at the P4 edge connector whenever it is present. If the AmSYS 8/8 Development System is attached to P3, the Monitor will also communicate with its console if the HOST program is running on the Development System. When the keyboard/ display console at P4 plus the Development System at P3 are attached, inputs may be received from both but outputs from the board will go only to the keyboard/display console. With consoles only at P3 and P6 (nothing at P4), the first one to communicate with the Evaluation Board becomes the system console and receives output.

The on-board memory space accessible to the Monitor includes hex addresses 0 through 5FFF, as indicated in figure 3-1. Both the Monitor and the optional Assembler also use up to 100 hex bytes each of RAM starting with address 4000 for the system stack and working storage at various times.

If the P3, P4 and P6 edge connectors are used for non-standard I/O (i.e., any way other than that illustrated in figure 1-3), or if the P5 connector is used, the I/O circuits controlling these connectors must be reprogrammed after initialization by the Monitor. The Peripheral Programming chapter discusses the methods for doing this.

Since the line-by-line Assembler is an option with the Evaluation Board, a description of it is given in a separate manual entitled Am96/4016-ASM Assembler User's Manual.

3-2. MONITOR FUNCTIONS AND USER CONTROLS

The Monitor allows you to perform the following functions:

- Examine, fill or substitute memory locations
- Examine or fill CPU registers
- Execute a program starting at any location
- Single-step through a program
- Specify breakpoints
- Call the line-by-line Asssembler
- Initiate and manage up/down loading from the AmSYS 8/8 Development System

There are two sets of operating modes for the Monitor:

- Normal/System Modes - These modes differentiate between the abilities to execute protected and privileged AmZ8000 instructions, respectively. The Monitor always comes up in Normal Mode; any hex or Assembler instructions can be entered, but

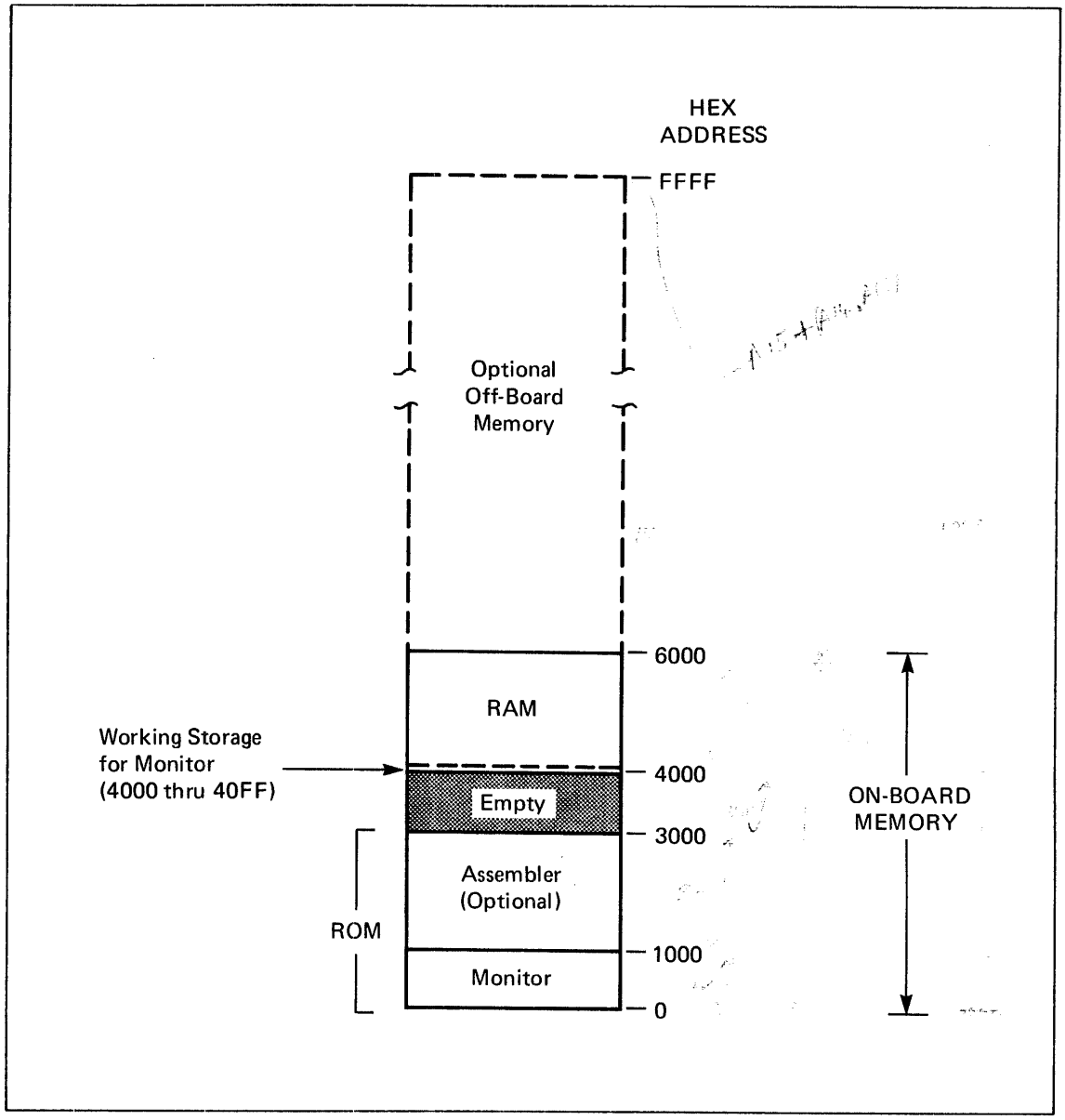


Figure 3-1. Memory Address

only protected instructions are executed. The SM command drops you into System Mode. These modes correspond to the CPU's distinction between Normal and System modes.

Command/Program Modes - These modes differentiate occasions when you are directly interfacing with the Monitor versus interfacing with the Assembler or an application program. In Program Mode, the Monitor acts as a slave to the other program being executed and services that program's needs. The G or ASM commands, which execute programs, exemplify actions that cause a change from Command Mode to Program Mode. In Program Mode, calls can be made to the Monitor either through the SC instruction or through direct keyboard entry at program input points. Direct keyboard entry must be preceded by the ESC (escape) key, and this only works when the Monitor is driving I/O for the application program.

An asterisk (*) is used for command prompting. However, since the keyboard/display console has only one line of display characters, the prompt does not appear on this console if a line of data is displayed in response to the previous command. When commands are used that require no display in response, the command prompt will appear on the keyboard/display console just as on conventional CRT or printer consoles.

There are two text-editing functions: The last character entered can be deleted with the DEL key on RS232C consoles or the RUBOUT key on Teletype (TTY) consoles. Also, the entire current line of entry can be deleted with the Control X key pair.

If unrecognized commands are entered, the Monitor will respond with a question mark (?).

3-3. MONITOR COMMANDS

The Monitor commands are listed according to functional categories in table 3-1. Upper case characters are literal entries, lower-case characters are variable entries. The commands are described in detail on the pages that follow, according to the alphabetical order of the command mnemonic; here the commands are enclosed in parantheses which should not be entered as part of the command. All memory address and CPU register values (the x,y,z parameters) are hexidecimal. All CPU register numbers, flag values and other m,n parameters are decimal.

In addition to these commands, any AmZ8000 hex-format instructions can be entered through the Monitor, without the Assembler. The Monitor initializes the program counter at hex 1000 and the stack pointer (register R15) at hex 40AE. System calls (the 7F instruction followed by a non-zero reference value) will display the reference value when the program exits to the Monitor.

Blank spaces separating single-character commands and variables are optional.

All addresses are 16 bits long. Memory reference always return words and instructions always begin on word boundries (even addresses).

3-4. (ASM) EXECUTE ASSEMBLER

Invokes the line-by-line Assembler, which is assumed to reside in ROM hex addresses 1000 through 2FFF. It will immediately prompt you for input. See the Am96/4016-ASM User's Manual for instructions on how the Assembler is operated.

TABLE 3-1. MONITOR COMMAND SUMMARY

Edit Functions	
Display memory	D x,y
Display and substitute memory	S x
Display program counter	XP
Display all CPU registers	X
Display word register	X n
Display flags	XF
Fill memory	F x,y,z
Fill program counter	P=x
Fill high-byte register	RHn=x
Fill low-byte register	RLn=x
Fill word register	Rn=x
Move memory	M x,y,z
Set carry flag	C n
Set decimal-adjust flag	D n
Set half-carry flag	H n
Set overflow flag	V n
Set parity flag	P n
Set sign flag	S n
Set Zero flag	Z n
Execution Functions	
Execute assembler	ASM
Execute program	G x
Enter system mode	SM
Enter normal mode	NM
Hardware breakpoint	E x
Software breakpoint	B x,y,z
Single-step	(cr) after B or T
Trace	T m,n
Up/Down Loading	
Down Load	LOAD d:file,x
Up Load	SAVE d:file,x,y

NOTE: m,n are decimal values
x,y,z are hexidecimal values

3-5. (B x,y,z) SOFTWARE BREAKPOINT

Sets two or three software breakpoint addresses (x,y and optionally z) and starts execution at the current program counter address. Only the first breakpoint encountered is used; the others are discarded when any one breakpoint is reached.

This command executes to, but not including, instruction x. Unlike the hardware breakpoint command (Ex), this command cannot be used in ROM space.

User code is modified temporarily by inserting a system call at the breakpoint address, but the code is restored upon break. Thus the breakpoints are cleared everytime and do not stay set.

Output includes the program counter (PC) at break and the first word of the next instruction (NI) to be executed.

You might need to set the program counter (P=x) prior to entering this command.

3-6. (C n) SET CARRY FLAG

Sets or resets the carry (C) flag to n=1 or 0. See the XF command for displaying flags.

3-7. [(cr) after B or T] SINGLE-STEP

After a B (breakpoint) or T (trace) command has been executed, single carriage returns (cr) will execute and display subsequent instructions one at a time. This single-step mode is disabled with any macro-type command such as G, ASM, LOAD or SAVE.

3-8. (D n) SET DECIMAL-ADJUST FLAG

Sets or resets the decimal-adjust (DA) flag to n = 1 or 0. This syntax takes precedence over the Display Memory (D x,y) command. See the XF command for displaying flags.

3-9. (D x,y) DISPLAY MEMORY

Displays the contents of memory at addresses x through y. Up to eight hexidecimal words, plus their ASCII byte equivalents and beginning address are displayed on each line. Bytes with no ASCII equivalent are represented by an underline (this character may vary with your terminal).

The y ending address is optional and if missing is assumed equal to x. The least significant bit of each address x and y is cleared to insure display on word boundries.

Display of locations Ø or 1 can conflict with the Dn command. To avoid this conflict, these addresses can be represented by ØØ and Ø1, respectively. This is not necessary, however, in the case of a range such as DØ,F.

The ASCII equivalents displayed in the right-hand column are useful for identifying alphanumeric data.

3-10. (E x) HARDWARE BREAKPOINT

Sets a hardware breakpoint at address x. It stays set until changed. Setting to zero has the same effect as a clear. Control is returned to Monitor following completion of instruction if the address is encountered during user program execution.

A breakpoint should not be set to the address immediately following a system call because unpredictable results will occur.

3-11. (F x,y,z) FILL MEMORY

The contents of memory words from the x address through the y address are filled with the 16-bit value z. The least significant bit of each address x and y is cleared to insure fill on word boundries (even addresses). If y is missing, it is assumed equal to x.

The new LDPR Monitor command has the form:

LDPR d:file.ext

LDPR reads the binary file named file.ext on drive d from the AmSYS 8/8 and transfers the program to the Evaluation Board memory. The drive, file name and extension (if any) must all be specified. The file must be a binary file (type .BIN) produced by MACRO8000 or LINK8000 on AmSYS 8/8.

The binary file includes destination addresses for the code. Also, a transfer address (main entry point) is automatically used to set the AmZ8000 program counter (PC). Therefore, the user can start the program simply with G, rather than G followed by an address.

3-12. (G :

Executes
ning at m
itted, ex
address i
command (
a breakpc
program e

You might
ter (P=x)

3-13. (H

DE

s nor-
ed in-

/erflow
:ommand
)w Flag
nd for

Sets or r
to n = 1 or 0. See the XF command for displaying flags.

3-14. (LOAD d:file,x) DOWN LOAD

Reads the object program named "file" on drive "d" from the AmSYS 8/8 Development System into the Evaluation Board memory beginning at memory address x. The "file" name must be in the AmSYS 8/8 format with the disk drive specified. The HOST program must be running on the Development System.

If this command is entered from the Development System, a prompt, consisting of the currently logged-in diskette identifier in parentheses, will appear on your console.

See the next section entitled AmSYS 8/8 Up/Down Loading if you are assembling programs on the Development System.

3-15. (M x,y,z) MOVE MEMORY

Moves the contents of memory from address x through address y to addresses z through z+(y-x). Memory is moved as 16-bit words. Therefore, the least significant bit of addresses x and z are cleared to ensure a memory move on word boundries (even addresses). Also, when address y is an even address, addresses x through y+1 are moved to addresses z through z+(y-x+1).

3-18. (P = x) FILL PROGRAM COUNTER

Fills the program counter with the address x. The counter can be displayed with the XF command.

3-19. (RHn = x) FILL HIGH-BYTE REGISTER

Fills the high-byte register n (where n = 0 to 7) with the 8-bit hex value x. The register can be displayed with the Xn command.

3-20. (RLn = x) FILL LOW-BYTE REGISTER

Fills the low-byte register n (where n = 0 to 7) with the 8-bit hex value x. The register can be displayed with the Xn command.

3-21. (Rn = x) FILL WORD REGISTER

Fills the general-purpose register n (where n = 0 to 15) with the 16-bit hex value x. The register can be displayed with the Xn command.

3-22. (SAVE d:file,x,y) UP LOAD

Writes the contents of Evaluation Board memory between the addresses x and y to the AmSYS 8/8 Development System disk "d" on the "file" specified. If the file already exists, it will be deleted

and recreated. The "file" name must be in the AmSYS 8/8 format with the disk drive specified, and the HOST program must be executing.

If this command is entered from the Development System, a prompt, consisting of the currently logged-in diskette identifier in parentheses, will appear on your screen. These simply acknowledge communications received from the Evaluation Board Monitor.

See the next section entitled AmSYS 8/8 Up/Down Loading if you are assembling programs on the Development System.

3-23. (SM) ENTER SYSTEM MODE

Drops you into the CPU's System Mode, in which all privileged instructions can be executed. The Monitor is initialized at power-up in Normal (protected) Mode.

3-24. (S n) SET SIGN FLAG

Sets or resets the sign (S) flag to n = 1 or 0. This syntax takes precedence over the Display and Substitute Memory command. The XF command can be used to display the flags.

3-25. (S x) DISPLAY AND SUBSTITUTE MEMORY

Displays the contents of the memory word at address x and waits for your substitution. A 16-bit hex value will replace the contents of the word at address x and advance to the next word. A carriage return only will advance to the next word without substitution. A period (.) will terminate substitution and return to the Monitor's command mode.

Substitutions of addresses Ø or 1 can conflict with the Sn command. To avoid this conflict, these addresses may be represented by ØØ and 01, respectively.

3-26. (T m,n) TRACE

Executes m instructions beginning at the current program counter address and displays each instruction in sequence. If n is specified, the display occurs in intervals of n instructions. This command is useful only for CRT or printer consoles, as an alternative to manual single-stepping.

You might need to set the program counter (P=x) before entering this command.

Care should be taken not to trace over system calls because unpredictable results will occur.

3-27. (V n) SET OVERFLOW FLAG

Sets or resets the parity/overflow (P/V) flag to n = 1 or 0. This command is equivalent to the Set Parity Flag (Pn) command. The flags can be displayed with the XF command.

3-28. (X) DISPLAY ALL REGISTERS

Displays the contents of all 16 CPU registers, plus the program counter (PC) and flags.

3-29. (XF) DISPLAY FLAGS

Displays the six flags contained in the CPU's Flag and Control Word. The bit-setting of the flag immediately follows its mnemonic. The flags are:

- C Carry
- Z Zero
- S Sign
- P Parity or overflow (P/V)
- D Decimal adjust (DA)
- H Half-carry

3-30. (X n) DISPLAY WORD REGISTER

Displays the 16-bit contents of CPU register n, where n = 0 to 15. Register 15 is the stack pointer and is initialized during power-up to 40AE.

3-31. (XP) DISPLAY PROGRAM COUNTER

Displays the address contained in the program counter register.

3-32. (Z n) SET ZERO FLAG

Sets or resets the zero (Z) flag to n = 1 or 0. The flags can be displayed with the XF command.

3-33. MONITOR I/O SUPPORT FOR USER PROGRAMS

I/O through the serial or parallel ports can be done either by your program, through the CPU's I/O instructions in system mode, or by the Monitor.
To use the Monitor for I/O, these general steps are followed:

1. Store a block of four 16-bit control words in memory.

2. Store the beginning address of this block in register R1.

3. Execute the SC instruction using a value of zero (a non-zero value will be interpreted as a program exit which will return control to the monitor).

The block of four 16-bit control words is ordered as shown in table 3-2. The function code is stored in the most significant byte of word one; the least significant byte of word one contains the response code. Words two, three and four provide the address of the file name, the beginning address of data, and the number of bytes to be written on read as described in the following function code description.

Read Control Statement (function code 0) - This command is intended for use by the assembler. It transfers the user call command line to the specified area in the same form as the Read Console function code 1

Read Console (function code 1) - Reads a single line from the console. The file name address is unused. The data length represents a maximum and is replaced by the actual length. A console message is always terminated by a carriage return. The response code is nomally zero unless the message was truncated, in which case, the response code is 1.

Write Console (function code 2) - Writes a single line to the console. The file name address is unused. The data length represents the write length. The system provides no automatic end of line thus, the message must contain any required carriage return or line feed codes. The response code is zero.

Write Line Printer (function code 3) - Outputs a single line to the line printer. The file name address is unused. The data length represents the write length. All printer controls must be user supplied. The System 8/8 host must be connected and its monitor in execution. The response code is zero.

Open Disk File (function code 4) - Prepares a disk file to be read. The data address and length are unused. The file name address points to the address of the file name, which must be thir-

TABLE 3-2. MONITOR I/O CONTROL BLOCK

Word	Byte	Contents
1	High	Function Code 1 = Read from console 2 = Write to console 3 = Write line printer 4 = Open disk file 5 = Close disk file 6 = Created disk file 7 = Read disk sector 8 = Write disk sector 0 = Read Control statement
	Low	No entry. Response code is stored here after I/O.
2	High Low	Address at which the file name is stored.
3	High Low	Beginning address of data to be written or read. Data written must include any necessary carriage return, line feeds etc. Data read will include them also.
4	High Low	Length in number of bytes. It indicates either the total number of bytes to be written, or the maximum number of bytes to be read. The total number of bytes read up to and including the carriage return is stored here upon return to user program.

teen characters long and in AMDOS format e.g., A:FILEbbbbEXT. The response code is zero if the file was opened, 1 if not found, 2 if a disk error occurred, and 3 if the file is already open. The Sytem 8/8 host must be connected and its monitor in execution.

Close Disk File (function code 5) - Closes a file. The data address and length are unused. The file name address points to the address of the file name, which must be thirtheen characters long and in AMDOS format (See function code 4). The response code is zero if the file was closed, 1 if not found, 2 if a disk error occurred, and 3 if not previously opened or created. The Sytem 8/8 host must be connected and its monitor in execution.

Create Disk File (function cod
Creates a disk file and prepares
be written. The data addre
length are unused. The file
address specifies the address at
the file name is stored. The fil
must be thirteen characters long
AMDOS format. The response c
zero if the file was created, 1
file space, 2 if a disk error occ
and 3 if the file is already o
created. If a prior file exist
will be deleted before the new
created. The Sytem 8/8 host mu
connected and its monitor in exec

Read Disk Sector (function code 7) - Reads one disk sector (128 bytes) Both the file name and record address must be given. The data length is returned. The next sequential sector on the specified file will be transferred to the data area. The response code is zero if no errors, 1 if end of file occurred, 2 if a disk error occurred, or 3 if this file was not previously opened or an attempt is made to read a created file. If a created file is to be read, it must be closed and re-opened. The Sytem 8/8 host must be connected and its monitor in execution.

Write Disk Sector (function code 8) - Write one disk sector (128 bytes) Both the file name and record address must be given. The data length is unused. The next sequentioal sector on the specified file will be written with the contents of that data area. The response code is zero if no errors, 1 if no disk space, 2 if a disk error occurred, or 3 if this file was not previously created. Attempting to write to an opened file will also return code 3. The System 8/8 host must be connected and its monitor in execution.

The section should be called HOST AND MONITOR COMMUNICATION.

The capabilities should be listed in a more reasonable order:

- **Assemble (or assemble and link) AmZ8000 sourc code with MACRO8000 (or MACRO8000 and LINK8000) on AmSYS 8/8.**
- **Download programs to the Evaluation Board with the LOAD Monitor command or LDPR Monitor command, as described later in this section.**
- **Store programs by uploading the memory image from the Evaluation Board to a file on AmSYS 8/8. The file is uploaded with the SAVE Monitor command and can later be downloaded again with the LOAD Monitor command.**

~~ating system supports a utility~~
HOST, which communicates with the Evaluation Board Monitor. The HOST utility interfaces with AMDOS8 for service calls to read the console, print lines, and process disk requests.

The program is activated like any other AMDOS8 program: by typing in its name, in this case HOST. It will respond with the message SYSTEM 8/8 Z8000 HOST followed by a prompt which consists of

the currently logged-in disk drive in parentheses, e.g., (A).

After an up or down load, the HOST program can be terminated with the Control L and END sequence so that execution on the Evaluation Board may proceed concurrently with unrelated execution under the Development System's operating system. The message HOST SHUTDOWN appears upon termination. This soft shutdown is provided so that the program can close any files left open.

The Control L entry indicates to the HOST program that the command to follow is meant for it. The Control L END sequence is currently the only user command to the HOST program. All other commands entered from the AmSYS 8/8 console (i.e., those without Control L) are transmitted to the Evaluation Board for interpretation. Upon transmission, the Development System will acknowledge this with its prompt. The Evaluation Board will acknowledge reception of the command with its prompt, another more specific response, or both. Thus, the Development System console can effectively become the Evaluation Board console.

The HOST program can issue five error messages, which are explained below.

COMMAND ERROR - Invalid Control L command.

Z8000 MESSAGE PENDING - A prior message to the Evaluation Board CPU has not yet been acted upon.

MESSAGE EXCEEDS 80 CHARACTERS - Re-enter your message using fewer characters.

ILLEGAL REQUEST FROM Z8000 - The Development System has received an unrecognized message from the Evaluation Board.

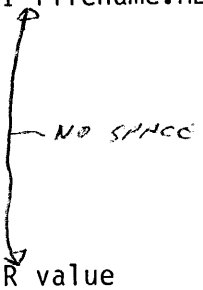
TRANSMISSION ERROR - Communication with the Evaluation Board produced a parity error and transmission is being retried. If this continues, reset the CPU (power off/on, unless you have connected a reset circuit).

The Development System's MACRO8000 (MACZ) Assembler produces hex code that must be converted to binary before down-loading to the Evaluation Board. Normally, the Development System's LOAD program is used for this translation. However, AMDOS8 assumes programs always start at 100 hex, while on the Evaluation Board programs must start no lower than about 4100 hex (see figure 3-1).

To overcome this situation, the Development System's DEBUG program can be used to load, translate and offset the hex source file before down-loading to the Evaluation Board. This is accomplished with the following entries:

1. DEBUG — Calls progra

2. I filename.HEX — Declar source for tr binary extens filena used).



3. R value — Loads, and c source value 10100 desire origin

4. Control C — Exits bug pr

5. SAVE nnn filename — Saves progra ette. value nnn is de-

The section should be called HEX FILE DOWNLOADING.

The download procedure involving a .HEX file, DEBUG, SAVE, and the LOAD Monitor command can still be used but is not recommended. The binary download using the LDPR Monitor command is recommended.

rived from the two most significant characters of a hex value returned by the R command in step 3.

After this sequence is entered on the Development System, the program can be down-loaded by executing the HOST program and entering the Evaluation Board Monitor's LOAD command.

For example, if you want your program origin to be hex 5000 for Evaluation Board execution, your entry in step 3 would be:

```
R B1ØØ
```

The value B1ØØ is obtained by subtracting hex 5000 from hex 10100. Following the R command, AMDOS8 returns a 4-character hex value called NEXT, as in:

```
NEXT
69E2
```

The first two hex characters of this value must be converted to their decimal equivalent to obtain the value nnn used in step 5. For example:

```
69 (hex) = 105 (decimal)
```

The SAVE command in step 5 would then be:

```
SAVE 105 filename
```

This file can then be down-loaded to the Evaluation Board by first running HOST and then entering the Evaluation Board Monitor's LOAD command.

The section sho

The AMC binary i
information, as
.COM file, the
code. Like a
address inform
address spaces.
transfer addres
Program Counter
Board.

Either MACRO800(
as output from
(type .BIN) has
the file. The

HOST

The section should be called SAVE/RESTORE with UPLOAD/DOWNLOAD.

The user can save the memory image of an AmZ8000 program by uploading to AmSYS 8/8. The SAVE Monitor command saves the specified memory space as a file on AmSYS 8/8. The file type .ZSV is recommended. The user should make a record of the current PC at the time of the SAVE.

The user can later restore the program by downloading from AmSYS 8/8 with the LOAD Monitor command. No special preparation of the file is involved; the information saved with the Monitor SAVE can be directly reloaded with the Monitor LOAD. The PC should then be set to the value it had when the program was saved.

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. POWER-UP SEQUENCE

The Evaluation Board requires three input voltages at the P1 edge conector. Their use is shown below:

+12V - RAM and serial I/O circuits

-12V - RS232C and TTY interfaces. -5V for RAM is derived from this voltage.

+5V - TTL

The ground (GND) pins at P1, P2, P3 and P4 are tied together with the Signal Ground pins at P5 and P6. They require external ground at P1. The Chassis ground pins at P5 and P6 can be jumpered into this ground plane as shown in figure 2-4.

When the board is powered up, an RC network generates a reset to the CPU and to the programmable parallel and serial I/O devices. The CPU's flag and control word (FCW) is initialized, with only the System/Normal flag set to System Mode. The Monitor program then begins execution.

The Monitor writes a value to the CPU's refresh counter that causes refresh at 30-microsecond intervals. The program status area pointer (interrupt vector table) is also written. Then, the Monitor writes control bytes to the Am8253 counter/timer, the two Am9551 serial I/O circuits, and the Am8255A parallel I/O circuit. It also samples a line to see if the optional keyboard/display console is present at P4 (when present, it receives all output).

The Monitor then sets the user's program counter to 1000 hex and sends a command prompt to either the keyboard/display (if attached) or to the console at P6. If consoles are attached to both P5 and P6, without the keyboard/display at P4, the first console to respond becomes the system console and gets all output.

4-2. CPU FUNCTIONS

The list of CPU pins below describes which pins are used for the internal functions of the Evaluation Board. All pins, after buffering, are available for external use at the P2 edge connector.

AS* - (output, three-state). Used in the normal way to indicate valid addresses, and to demultiplex the address/ data buses.

DS* - (output, three-state). Used in the normal way to indicate valid data, and to demultiplex the addreess/ data buses. Figure 4-1 shows how it is also used with R/W* and I/O* (a line decoded from the ST_0-ST_3 lines) to decode the IOR* and IOW* lines which gate the Am8255A, Am9551 and Am8253 circuits.

MREQ* - (output, three-state). Used in the normal way to gate memory.

R/W* - (output, three-state). Used with DS* and I/O*. See figure 4-1. RAM R/W*, which is forced high during memory refresh, is derived from this line.

N/S* - (output, three-state). Not used. Trapping of System Mode instructions is done independently of this output, which is designed primarily to distinguish physical memory spaces for Normal and System Modes.

B/W* - (output, three-state). Used in the normal way to distinguish byte or word memory references.

ST_0-ST_3 - (outputs, three-state).

Only three of the ten possible conditions meaningful for the AmZ8002 are used on-board:

1) I/O reference is used with R/W* and DS* as described under DS*

2) memory refresh becomes RFSH* and is used on the RAM

3) instruction fetch, first word, becomes IF1* and is used in the hardware breakpoint and single-step functions.

WAIT* - (input). Used to generate Wait states between the T2 and T3 clock cycles of a memory cycle during memory references to address 0-5FFF.

STOP* - (input). Not used. It stops the CPU entirely, which prevents the Monitor program from executing.

BUSRQ* - (input). Not used on-board since only the CPU controls the system buses.

BUSAK* - (output). Not used. However, it is connected to disable P2 buffers if the BUSRQ* is used by an external device.

NMI* - (input). Used by the breakpoint, single-step and break switch functions to force control back to the Monitor program.

VI* - (input). Not used.

NVI* - (input). Not used.

MI* - (input). Not used.

MO* - (output). Not used.

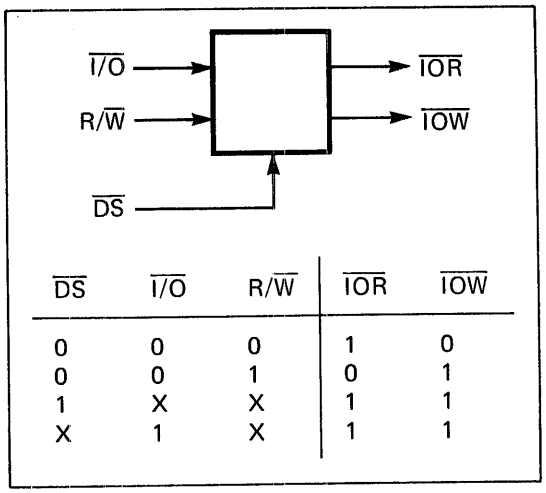
RESET* - (input). Connected to the RST* line on the board, which resets the CPU and all other programmable circuits during power-up.

4-3. BUS STRUCTURE

The CPU's 16-bit multiplexed address/data pins are demultiplexed into separate 16-bit data and address buses, as shown in figure 4-2. The address bus is latched and the data bus is buffered before use on the board and termination at the P2 edge connector. A transparent latch instead of a register is used on the buffered address bus so that addresses may become valid before the trailing edge of the address strobe (AS*).

The status lines and control strobes are also buffered to P2. All of these lines and buses float to the high impedance state when an external device's bus request (BUSRQ*) is acknowledged (BUSAK*).

The CPU's data bus is separated from a 16-bit internal data bus (ID_0-ID_{16}) by a transceiver which can be disabled by an active-low input on the INH*



DS	I/O	R/W	IOR	IOW
0	0	0	1	0
0	0	1	0	1
1	X	X	1	1
X	1	X	1	1

Figure 4-1. IOR* and IOW* Decoding

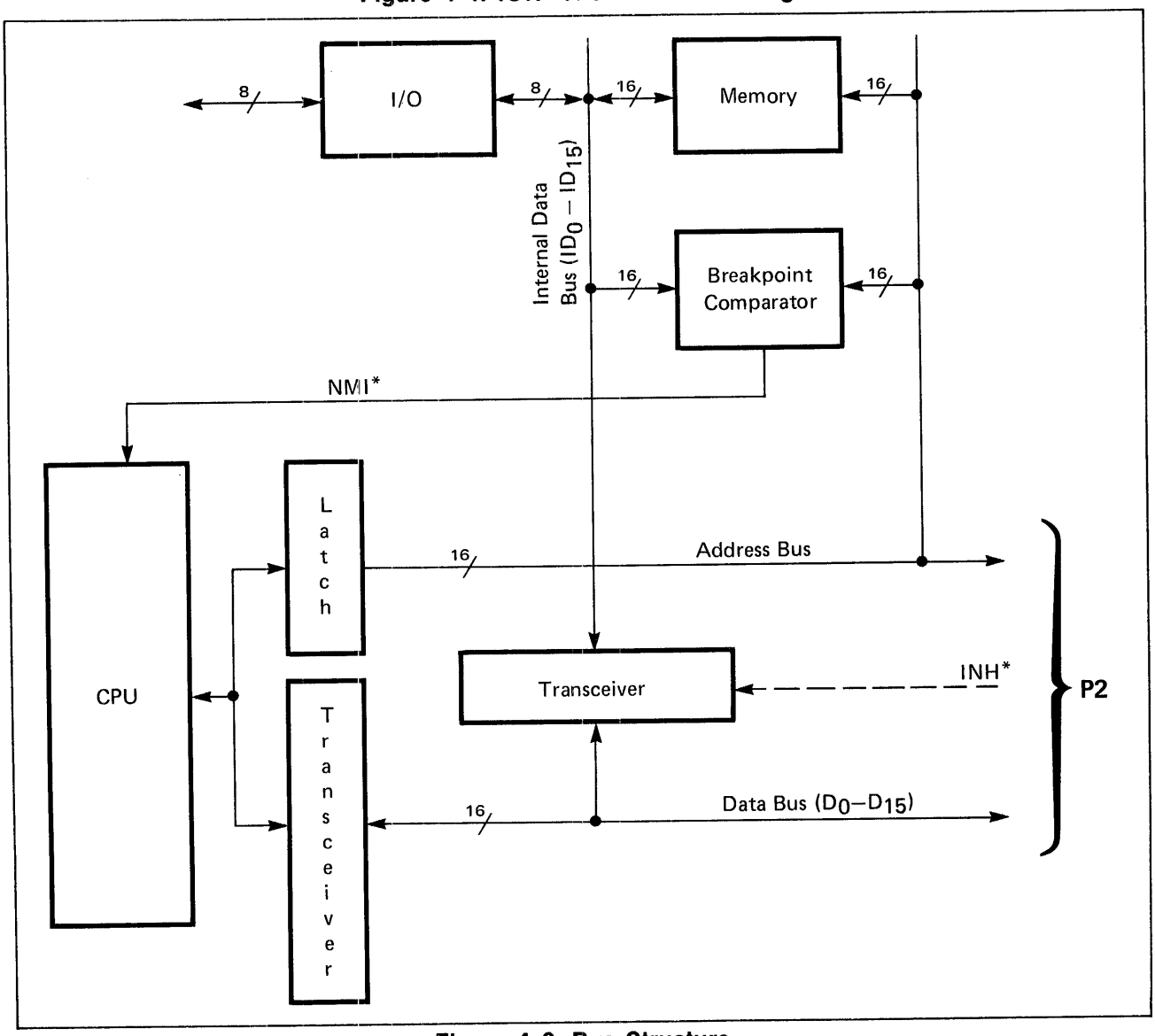


Figure 4-2. Bus Structure

line. The INH* line is normally an output on P2 during memory references to the on-board memory space (0-5FFF); this disables off-board memory, but it can be jumpered (see figure 2-4) to become an input and thereby give priority to off-board memory.

The internal data bus services on-board memory (16 bits) and I/O ports (lower 8 bits). A 16-bit hardware breakpoint register sits between the internal data bus and the address bus. When loaded through the data bus with a hardware breakpoint address (the Bx command), it generates a non-maskable interrupt to the CPU upon seeing that address on the address bus.

4-4. MEMORY

Figure 3-1 shows the allocation of memory space on the board. The ROM Monitor occupies addresses 0-0FFF. The optional ROM Assembler occupies 1000-2FFF. There is an empty hole at 3000-3FFF due to lack of space on the board for additional memory. RAM occupies 4000-5FFF, with up to hex 400 low bytes used by working storage for the ROM programs and CPU stack pointer. (i.e., up to hex address 4200.)

RAM memory is refreshed at 30-microsecond intervals by the CPU, according to the Monitor's initialization of the CPU's fresh counter. ROMs are disabled during this refresh. Since there is only one row of RAM, the internal data bus is sourced only by the RAM during refresh. Care should be taken if the INIT* input on P1 is enabled by jumpers 14 and 15 (figure 2-4): this causes a CPU reset, during which memory refresh ceases.

Each memory address contains an 8-bit byte. For a RAM read, both high and low bytes of the word-oriented memory are enabled, irrespective of whether the operation is on a byte or a word. In a byte write to RAM, however, only the high or low byte of memory is enabled (internal data bus lines ID_{15}-ID_8 or ID_7-ID_0, respectively). By contrast, all ROM transfers enable the entire word.

A single Wait state is inserted betwen clock cycles T2 and T3 during on-board memory cycles, but it can be disabled by a jumper (figure 2-4).

An INH* line is present at the P2 edge connector for inhibiting either on- or off-board memory, depending on the use of optional jumpers 16, 17 and 18 (figure 2-4). The board is shipped with no jumpering at these connections; therefore, the INH* line is never activated. When jumpers 16 and 17 are connected, INH*O is an active-low output at P2 during memory references to on-board memory space (0-5FFF); this is useful in disabling off-board memory that overlaps this space. When jumpers 17 and 18 are connected, INH* is an active-low input to the on-board memory for all memory references; on-board memory is never accessed in this case.

The INH* line can be gated off-board with the MREQ* line and selected address lines to vary this priority scheme within the 0-5FFF address space. For example, figure 4-3 shows how off-board memory can take precedence at all addresses except 0-0FFF, where the Monitor resides.

4-5. PERIPHERAL DECODING

Only the low-order 12 address bits on the Evaluation Board are decoded for peripherals, giving a total of up to 4K I/O ports. Some peripheral circuits use A_0 and A_1 to directly address internal channels or registers. Therefore, these two bits are uniformly treated as don't-care bits for device addressing as a result, each decoded I/O port consists of a block of four contiguous addresses.

These address lines are gated by the decoded status signal I/O*, indicating an input or output cycle (either one). In order to be compatible with the peripheral chips, two control strobes, IOR* and IOW* are generated from the R/W* line when I/O* is active, and they are gated by DS* as illustrated in the CPU Functions discussion above. Furthermore, the last eight groups are decoded as write-only ports by gating with the IOW* strobe.

The complete list of I/O port addresses is shown in table 4-1. The range of four contiguous addresses in each group is first shown. If the device uses the A_0 or A_1 lines for direct addressing of channels or registers within the circuit, these are listed below the group range.

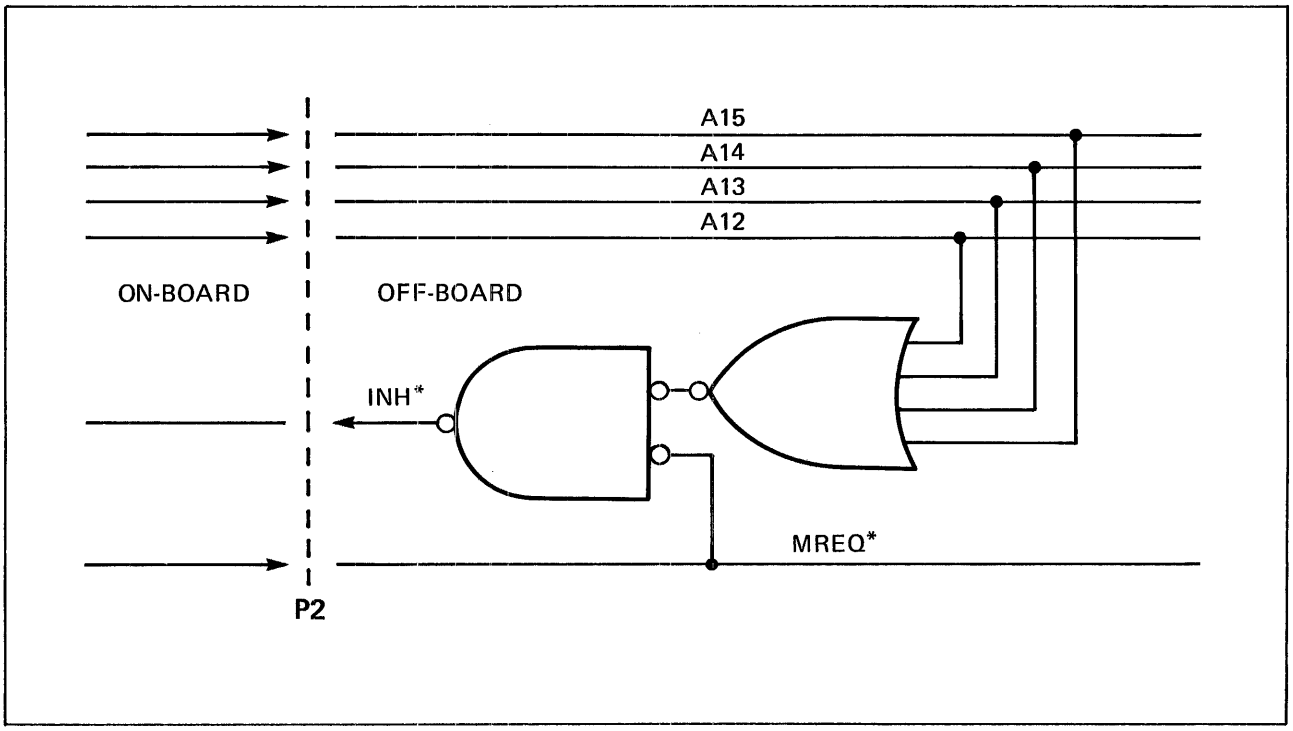


Figure 4-3. Customizing Off-Board Memory References

TABLE 4-1. PERIPHERAL ADDRESSES

FFC-FFF	:	N/C
FF8-FFB	:	N/C
FF4-FF7	:	N/C
FF3-FF0	:	Am8255A buffered user ports
FF3	:	Control port
FF2	:	Port C
FF1	:	Port B
FF0	:	Port A
FEF-FEC	:	Am9551 RS232 port
FEF	:	Control
FEE	:	Data
FED	:	Control (same as FEF)
FEC	:	Data (same as FEE)
FEB-FE8	:	Am9551 RS232 or TTY port
FEB	:	Control
FEA	:	Data
FE9	:	Control (same as FEB)
FE8	:	Data (Same as FEA)
FE7-FE4	:	Am8253 counter time
FE7	:	Mode control
FE6	:	Counter 2
FE5	:	Counter 1
FE4	:	Counter 0
FE3-FE0	:	Keyboard return lines
FDF-FEC	:	Keyboard scan lines
FD8-FDB	:	Single-step control
FD7-FD4	:	Breakpoint register
FD3-FD0	:	LED display
FD3	:	20th character (left most)
FD2	:	19th character
FD1	:	18th character
FD0	:	17th character
FCF-FCC		
FCF	:	16th character
FCE	:	15th character
FCD	:	14th character
FCC	:	13th character

TABLE 4-1. PERIPHERAL ADDRESSES (CONT'D)

```
FCB-FC8
    FCB  :  12th character
    FCA  :  11th character
    FC9  :  10th character
    FC8  :   9th character


FC7-FC4
    FC7  :   8th character
    FC6  :   7th character
    FC5  :   6th character
    FC4  :   5th character


FC3-FC0
    FC3  :   4th character
    FC2  :   3rd character
    FC1  :   2nd character
    FC0  :   1st character  (right-most)
```

CHAPTER 5
PERIPHERAL PROGRAMMING

5-1. PARALLEL I/O

The Am8255A provides three 8-bit parallel I/O ports into or out of the lower eight lines of the internal data bus. In the standard Evaulation Board configuration, the three ports (A, B and C) are used for up/down program loading and remote console control from the AmSYS 8/8 Development System. Port A is used for data output to the Development System, port B for data input, and port C for software-controlled handshaking (4 bits in, 4 bits out).

During power-up initialization, the Monitor writes an 8-bit Operation Control Word to the Am8255A control register for this purpose. In addition, a Bit Set/Reset handshaking byte is written to the same I/O address by the Monitor for each byte of data sent to port A, and the port C lines are read for a response from AmSYS 8/8 that the last data byte was received.

For non-standard uses of the P3 edge connector, the 8-bit Operation Control Word must be rewritten after initialization by the Monitor. There are three modes of operation possible:

Mode 0 - Basic input or output without strobed handshaking (but allowing software handshake routines). Ports A and B are 8 bits each and port C consists of two 4-bit ports. Any port can be input or output. Outputs are latched; inputs are not. In the standard Evaluation Board, the Am8255A is initialized in this mode.

Mode 1 - Input or output in conjunction with strobed handshaking signals. Port A consists of 8 data lines in conjunction with the upper four handshake lines of port C. Port B is similar but uses the lower four lines of port C for handshake. All data lines are latched, whether input or output.

Mode 2 - Bidirectional data transfers on the eight lines of port A, controlled by the upper five monodirectional lines of port C. Port A is latched on both input and output. The lower three lines of port C and the eight lines of port B are monodirectional input or output data lines.

The form of the 8-bit Operation Control Word is shown in table 5-1.

Port C contains an 8-bit output latch/buffer and an 8-bit input buffer (no latch). Any of the output bits can be set or reset with an output instruction to the same address according to the 8-bit Bit Set/Reset Control Word shown in table 5-2.

After initialization, data or control bytes can be transfered at ports A, B and C using the I/O addresses shown in table 5-3.

The six 14-pin sockets provided for drivers and terminators between the Am8255A and the P3 edge connector limit the use of all three ports to either input or output, i.e., no bidirectionality, which is normally possible with port A in Mode 2. However, if there is only a short distance between the P3 edge connector and the external device, the driver/terminator sockets can be shorted with headers and jumpers to get bidirectionality in port A at the expense of sacrificing buffering.

Refer to the AMD Am8255A Data Sheet for more details.

TABLE 5-1. Am8255A OPERATION CONTROL WORD FORMAT

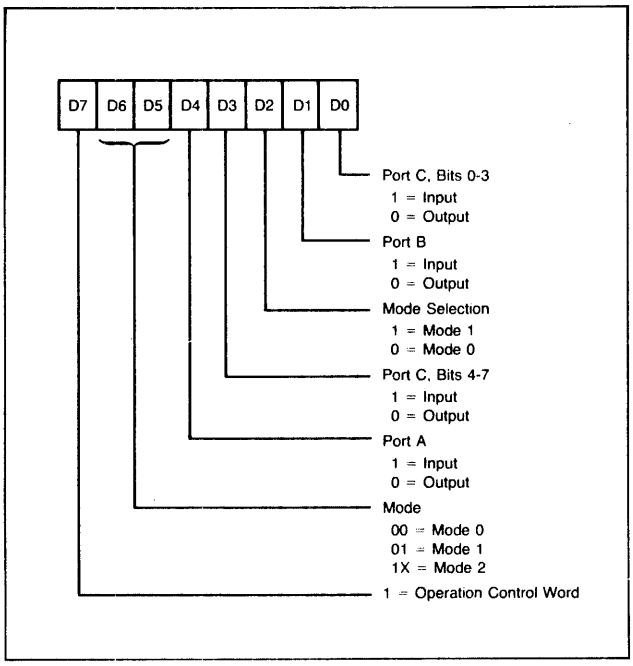
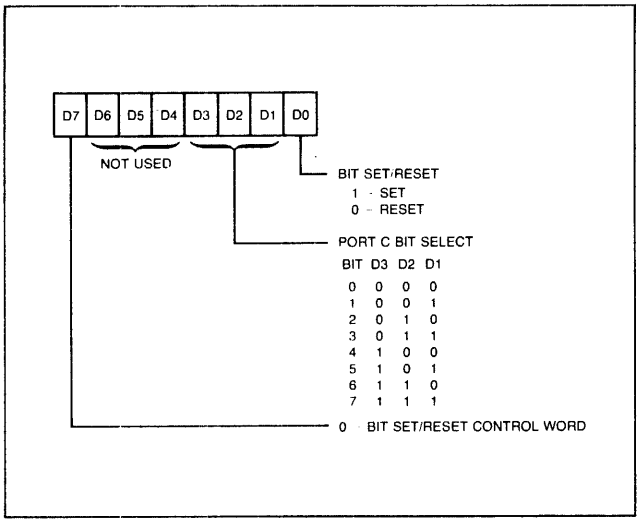


TABLE 5-2. Am8255A BIT SET/RESET CONTROL WORD FORMAT



5-2. SERIAL I/O

Two Am9551 USARTs provide full-duplex serial transmission between the lower eight lines of the internal data bus and the P5 and P6 edge connectors. Both the transmitter and receiver clock inputs to these circuits come from the Am8253 counter/timer.

In the standard Evaluation Board configuration, the Am9551 at P6 devices are initialized by the Monitor with control bytes at power-up, independently of whether the ports are jumpered for RS232C or TTY compatiblity. The devices are configured for 8-bit asynchronous characters with two stop bits, parity disabled and 16x baud rate factor. They are also enabled for transmission and reception, with the Request-To-Send line forced active and without Hunt Mode. This is accomplished by first writing a hex CE Mode Control Code to I/O addresses FE9 and FED, followed by a hex 27 Control Command to the same address (11001110 followed by 00100111). The format for the Asynchronous Mode Control Code is shown in table 5-4.

The format for the Control Command that follows it is shown in table 5-5.

Synchronous transmission/reception is obtained by first writing a Synchronous Mode Control Code followed by one or two 8-bit synch characters, followed by the same Control Command format illustrated above. The format for the Synchronous Mode Control Code is shown in table 5-6.

If you wish to change the Monitor's initialization of the P6 USART after power-up, or if you intend to use the P5 USART, the following steps are recommended:

1. Write three successive null bytes to the control port (FE9 for P6 or FE0 for P5).
2. Write a hex 40 to the port for a software reset.
3. Initialize the device by writing new control information as described above.

After initialization, data can be transferred using the I/O addresses shown in table 5-7.

A readable status register maintains information on the current operational status of the device. Its format is shown in table 5-8.

The definition of the status bits is as follows:

TxRDY Transmitter Ready indicates the Am9551 is ready to accept a data character or command.

RxRDY Receiver Ready indicates the Am9551 has received a character on its serial input and is ready to transfer it to the CPU.

TxE Transmitter Empty signals the processor that the transit register is empty.

PE Parity Error indicates the character stored in the receive character buffer was received with an incorrect number of binary 1 bits.

OE Overrun flag is set when a byte stored in the receiver character register is overwritten with a new byte before being transferred to the processor.

FE Framing Error indicates the asynchronous mode byte stored in the receiver character buffer was received with incorrect character bit format.

SYNDET When Sync Detect is set for internal sync detect, this bit

TABLE 5-3. Am8255A ADDRESSES

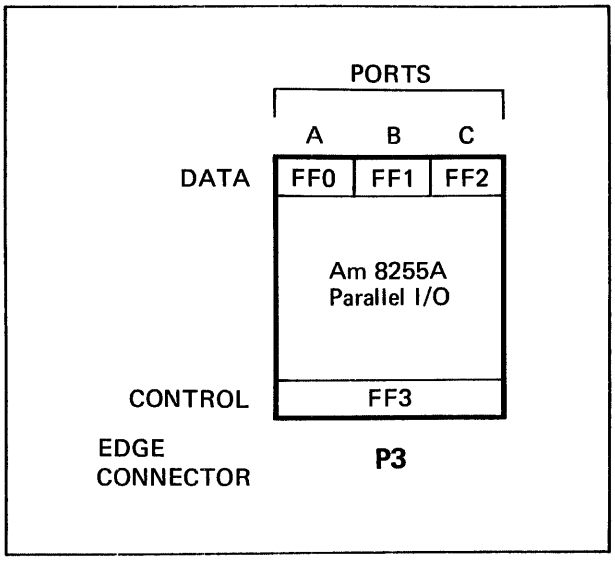


TABLE 5-4. Am9551 ASYNCHRONOUS MODE CONTROL CODE

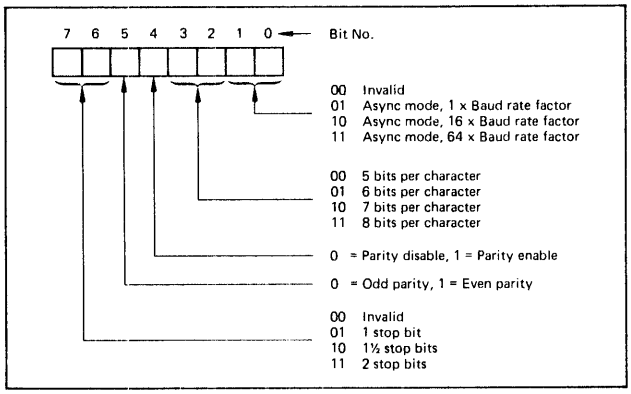


TABLE 5-5. Am9551 CONTROL COMMAND

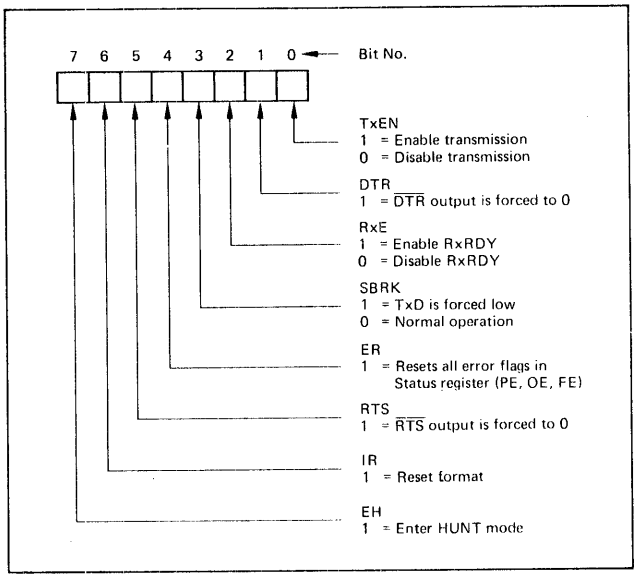


TABLE 5-6. Am9551 SYNCHRONOUS MODE CONTROL CODE

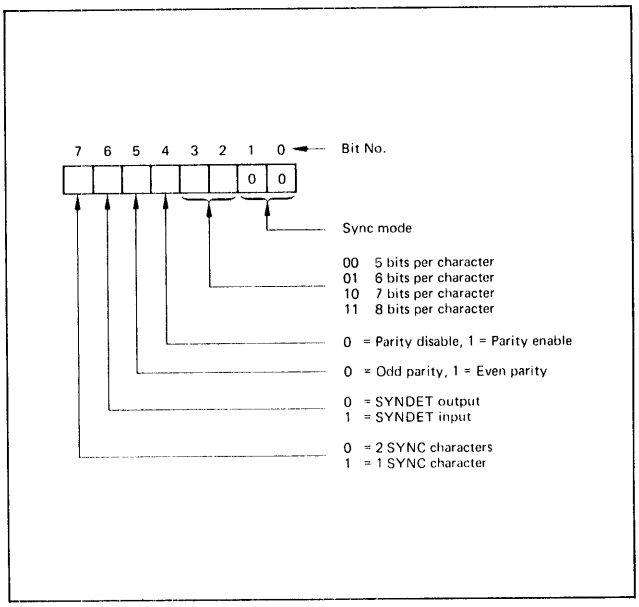


TABLE 5-7. Am9551 ADDRESSES

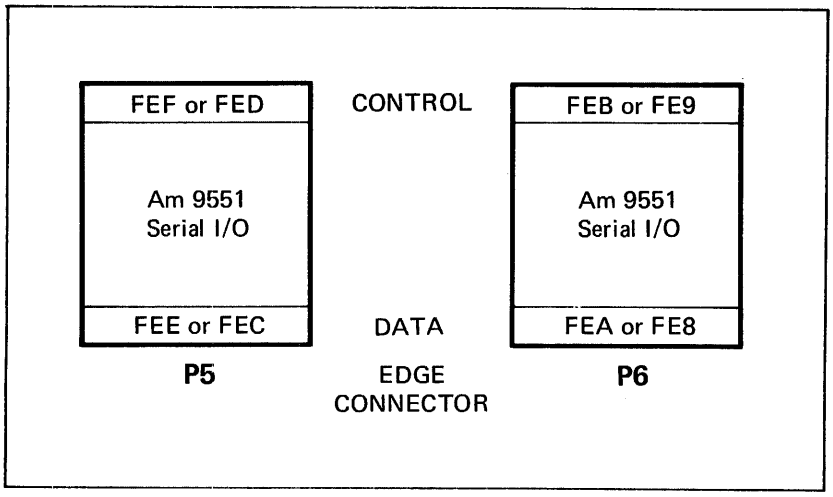
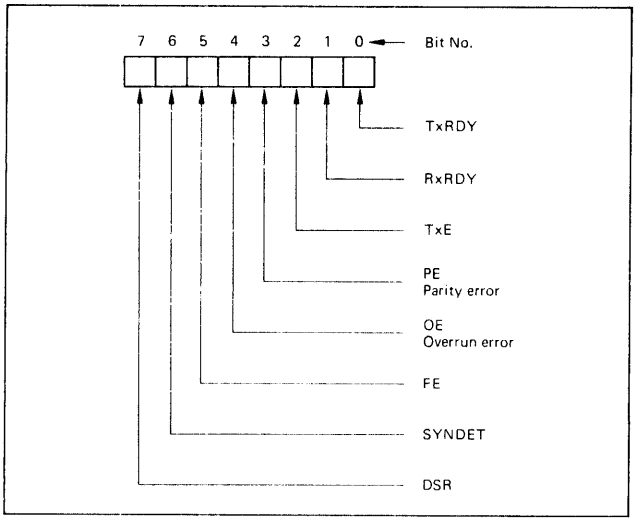


TABLE 5-8. Am9551 STATUS REGISTER



indicates character sync has been achieved and the Am9551 is ready for data.

After initialization, always check the status of the TxRDY bit prior to writing data or a new command word to the Am9551. The TxRDY bit must be true to prevent overwriting and subsequent loss of commands or data. The TxRDY is inactive until initialization has been completed.

Refer to the AMD Am8251/Am9551 Data Sheet for more details.

5-3. COUNTER/TIMER

The Am8253 provides three counter/timer channels using a 2MHz clock input derived from the 4MHz CPU clock. Two of the three counter outputs drive the transmit and receive clock inputs of the two Am9551 USARTs at 9600 baud; counter 1 is attached to the USART at P6, and counter 2 is attached to the USART at P5. The third counter output, together with its associated gate and clock inputs, are available for external use on P5 together with the serial port.

A 16-bit binary counter in each channel counts down at the clock input rate and generates a signal when reaching zero. Alternatively, a 4-decade BCD counter can be used.

There are five modes associated with the manner in which signals are output:

Mode 0 Interrupt on terminal count

The output will be initially low after the mode-set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached, the output will go high and remain high until the selected count register is reloaded with the mode.

Reloading a counter register during counting results in the following:

(1) Load 1st byte stops the current counting.

(2) Load 2nd byte starts the new count.

The GATE input will enable the counting when high and inhibit counting when low.

Mode 1 Programmable One-Shot

The output will go low on the count following the rising edge of the GATE input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

Mode 2 Rate Generator

Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If

the count register is reloaded between output pulses, the present period will not be affected, but the subsequent period will reflect the new value.

The GATE input, when low, will force the output high. When the GATE input goes high, the counter will start from the initial count. Thus, the GATE input can be used to synchronize the counter. When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

Mode 3 Square Wave Rate Generator.

Similar to Mode 2 except that the output will remain high until one-half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts.

If the count register is reloaded with a new value during counting, this new value will be reflected immediately after the output transition of the current count.

Mode 4 Software-triggered strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

Mode 5 Hardware-triggered strobe

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

The format of the control byte is shown in table 5-9; the various bits in the control byte are defined by table 5-10. Counter 0 is not initialized by the Monitor during power-up. It is available for use at P5 and must be programmed, if used, in the same manner described above. There are two inputs (clock and gate) and one output available. A jumper is provided on the Evaluation Board for tieing the clock input to the same 2MHz clock used in channels 1 and 2.

The current counter values at each channel can be read while actively counting in the following manner: first, the control byte shown in table 5-11 is written to the control register (FE7) in order to latch the current value. Then the counter is read by addressing it as shown in table 5-12.

TABLE 5-9. Am8253 CONTROL BYTE FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

TABLE 5-10. Am8253 CONTROL BYTE DEFINITION

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL1	RL0	
0	0	Counter Latching operation
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, than most significant byte.

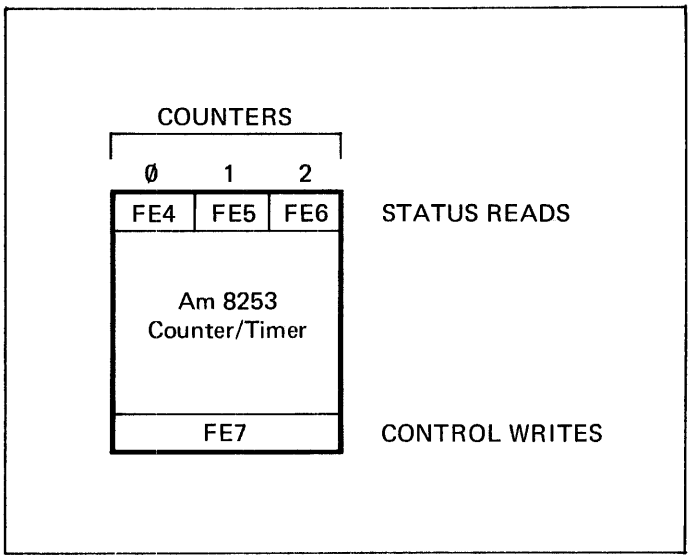
M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

TABLE 5-11. Am8253 CONTROL BYTE TO LATCH COUNT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

TABLE 5-12. Am8253 ADDRESSES



APPENDIX A
CPU BUS BUFFERING CHARACTERISTICS AT P2

The following output delay and input setup times need to be considered when interfacing external logic through the P2 edge connector.

P2 Pin	Delay (output)	Setup (input)
BUSREQ*		0ns
VI*		0ns
NVI*		0ns
MI*		0ns
STOP*		0ns
WAIT*		20ns
NMI		37ns
NREQ*	9ns	
BUSAK*	9ns	
R/W*	9ns	
N/S*	9ns	
B/W*	9ns	
AS*	9ns	
DS*	9ns	
ST_0-ST_3	9ns	
A_0-A_{15}	Valid at least 35ns before rising edge of AS*. Addresses remain valid at least 71ns after rising edge of DS*.	
D_0-D_{15}	Output valid within 66ns after falling edge of DS*. Input must be valid at least 93ns before falling edge of T3. It must remain valid until rising edge of DS*.	

APPENDIX B
ASCII CHARACTER SET

The ASCII internal character set used with the Evaluation Board is the ANSI X3.4 1968 version. The following is a summary.

Table B-1. ASCII

Hex	Dec	Char	Hex	Dec	Char	Hex	Dec	Char	Hex	Dec	Char
00	0	NUL	20	32	SP	40	64	@	60	96	`
01	1	SOH	21	33	!	41	65	A	61	97	a
02	2	STX	22	34	"	42	66	B	62	98	b
03	3	ETX	23	35	#	43	67	C	63	99	c
04	4	EOT	24	36	$	44	68	D	64	100	d
05	5	ENQ	25	37	%	45	69	E	65	101	e
06	6	ACK	26	38	&	46	70	F	66	102	f
07	7	BEL	27	39	'	47	71	G	67	103	g
08	8	BS	28	40	(	48	72	H	68	104	h
09	9	HT	29	41	)	49	73	I	69	105	i
0A	10	LF	2A	42	*	4A	74	J	6A	106	j
0B	11	VT	2B	43	+	4B	75	K	6B	107	k
0C	12	FF	2C	44	,	4C	76	L	6C	108	l
0D	13	CR	2D	45	-	4D	77	M	6D	109	m
0E	14	SO	2E	46	.	4E	78	N	6E	110	n
0F	15	SI	2F	47	/	4F	79	O	6F	111	o
10	16	DLE	30	48	0	50	80	P	70	112	p
11	17	DC1	31	49	1	51	81	Q	71	113	q
12	18	DC2	32	50	2	52	82	R	72	114	r
13	19	DC3	33	51	3	53	83	S	73	115	s
14	20	DC4	34	52	4	54	84	T	74	116	t
15	21	NAK	35	53	5	55	85	U	75	117	u
16	22	SYN	36	54	6	56	86	V	76	118	v
17	23	ETB	37	55	7	57	87	W	77	119	w
18	24	CAN	38	56	8	58	88	X	78	120	x
19	25	EM	39	57	9	59	89	Y	79	121	y
1A	26	SUB	3A	58	:	5A	90	Z	7A	122	z
1B	27	ESC	3B	59	;	5B	91	[	7B	123	{
1C	28	FS	3C	60	<	5C	92	\	7C	124	|
1D	29	GS	3D	61	=	5D	93	]	7D	125	}
1E	30	RS	3E	62	>	5E	94	^	7E	126	~
1F	31	US	3F	63	?	5F	95	_	7F	127	DEL

APPENDIX C
SERVICE PARTS AND SCHEMATICS

If it is necessary to return the Evaluation Board for service, contact the Service Manager for OEM Products at the telephone number listed below. A Return Material Authorization number be obtained prior to shipment. If the service requirement arises from damage during shipment from AMC, or the the board is out of warranty, a purchase order is required.

Repackage the board in the original packing material, or an equivalent substitute, and enclose in a corrugated carton suitable for shipping. Seal the shipping carton securely, mark it FRAGILE, and address to:

Advanced Micro Computers
Service Manager, OEM Products
3340 Scott Boulevard
Santa Clara, California 95051

TELEPHONE: (408) 988-7777

TOLL-FREE: (800) 672-3548
California

(800) 538-9791
U.S.A. (except Calif.)

A component location diagram for the Am96/4016 board is shown in figure C-1. Schematic diagrams are shown in figures C-2 through C-8.

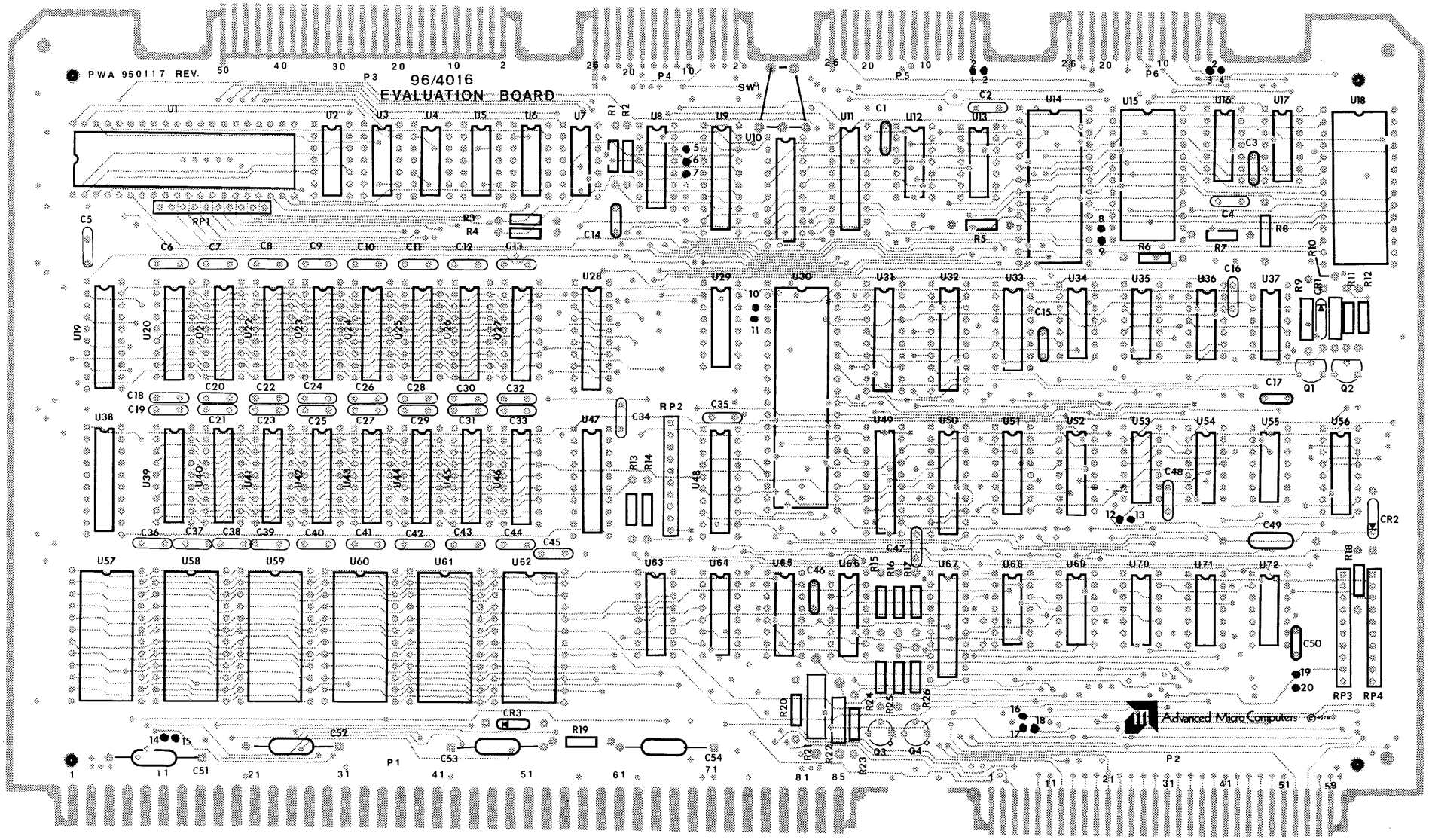


Figure C-1. Component Location Diagram

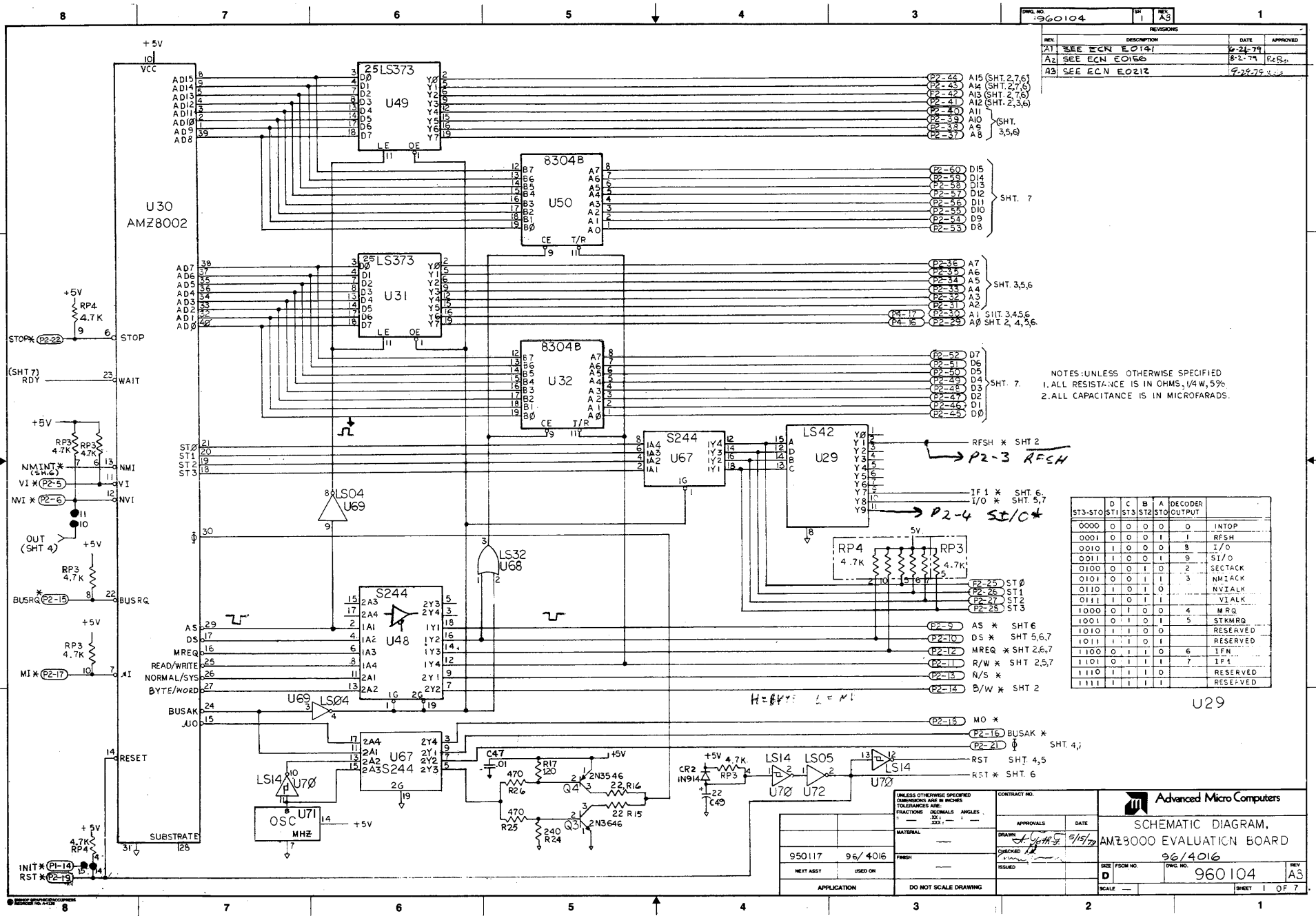


Figure C-2. Am96/4016 Schematic Sheet 1

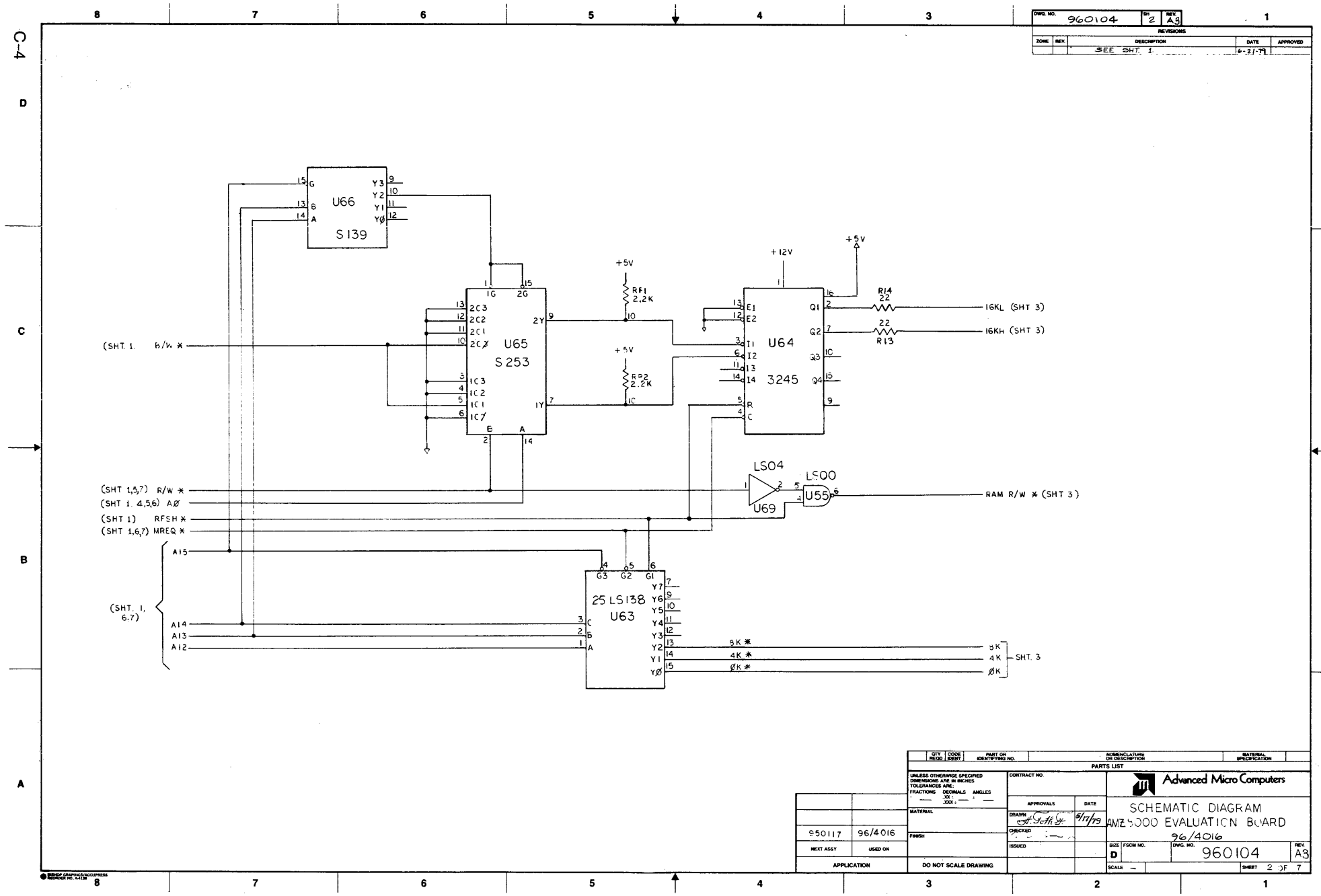


Figure C-3. Am96/4016 Schematic Sheet 2

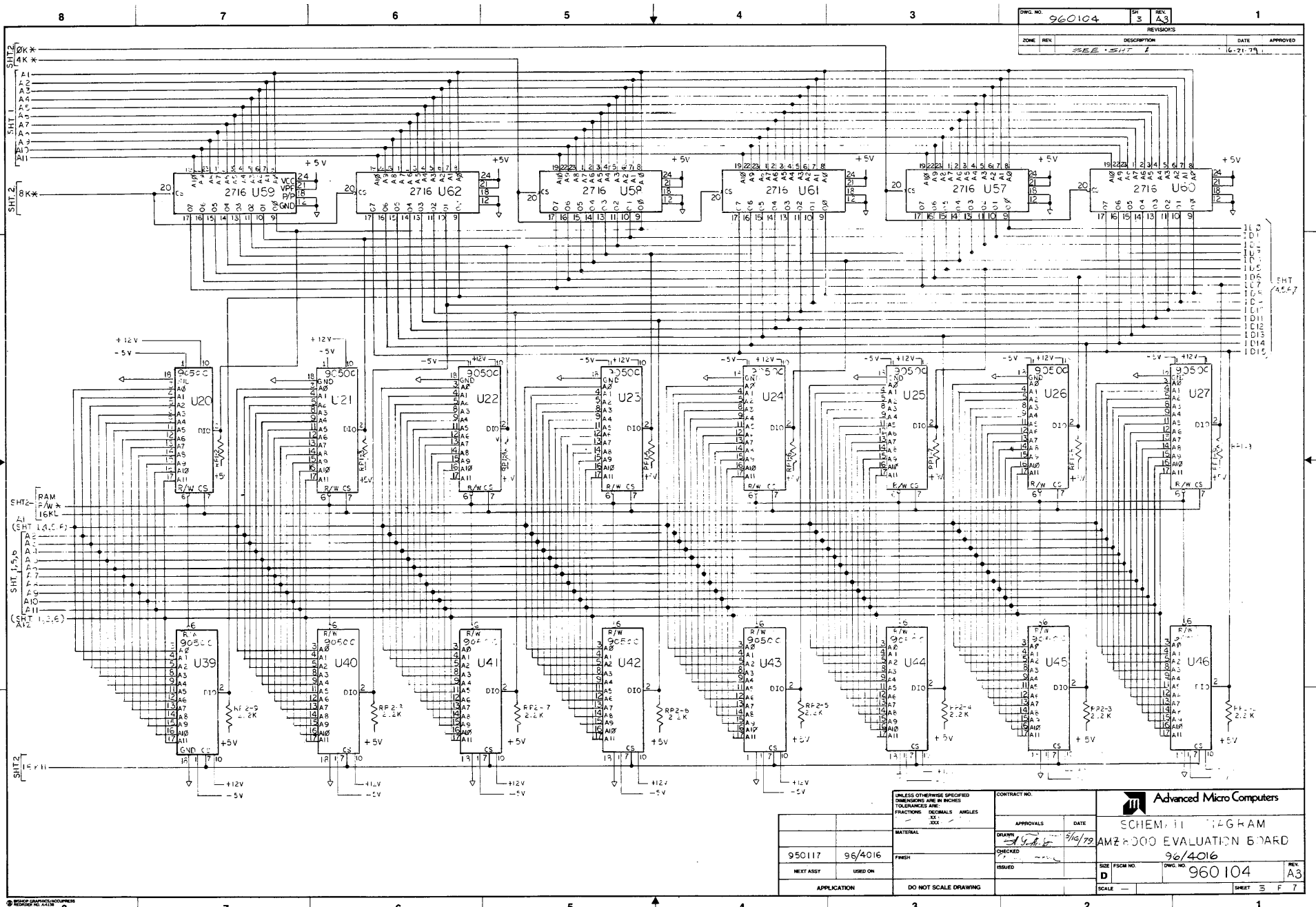


Figure C–4. Am96/4016 Schematic Sheet 3

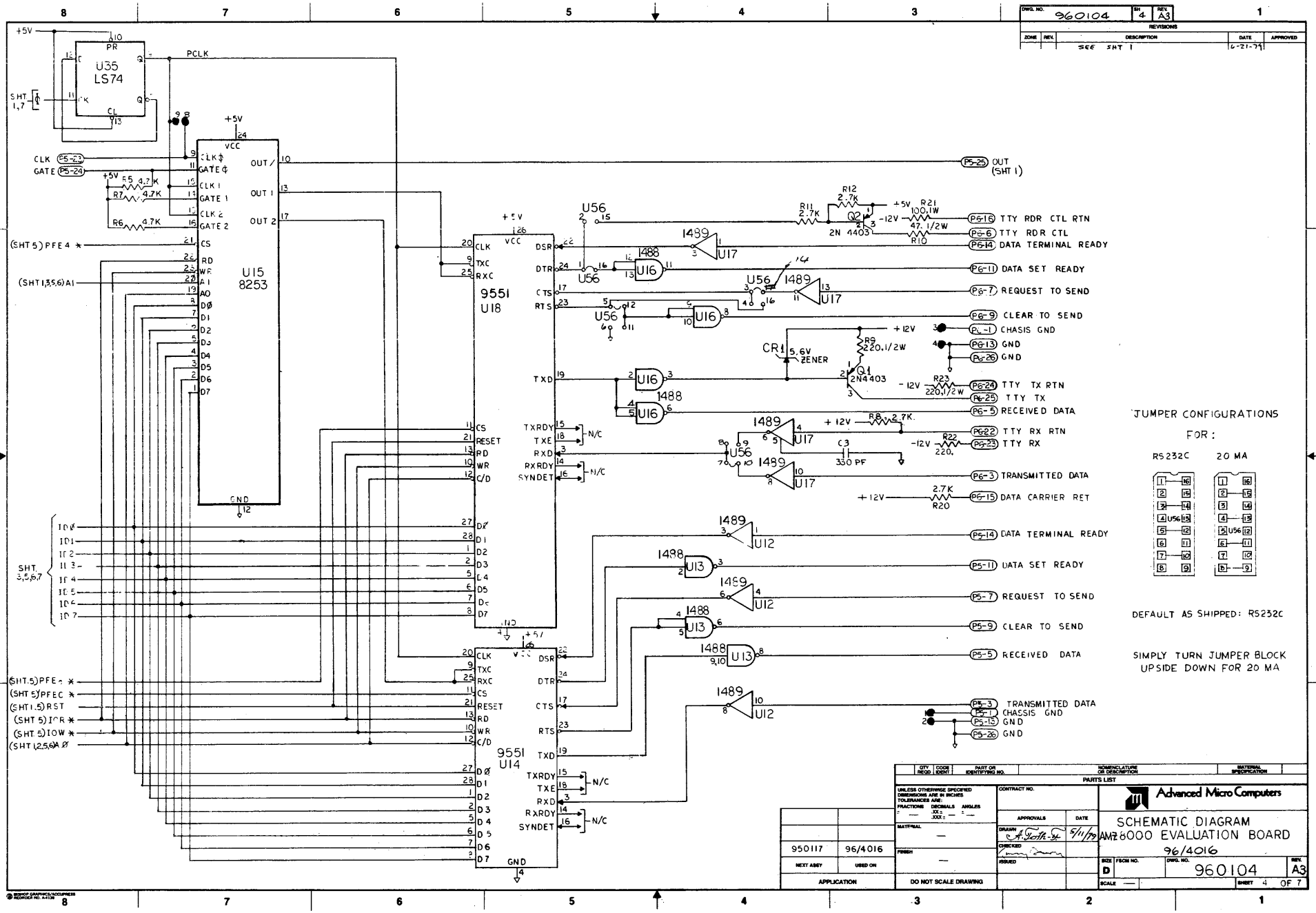


Figure C-5. Am96/4016 Schematic Sheet 4

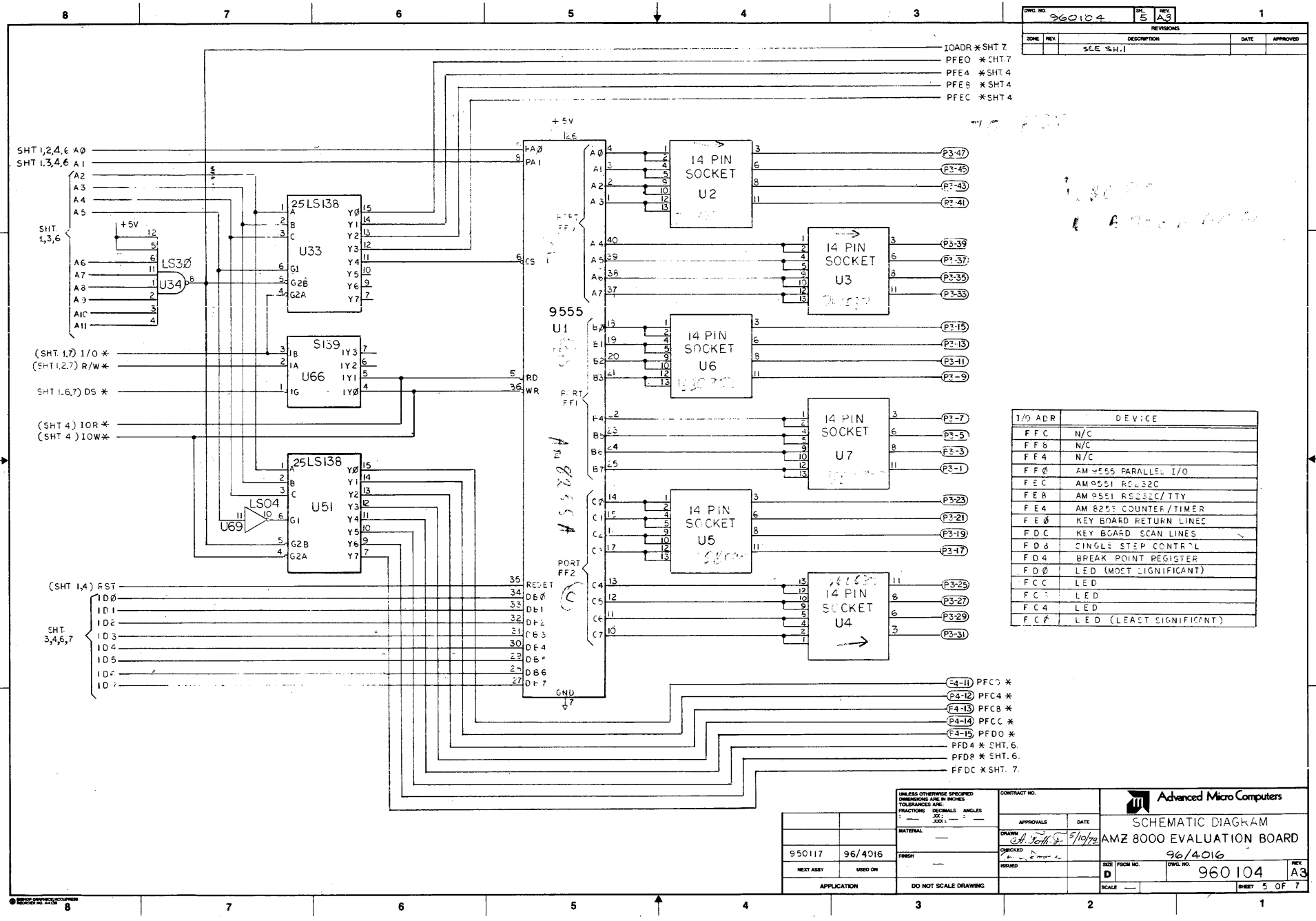


Figure C–6. Am96/4016 Schematic Sheet 5

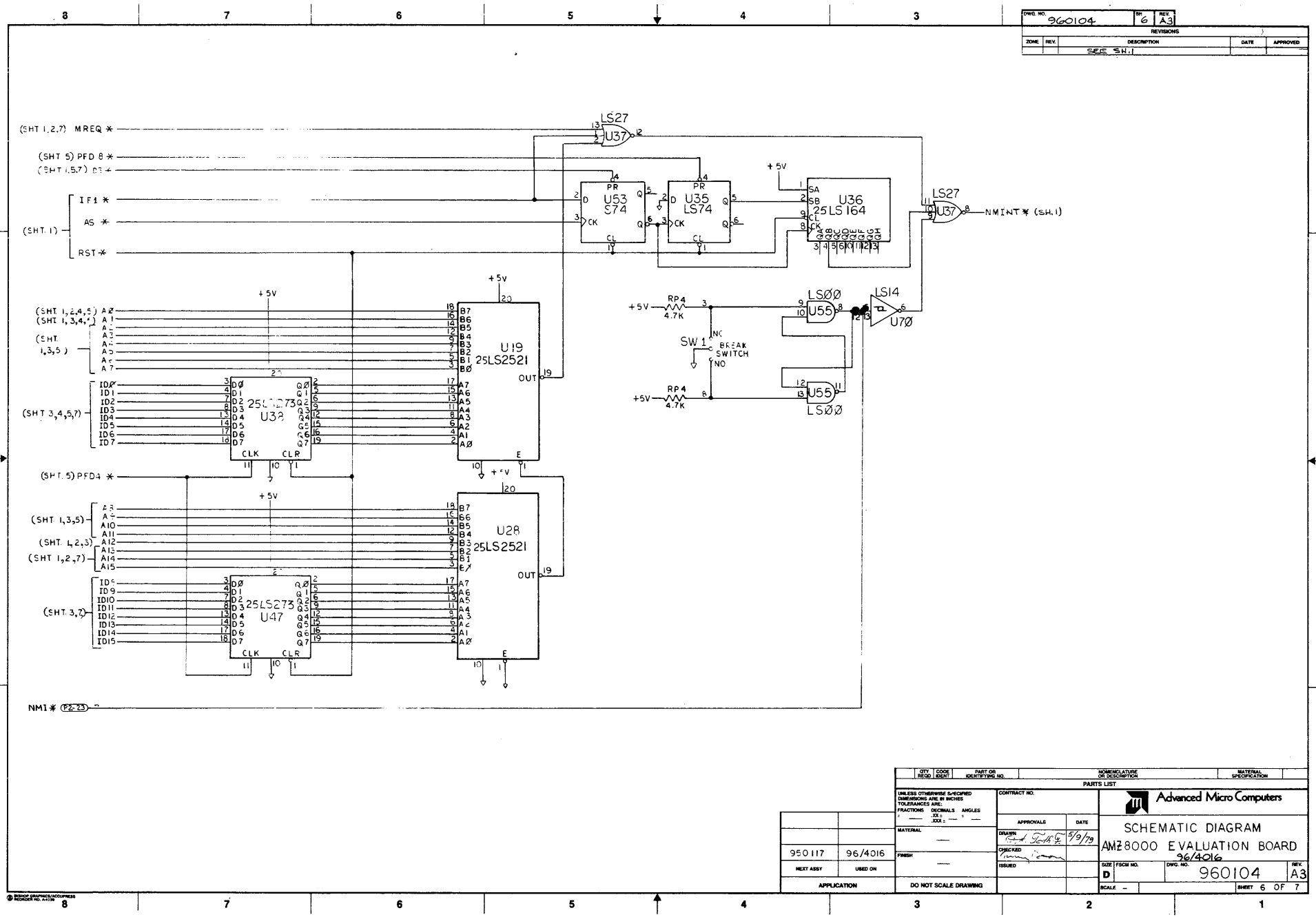


Figure C-7. Am96/4016 Schematic Sheet 6

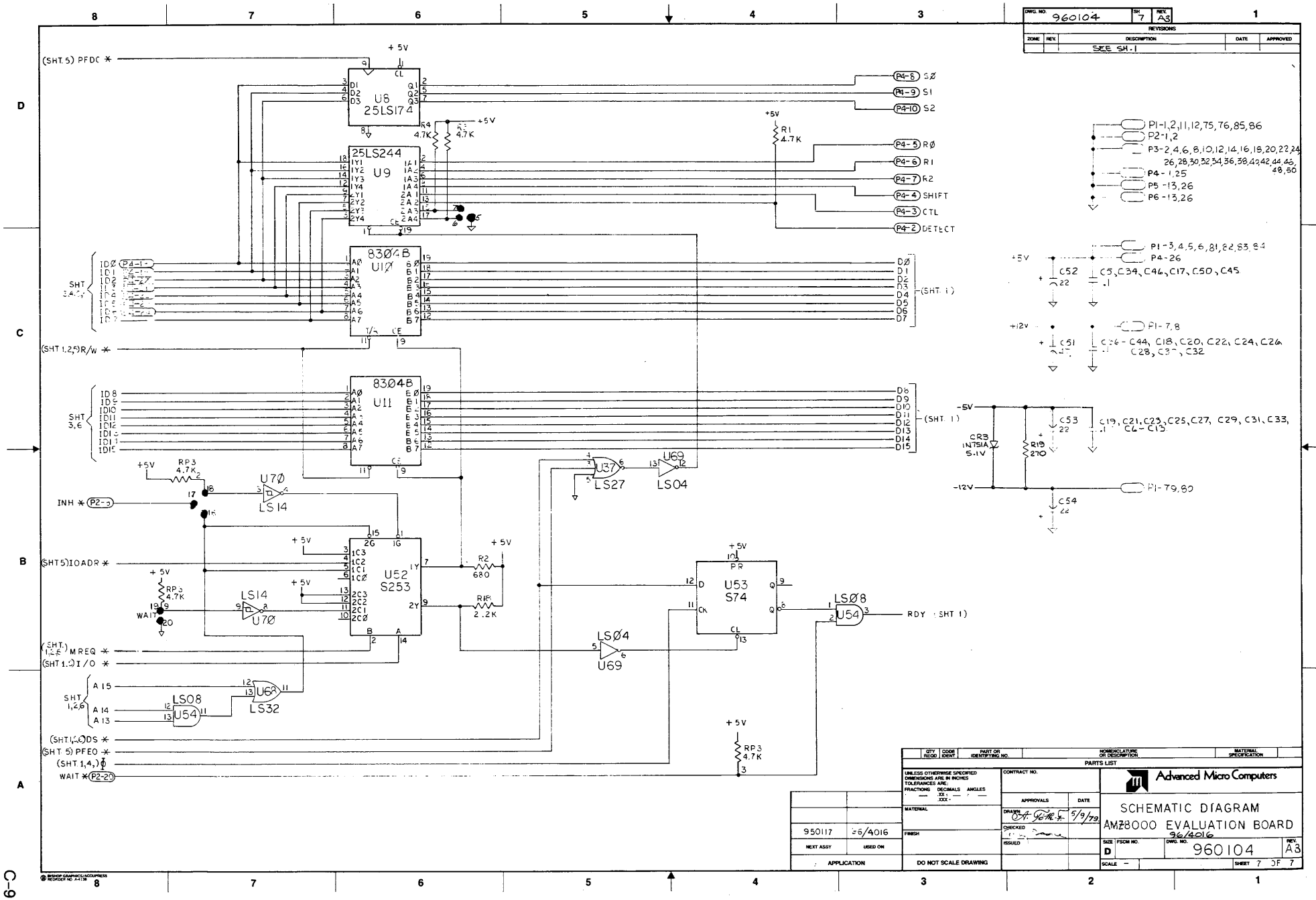


Figure C-8. Am96/4016 Schematic Sheet 7

COMMENT SHEET

Address comments to:

Advanced Micro Computers
Publications Department
3340 Scott Boulevard
Santa Clara, CA 95051

TITLE: Am96/4016 AmZ8000 EVALUATION BOARD USER'S MANUAL
PUBLICATION NO. 00680131 B

COMMENTS: (Describe errors, suggested additions or deletions, and include page numbers, etc.)

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