AMD-8132™ HyperTransport™ PCI-X® 2.0 Tunnel Revision Guide

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Trademarks

Revision History

Rev	Date	Description
3.02	9/2005	Changed erratum #35; Added B2 silicon information.
3.00	4/2005	Initial public release.

AMD-8132™ HyperTransport™ PCI-X® 2.0 Tunnel Revision Guide

The purpose of the *AMD-8132™ HyperTransport™ PCI-X®* 2.0 Tunnel Revision Guide is to communicate updated product information to system designers and software developers. The revision guide has three sections:

- **Revision Determination:** This section describes the mechanism used to identify the part's current revision.
- **Product Errata:** This section provides a detailed description of product errata including potential effects on system operation and suggested workarounds.
- **Documentation Support:** This section provides a listing of available technical support resources.

Revision Guide Policy

An erratum is defined as a deviation from product specifications which may cause the behavior of the AMD-8132™ HyperTransport™ PCI-X®2.0 tunnel to deviate from the published specifications. Occasionally, AMD identifies product errata. The erratum listed in this revision guide may be subject to periodic updates.

Revision Determination

When the BIOS checks the PCI revision ID register Dev[B,A]:0x08, the value in bits 7:0 identify the version of the silicon as shown in Table 1.

Table 1. AMD-8132™ HyperTransport™ PCI-X®2.0 Tunnel Revision IDs

Revision	Dev[B,A]:0x08
A1	01h
B1	11h
B2	12h

Product Errata

Within this section each product erratum for the AMD-8132™ HyperTransport™ PCI-X® 2.0 tunnel is assigned a unique tracking number for the convenience of tracking the errata within specific revision levels. Table 2 provides a cross-reference between the erratum and the different revisions of the part (identified by their silicon rev number). In Table 2:

- An x in a revision number column indicates the erratum applies to that revision.
- The absence of an x in a revision number column indicates the erratum does not apply to that revision.
- An asterisk (*) indicates advance information that the erratum has been fixed but not yet verified.

Table 2. Erratum to Product Revision Cross-Reference

Erratum	Revision		
	A1	B1	B2
24 Clock Gating May Cause Lost Transactions	X		
25 Inbound Memory Reads May Cause Inbound I/O Reads to Be Re-issued	X		
26 Bus Contention in Hot-Plug with External Arbiter	X		
27 Failure to Force Bad Parity or ECC	X		
28 Two Reads to the Same Address But With Differing Prefetch Settings Will Malfunction	X	X	X
29 PCI-X® Mode2 Category 1 Signals Driven During Reset	X		
30 PCI-X® Mode 2 I/O Pad Violates Specification	X		
31 Internal State May Be Corrupted During PCI/PCI-X® Hot-Plug Clock Changes if System or Comp Logic Is Not Quiescent	X		
32 Excessive Disconnect NOPs Driven in 16-Bit Mode	X		
33 Incorrect Values in CLASS2_MSG_IDX	X		
34 Unexpected Split Completion Error Log Bit Set Incorrectly	X		
35 PCI-X® Split Completion Errors Fail To Set RMA/RTA Bits		X	X

Table 2. Erratum to Product Revision Cross-Reference (Continued)

Erratum	Revision		
	A1	B1	B2
36 TPS2342 Interface Operating Above Max Frequency	X		
37 Outbound MemRdMult Causes Read Responses to Be Lost	X		
38 Upstream Split Transaction Capacity Is Incorrect	X		
39 Bus Can Be Placed in PCI-X® QDR Mode Even Though It Is Not Supported	X		
40 Secondary Buses Are Always Declared to Be 64 Bits Wide	X		
42 HyperTransport™ Outputs Are Not Driven to Proper Levels During JTAG EXTEST Operations	X		
43 Phase Shift on External PCI Clocks	X		
44 APIC ID and IOAPIC Arbitration ID Registers Only 4 Bits Wide	X		
45 PCI Bus Does Not Work with DIS64 Set	X		
46 Incorrect Tx Calibration Results	X		
47 SHPC A/B Serial Bus Operation Depends on Other Bus NSI Settings	X		
48 Sync Flood Causes False Message to Set CRCERR and Incorrect CRCERR Setting	X		
50 AMD-8132™ Tunnel Signal Name and Functionality Changes	X		
51 AMD-8132™ Tunnel Responds to HyperTransport™ Compat Traffic without Waiting for Compat PCI Bus Reset Deassertion	X		
52 PCI and PCI-X® Bursts and PCI Prefetches Aren't Properly Bounded	X		
53 Arbiter Can Starve PCI/PCI-X® Devices When AMD-8132™ Tunnel Buffers Are Full	X		
54 Extended Configuration Cycles Issued Incorrectly with Non-Default Extended Configuration Address Setting	X		

Table 2. Erratum to Product Revision Cross-Reference (Continued)

Erratum	Revision		
	A1	B1	B2
55 HyperTransport™ Tx Updates Can Overlap Rx Updates	X		
56 AMD-8132™ Tunnel Incorrectly Chains Certain Outbound Writes Causing Data Corruption	X		
57 Broadcasts Can Corrupt Posted Requests if One PCI Bus Clock Is 25 MHz and the Other Is 33 MHz	X		
58 SHPC[B,A]:14[BSY] Doesn't Clear When the PCI Bus Is Running at 25 MHz	X		
59 AMD-8132™ Tunnel Write Chaining Behavior Violates PCI Retry Re-issue Requirements	X		
60 SHPC PCI Initialization Pattern Violates Hold Time	X		
61 Error Log CSRs Can Be Incorrectly Set or Loaded by Discarded Split Completion Messages	X		
64 Instability at Nominal VLDT and VDDCORE Voltages	X		
65 PCI/PCI-X® Outputs Are Indeterminate Until VDDCORE Power Is Applied	X		
66 SHPC Hangs When 0x3C[SBRST] Is Asserted in PCI-X® Mode 2 with Hot-Plug Enabled	X		
67 AMD-8132™ Tunnel Unimplemented Registers	X		
68 PERR_OBSERVED and Received System Error CSRs Incorrectly Set by SHPC Bus Enable	X	X	X
69 Increased VLDT Power Supply Noise With Pre-Production Package	X		
71 Pre-production AMD-8132™ Tunnel Compensation Logic	X		
72 Back-Driven M66EN May Be Incorrectly Sampled	X	X	X
73 Incorrect Default Values in Reserved Registers		X	X

Table 2. Erratum to Product Revision Cross-Reference (Continued)

Erratum	Revision		
	A1	B1	B2
74 Incorrect Default Value in EXT_PCLK_DLY Register		X	X
75 AMD-8132™ Tunnel May Violate Conventional PCI Minimum Tval		X	X
76 Electrostatic Discharge Sensitivity On A_PCIXCAP And B_PCIXCAP Inputs		X	
77 Incorrect Bus Number Used In PCI-X® Attributes	X	X	X

24 Clock Gating May Cause Lost Transactions

Description

Transactions may be lost if clock gating, as controlled by DevA:0xF0 bits 18 and 7:0, is enabled.

Potential Effect On System

The system hangs.

Suggested Workaround

Do not enable clock gating.

Fix Planned

Yes

25 Inbound Memory Reads May Cause Inbound I/O Reads to Be Re-issued

Description

To avoid returning stale data to the PCI bus in the midst of a delayed read, the AMD-8132™ tunnel contains logic to discard reads when a burst for one delayed read is disconnected at the address of another outstanding delayed read. However, the address compare performed between the various outstanding delayed reads only looks at the address and does not take into account whether the various reads are to memory or I/O space. Memory read bursts may collide with outstanding I/O reads causing the I/O reads to be discarded, which violates section 3.3.3.3.3 of *PCI Local Bus Specification, Rev 2.3*.

Potential Effect On System

Inbound I/O traffic is not likely to occur on most systems. In the unlikely case that it does occur, repeating the discarded I/O reads may cause undesired side effects, including system hangs or crashes.

Suggested Workaround

Do not populate the system with devices using peer-to-peer I/O reads with side effects. Peer-to-peer traffic using memory-mapped IO is not a problem.

Fix Planned

Yes

26 Bus Contention in Hot-Plug with External Arbiter

Description

When using hot-plug in external arbiter mode, the hot-plug controller takes an additional clock cycle to relinquish the bus which may cause bus contention.

Potential Effect On System

Transaction corruption on the PCI bus and possible system failure.

Suggested Workaround

The external arbiter should wait an extra clock cycle between removing grant from hot-plug and asserting grant to the next device. There should be a minimum of two clock cycles between removing the hot-plug grant and asserting the grant to the next device.

Fix Planned

Yes

27 Failure to Force Bad Parity or ECC

Description

AMD-8132™ tunnel support for HyperTransport™ packets indicating data errors, as defined in section 10.2 of *HyperTransport™ I/O Link Specification, Rev 1.05*, is incomplete.

HyperTransport packets with the Data Error bit set may not be correctly forwarded to PCI as poisoned data. Uncorrectable data errors on PCI may not be correctly forwarded to HyperTransport with the Data Error bit set.

Note: This erratum does not cause any loss of error detection. For example, it does not prevent detection or reporting of parity or ECC errors on the PCI/PCI-X® bus. This erratum indicates that data errors may not be correctly forwarded.

Potential Effect On System

Data errors may not be correctly forwarded or poisoned, allowing the possibility that erroneous data can arrive at its destination prior to the system seeing and responding to the error indication.

Suggested Workaround

None

Fix Planned

Yes

28 Two Reads to the Same Address But With Differing Prefetch Settings Will Malfunction

Description

The AMD-8132™ tunnel may malfunction if multiple conventional PCI requestors with differing prefetch enable CSR settings on one of its secondary buses are attempting to read the same address simultaneously.

Potential Effect On System

The AMD-8132 tunnel may return incorrect data, hang, or otherwise malfunction.

Suggested Workaround

The PFEN[4:0]_L per-requestor prefetch enable CSR bits Dev[B,A]:0x40[12:8] should be set to the same value, either all asserted or all deasserted.

Fix Planned

No

29 PCI-X® Mode2 Category 1 Signals Driven During Reset

Description

The AMD-8132™ tunnel is not in low-power mode during reset state in PCI-X® Mode 2 and drives all Category 1 signals to the electrical low state in violation of *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.

Potential Effect On System

None

Suggested Workaround

None

Fix Planned

Yes

30 PCI-X® Mode 2 I/O Pad Violates Specification

Description

For PCI-X® Mode 2, the 266 MHz specification calls for a maximum input capacitance of 4 pF. The AMD-8132™ tunnel capacitance may be slightly higher than the specification.

Potential Effects On System

High-speed signal fidelity may be compromised.

Suggested Workaround

This erratum is not expected to result in any failures. However, if failures are observed, the issue may be resolved by limiting the bus operating frequency to no more than 200 MHz.

Fix Planned

Yes

31 Internal State May Be Corrupted During PCI/PCI-X® Hot-Plug Clock Changes if System or Comp Logic Is Not Quiescent

Description

When a SHPC command causes the PCI clock speed to change, temporary erratic behavior of the PCI clock may cause some internal state to be corrupted and bad compensation settings to be sent to the HyperTransport™ PHYs and PCI I/O cells.

- The internal state corruption can occur if there is traffic in flight from HyperTransport to PCI, from PCI to HyperTransport, or from HyperTransport to internal CSRs.
- The bad compensation settings can occur if the HyperTransport compensation logic is in the midst of sending updated values to the HyperTransport PHY or PCI I/O cells.

Potential Effect On System

System hangs and data corruption are possible.

Suggested Workaround

The AMD-8132™ tunnel must be put into an idle state prior to issuing an SHPC Set Bus Segment Speed/Mode command that will cause the PCI clock speed to change. During this idle state, no traffic must be issued from this PCI bus to HyperTransport, from HyperTransport to this PCI bus, or from HyperTransport to internal CSRs related to this PCI bus (including HyperTransport interrupt acknowledges and polling SHPC[B,A]:16[BSY]).

Also during this idle state, compensation logic must be turned off to prevent compensation updates. The SHPC device driver provided by AMD automatically ensures this.

Fix Planned

Yes

32 Excessive Disconnect NOPs Driven in 16-Bit Mode

Description

When performing a link disconnect, *HyperTransport™ I/O Link Specification, Rev 1.05* requires that transmitters drive disconnect NOPs until CRC covering the first disconnect NOP is driven. Transmitters then continue driving disconnect NOPs for a minimum of 64 bit-times and a maximum of 400 ns following the CRC. If the link is 16 bits wide, the AMD-8132™ tunnel may drive NOPs beyond this 400 ns maximum. In the worst case, when the transmitter is running at 200 MHz disconnect NOPs are driven for a maximum of approximately 1500 ns instead of 400 ns. If LDTSTOP_L is de-asserted prior to the completion of these NOPs, the NOPs could be perceived as part of the link initialization sequence and prevent the link from re-initializing.

Potential Effect On System

16-bit HyperTransport™ links may not re-initialize after assertion of LDTSTOP_L.

Suggested Workaround

If the use of LDTSTOP_L is required, extend the LDTSTOP_L assertion period to 2.5 us (as opposed to the *HyperTransport™ I/O Link Specification, Rev 1.05* minimum of 1 us).

Fix Planned

Yes

33 Incorrect Values in CLASS2_MSG_IDX

Description

CLASS2_MSG_IDX does not log error correctly.

Potential Effect On System

Error-handling software that depends on the CLASS2_MSG_IDX value may not operate as expected.

Suggested Workaround

Error-handling software should not rely on data found in CLASS2_MSG_IDX.

Fix Planned

Yes

34 Unexpected Split Completion Error Log Bit Set Incorrectly

Description

When the AMD-8132™ tunnel receives an unexpected split completion (the tag does not match any that the AMD-8132 tunnel has outstanding) it will not assert DEVSEL_L, letting the unexpected split completion master abort on the PCI-X® bus. The AMD-8132 tunnel also incorrectly sets the Unexpected Split Completion (USC) error log bit Dev[B,A]:0x60[19]. This error log bit should only be set if a target asserts DEVSEL_L and discards the unexpected split completion. See *PCI-X Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*, section 5.2.5. Since the AMD-8132 tunnel will never assert DEVSEL_L for an Unexpected Split Completion, this CSR should never be set.

Potential Effect On System

Error-handling software may not operate as expected when Dev[B,A]:0x60[USC] is set.

Suggested Workaround

Error-handling software should ignore Dev[B,A]:0x60[USC].

Fix Planned

Yes

35 PCI-X® Split Completion Errors Fail To Set RMA/RTA Bits

Description

The AMD-8132™ tunnel Received Target Abort (RTA) bit Dev[B,A]:0x1C[28] is erroneously clear when the AMD-8132 tunnel issues a PCI-X® Split-Completion which target aborts on the PCI-X bus, violating section 8.7.1.3 of the *PCI-X® Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*. The AMD-8132 tunnel Received Master Abort (RMA) bit Dev[B,A]:0x1C[29] is erroneously clear when the AMD-8132 tunnel issues a PCI-X Split-Completion which master-aborts on the PCI-X bus, violating section 8.7.1.2 of the *PCI-X® Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a*.

Potential Effect On System

Error-handling software may not operate as expected.

Suggested Workaround

Error-handling software should not rely on the RTA and RMA bits if the Split Completion Discarded (SCD) bit Dev[B,A]:0x60[18] is set.

Fix Planned

No

36 TPS2342 Interface Operating Above Max Frequency

Description

The AMD-8132™ tunnel is intended to support the TPS2340A or the TPS2342 hot-plug controller. When the AMD-8132 tunnel is configured to interface to the TPS2342, the hot-plug serial interface runs at 16 MHz, which violates the 10 MHz maximum frequency requirement of the TPS2342. When the AMD-8132 tunnel is configured to interface to the TPS2340A, the hot-plug serial interface runs at 8 MHz, which does not violate the requirement of the TPS2340A.

Potential Effect On System

Devices in hot-plug slots controlled by the TPS2342 may not function correctly.

Suggested Workaround

For systems that do not require PCI-X® Mode 2 hot-plug slots, the TPS2340A should be used.

Fix Planned

Yes

37 Outbound MemRdMult Causes Read Responses to Be Lost

Description

Some internal state may be corrupted when the AMD-8132™ tunnel issues PCI Memory Read Multiple commands to one of its secondary PCI buses while inbound DMA reads are also in progress.

Potential Effect On System

If this failure occurs, the AMD-8132 tunnel may hang or fail to return requested read data to PCI devices attached to one of its secondary PCI buses.

Suggested Workaround

To prevent the AMD-8132 tunnel from generating PCI Memory Read Multiple commands, BIOS should verify the Dev[B,A]:0x0C[7:0] CACHE CSR value is not set to 0x08 (the preferred value is 0x10).

Fix Planned

Yes

38 Upstream Split Transaction Capacity Is Incorrect

Description

Dev[B,A]:0x68[USTC] is a read-only value of 0x0E, indicating that the AMD-8132™ tunnel can store 14 ADQs of downstream response data. The correct value for this field is 0x0D for 13 ADQs.

Potential Effect On System

None

Suggested Workaround

None

Fix Planned

Yes

39 Bus Can Be Placed in PCI-X® QDR Mode Even Though It Is Not Supported

Description

The AMD-8132™ tunnel may attempt to operate at quad data rate (QDR) if a PCI-X® Mode 2 QDR capable card is plugged into one of its secondary buses. However, the AMD-8132 tunnel is not expected to function correctly at that speed.

Potential Effect On System

System may hang or data may be corrupted.

Suggested Workaround

Do not place the buses into QDR mode or use PCI-X Mode 2 cards capable of QDR operation.

Fix Planned

Yes

40 Secondary Buses Are Always Declared to Be 64 Bits Wide

Description

The secondary PCI buses are generally 64-bits wide, but can be forced to 32-bits wide by setting the Dev[B,A]:0x40[DIS64] CSR. If Dev[B,A]:0x40[DIS64] is asserted, the Dev[B,A]:0x60[16] CSR (64-bit secondary bus) erroneously declares the bus to be 64-bits wide.

Potential Effect On System

None

Suggested Workaround

None

Fix Planned

Yes

42 HyperTransport™ Outputs Are Not Driven to Proper Levels During JTAG EXTEST Operations

Description

The HyperTransport™ differential outputs L[1,0]_CADOUT_H/L[15:0], L[1,0]_CLKOUT_H/L[1:0], and L[1,0]_CTLOUT_L0 are not driven to proper voltage levels during JTAG EXTEST operations. If the nets are unterminated, the voltage levels are nominally Vol=0 mV, Voh=400 mV. If the differential pairs are differentially terminated to 100 ohms, then the levels seen are nominally Vol=236 mV and Voh=355 mV.

Potential Effect On System

JTAG EXTEST operations may fail on L[1,0]_CADOUT_H/L[15:0], L[1,0]_CLKOUT_H/L[1:0], and L[1,0]_CTLOUT_L0.

Suggested Workaround

None

Fix Planned

Yes

43 Phase Shift on External PCI Clocks

Description

The phase interpolator used for skew-aligning the external PCI clocks is dependent on the value of IREF calculated by the HyperTransport™ compensation logic. Under some circumstances, a change in the calculated value of IREF causes an unintended phase shift on the external PCI clocks.

Potential Effect On System

PCI bus errors, indicated by parity errors, ECC errors, and system hangs.

Suggested Workaround

BIOS should read out the current calculated value of IREF, and then override subsequent calculations with this constant value as follows:

1) Read out the current value of Dev[B,A]:1xC8[16:13] (IREFADJ).

2) Write back to Dev[B,A]:1xC8 with this value in bits 16:13, and 2'b11 in bits 24:23 (IREFADJMODE).

Fix Planned

Yes

44 APIC ID and IOAPIC Arbitration ID Registers Only 4 Bits Wide

Description

The AMD-8132™ tunnel APIC ID register and IOAPIC Arbitration ID register only have 4 read-write bits (bits [27:24]). These registers should have 8 read-write bits (bits [31:24]).

Potential Effect on System

System configurations requiring more than 4 bits of APIC ID or IOAPIC ID are not supported.

Suggested Workaround

None

Fix Planned

Yes

45 PCI Bus Does Not Work with DIS64 Set

Description

The AMD-8132™ tunnel can corrupt data and/or cause parity/ECC errors on the attached PCI/PCI-X® bus if Dev[B,A]:0x40[DIS64] associated with that bridge is set.

Potential Effect On System

PCI/PCI-X bus data may be corrupted.

Suggested Workaround

Do not set Dev[B,A]:0x40[DIS64].

Fix Planned

Yes

46 Incorrect Tx Calibration Results

Description

HyperTransport™ calibration results can be incorrect when running the PCI clock at 133 MHz.

Potential Effect On System

Data could become corrupted, leading to CRC or system errors.

Suggested Workaround

Increase the CSR Dev[B,A]:1xCC[CALTIMELO] to 0x5.

Fix Planned

Yes

47 SHPC A/B Serial Bus Operation Depends on Other Bus NSI Settings

Description

The serial interface from the AMD-8132™ tunnel to the power controllers will not operate until both SHPC controller Number of Slots Implemented (NSI, SHPC[B,A]:0C bits [4:0]) register values are set to some value other than 0 if both SHPC controllers are enabled.

Potential Effect On System

Hot-plug commands hang if both SHPC controllers are enabled but one or both of the NSI register values are 0.

Suggested Workaround

Set both NSI registers to non-zero values before SHPC initialization.

Fix Planned

Yes

48 Sync Flood Causes False Message to Set CRCERR and Incorrect CRCERR Setting

Description

If a sync flood starts at the time when the AMD-8132™ tunnel is expecting a CRC packet, the AMD-8132 tunnel erroneously logs a CRC error.

Potential Effect On System

When a sync flood occurs a CRC error may be logged when, in fact, there was no CRC error prior to the sync flood.

Suggested Workaround

Ignore the log of the CRC error status bit if multiple error bits are set.

Fix Planned

Yes

50 AMD-8132™ Tunnel Signal Name and Functionality Changes

Description

The following signal name and functionality changes were made between initial and production silicon revisions:

Revision A*x*: Pin AA27 = A_GNT_L0/Dev[A]:0x48[PSLOW_L]. The Dev[A]:0x48[PSLOW_L] CSR value was Read Only and was loaded from this pin at the rising edge of PWROK.

Production B1 and Up: Pin AA27 = A_GNT_L0. The Dev[A]:0x48[PSLOW_L] CSR value is Read-Write. PCI/PCI-X® clocks on non hot-plug buses are affected by the CSR value after a secondary bus reset to that bus. PCI/PCI-X clocks on hot-plug buses are affected by the CSR value immediately if the SHPC[A]:0C Number Of Slots Implemented value is 0; otherwise it has no effect.

Revision A*x*: Pin AG14 = B_GNT_L0/Dev[B]:0x48[PSLOW_L]. The Dev[B]:0x48[PSLOW_L] CSR value was Read Only and was loaded from this pin at the rising edge of PWROK.

Production B1 and Up: Pin AG14 = B_GNT_L0. The Dev[B]:0x48[PSLOW_L] CSR value is Read-Write. PCI/PCI-X clocks on non hot-plug buses are affected by the CSR value after a secondary bus reset to that bus. PCI/PCI-X clocks on hot-plug buses are affected by the CSR value immediately if the SHPC[B]:0C Number Of Slots Implemented value is 0; otherwise it has no effect.

Revision A*x*: Pin W24 = A_GNT_L1/A_PCIX_100.

Production B1 and Up: Pin W24 = A_GNT_L1.

Revision A*x*: Pin AG13 = B_GNT_L1/B_PCIX_100.

Production B1 and Up: Pin AG13 = B_GNT_L1.

Revision A*x*: Pin U5 = SPARE01.

Production B1 and Up: Pin U5 = VDDOK.

Revision A*x*: Pin AB19 = SPARE02.

Production B1 and Up: Pin AB19 = PCIXA_100.

Revision A*x*: Pin AA19 = SPARE03.

Production B1 and Up: Pin AA19 = PCIXB_100.

Revision A*x*: Pin W27 = A_PCLK[4]/A_BUSEN_L.

Production B1 and Up: Pin W27 = A_PCLK[4]/A_BUSEN_L/VIOA_OVERRIDE_DELAY.

Revision A*x*: Pin Y1 = B_PCLK[4]/B_BUSEN_L.

Production B1 and Up: Pin Y1 = B_PCLK[4]/B_BUSEN_L/VIOB_OVERRIDE_DELAY.

Also see Erratum 69 Increased VLDT Power Supply Noise With Pre-Production Package.

Potential Effect On System

Printed circuit boards using the initial AMD-8132™ tunnel pinout will need to be updated to use the production pinout or to accommodate both pinouts.

Suggested Workaround

Not Applicable

Fix Planned

Not Applicable

51 AMD-8132™ Tunnel Responds to HyperTransport™ Compat Traffic without Waiting for Compat PCI Bus Reset Deassertion

Description

If the AMD-8132™ tunnel PCI bus A is the system compatibility bus and HyperTransport™ requests to the compatibility bus are received before PCI bus A reset has deasserted, the AMD-8132 tunnel returns responses as if those requests master aborted on the compatibility bus.

Potential Effect On System

Compatibility devices, such as a PCI southbridge or boot ROM, may not be found correctly after HyperTransport reset deassertion if they are attached to the AMD-8132 tunnel PCI bus A.

Suggested Workaround

The AMD-8132 tunnel PCI bus A should not be the system compatibility bus. A southbridge and boot ROM attached to the HyperTransport bus, or attached to a device other than the AMD-8132 tunnel, should be used if requests to the system compatibility bus cannot be delayed until after the AMD-8132 tunnel deasserts reset on its PCI bus A.

Fix Planned

Yes

52 PCI and PCI-X® Bursts and PCI Prefetches Aren't Properly Bounded

Description

If the AMD-8132™ tunnel receives either a read or write burst request from its secondary PCI/PCI-X® bus crossing from a region it would forward to the HyperTransport™ bus to one that it wouldn't, the AMD-8132 tunnel continues the burst until entirely forwarded to the HyperTranport bus. Conventional PCI prefetches issued by the AMD-8132 tunnel can also incorrectly cross address boundaries. The boundaries the AMD-8132 tunnel will erroneously cross are:

- Top of the 64-bit address space, wrapping to address 0.
- Top of the 40-bit memory space (FD_0000_0000h).
- Base of the non-prefetchable memory range, if enabled (defined by Dev[B,A]:0x20).
- Base of the prefetchable memory range, if enabled (defined by Dev[B,A]:0x24, 28, 2C).
- Base of the VGA memory range, if enabled (A_0000).

Potential Effect On System

PCI/PCI-X requesters and bridges should not generate read requests that cross any of these boundaries. However, write requests that cross boundaries can be performed through the process of write combining, which can occur at any bridge in the system. Should writes that are intended for different address spaces (one above the bridge and one below) get combined, the writes to the spaces below are forwarded to HyperTransport, leading to potentially unpredictable behavior. Conventional PCI prefetch reads issued by the AMD-8132 tunnel that cross any of these address boundaries can also cause unpredictable behavior.

Suggested Workaround

None needed because correctly behaving devices will not cross these address boundaries.

Fix Planned

Yes

53 Arbiter Can Starve PCI/PCI-X® Devices When AMD-8132™ Tunnel Buffers Are Full

Description

The PCI-X® bridge arbiter uses a round robin protocol for selecting between external masters and internal requests. If all eight nonposted request buffers are consumed by external masters, then the following starvation scenario is possible:

1. The PCI-X tunnel is granted the bus by the arbiter for a split completion to the PCI-X bus for an outstanding nonposted request. As a result of this split completion, there are seven outstanding nonposted requests.
2. The arbiter grants the bus to a first master. This master generates a nonposted request. As a result, all eight nonposted request buffers of the bridge are occupied.
3. The arbiter grants the bus to a second master. This master generates a nonposted request. However, since all nonposted request buffers of the bridge are occupied, this request is retried by the PCI-X tunnel.

This sequence can repeat indefinitely.

Potential Effect On System

PCI-X bus bandwidth may be granted to external masters unevenly.

Suggested Workaround

System BIOS should program the Maximum Outstanding Split Transactions field of the PCI-X command register in external masters such that a master cannot be starved. See Table 3.

Table 3. Maximum Outstanding Split Transactions

Number of Masters	1ST Master	2ND Master	3RD Master	4TH Master
1	8			
2	4	4		
3	2	3	3	
4	2	2	2	2

Fix Planned

Yes

54 Extended Configuration Cycles Issued Incorrectly with Non-Default Extended Configuration Address Setting

Description

If the AMD-8132™ tunnel DevA:0xB4 Extended Configuration Address Range register is changed from its default value, extended configuration reads or writes claimed by the AMD-8132 tunnel can be issued to the secondary bus with an incorrect PCI/PCI-X® command encoding.

Potential Effect On System

Extended configuration writes could write to memory space addresses. Extended configuration reads could return incorrect data.

Suggested Workaround

Do not change the DevA:0xB4 Extended Configuration Address Range register from its default value.

Fix Planned

Yes

55 HyperTransport™ Tx Updates Can Overlap Rx Updates

Description

Large changes in HyperTransport™ Tx compensation override values can cause the system to hang.

Potential Effect On System

HyperTransport Tx calibration fails and eventually the system hangs.

Suggested Workaround

Do not use the CSR Dev[B,A]:1xC0[TXADJMODE].

Fix Planned

Yes

56 AMD-8132™ Tunnel Incorrectly Chains Certain Outbound Writes Causing Data Corruption

Description

The AMD-8132™ tunnel write chaining logic can incorrectly chain two outbound writes if the two writes meet all the specified requirements for write chaining and the addresses of the two writes satisfy both of the following conditions:

1. Both writes have the same value for address bit 7.
2. The starting address of the second write would appear to immediately follow the address of the last doubleword of the first write if address bit 7 was ignored.

Potential Effect On System

Data corruption can occur. The second write will not be written to the correct address, but will overwrite addresses subsequent to the first write.

Suggested Workaround

Do not set the WriteChainEnable Dev[B,A]:0x40[31].

Fix Planned

Yes

57 Broadcasts Can Corrupt Posted Requests if One PCI Bus Clock Is 25 MHz and the Other Is 33 MHz

Description

When the A_PCLK and B_PCLK frequencies are set to 25 and 33 MHz (or vice-versa), broadcast commands can cause the posted channel to experience internal flow control problems.

Potential Effect On System

Loss of posted writes directed to the PCI/PCI-X® buses, data corruption, and hangs are all possible.

Suggested Workaround

Do not simultaneously run the two PCI buses at 25 and 33 MHz.

Fix Planned

Yes

58 SHPC[B,A]:14[BSY] Doesn't Clear When the PCI Bus Is Running at 25 MHz

Description

The AMD-8132™ tunnel SHPC hangs if software issues the Power On command to SHPC and the PCI bus is running at 25 MHz. If software does issue the Power On command to the SHPC, the SHPC will perform the operation to the slot but it doesn't clear the SHPC[B,A]:14[BSY] bit and doesn't send the command completion interrupt.

Potential Effect On System

The system may hang when the hot-plug command is issued.

Suggested Workaround

Do not enable hot-plug when the PCI bus is configured to run at 25 MHz.

Fix Planned

Yes

59 AMD-8132™ Tunnel Write Chaining Behavior Violates PCI Retry Re-issue Requirements

Description

The AMD-8132™ tunnel can violate section 3.3.3.2.2 of *PCI Local Bus Specification, Rev 2.3*, if write chaining is enabled. A write issued by the AMD-8132 tunnel on its secondary PCI bus that is retried but transfers no data can be internally combined with subsequent writes by the AMD-8132 tunnel and re-issued with a command or REQ64# signal state different from the initial request.

Potential Effect On System

None known.

Suggested Workaround

Clear the WriteChainEnable bit Dev[B,A]:0x40[31].

Fix Planned

Yes

60 SHPC PCI Initialization Pattern Violates Hold Time

Description

The AMD-8132™ tunnel violates the RST# to PCI-X® initialization pattern hold time of 50 ns if hot-plug is enabled. The SHPC in the AMD-8132 tunnel drives the PCI-X initialization pattern for twelve PCI clocks after slot reset deassertion while it is holding bus ownership by asserting its REQ# to the arbiter.

Potential Effect On System

None known.

Suggested Workaround

None required.

Fix Planned

No

61 Error Log CSRs Can Be Incorrectly Set or Loaded by Discarded Split Completion Messages

Description

If the AMD-8132™ tunnel receives a split completion message with an uncorrectable data error and data error checking is enabled (Dev[B,A]:0x3C, bit 16 is set), then message data that should be discarded can incorrectly set certain CSR log bits. Specifically:

- If the corrupt message data appeared to be a Class 2 message, the AMD-8132 tunnel incorrectly sets CLASS2_SCM_ERR (Dev[B,A]:0x80, bit 9).
- If the corrupt message data appeared to be a Class 2 message, the AMD-8132 tunnel incorrectly loads CLASS2_MSG_IDXHI (Dev[B,A]:0x80, bits [12:10]) and CLASS2_MSG_IDXLO (Dev[B,A]:0x80, bits [8:4]) with the message index.
- If the corrupt message data appeared to be a Class 1/Master Abort, the AMD-8132 tunnel incorrectly sets the secondary Received Master Abort bit (Dev[B,A]:0x1C, bit 29).
- If the corrupt message data appeared to be a Class 1/Target Abort, the AMD-8132 tunnel incorrectly sets the secondary Received Target Abort bit (Dev[B,A]:0x1C, bit 28).

Potential Effect On System

Error-handling software may read incorrect values in the error-logging CSR bits listed above.

Suggested Workaround

None

Fix Planned

Yes

64 Instability at Nominal VLDT and VDDCORE Voltages

Description

The AMD-8132™ tunnel has an internal hold time problem where certain signals cross from circuits powered by the VLDT power supplies to circuits powered by the VDDCORE power supply.

Potential Effect On System

The AMD-8132 tunnel may hang or corrupt data.

Suggested Workaround

Lowering the VLDT power supplies from their nominal 1.2 V levels to 1.1 V and raising the VDDCORE power supply from its nominal 1.2 V level to 1.3 V allows the AMD-8132 tunnel to operate correctly.

Fix Planned

Yes

65 PCI/PCI-X® Outputs Are Indeterminate Until VDDCORE Power Is Applied

Description

The AMD-8132™ tunnel PCI/PCI-X® I/O cells are powered by the V33 power supply, but are controlled by logic that is powered by the VDDCORE power supply. If V33 power is applied but VDDCORE power is not, the AMD-8132 tunnel PCI/PCI-X I/O cells can be in indeterminate states.

Potential Effect On System

Contention on the PCI/PCI-X signals between the AMD-8132 tunnel and PCI/PCI-X devices attached to it and incorrect assertion or deassertion of important signals such as RESET# and VIOEN before the VDDCORE power supply is applied.

Suggested Workaround

For AMD-8132 revisions that do not have a VDDOK input, the following power sequencing is recommended:

- V33, VDDA, VDDCORE, and VLDT power supplies should be ramped as close together as possible.
- VDDCORE and VLDT power supplies should always be less than the V33 power supply.
- VLDT power supplies should always be less than the VDDCORE power supply.

For PCI-X Mode 2 capable buses, the AMD-8132 tunnel PWROK input should not be asserted until VIO_A and/or VIO_B power planes are at ground (0V).

Fix Planned

Yes, with the addition of the VDDOK input whose function is described in the AMD-8132 tunnel data sheet.

66 SHPC Hangs When 0x3C[SBRST] Is Asserted in PCI-X® Mode 2 with Hot-Plug Enabled

Description

The AMD-8132™ tunnel can hang if [B,A]:0x3C[SBRST] is asserted to reset the secondary PCI bus when the targeting PCI bus is in PCI-X® Mode 2 and hot-plug is enabled.

Potential Effect On System

The system may hang because the AMD-8132 tunnel is not responding to any accesses to it.

Suggested Workaround

In a PCI-X Mode 2 capable system there is only one slot available in the PCI bus. The slot disable/enable hot-plug operation uses the same operation with the secondary bus reset. The system software/driver should use the hot-plug command instead of [B,A]0x3C[SBRST] to reset the secondary PCI bus.

Fix Planned

Yes

67 AMD-8132™ Tunnel Unimplemented Registers

Description

The following control and status registers (CSRs) listed in the AMD-8132™ tunnel data sheet were unimplemented in pre-production silicon:

Dev[B,A]:0x40, bit 24: MSIErrorFatalEn

Dev[B,A]:0x40, bit 25: MSIErrorNonfatalEn

Dev[B,A]:0x40, bit 26: POSTFPEN

Dev[B,A]:0x40, bit 27: NONPOSTFPEN

Dev[B,A]:0x40, bit 30: PCIMemWrBufMode

Dev[B,A]:0x48, bit 9: SCF25

Dev[B,A]:0x48, bit 10: PCIX100

Dev[B,A]:0x80, bit 14: DROPPED_MSI

Dev[B,A]:0x80, bit 15: SCM_Class2_DeviceSpecificError

Dev[B,A]:0x80, bit 16: SCM_Class2_ByteCountOutOfRangeError

Dev[B,A]:0x80, bit 17: SCM_Class1_TargetAbortError

Dev[B,A]:0x80, bit 18: PCI Busy Time Out Error

Dev[B,A]:0x80, bit 19: Primary Signalled Master Abort

Dev[B,A]:0x84, bit 0: SCM_Class2_DeviceSpecificErrFatalEn

Dev[B,A]:0x84, bit 1: SCM_Class2_DeviceSpecificErrNonfatalEn

Dev[B,A]:0x84, bit 2: SCM_Class2_ByteCountOutOfRangeFatalEn

Dev[B,A]:0x84, bit 3: SCM_Class2_ByteCountOutOfRangeNonfatalEn

Dev[B,A]:0x84, bit 4: SCM_Class1_TargetAbortErrFatalEn

Dev[B,A]:0x84, bit 5: SCM_Class1_TargetAbortErrNonfatalEn

Dev[B,A]:0x84, bit 6: Received Secondary Target Abort Fatal Enable

Dev[B,A]:0x84, bit 7: Received Secondary Target Abort Nonfatal Enable

Dev[B,A]:0x84, bit 8: Signalled Secondary Target Abort Fatal Enable

Dev[B,A]:0x84, bit 9: Signalled Secondary Target Abort Nonfatal Enable

Dev[B,A]:0x84, bit 10: PCI Busy Time Out Nonfatal Enable

Dev[B,A]:0x84, bit 11: PCI Busy Time Out Fatal Enable

Dev[B,A]:0x84, bit 12: Primary Signalled Master Abort Nonfatal Enable

Dev[B,A]:0x84, bit 13: Primary Signalled Master Abort Fatal Enable

Dev[B,A]:0x84, bit 14: Recieved Secondary Master Abort Nonfatal Enable

Dev[B,A]:0x84, bit 15: Recieved Secondary Master Abort Fatal Enable

Dev[B,A]:0x84, bit 16: Discarded Post Log Override

DevA:1xA0, bits 31: 0: Counter

DevA:1xA4, bits 31: 0: Counter

DevA:1xA8, bits 31: 0: Counter Control

DevA:1xAC, bits 31: 0: Counter Control

Dev[B,A]:1xD8, bit 28: RXUPDATE

Dev[B,A]:1xD8, bit 29: IREFUPDATE

Potential Effect On System

These registers and the functions they control are not available in pre-production AMD-8132 devices.

Suggested Workaround

None

Fix Planned

Yes

68 PERR_OBSERVED and Received System Error CSRs Incorrectly Set by SHPC Bus Enable

Description

The AMD-8132™ tunnel may incorrectly set Dev[B,A]:0x80[PERR_OBSERVED] and Dev[B,A]:0x1C[RSE] after the SHPC enables one of the PCI/PCI-X® secondary buses in single-slot mode.

Potential Effect On System

Dev[B,A]:0x80[PERR_OBSERVED] can cause:

- sync-flooding if Dev[B,A]:0x48[PERR Flood Enable] is set, or
- a fatal error interrupt if Dev[B,A]:0x48[PERR Fatal Enable] is set, or
- a nonfatal error interrupt if Dev[B,A]:0x48[PERR Nonfatal Enable] is set.

Dev[B,A]:0x1C[RSE] can cause:

- sync-flooding if Dev[B,A]:0x3C[System Error Enable] is set, or
- a fatal error interrupt if Dev[B,A]:0x48[SERR Fatal Enable] is set, or
- a nonfatal error interrupt if Dev[B,A]:0x48[SERR Nonfatal Error] is set.

Suggested Workaround

The following workaround is recommended when software issues a slot enable or enable all slots SHPC command in single-slot mode:

1. Save the current state of and then clear the following CSR enable bits: Dev[B,A]:0x3C[17] System Error Enable; Dev[B,A]:0x48[22] SERR Fatal Enable ; Dev[B,A]:0x48[21] SERR Nonfatal Enable; Dev[B,A]:0x48[20] PERR Flood Enable; Dev[B,A]:0x48[19] PERR Fatal Enable; and Dev[B,A]:0x48[18] PERR Nonfatal Enable.
2. Issue SHPC command.
3. When SHPC command is completed write a 1 to clear CSR bits Dev[B,A]:0x80[0] PERR_OBSERVED and Dev[B,A]:0x1C[30] Received System Error.
4. Restore the saved state of the following CSR enable bits: Dev[B,A]:0x3C[17] System Error Enable; Dev[B,A]:0x48[22] SERR Fatal Enable; Dev[B,A]:0x48[21] SERR Nonfatal Enable; Dev[B,A]:0x48[20] PERR Flood Enable; Dev[B,A]:0x48[19] PERR Fatal Enable; and Dev[B,A]:0x48[18] PERR Nonfatal Enable.

Fix Planned

No

69 Increased VLDT Power Supply Noise With Pre-Production Package

Description

AMD-8132™ devices using a pre-production package have separate balls for HyperTransport™ Link 0 and Link 1 VLDT power supplies. Package balls A14, B14, C14, P1, P2, and P3 provide power to HyperTransport Link 0 only. Package balls A16, B16, C16, P27, P28, and P29 provide power to HyperTransport Link 1 only.

Potential Effect On System

Increased noise on VLDT power supplies.

Suggested Workaround

None

Fix Planned

Yes. The production package has a single VLDT power plane that must be connected to a single VLDT power supply.

71 Pre-production AMD-8132™ Tunnel Compensation Logic

Description

Pre-production revisions of the AMD-8132™ tunnel have different PCI-X® Mode 2 compensation logic than the production revisions of the AMD-8132 tunnel have. The following control and status registers (CSRs) are implemented in pre-production silicon to contol its PCI-X Mode 2 compensation logic but are unimplemented reserved bits in the production revisions:

Dev[B,A]:0x80, bit 31: COMPOFFSETNADD

Dev[B,A]:0x80, bits 29:25: COMPAVGN

Dev[B,A]:0x80, bits 19:15: COMPOFFSETN

Dev[B,A]:0x88, bit 31: COMPOFFSETNADD

Dev[B,A]:0x88, bits 29:25: COMPAVGN

Dev[B,A]:0x88, bits 19:15: COMPOFFSETN

Potential Effect On System

These registers and the functions they control are not needed and do not exist in production AMD-8132 devices.

Suggested Workaround

None

Fix Planned

Yes

72 Back-Driven M66EN May Be Incorrectly Sampled

Description

Under certain conditions, some 66 MHz-capable conventional PCI devices back-drive the M66EN signal to ground. The AMD-8132™ tunnel may then sample this incorrect low level on M66EN at the assertion edge of the PWROK signal for such devices in non-hot-plug PCI slots. This problem does not occur in hot-plug PCI slots.

Potential Effect On System

The AMD-8132 tunnel can clock such PCI devices at 33 MHz rather than the desired 66 MHz.

Suggested Workaround

The 66 MHz-capable conventional PCI devices that exhibit this back-driving behavior do not all behave identically. In general, it is desirable for a system using these devices with the AMD-8132 tunnel to have the devices see stable power, PCI clocks, and PCI reset for as long as possible before the assertion edge of PWROK. It is recommended that the assertion edge of VDDOK precede the assertion edge of PWROK by at least 1 ms so that the AMD-8132 tunnel outputs, especially the PCI clocks, are enabled before M66EN is sampled.

Certain 66 MHz-capable conventional PCI devices whose back-driving of M66EN occurs if VIO is not powered to 3.3 V will not be sampled correctly by the AMD-8132 tunnel in a PCI-X® Mode 2-capable, non-hot-plug slot because VIO is not powered until after PWROK asserts. If PCI-X Mode 2 capability is not required, it is also recommended that VIO be powered to 3.3 V before the assertion edge of PWROK.

Fix Planned

No

73 Incorrect Default Values in Reserved Registers

Description

Default values in reserved registers Dev[B,A]:1x80 bits 9:5 and Dev[B,A]:1x88 bits 9:5 are incorrectly set to 0x12.

Potential Effect On System

Incorrect operation of the PCI-X® I/O cells when the secondary bus is in PCI-X Mode 2.

Suggested Workaround

BIOS should write Dev[B,A]:1x80 bits 9:5 and Dev[B,A]:1x88 bits 9:5 to 0x1F.

Fix Planned

No

74 Incorrect Default Value in EXT_PCLK_DLY Register

Description

The default value in register Dev[B,A]:1x7C bits 31:30 is incorrectly set to 2'b10.

Potential Effect On System

Reduced timing margin or timing violations on the AMD-8132™ tunnel secondary PCI/PCI-X® buses.

Suggested Workaround

BIOS should write Dev[B,A]:1x7C bits 31:30 to 2'b01 for optimal PCI/PCI-X timing.

Fix Planned

No

75 AMD-8132™ Tunnel May Violate Conventional PCI Minimum Tval

Description

The AMD-8132™ tunnel PCI/PCI-X® output signals in all PCI/PCI-X modes have a minimum Tval time of 0.7ns. The conventional PCI specification requires a minimum Tval time of 2ns.

Potential Effect On System

None expected. The conventional PCI specification allows 2ns of clock skew (Tskew), effectively resulting in 0ns of hold time to a PCI device (Tval - Tskew = 0ns). Systems implemented using the AMD-8132 tunnel should have much lower clock skew, especially systems designed to support PCI-X. Devices attached to the AMD-8132 tunnel with appropriately controlled clock skew should have sufficient hold time in conventional PCI mode.

Suggested Workaround

None required.

Fix Planned

No

76 Electrostatic Discharge Sensitivity On A_PCIXCAP And B_PCIXCAP Inputs

Description

The electrostatic discharge (ESD) protection on the AMD-8132 tunnel's A_PCIXCAP and B_PCIXCAP inputs can withstand a 300V charged device model (CDM) ESD event but may not meet AMD's 500V CDM ESD specification.

Potential Effect On System

A_PCIXCAP and B_PCIXCAP inputs may be damaged by ESD.

Suggested Workaround

Exposing the A_PCIXCAP or B_PCIXCAP inputs to CDM ESD events above 300V should be avoided during handling of AMD-8132 parts.

Fix Planned

Yes

77 Incorrect Bus Number Used In PCI-X® Attributes

Description

The AMD-8132 tunnel incorrectly issues PCI-X® requests on its secondary PCI-X buses using its secondary bus number as the Requester Bus Number in the PCI-X attribute bus phase, instead of its primary bus number. This is a violation of section 8.4.3.1.3 "Conventional PCI to PCI-X Attribute Creation" of the *PCI-X Protocol Addendum to the PCI Local Bus Specification*, revision 2.0a.

Potential Effect On System

If a PCI-X device on the AMD-8132 tunnel's secondary bus is configured to have the same attributes (bus number, device number = 0, function number = 0) that the AMD-8132 tunnel uses, data corruption or system hangs may occur if the PCI-X device and the AMD-8132 tunnel have operations using the same tag outstanding at the same time.

Suggested Workaround

None needed. Device number = 0 is reserved for the source bridge on a PCI-X bus so no conflicts should occur.

Fix Planned

No

Documentation Support

For specific information about the AMD-8132 tunnel and its operation see the *AMD-8132™ HyperTransport™ PCI-X®2.0 Tunnel Data Sheet,* order# 26792.

Specifications and protocols used in designing the AMD-8132 tunnel are as follows:

HyperTransport™ I/O Link Specification, Rev 2.00

PCI-X® Protocol Addendum to the PCI Local Bus Specification, Rev 2.0a

PCI-X® Electrical and Mechanical Addendum to the PCI Local Bus Specification, Rev 2.0a

PCI Local Bus Specification, Rev 2.3

PCI Hot-Plug Specification, Rev 1.1

PCI Bus Power Management Interface Specification, Rev 1.1

PCI-to-PCI Bridge Architecture Specification, Rev 1.1

PCI Standard Hot-Plug Controller and Subsystem Specification, Rev 1.0

TPS2340A Dual-Slot PCI Hot-Plug Power Controller Product Data

82093AA I/O Advanced Programmable Interrupt Controller (IOAPIC) Product Data

Other useful documents are:

PCI-to-PCI Bridge Architecture Specification, Rev 1.2 (DRAFT)

HyperTransport™ I/O Link Errata, Rev 1.05c (HTC200335-0024-0005)

HyperTransport™ I/O Link Errata, Rev 1.05b (HTC200335-0024-0003)

HyperTransport™ I/O Link Errata, Rev 1.05a