Designing for Electromagnetic Interference (EMI) Compliance

AMD

Application Note

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This application note describes how to integrate any microprocessor or microcontroller into an embedded system successfully while maintaining electromagnetic interference (EMI) compliance. It does this by providing an understanding of the system parameters that affect EMI. The discussion includes theoretical concepts that are helpful to the systems designer as well as practical system solutions. For example, it discusses how to bypass noisy integrated circuit (IC) pins for more effective noise containment, and how to improve utilization of the ground plane to reduce signal loop inductance. The application note includes a case study that demonstrates the concepts presented.

INTRODUCTION

We are reminded of the importance of EMI compliance every time we take off or land in an airplane and are instructed by a flight attendant to turn off all electronic devices. This request on the part of the airline suggests that the electromagnetic energy radiated by our laptops and personal digital assistants (PDA) might do anything from induce noise in the pilot's headset to interfere with the airliner's avionics. In any case, the requirement to keep electronic systems from interfering with one another is fully agreed upon and, therefore, should be of interest to all designers.

The subject of radiated emissions is a concern to most electrical engineers, especially those that design embedded consumer electronic devices that must pass EMI compliance (e.g., FCC Class B) testing to be approved for sale. This discussion focuses specifically on the emissions radiated by a system that are propagated through space and measured by an antenna and receiver.

Passing certification for EMI compliance can be very challenging with today's products. Minimal enclosures, high-speed digital circuitry, and lots of I/O cabling can create real problems for design engineers seeking to achieve compliance. Also, today's microprocessors can often be a significant source of EMI energy in and of themselves. Microprocessors inherently produce a lot of EMI energy due to the nature of their architecture. Typically, a significant portion of the die area inside a microprocessor is switching states on the positive and negative edge of the core clock. CMOS gates momentarily short power and ground together as the gate changes states. This results from both transistors in the totem pole output structure being on momentarily during the transition. At AMD we realize that microprocessors are inherently noisy devices. Our engineers continue to make progress in this area by designing quieter devices. However, we also realize that achieving EMI compliance is a systems issue. By systems, we mean circuit board layout. Layout, or the system design, does have an impact on EMI performance. Therefore, to assist the electronic device designer in achieving system compliance, AMD provides this application note as a guide to the process.

This application note discusses theoretical issues, then discusses more practical topics. If you are starting a new design, read the entire application note. If you are a few weeks from a ship deadline and are wondering how you are going to get your design to pass after it failed miserably on the first attempt, skip to "What To Do If You Had To Ship Yesterday" on page 4. Then read the rest when you go on to your next design, so you can avoid a repeat of that stressful predicament.

Because EMI compliance is a systems issue, we must first address the enclosure. Some designs do not have enclosures. We will address this later. For now, it is instructive to know the theory behind having a good enclosure.

GAUSS' LAW AND ENCLOSURES

Do you remember Gauss' Law? We can use Gauss' Law to mathematically define the goal of no electromagnetic interference emanating from the system of interest. This definition helps us get a handle on what exactly we are trying to do.

Gauss' Law states,

$$\oiint D \bullet dA = Q$$

where *D* represents flux density. Flux density is the electric field *E* multiplied by the permittivity of the medium through which the field is passing. That is, the electric field strength *E* is altered by the permittivity of the medium through which it is passing. *D* is simply *E*

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without the complication of what the medium is doing to the field strength. *dA* is an element of an arbitrary surface. *Q* is the total charge enclosed. Gauss' Law states that the surface integral of the dot product of the flux density and the enclosure surface area is equal to the charge enclosed.

That is, the total field strength emanating from an arbitrary enclosure is equal to the charge enclosed. Gauss' Law is interesting because it shows that we can establish an earth ground in or, better yet, around our system. This is highly desirable because the important property of an earth ground is that no matter how much current we put into or take out of it, its potential does not change. This is also important because if the enclosure potential does not change, then it does not radiate. At low frequencies, this can be accomplished by simply making use of the earth ground from the wall outlet. However, at any frequency much beyond audio, the inductance in the power cord defeats the low impedance of this earth ground. This leaves us with the task of establishing a local radio frequency (RF) earth ground.

Using Gauss' Law, we can make a simple observation. If the only currents flowing into or out of the enclosure are differential, then the charge *Q* enclosed by the system is a constant. Differential current is defined as current going in opposite directions at the same rate, such that the charge *Q* enclosed by the system is constant at any point in time. Contrast this with common mode current which is not constant at any point in time. If *Q* is a constant, then by Gauss' Law we can see that the field strength emanating from the enclosure at any point in time must be a constant. Moreover, if the enclosure is a good conductor, the potential across the surface at any point in time is constant. Because at any point in time there can be no potential variation, and because over the surface of the enclosure the total field strength emanating from the enclosure is constant, then there is no AC variation in the potential of the enclosure surface and it is, therefore, an RF earth ground that does not radiate.

It is critical to note that only differential currents are allowed for an RF earth ground to be established. Signals leaving the enclosure that carry information by design are only differential. Or, stated another way, all signals leaving the system that are of any interest, unless you are building a radio, are differential in nature.

One of the properties of differential signals is that there is no net charge transfer at any point in time associated with them. Because conductive enclosures have uniform potential all across their surface, and if there is no net current leaving the system, then by Gauss' Law the system conductive enclosure is a local earth ground. By defining the problem mathematically, this discussion illustrates that EMI compliance is absolutely a systems issue. We see that the behavior of the system I/O can have a dramatic effect on the integrity of the system earth ground and enclosure radiation. The goal is a seamless conductive enclosure surrounding the electronics with any I/O carrying only differential currents. It is understood this goal may be too lofty for many reasonable endeavors; however, it is good to know what the ideal is before departing from it.

Because many systems do not have the luxury of an enclosure, we will deal with this in "Circuitry and Layout" on page 3.

INDUCTANCE

It is now pertinent to define inductance. Having a good understanding of inductance is critical to making excellent PCB layouts that inherently minimize EMI.

Rather than bring up more calculus, let's look at the simple formula for the inductance of a single loop coil.

$$(B \times A)/I = L$$

where *L* is inductance of the loop, *I* is current in the loop, *A* is the area of the loop, and *B* is the magnetic field in the loop. The magnetic field exists due to the current in the loop. This we cannot change. But it is easy to see that if the loop area is reduced, then the inductance is also reduced. It is instructive to note that the magnetic field currents reinforce inside the loop and cancel outside the loop. This is easy to demonstrate using the right-hand rule. So the lesson here is: trace inductance can be minimized by minimizing loop area. What does this mean in terms of the practicality of PCB layouts? Well, it means something very strange to the uninitiated.

As the frequency of the signal goes up, the return current path found in the ground plane or power plane (the power plane is an AC ground) tends to be found directly under the signal trace, even if the signal trace snakes around on the board. This seems strange at first, but the return current is following the path of least resistance so to speak, or in our case, of least impedance. As the frequency goes up, the path of least inductance is the path with the least loop area. If ground plane exists under the signal trace, then directly under the signal trace is the path of least inductance. This is important to keep in mind when laying out a PCB. Cuts in the ground plane, such as those caused by closely spaced signal vias, can greatly increase trace inductance and EMI because *B*, the magnetic field produced by the current *I*, reinforces inside the loop but cancels outside the loop.

Another area where inductance can really hurt is with decoupling capacitors. First, vias add significantly to trace inductance—more on this later. Also, due to lead inductance, decoupling capacitors have a self-resonance. Below the self-resonance frequency the

decoupling capacitor acts like a capacitor with its impedance decreasing as the frequency increases. The impedance of the capacitor hits a minimum at the resonant frequency and then starts becoming inductive and, therefore, begins to rise as the frequency increases. The resonant frequency of common decoupling capacitors can be surprisingly low. For ceramic capacitors with X7R dielectrics (do not use Z5U dielectrics for high-speed decoupling), the resonant frequency for a 0.1 µF capacitor is 7 MHz. For a 0.01 µF capacitor, the resonant frequency is 70 Mhz. For a 0.001 µF capacitor, the resonant frequency is greater than 500 MHz. It becomes obvious that the choice of the type and size of decoupling capacitor, as well as its layout, can be crucial to success. It is best to have a mixture of sizes with larger values sprinkled around for storage and lots of smaller values for fast response to current transients. Watch placement and vias! We cover this in greater detail in the following sections.

CIRCUITRY AND LAYOUT

We now examine the actual system circuitry and recommended layout techniques.

Again, EMI must be viewed as a system problem where every circuit board, power bus and plane, component and connector location, signal trace, and cable combine to form a noise source and an antenna. Microcontrollers and other ICs that drive high-speed digital circuitry qualify as noise sources. But these noise sources must have an amplification mechanism to propagate an electromagnetic field out into space. The circuit board traces and cables connected to the microcontroller pins act as an antenna, amplify the microcontroller noise, and propagate the electromagnetic energy out into space.

To reduce radiation levels, we must first take a broader view of everything in our system. Start by simply identifying each component as either part of the noise source or part of the antenna. Almost everything in the system is part of the antenna. The antenna is a complex mechanism created by IC lead frames, circuit board signal and power traces, and cables. The product layout is important because everything in it affects the overall gain of the antenna and, therefore, the radiated energy emitted from the product.

In general microcontrollers are noise sources, and circuit board traces and cables are antennas. All microcontrollers potentially generate noise and, therefore, radiate to some degree. Some are worse than others, but no matter which microcontroller you use, an antenna with a high efficiency (high gain) can amplify this noise to the point of exceeding EMI limits. Even microcontrollers advertised as “reduced EMI” can easily be made noisy with a bad circuit board layout. There are two actions to take: 1) spoil the antenna, and 2) suppress the noise at the source. Of course, we want to do both.

ANTENNAS

Circuit board traces unintentionally create antennas—often resulting from compromises made by layout personnel in trace routing, component placement, and orientation. These compromises most often occur because of electrical functional changes, mechanical packaging requirements, or project schedules. The purpose of this discussion is to make the hardware and system designers more aware of these compromises and their effect on radiated emission performance.

Most of the current sourced by the high-speed microcontroller address and data pins are differential in nature, with the return path being through the system ground. The differential currents create fields that cancel one another outside the trace loop and, therefore, are not an EMI concern. However, a small high-frequency portion of the current sees this signal trace path as the highest impedance path (highest inductance) and determines that the path of least inductance is a capacitive (airborne) jump back to its source. This airborne jump creates and propagates an EMI field.

To better understand how circuit board traces and cables accidentally act like antennas, we need to understand that inductance makes an antenna efficient (high gain) because of the voltage developed across the inductance at higher frequencies. This voltage drives common mode current in the antenna resulting in radiated EMI. Inductance increases as the area enclosed by the loop increases. A monopole antenna can be created by a circuit board trace that has a large loop area when referenced to its return path or ground. The idea is to remove the inductance by decreasing the loop area. The loop area is decreased by adding ground closer to the signal traces. Adding ground planes helps the most because they affect all signal traces including power.

The case study beginning on page 6 demonstrates the benefits of multiple ground planes. It is a good example because it is a four-layer board that goes to the extreme in adding ground plane, but pays off in significantly reduced radiated emissions.

The antenna effects of the circuit board traces propagate common mode current out from the microcontroller pins and amplify it. Stated another way, the lack of only differential current in the signal loop results in the generation of common mode current. Remember that current must return to its source in some way either differentially or in common mode form. We want only the differential form. Common mode current causes the propagation of the field into space because it does not maintain a constant amount of charge inside the system at any single point in time.

When only differential currents are established by an extremely low signal loop inductance, then common mode currents are automatically minimized. The explanation of Gauss' Law is important here because it helps us understand the importance of ensuring that the amount of charge does not change within the system (or enclosure) over time. This in turn ensures that the field strength emanating from the system remains constant and, therefore, does not propagate into space. This is the ideal. It is practically impossible to implement perfectly, but layout and grounding techniques discussed in this application note can significantly minimize the common mode currents.

We have described how important it is to reduce signal trace inductance and, therefore, reduce the noise amplification effects (i.e., antenna effects) of circuit board traces by adding ground in a way that squelches signal loop inductance. Simply put, this is accomplished by adding a close return path for each signal trace. Adding ground plane is the most effective technique because of its ability to cover all signal traces. Multiple ground planes that are stitched together to ensure equal potential are even better. The case study described on page 6 is a four-layer circuit board with two ground planes stitched together. All open areas between traces on signal layers are filled with ground and stitched to the adjacent ground plane. Components are positioned and oriented such that signal trace length is as short as possible, which opens new areas for even more ground fill. All four layers contain stitched ground plane directly under the microcontroller core with all signal I/O running out and away from the microcontroller package.

NOISE SOURCES

Microcontrollers act as noise sources because of their large current-sourcing clock drivers and lead frame inductance. Manufacturers use techniques to minimize these problems, but system designers still have to contend with them. The clock drivers may generate noise, which can be seen at some level on all I/O pins, and can drive common mode current out onto the circuit board traces. The circuit board traces form loop antennas which, if not laid out carefully, have high inductance due to a large loop area and, therefore, increase the antenna's gain.

Capacitors on any and all of the microcontroller pins hold the voltage levels more stable and, therefore, help prevent the propagation of common mode current out onto the circuit board traces. This is why in the case study on page 6, power supply and microcontroller I/O pin bypassing is very effective. Also, address and data pins may not allow much more capacitance than 100 pF to be added without signal degradation, but this is enough to make a big difference in EMI performance, as the case study demonstrates. Location of these bypass capacitors also is critical. The closer they are to their respective IC pins, the more effective they are.

The top reflow side is one of the ground layers that works effectively because it also provides a good solid low-impedance ground for all bypassing capacitors. Adding a bypass capacitor is a waste of time if it is connected to its respective IC pin with a long skinny trace that has high inductance.

WHAT TO DO IF YOU HAD TO SHIP YESTERDAY

This section describes system grounding improvements and the addition of bypassing capacitors to reduce radiated emission energy. "Bypassing and ground? I already do that," you say. At AMD we have analyzed many of our customers' system designs and each time we found that many layout improvements could be made by adding capacitive bypassing and ground, and by creating a local system earth ground.

Add Capacitive Bypassing and Ground

Bypassing and ground go hand-in-hand because you cannot adequately achieve effective bypassing without an effective ground. This mean that a bypass capacitor has a smaller effect of voltage stabilization with an inductor between it and the IC pin it is bypassing. The circuit board trace acts like an inductor. And at higher frequencies, the inductor's impedance grows larger. Designers sprinkle their design with capacitors but see no effect because the placement is simply too far away from the IC pin being bypassed. Even a via hole between the IC pin and the bypass capacitor limits the bypass capacitor's effectiveness. The most effective bypass capacitor resides as close to its associated IC pin as physically possible with its other end connected directly to the system ground plane. A ground plane on the same circuit board layer as the IC is sometimes a good idea for the purpose of easily grounding bypass capacitors in a low impedance manner relative to the IC ground pin. The ground plane provides the lowest impedance path back to the IC ground pin. Placing the bypass capacitor on the same layer as the IC's ground plane eliminates a via hole between the capacitor and the IC pin and, therefore, makes it much more effective as a noise filter. Also, having the bypass capacitor physically close to the IC pin to be filtered and to the IC ground pin provides containment of the RF noise close to the IC package.

This concept of "noise containment" to the IC package is very important because it can be used on any pin of any IC where RF noise exists. This applies not only to power supply pins but also to I/O pins of a microcontroller or any other CMOS device. Select the capacitor value carefully to avoid compromising signal integrity. Typically, the highest value capacitor that can be placed

on the IC pin that still maintains signal integrity provides the most effective radiated emissions reduction.

Multiple ground planes can also further decrease the system signal return path impedance. In systems that have few connections to the power plane, two ground planes can be used in place of one power plane and one ground plane. You can achieve improved EMI performance by using two ground planes stitched together to form parallel return paths. These parallel return paths for bypass capacitors and IC signals provide an even lower impedance return path.

To make the largest impact on EMI performance, you must bypass all noisy IC pins. This includes, but is not limited to, the power supply pins. Highly active address and data pins of an embedded microcontroller are typical sources of noise due to inadequate system ground and placement of micro and memory ICs far apart with long trace lengths. The address and data lines of embedded microcontrollers running with internal bus speeds of 40 to 50 MHz can typically drive 50- to 100-pF worth of capacitance without signal degradation. The intent here is threefold: 1) contain noise by placing the bypass capacitor close to the noisy IC pin and ground pin, 2) slew the signal edge (thereby reducing the high-frequency content), and 3) stabilize the voltage at the IC pin.

Create a Local System Earth Ground with Ground Planes

As discussed during the explanation of Gauss' Law, theoretically you can establish an effective earth ground within any system using a conductive enclosure. A conductive enclosure can operate as an effective earth ground due to its low inductance characteristics; however, weight, size, and cost considerations restrict many products to plastic enclosures or housings that cannot be utilized as electric return paths. You also can establish an effective earth ground within the circuit board itself with a single ground plane or, even better, multiple ground planes stitched together with many vias. The use of a solid ground plane or multiple ground planes stitched together offers every IC and component connected to it a more stable reference. Multiple planes can also act as an effective enclosure and act as an EMI shield by placing noisy circuit board traces on a plane in between the two ground planes. The case study demonstrates the use of multiple ground planes and their ability to improve the effectiveness of all bypass capacitors (noise suppression), and to reduce the trace inductance of the entire system, including signal and power.

Further, as mentioned during the discussion of Gauss' Law, maintaining only differential (versus common mode) currents is also an important aspect in creating a local earth ground. Again, the low impedance of a conductive enclosure aids this effort and at the same time prevents the common mode current. As previously discussed, ground planes, which encourage differential mode current flow and restrict common mode current, can act as the enclosure. Reducing the common mode current is important because it takes such a small quantity to create enough radiated energy to fail to comply with FCC specifications. For example, within some systems, it only takes an estimation of 30 nA of common mode current to fail FCC Class B. 30 nA is an extremely small amount of current and can easily change based on system layout. The exact amount of common mode current each system generates depends on the noise characteristic of the components used and the system layout. Therefore, PCB layout is an extremely important factor in EMI performance. System layout parameters, including circuit board trace routing, power distribution, system ground, attached cables, and component locations, all play key roles in contributing to or reducing this common mode current and, therefore, radiated emissions.

Add ground plane wherever possible. Two-layer circuit boards make this very difficult; however, you can stitch together ground islands on both layers with vias so that all islands are electrically grounded to the system. Think of a two-layer design as a four-layer approximation, where ground islands are stitched together to approximate the performance of a solid unbroken ground plane on one layer. Ground planes should be as large as possible, run directly under high-speed signal traces, and not be broken with signal vias, signal traces, or cutouts. The "swiss cheese" effect of many signal vias passing through the ground planes can easily reduce the ground plane's effectiveness, so keep via hole diameters to a minimum. Slots and cutouts in the ground plane also increase ground inductance due to the longer path for the return current to get back to its source.

Less ground directly correlates to higher inductance and, therefore, higher antenna gain and, in turn, higher radiated emissions. Therefore, lower radiated-emissions performance requires more ground plane. Ground plane is not free. To obtain low radiated-emission performance, you must add more ground plane. If more planes are added, this could increase system costs. This is not to say that the current system configuration cannot be improved or optimized. Ground is only one item in the long list of layout considerations. However, with all other layout variables being equal, adding more ground correlates directly into lower radiated emissions.

The following case study demonstrates the effectiveness of utilizing the above-mentioned bypassing and grounding techniques.

EMI CASE STUDY

This case study documents the success of using certain capacitive bypassing and circuit board grounding techniques to reduce radiated emissions from a two-circuit board embedded electronic module. Customer requirements dictated stringent specifications for the radiated emission levels (i.e., 15 dBuV/m in the FM band).

The following sections describe what was done to reduce radiated emissions from this embedded microcontroller-based product.

Mechanization

This product consists of two circuit boards (display board and microcontroller board) connected by approximately four inches of discrete wire cable and mounted at a right angle relative to one another. Style requirements dictated a plastic housing, thereby eliminating the case as a source of shielding.

This product was tested at the component level using a three-meter harness to a passive load box to simulate the system loads.

The microcontroller has an internal phase-locked loop (PLL) to maintain the bus speed. It has integrated memory. A serial interface provides communication with the display board. And an integrated interface communicates with devices separate from this product. All serial interfaces were active during the radiated emissions testing.

Radiated Emissions Performance Development History

Originally, the designers used typical circuit-board construction methods. They constructed a four-layer microcontroller board containing the following layers, beginning with the reflow side on which the microcontroller, bus interface ICs, and voltage regulators were mounted.

Layer 1: Reflow component side: Signal layer.

Layer 2: Reflow inner layer: All ground layer (the ground plane).

Layer 3: Wave side inner layer: +5V supply plane.

Layer 4: Wave component side: Signal layer.

Lessons Learned From This Design

The designers made many circuit board turns attempting to make this design quiet. Unfortunately, surface-mounting processes in manufacturing required them to minimize the number of reflow components. This manufacturing requirement forced most surface mounted chips to be located on the wave solder side, including all the critical bypassing capacitors, therefore significantly reducing their effectiveness. Also, this design struggled due to the inadequate ground structure. It was not significantly improved until the designers replaced the +5V plane with another ground plane.

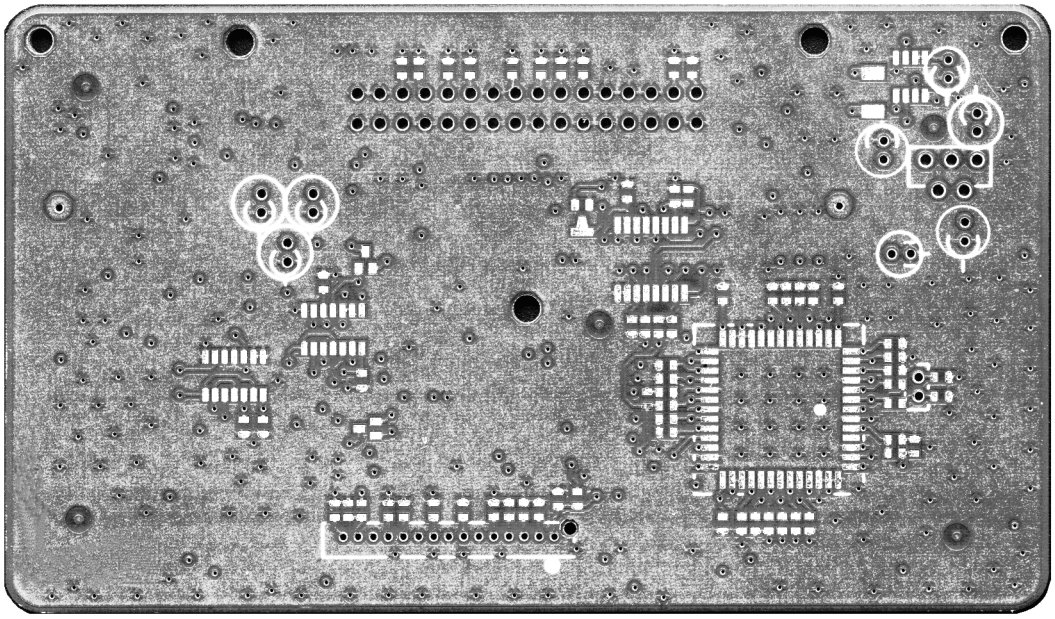
Two modifications to this design made the most improvement in reducing radiated emissions: more efficient bypassing and better ground structuring. The modifications resulted in the following layer arrangement.

Layer 1: Reflow component side: All ground layer (ground plane). See Figure 1 on page 7 for an image of the actual board.

Layer 2: Reflow inner layer: Signal layer.

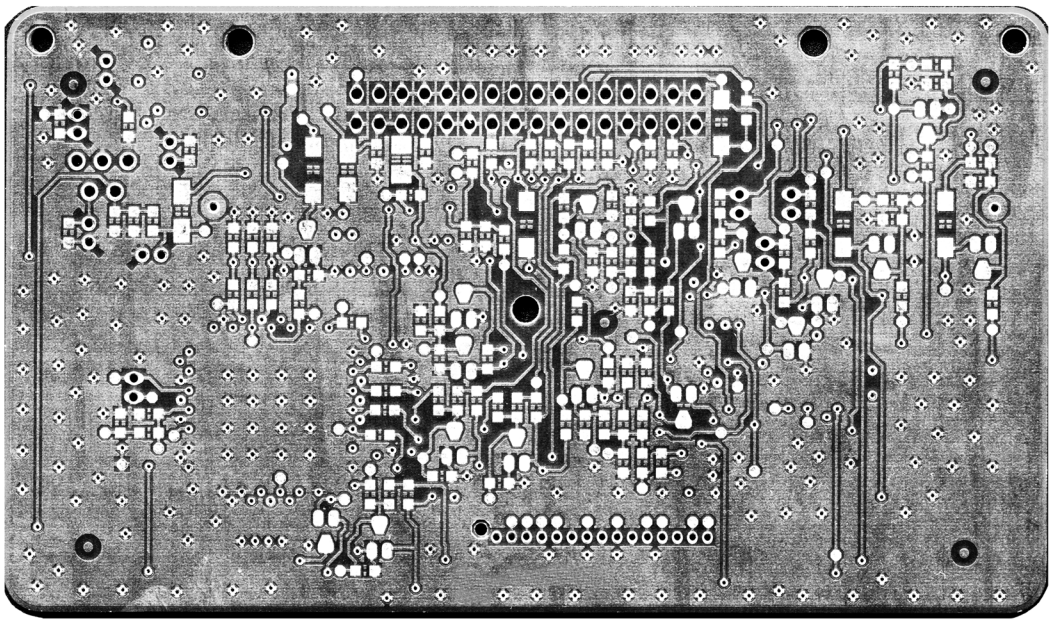
Layer 3: Wave side inner layer: All ground layer (ground plane).

Layer 4: Wave component side: Signal layer. See Figure 2 on page 7 for an image of the actual board.



Ground layer with bypass capacitors around controller and connector pins.

Figure 1. Reflow Component Side of Microcontroller Board



Signal layer with discrete components and ground fill, with many ground stitches used.

Figure 2. Wave Component Side of Microcontroller Board

Ground Structuring

The designers replaced the original +5V supply plane with another ground layer to lower ground return impedance. They used extensive ground stitching to connect the two ground planes together, further reducing ground impedance. They used ground fill in open areas on the signal planes. This new and improved ground structuring also increased the effectiveness of the bypass capacitors because the traces connecting them to their respective surface-mount IC did not have to go through the isolation impedance of a via hole. This circuit board layout provides its own shielding, a technique usable wherever external shielding cannot be used. All used microcontroller I/O pins have a via hole connecting the pin to its signal trace on the inner layer. Therefore, all signal traces with high-frequency content run on an inner layer sandwiched between the two ground layers.

Bypassing

The designers increased the overall amount of bypassing to include a bypass capacitor at every used I/O pin of the microcontroller and connector pins, as shown in Figure 3. They grounded all unused I/O pins. They kept the ground plane unbroken and solid on all four layers under the microcontroller package, and connected the four layers with sixteen ground stitch holes. All via holes and surface mount pads were thermally relieved to maintain manufacturing compliance.

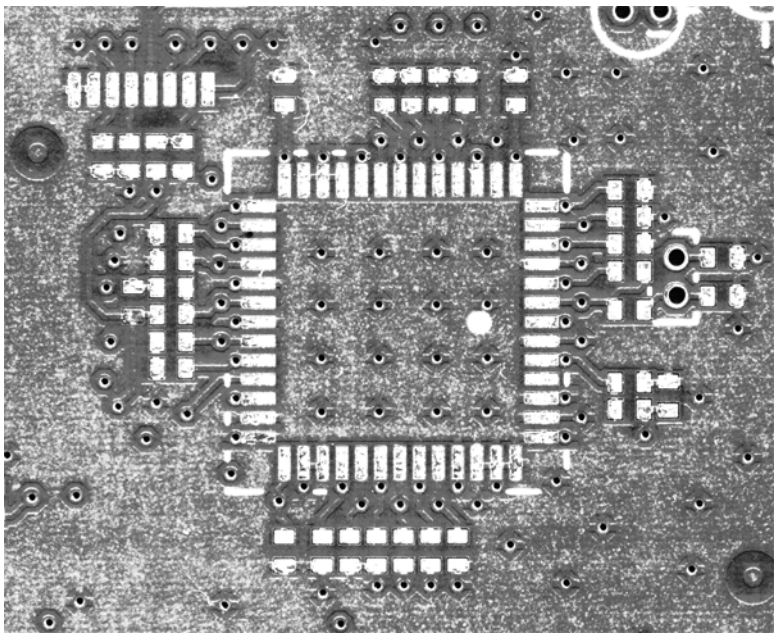
The first design had all I/O bypassing capacitors located on the wave solder side, forcing the I/O switching currents to travel through two via holes. This technique did not provide good emissions containment.

In the redesign, they moved the microcontroller I/O bypassing capacitors from the opposite side of the microcontroller to the same side as the microcontroller. This technique provided the lowest impedance path for the I/O switching current (noise current) to get from the microcontroller I/O pin to the microcontroller ground pin. Also, because layer 1 is a ground layer, placing the bypass capacitors on this layer makes routing the circuits a simple chore.

EMI Case Study Summary

This development work revealed that an improved circuit board layout and more effective bypassing can improve EMI performance. Radiated emission levels dropped from approximately 100 dBuV/m in the FM band for the original design to approximately 10 dBuV/m in the FM band, well within the customer specification of 15 dBuV/m.

These techniques have also been used on other embedded designs using other manufacturers' microcontrollers with the same reduction in emission levels, further validating this system-level EMI fix.



Solid unbroken ground under microcontroller package. Microcontroller signals run out to vias and down to the reflow-inner layer. Bypass capacitors are carefully placed very close to microcontroller signal pins and the reflow ground plane.

Figure 3. Microcontroller Area on Reflow Side

APPLICATION NOTE SUMMARY

We have discussed how EMI is a systems issue, because it requires a combination of both a noisy IC and a bad circuit board layout acting as the antenna to generate, amplify, and propagate EMI.

This application note shows that layout has a big impact on EMI performance, and that layout can be a very cost effective and manufacturable means of solving EMI problems. Layout changes can entail a slight modification of the current layout if you are 5dB to 10dB away from passing. Or, if you are 20dB to 30dB or more away from passing, you may actually save time by starting the layout over from scratch. In either case, you should determine how much you have compromised in the layout. Before your first circuit board goes into layout, you should analyze your design from an EMI point of view. Look at all aspects of the layout in terms of how it effects the overall EMI performance of the product. Start with the layout considerations listed below and add any others you feel may be important. Then sketch out preliminary drawings of where components should be placed on the circuit board and how they will be grounded and bypassed, keeping in mind IC package size, type, and pin pitch.

Typically, EMI is a balancing act. If your EMI performance is good, your layout is well balanced; if your EMI performance is poor, your layout is out of balance. What does it mean for a layout to be balanced? After you identify all the layout characteristics that are most important for your specific product, then you must incorporate each of these characteristics into the design with the appropriate emphasis on each, without compromise. When too many compromises are made, the layout is then out of balance.

Every product is different in so many ways that it is impossible to have a hard and fast rule for layout. Some products may be on a circuit board, others on flex circuitry. Some have multiple circuit boards connected in various ways to each other with an endless number of different cabling and attachment methods, while others are single board designs. Many products are connected to other products by a wide variety of communication mechanisms. Communications are usually not a problem if they have been designed with EMI in mind (which most of them are) and you comply with all the recommended layout guidelines suggested by the manufacturer. All these layout variables combine to make it an almost impossible task to identify what exactly you must do in layout to make your product EMI compliant. Each product must be analyzed independently and key layout characteristics identified to determine how to approach the layout.

Adding critical bypassing capacitors and ground plane structuring are the top two most important layout recommendations. However, you must evaluate other layout considerations as well. The best implementation of these top two layout recommendations depends on how adequately you incorporate the other layout guidelines.

The following is a general list of layout recommendations that must be considered as a whole. Spend a few extra days in layout, if necessary, to achieve the appropriate amount of emphasis on each of the following:

- Utilize a comprehensive ground structure, including the use and design of ground plane and attachment methods to each component within the system. The goal should be a low impedance grounding structure for all powered IC components, filtering devices, and signal traces. Consider multiple ground planes heavily stitched together to ensure they remain at the same RF potential. Consider ground plane on multiple layers underneath the microcontroller with many ground vias connecting them together.
- Determine the best layout for power routing to each IC, especially the microcontroller.
- Incorporate capacitive bypassing, including bypassing of all power supply IC pins and I/O pins.
- Consider grounding all unused I/O pins.
- Use as low clock frequencies as possible to minimize energy levels across the spectrum
- Keep all trace lengths as short as possible. Long traces make efficient antennas.
- Route traces so they run out and away from the microcontroller package instead of underneath it.
- Group external discrete circuits tightly together with all filtering components as close as possible to the device pin being protected. Remember to keep all trace lengths as short as possible.
- Consider placing all high speed and active peripherals (memory and communication ICs) close to the microcontroller with special attention given to their signal routing and return ground planes.
- Consider laying out with the option to add capacitive bypassing to the microcontroller and other IC I/O pins if necessary.
- Avoid “swiss cheese” effects on copper planes caused by large clearance holes around signal vias. Make your plane look like a solid plane with no slots or cutouts.
- Consider a ground plane on the reflow component side directly underneath all ICs with all filtering and bypassing components on this same side, grounded to this ground plane.
- Locate the microcontroller away from internal cables and jumpers. Dress any loose wiring or cables away from the microcontroller.