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TEST INTERFACE PORT

(TIP)

Schematics

REV 1.1

Sheet 2: Removed 1K pull down on AEN.
 Changed resistor values of R10 and R11.
 Added a Schottky Barrier Rectifier
 to power supply circuit.

Sheet 3: Added TRESET net to MACH.

Sheet 5: Changed resistor R66 form 10K to 0 ohm.

Sheet 6: Changed resistors R84 - R91 from 10K to 1K.

Sheet 7: Ground AVSS1 on U26.
 Added 1k pull up resistor to IOCHRDY signal.

Sheet 8: Changed SW_IRQ# nodename to MAIN_IRQ.

REV 1.2

Sheet 3: Replace 74HC4072 OR gate with 74HC21 AND gate.
 Removed pull down resistor R15 - R18 from
 shared interrupt signals.

Added a pull up resistor to the PARINT signal.

Sheet 4: Added a pull up resistor to the PEMD signal.
 while making the existing pull down resistor
 an optional populate resistor.

Sheet 8: Routed IOCHRDY and TIPFLHCS# nets to debug header

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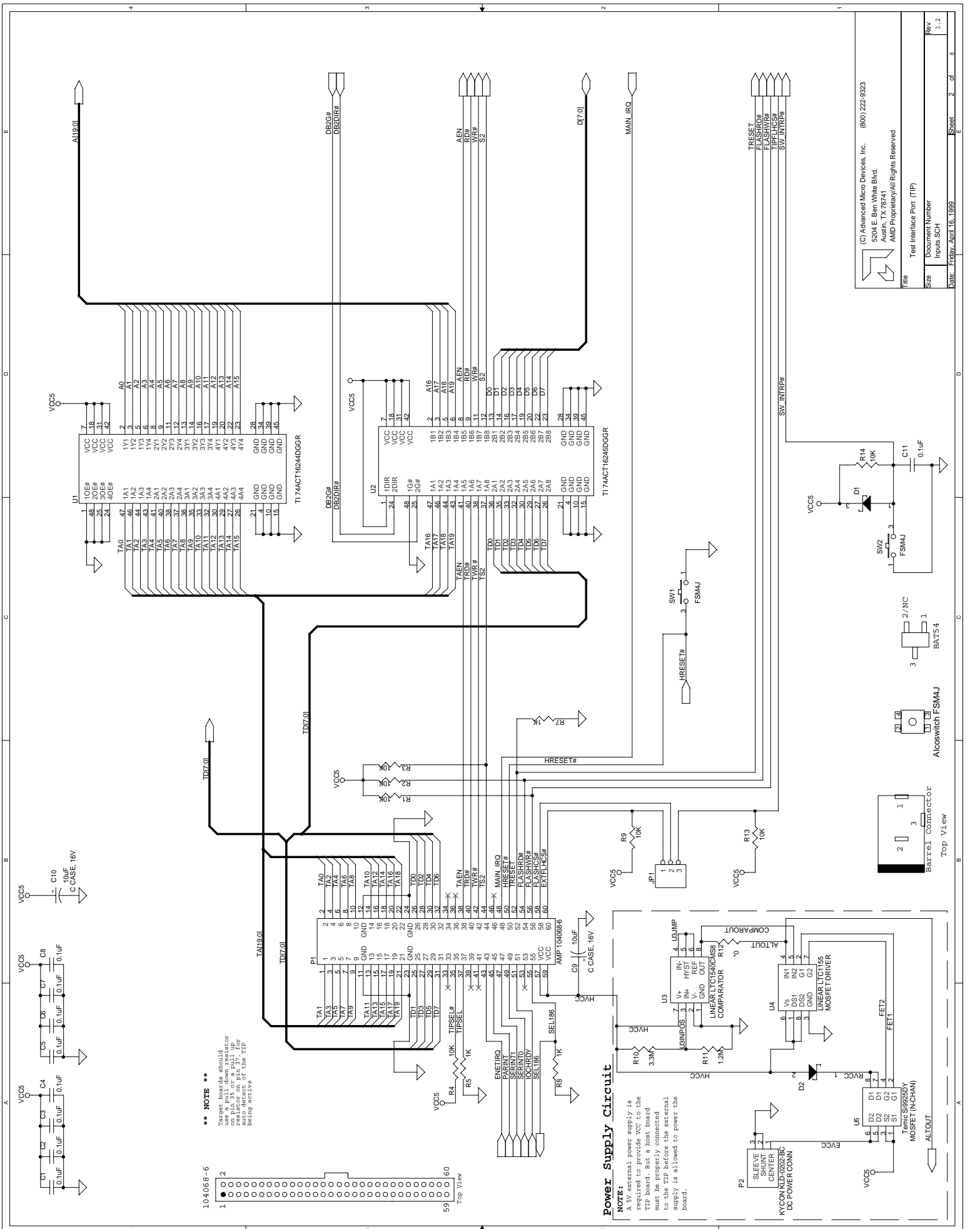
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 damage may occur. AMD assumes no liability whatsoever for claims associated with the sale or use
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Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

NOTE: An asterisk (*) in front of a resistor or capacitor value
 indicates a non populated component.

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**** NOTE ****

These boards should use a pull down resistor on pin 177 for auto detect of the TIP being active

Power supply Circuit

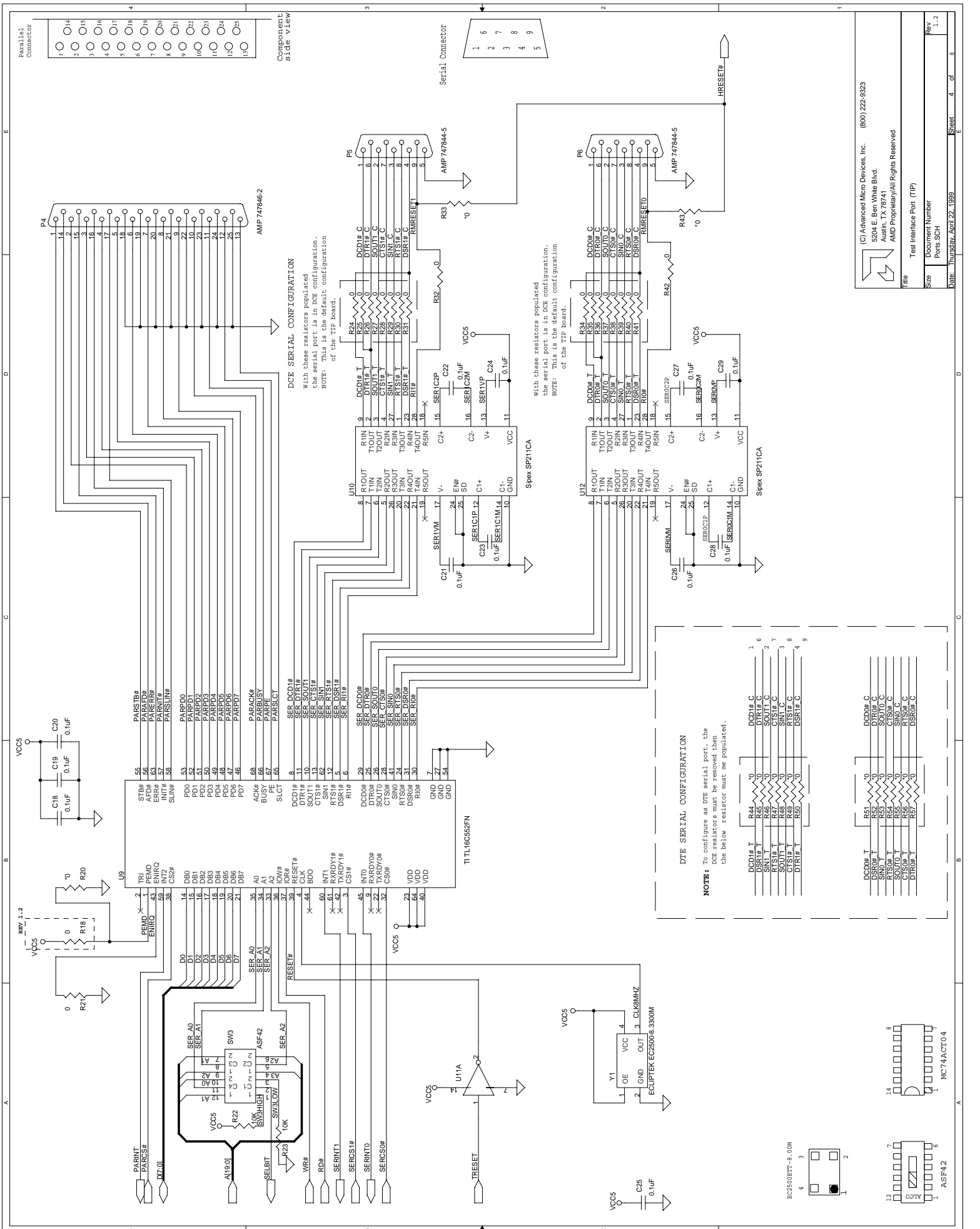
A 5v external power supply is required to provide VCC to the TIP board. But a host board must be properly connected to the TIP before the external supply is allowed to power the board.

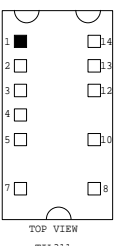
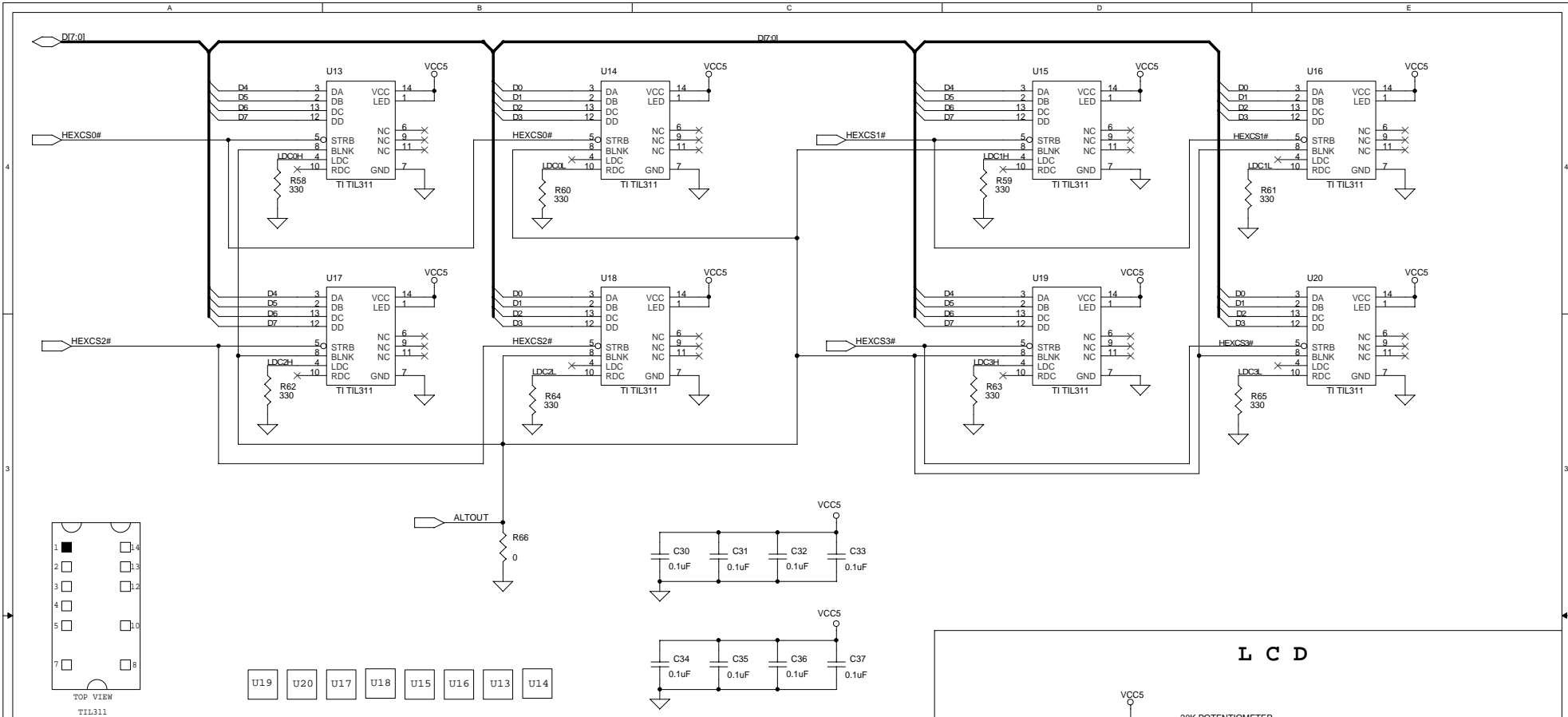
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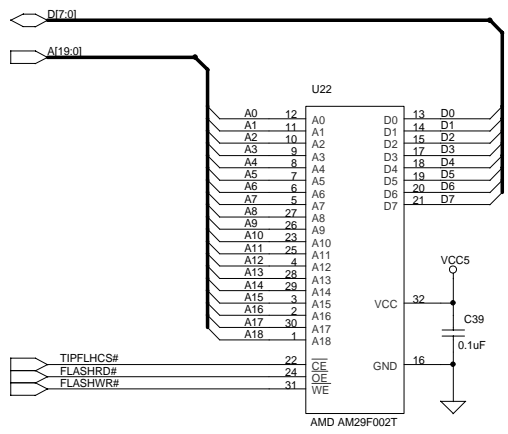
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Top View

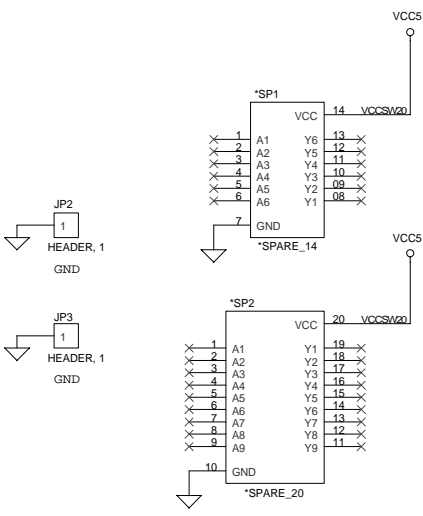




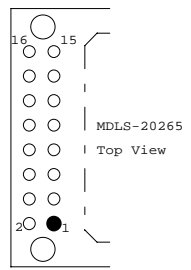
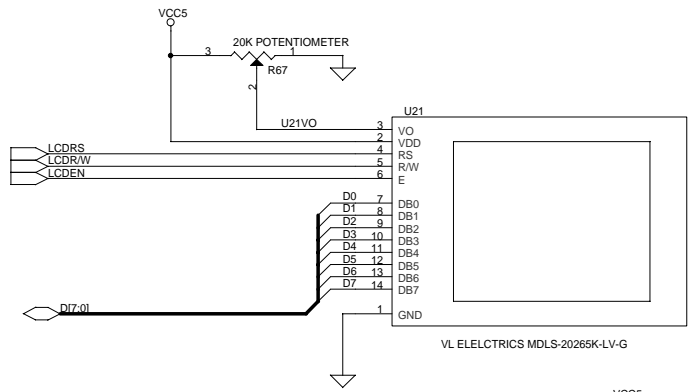
FLASH



SPARES

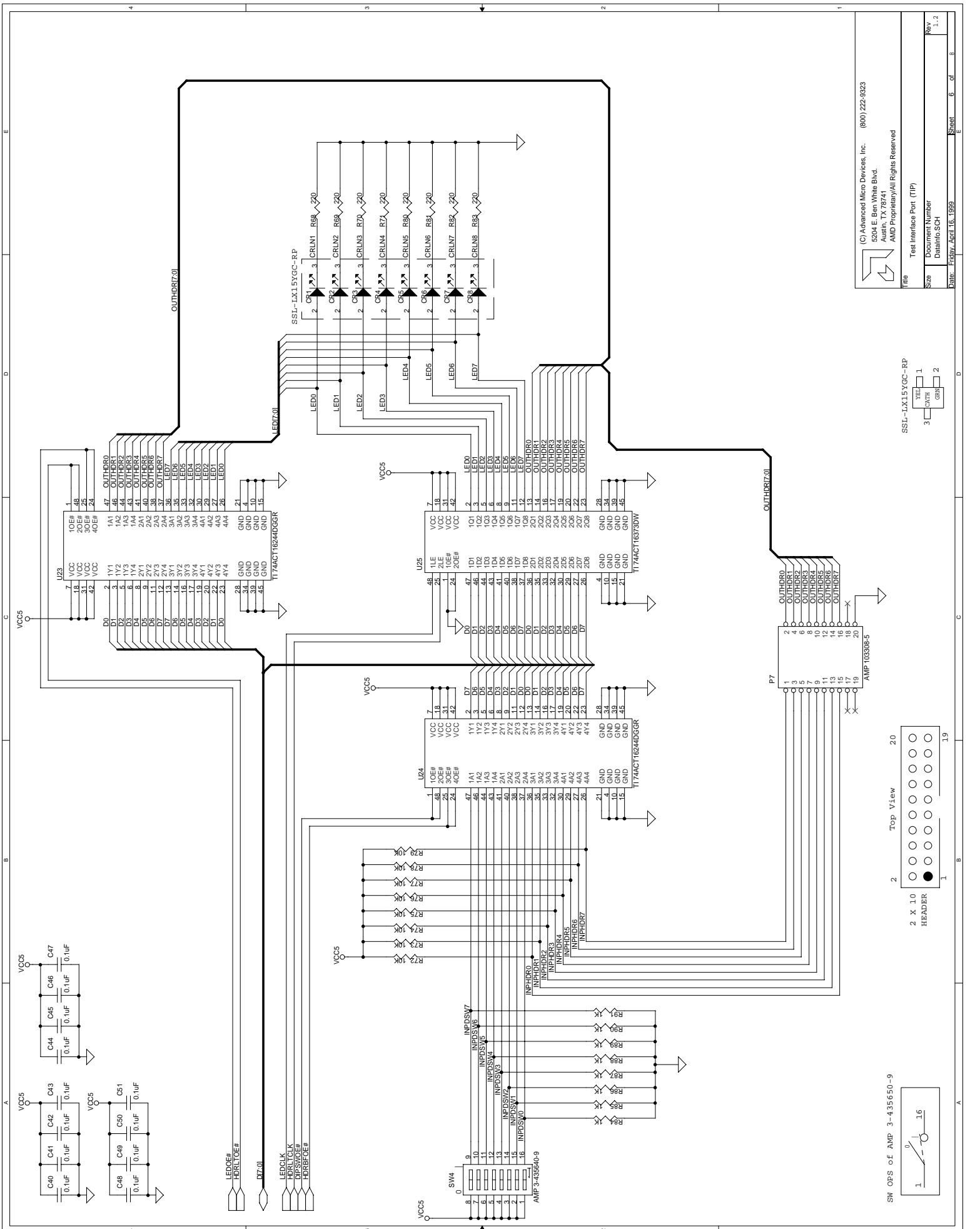


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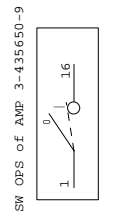
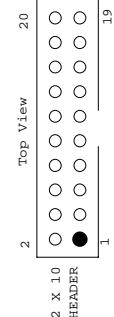
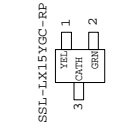
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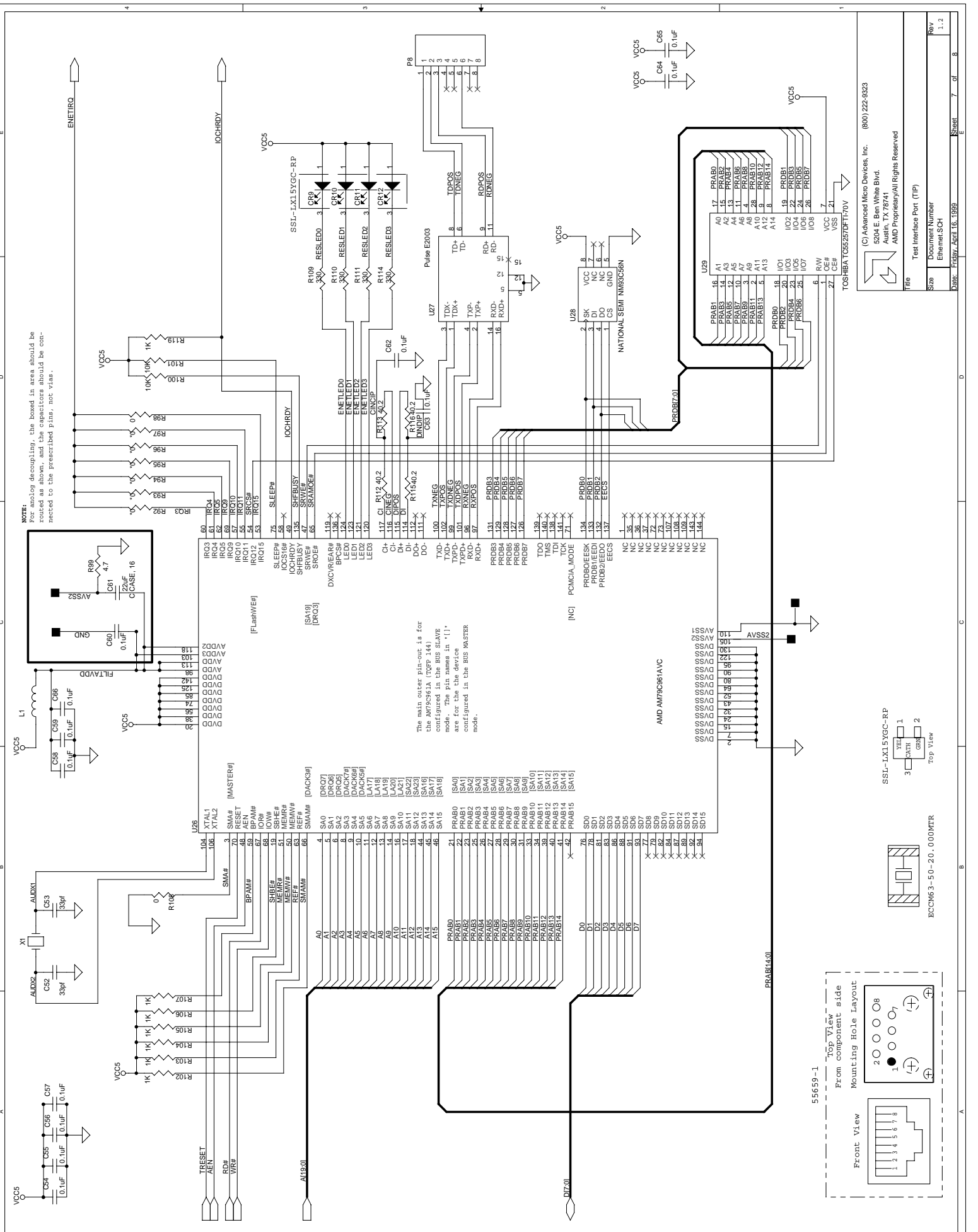


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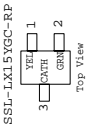
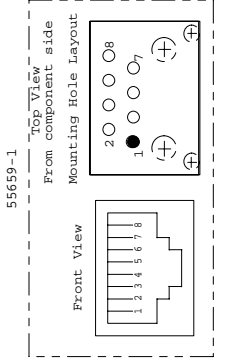
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NOTE: For analog decoupling, the boxed in area should be routed as shown, and the capacitors should be connected to the prescribed pins, not vias.



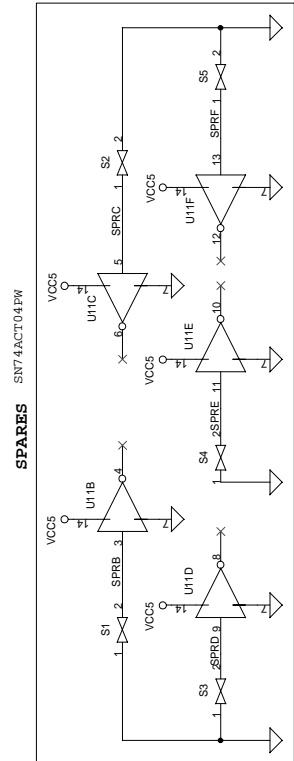
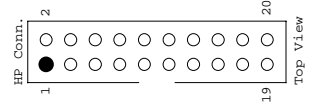
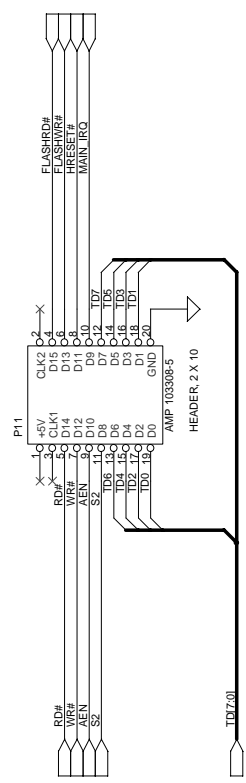
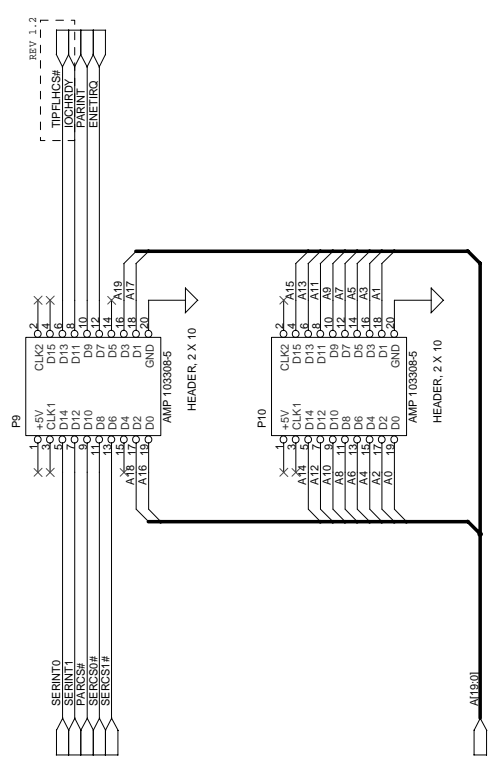
The main output pins are for the AM75C86-1AVC configured in the BUS MASTER mode. The pin names in '1' are for the device configured in the BUS SLAVE mode.



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