Application Note

AMD-640™ Chipset I/O Model

Introduction

Advances in semiconductor process technology have allowed the performance of integrated circuits to increase dramatically. The operating frequency of output signals driven from these circuits continues to increase, while the switching transitions of these signals has decreased. These particular characteristics of high-speed signals pose challenges to a system designer responsible for the placement and routing of components on printed circuit boards (PCBs). In particular, the propagation delay of a signal must be considered to ensure that sufficient setup and hold time, with adequate margin, exist at a signal's destination. In addition, as the rise and fall times of signals decrease, the system designer must ensure the signal quality meets the system requirements.

Ensuring that system timing and signal quality objectives are met prior to PCB manufacturing reduces the development expense and expedites the time-to-market of a product. This application note describes the format and usage of the AMD-640 chipset I/O buffer behavioral model, which allows a system designer to perform analog simulations of chipset signals that interface with the system logic. This model adheres to the *I/O Buffer Information Specification (IBIS), Version 2.1*.

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IBIS Modeling

Overview

IBIS is a specification developed to provide an industry-standard method for semiconductor manufacturers to model the analog behavior of I/O buffers without disclosing proprietary process data. As the availability of IBIS models has grown, so too have the number of analog simulators that accept IBIS models.

IBIS Usage

Modeling a PCB Net

To simulate the analog behavior of a signal on a PCB net, all elements of the net must be modeled to ensure the simulator generates accurate results. A net that is driven by a signal that has a short switching transition relative to its propagation delay is best modeled as a transmission line. The general criterion used for deciding on a transmission line as an appropriate model is as follows:

$$T_{switch} < 2(T_{prop})$$

Where:

- T_{switch} is the time required for a signal to switch states
- T_{prop} is the time required for a signal to propagate from its source to its destination

The typical elements of a net sourced by the chipset include the chipset's I/O buffer (modeled using IBIS), the transmission line that models the PCB trace, the destination receiver(s), and any components used for termination (See Figure 1). This net topology is then defined in the format understood by the target simulator.

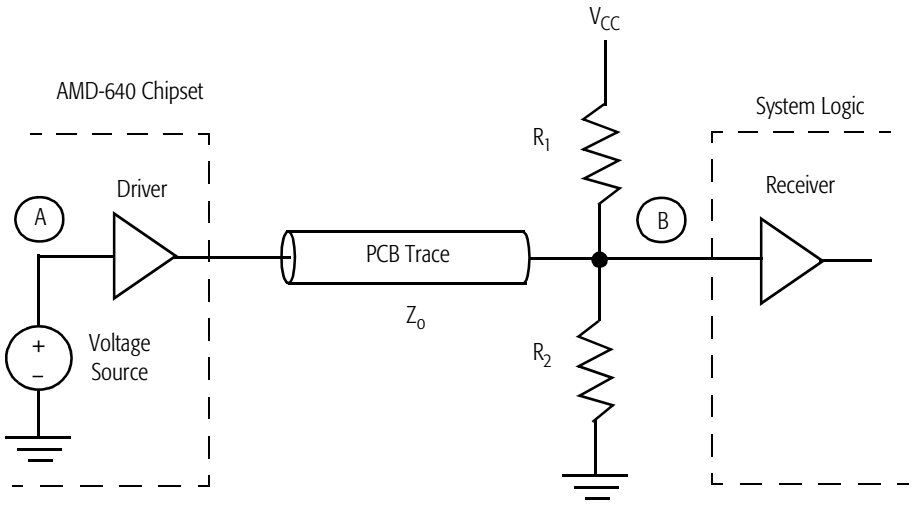

Figure 1. Modeling Example of Typical PCB Net

After the simulator has loaded the net input file, the simulator can be instructed to generate a rising or falling transition at the driver input to the chipset driver (point 'A' in Figure 1). This signal generator is represented in Figure 1 by the voltage source input to the chipset driver.

Setup and Hold Times

For each signal transition, the simulator can determine the signal propagation delay from point 'A' to point 'B' under worst-case, typical, and best-case conditions. The propagation delay under worst-case conditions is used to determine if the setup time at the destination receiver is met. Likewise, the progagation delay under best-case conditions is used to determine if the hold time at the destination receiver is met.

Figure 2 illustrates the timings that must be considered when determining whether the setup time of a signal is met. The timings are defined as follows:

- T_{period} is the period of the system clock
- T_{skew} is the maximum clock skew between the clock that launches a signal (solid-line clock) and the clock that captures a signal (dashed-line clock)
- T_{jitter} (not shown in Figure 2) is the maximum variance allowance between successive periods of the system clock

- $T_{validmax}$ is the maximum valid delay of a signal from its source
- $T_{propmax}$ is the maximum propagation delay of the signal along the PCB trace from its source to its destination. This delay is obtained by simulating with the worst-case conditions.
- $T_{setupmin}$ is the minimum required setup time of a signal at its destination

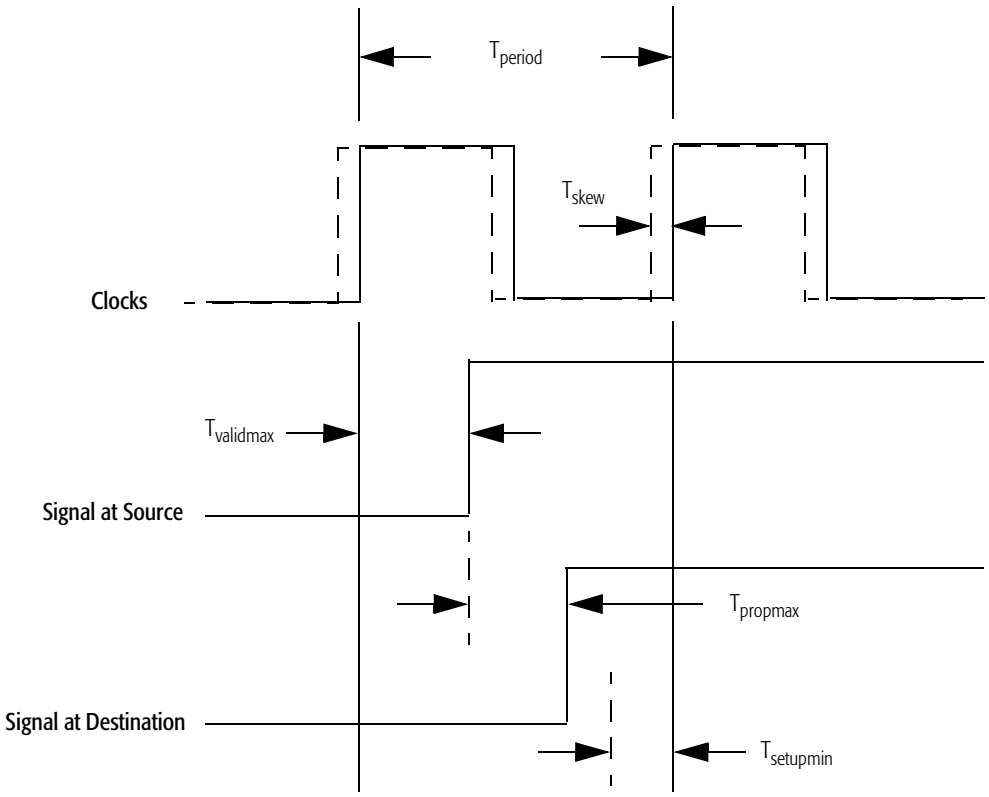

Figure 2. Timing Considerations for Meeting Setup Time

To ensure the setup time of a signal is met, the following relationship must be met:

$$T_{validmax} + T_{propmax} + T_{setupmin} < T_{period} - T_{skew} - T_{jitter}$$

Figure 3 illustrates the timings that must be considered when determining whether the hold time of a signal is met. The timings are defined as follows:

- T_{period} is the period of the system clock
- T_{skew} is the maximum clock skew between the clock that launches a signal (solid-line clock) and the clock that captures a signal (dashed-line clock)
- T_{jitter} (not shown in Figure 3) is the maximum variance allowance between successive periods of the system clock
- $T_{validmin}$ is the minimum valid delay of a signal from its source
- $T_{propmin}$ is the minimum propagation delay of the signal along the PCB trace from its source to its destination. This delay is obtained by simulating with the best-case conditions.
- $T_{holdmin}$ is the minimum required hold time of a signal at its destination

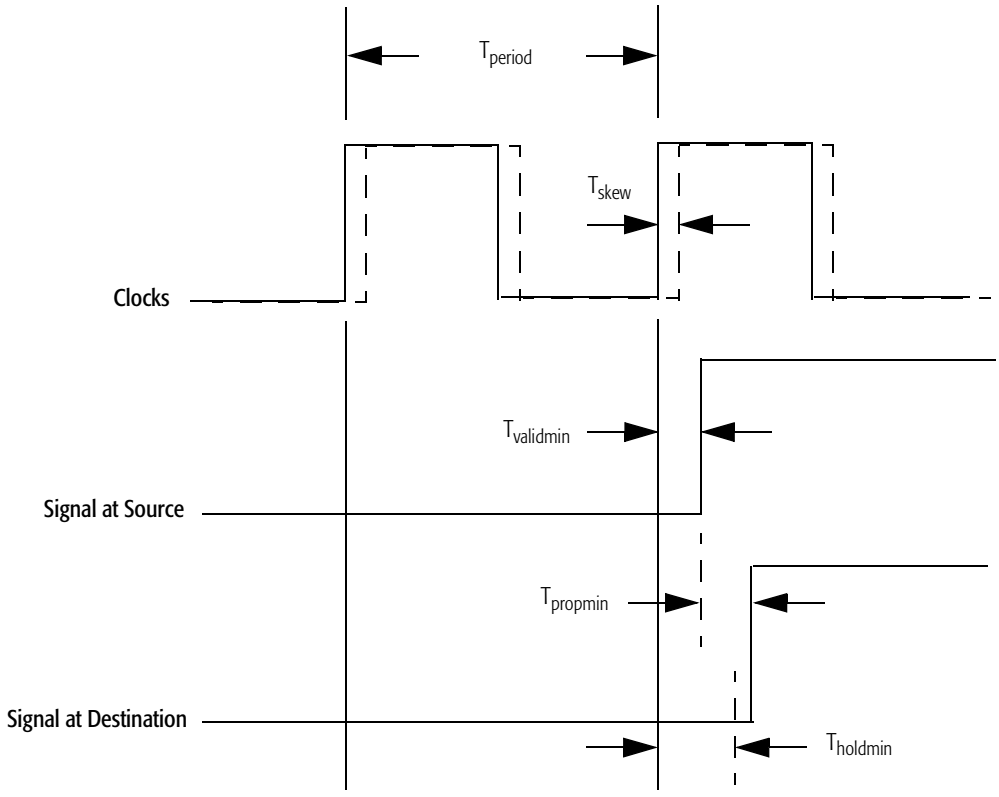

Figure 3. Timing Considerations to Meet Hold Time

To ensure the hold time of a signal is met, the following relationship must be met:

$$T_{validmin} + T_{propmin} - T_{skew} - T_{jitter} < T_{holdmin}$$

Signal Quality

In addition to providing propagation delays, the simulator can graphically display the input waveform presented at the input of the driver and the corresponding waveform produced at point 'B' in Figure 1. This display allows a designer to determine if the signal quality at the destination is acceptable. In addition to providing graphical data, most simulators generate numerical data that quantifies various signal quality characteristics.

The following list shows the signal quality characteristics that typically concern designers (all measurements are taken at the destination receiver):

- *Overshoot*—The difference between the maximum value of the voltage of a rising signal and the nominal I/O V_{cc} voltage (See Figure 4). Overshoot can adversely affect the reliability of the destination receiver. The time during which a signal remains above the nominal I/O V_{cc} voltage is also a reliability factor.
- *Undershoot*—The difference between the minimum value of the voltage of a falling signal and ground (See Figure 5). As with overshoot, undershoot can adversely affect the reliability of the destination receiver.
- *Ringback*—In the case of a rising waveform, the difference between the nominal I/O V_{cc} voltage and the minimum voltage of a signal after that signal has reached its maximum value. In the case of a falling waveform, ringback is the difference between the maximum voltage of a signal after that signal has reached its minimum value and ground (See Figures 4 and 5). Excessive ringing can cause the destination receiver to falsely switch if the signal traverses the switching threshold of the receiver.
- *Ring Settling Time*—In the case of a rising waveform, the time between when a signal crosses one-half of the nominal V_{cc} I/O voltage and when the signal settles within the specified tolerance of the I/O V_{cc} voltage. In the case of a falling waveform, ring settling time is the time between when a signal crosses one-half of the nominal I/O V_{cc} voltage and when the signal settles within a specific

percentage above and below ground (the percentage is dependent upon the electrical characteristics of the destination receiver). See Figure 6 for an example of ring settling time for a rising waveform. Settling time that approaches the period of the clock that launches a signal can potentially increase the switching time of that signal. This increase occurs if the signal is advancing in the opposite direction of the signal transition that occurs on the next clock edge.

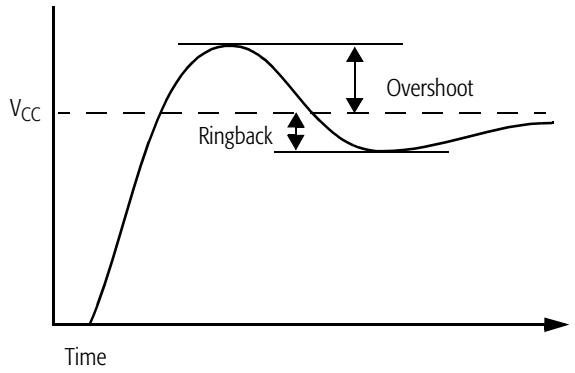

Figure 4. Example of Overshoot

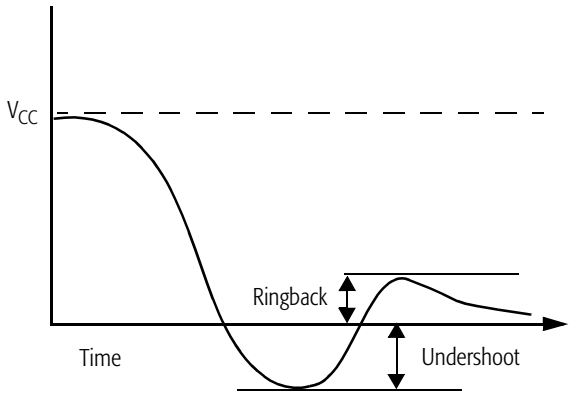

Figure 5. Example of Undershoot

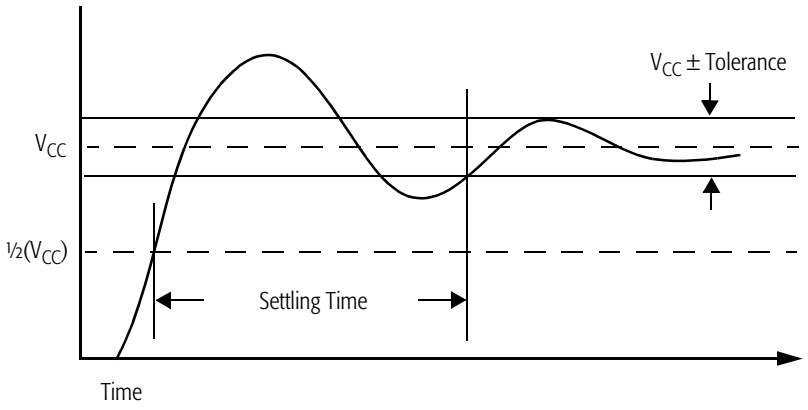

Figure 6. Example of Ring Settling Time for Rising Waveform

IBIS Structure

The IBIS specification defines a template that describes the properties of most elements of an I/O buffer design. The template uses required keywords and sub-parameters as well as optional keywords. The keywords and sub-parameters used by the AMD-640 chipset IBIS model, along with their definitions, are as follows:

- *IBIS Ver*—Specifies the version of the IBIS model.
- *File name*—Specifies the name of the file that contains the model.
- *File Rev*—Specifies the revision of the IBIS model.
- *Date*—Specifies the date the IBIS model was last modified.
- *Copyright*—The copyright claim.
- *Component*—Specifies the name of the component the model represents.
- *Manufacturer*—Specifies the manufacturer of the component.
- *Package* (R_pkg, L_pkg, C_pkg)—Specifies the R/L/C values of the package. These values are specified as 0 because the package R/L/C values are accounted for in the R_pin, L_pin, and C_pin sub-parameters of the *Pin* keyword.
- *Pin* (signal_name, model_name, R_pin, L_pin, C_pin, C_comp)—Itemizes each physical pin number along with its signal name, its I/O buffer name, and its R/L/C values.

Power, ground, and no-connect pins do not have R/L/C values specified.

- *Model* (model_type, Vinl, Vinh, Vmeas, Cref, Rref, Vref)—Specifies the type of I/O buffer.

  In the model I/O, Vinl equals 0.8V, Vinh equals 2.0V, and Vmeas = 1.5V. Cref, Rref, and Vref, which represent the test load under which the specified propagation delays and switching times are defined, equal 0. C_comp specifies the capacitance of the silicon die.
- *Temperature Range*—Specifies the temperature range within which the operation of the component is guaranteed.
- *Voltage Range*—Specifies the I/O voltage range.
- *Pulldown*—Specifies the voltage versus current (V/I) curves of the pulldown device within the I/O buffer.
- *Pullup*—Specifies the V/I curves of the pullup device within the I/O buffer.
- *GND Clamp*—Specifies the V/I curves of the ground clamp device within the I/O buffer.
- *POWER Clamp*—Specifies the V/I curves of the power clamp device within the I/O buffer.
- *Ramp* (dV/dt_r, dV/dt_f, R_load)—Specifies the rise and fall times of a signal at a load defined by R_load. R_load is equal to 50 ohms.
- *Rising Waveform*—Specifies the voltage versus time (V/T) curves of the rising edge of the waveform.
- *Falling Waveform*—Specifies the V/T curves of the falling edge of the waveform.

IBIS Models

AMD provides models of the AMD-640 system controller and the AMD-645™ peripheral bus controller I/O buffers for system designers to use in board-level simulations. These I/O buffer models conform to the *I/O Buffer Information Specification (IBIS), Version 2.1*.

I/O buffer models represent the characteristics of the drive strength configuration supported by the AMD-640 chipset. The model also associates the appropriate driver type to its respective pin. In the AMD-640 system controller, the memory drivers are programmable by configuration registers. Hence the designer must select the 12ma or 24ma driver, depending on the intended use.

Each I/O model contains voltage versus current (V/I) and voltage versus time (V/T) data tables for accurate modeling of I/O buffer behavior.

The following list summarizes the properties of each I/O buffer model:

- All data tables contain minimum, typical, and maximum values to allow for worst-case, typical, and best-case simulations, respectively.
- The pullup, pulldown, power clamp, and ground clamp device V/I tables contain enough data points to accurately represent the nonlinear nature of the V/I curves. In addition, the voltage ranges provided in these tables extend beyond the normal operating range of the AMD-640 chipset for those simulators that yield more accurate results based on this wider range.
- Rising and falling ramp rates are specified.
- The min/typ/max V_{CC3} operating range is specified as 3.135 V, 3.3 V, and 3.465 V, respectively.
- V_{il} = 0.8 V, V_{ih} = 2.0 V, and V_{meas} = 1.5 V.
- The R/L/C of the package is modeled.
- The capacitance of the silicon die is modeled.
- The model assumes 0 capacitance, resistance, inductance, and voltage in the test load.

Standard I/O Model

The standard I/O model is available from the AMD web site at *http://www.amd.com*.