Systems in Silicon™

AMD Élan™SC520 Microcontroller Technical Details

Systems in Silicon™

Contents

AMD

Systems in Silicon™

ÉlanSC520 Microcontroller

- Architectural Goals, Block Diagrams
- Memory, I/O Space, Memory Control
- PCI Host Bridge, Arbitration Unit
- GP-Bus Controller, GPDMAC
- ROM and SDRAM Controllers
- GP-Bus Peripherals Overview

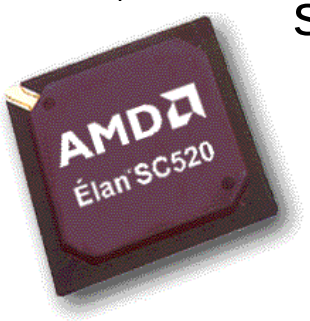
Systems in Silicon™

Architectural Goals
Basic Embedded System Example
ÉlanSC520 Block Diagram Explanation

Systems in Silicon™

Architectural Goals

- Provide mid-range to high-end x86 based embedded solution for general embedded and communications market
- Enable connectivity of industry standard memory and peripheral components (SDRAM, PCI Bus)
- Create system architecture that can be carried forward to meet needs of several communications market segments (Datacom, Telecom, Information Appliances)



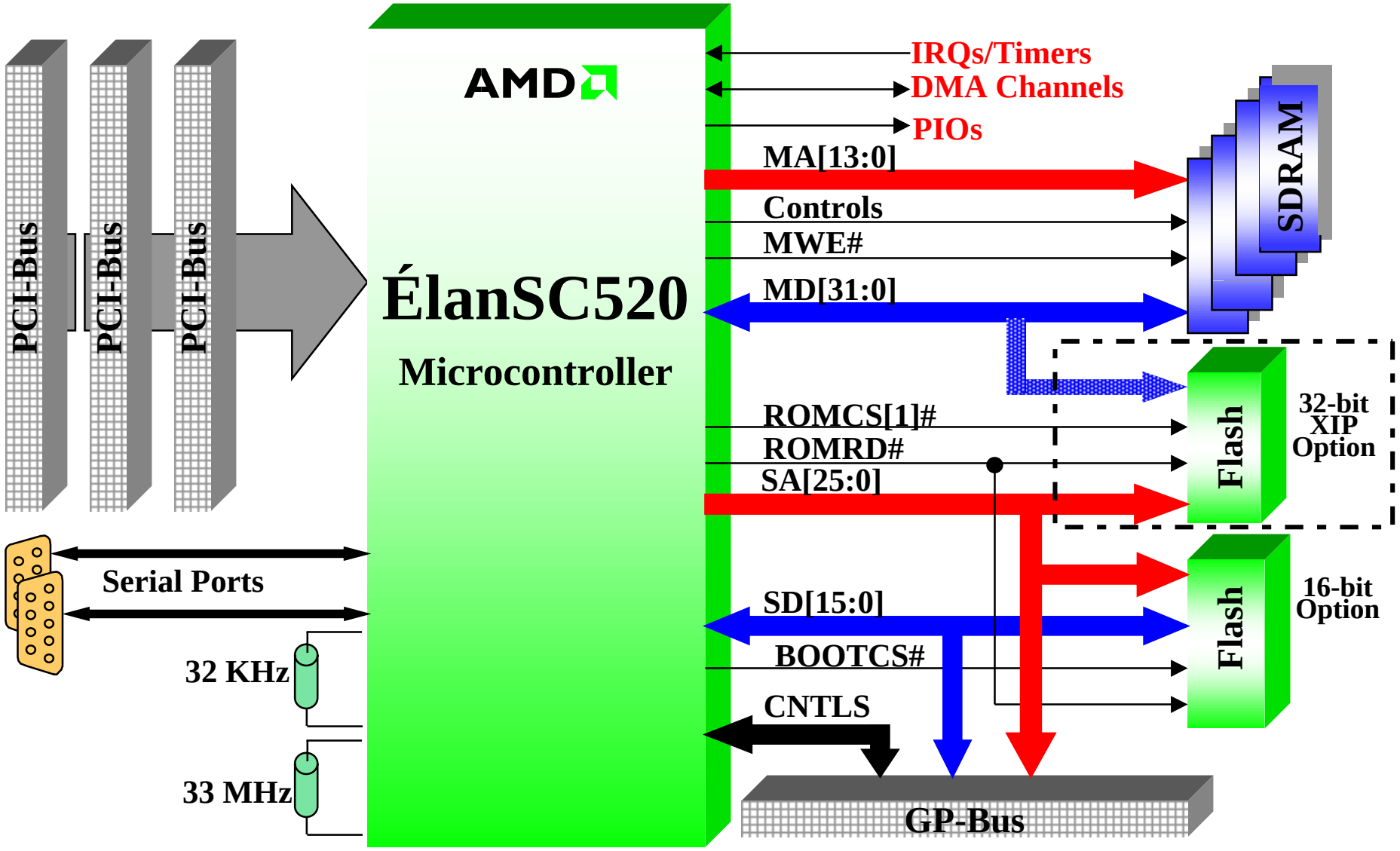
Architectural Goals (cont'd)

- Technical Solution
  - Provide superior code debug capabilities in CPU core
    - Add system debug features to the Am5x86 CPU core
  - Squeeze lower cost 32-bit performance
    - 133 Mhz Am5x86 CPU Core, 16 KB WB Cache (486DX5)
    - 66 MHz SDRAM Interface optimized for CPU execution
    - Write buffering/prefetching to optimize performance
    - Support industry standard PCI Bus and provide high bandwidth pipe to main memory via FIFOs
  - Integrate chipset and clock generation to minimize external components required
  - Provide flexibility for multiple applications
    - General purpose bus, programmable address space

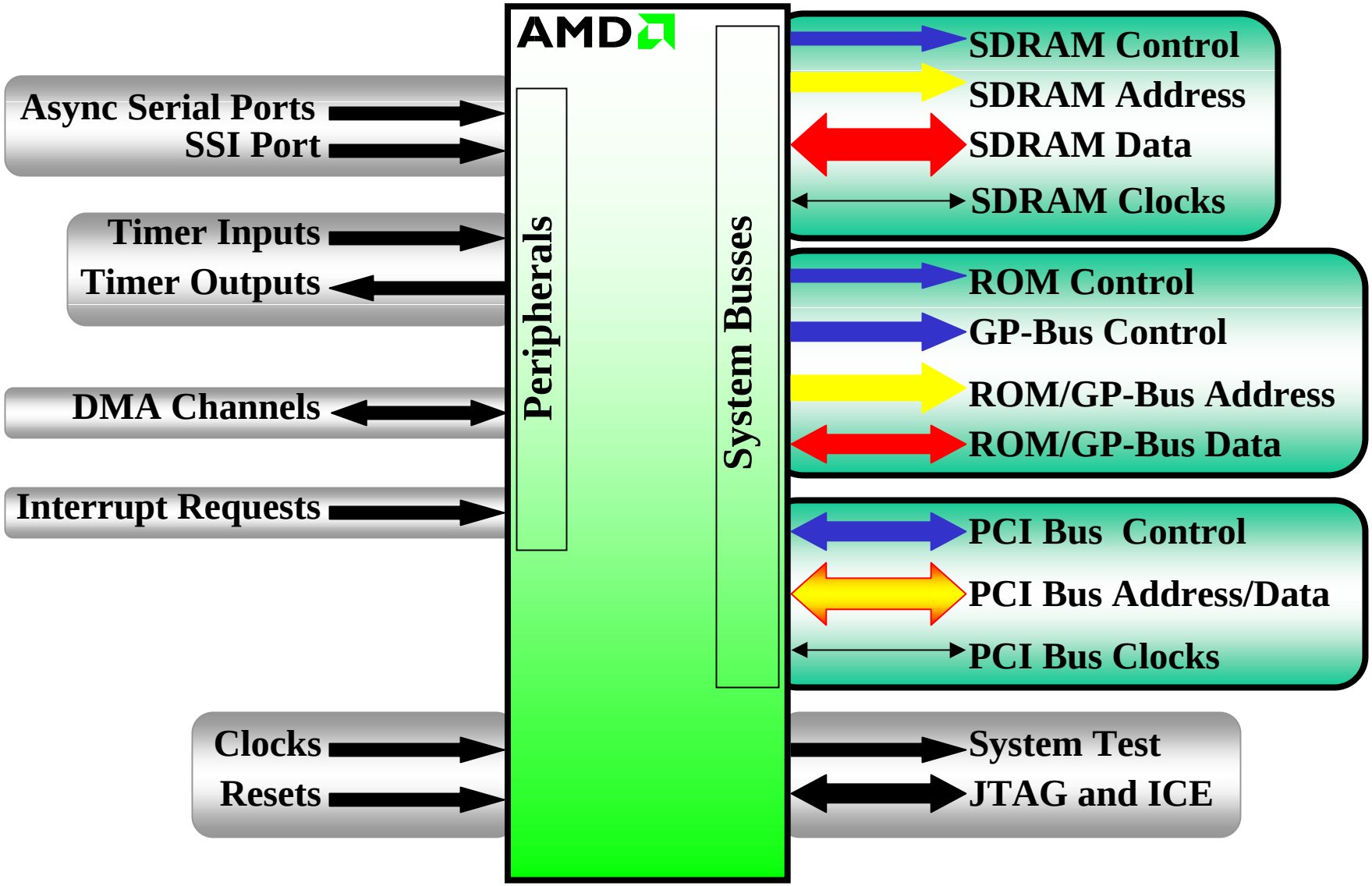
Architectural Goals (cont'd)

- Performance Goals and Features
  - 3-1-1-1 SDRAM Cache-line fills (Page Hit)
    - 2-1-1-1 for Read Ahead Buffer hits
  - 2-1-1-1 SDRAM Write-backs, copy-backs (Page Hit)
  - 2-1-1-1 Flash Cache-line fills (32-bit XIP, 50 nS)
  - Sustain 132 MB/s PCI Bus bursts for 64 DWORD transfers
  - 4 clock minimum GP-Bus access (non-burst)
  - Concurrent arbitration mode to allow simultaneous PCI Bus mastering and CPU code execution
  - 32 rank write buffer to improve DRAM throughput
    - Write merging and collapsing
    - Reordering of reads around writes
  - DRAM prefetching (RAB) improves read performance

Basic Embedded System



Overview of ÉlanSC520 Pins

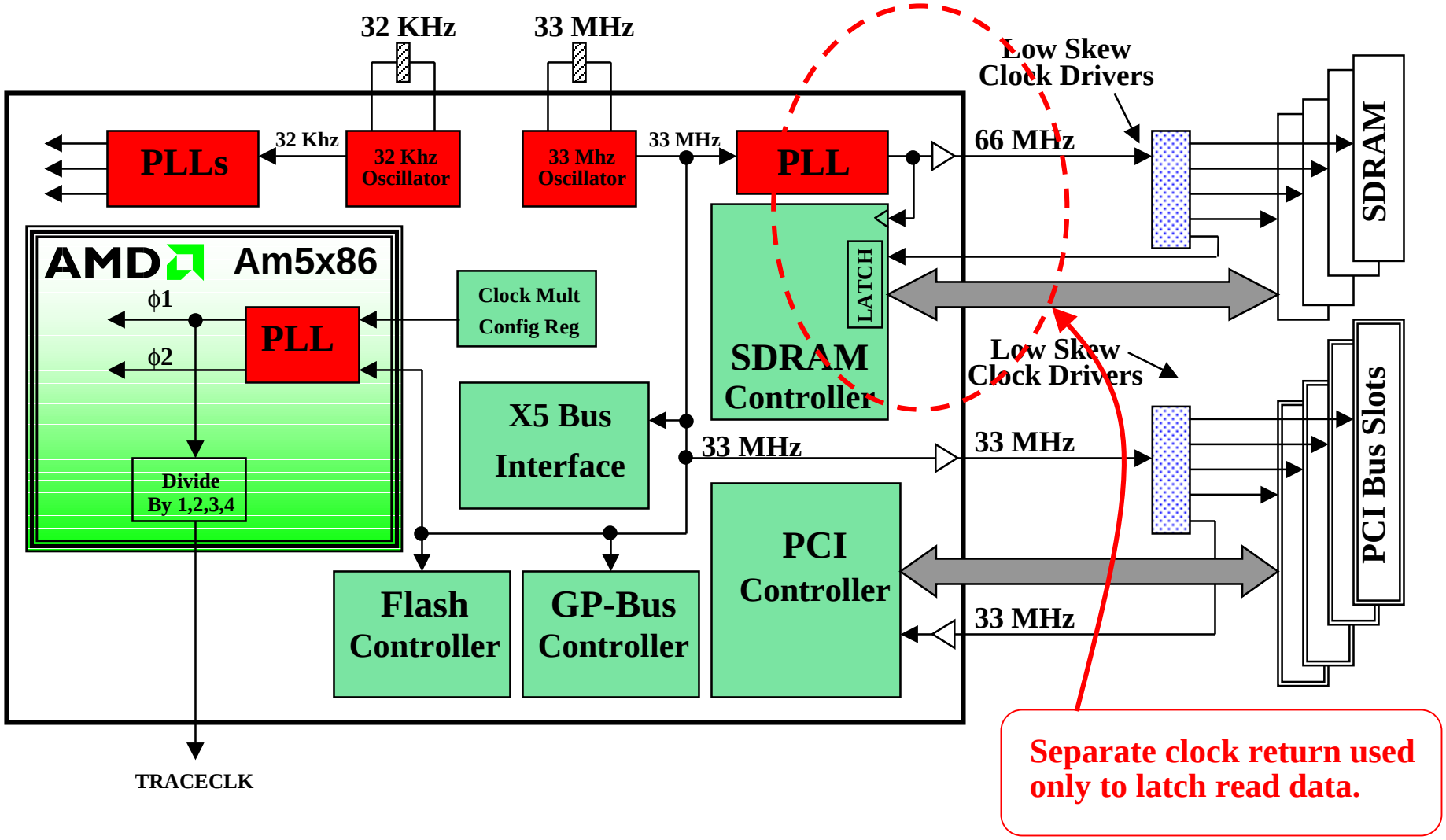


ÉlanSC520 Pin Sharing

- Pins not shared:
  - PCI Bus
  - SDRAM Interface
  - GP-Bus Address/Data
  - JTAG
  - AMDebug (ICE)
  - XTALs and Clocks
  - Resets
  - Power and Ground

- Pins shared:
  - ROM/Flash Chip Selects muxed with GP-Bus chip selects
  - GP-Bus signals are muxed with PIOs
    - Some Control Signals
    - GPDMA REQ/GNT
    - GPIRQ
  - GP-Bus chip selects muxed with Timer pins
  - Some UART-2 signals are muxed with PIOs
  - System Test

ÉlanSC520 Clock Distribution



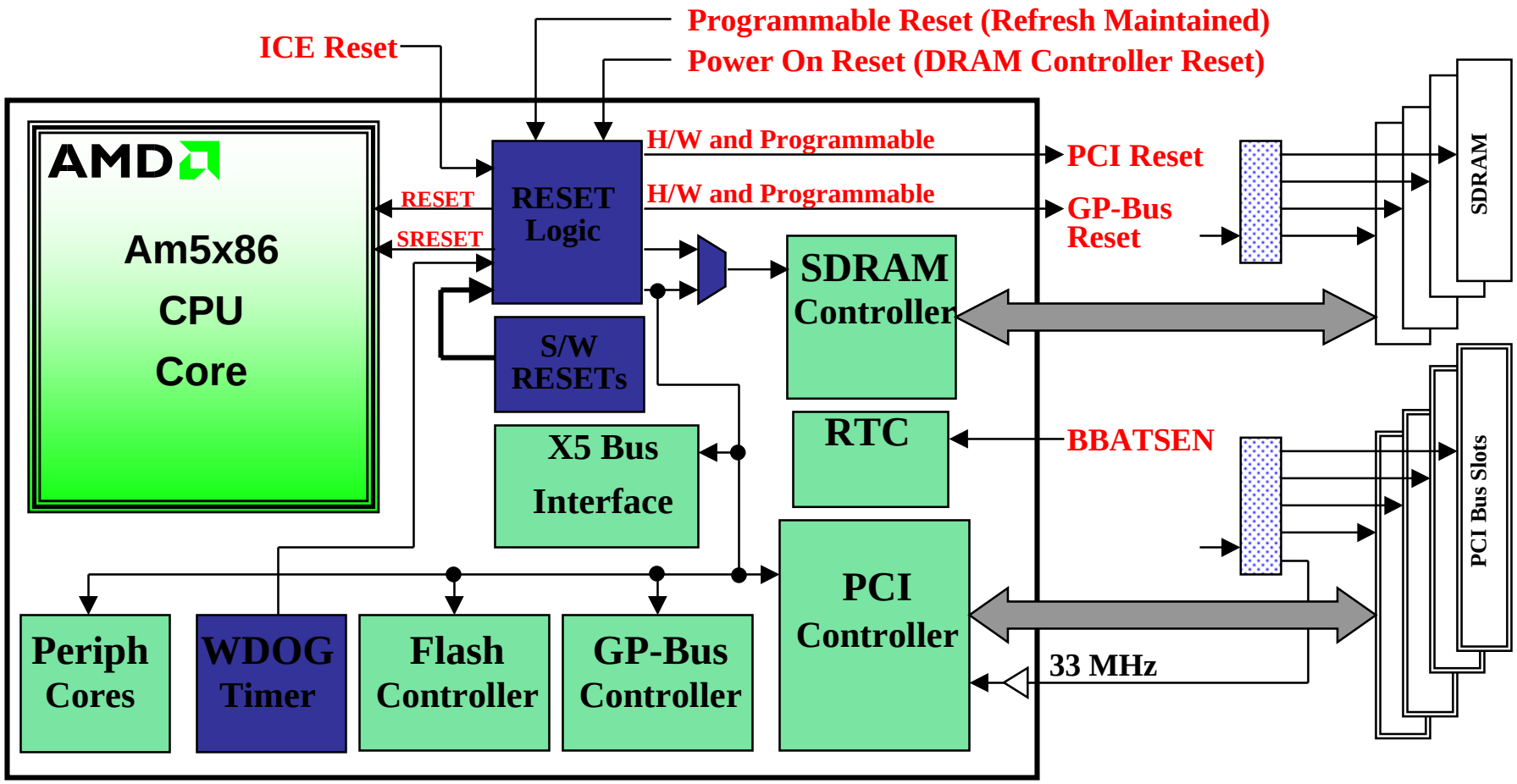
Systems in Silicon™

ÉlanSC520 Clock Generation

- Internal PLLs generate system clocks
- Internal 33 MHz oscillator feeds PLL for CPU, PCI, and SDRAM clocks
  - Requires external 33 MHz crystal
- 66 MHz routed directly to SDRAM Controller
  - Requires external clock buffers to the SDRAM array for heavy loading
  - Separate buffer output wraps back to ÉlanSC520 for synchronizing commands and data
- Internal 32 KHz oscillator feeds miscellaneous PLLs for system clocks
  - Requires external 32 KHz crystal
- Miscellaneous system clocks
  - UARTs
  - 8254 PIT
  - S/W Timers
  - SSI Port

AMD

ÉlanSC520 System Resets

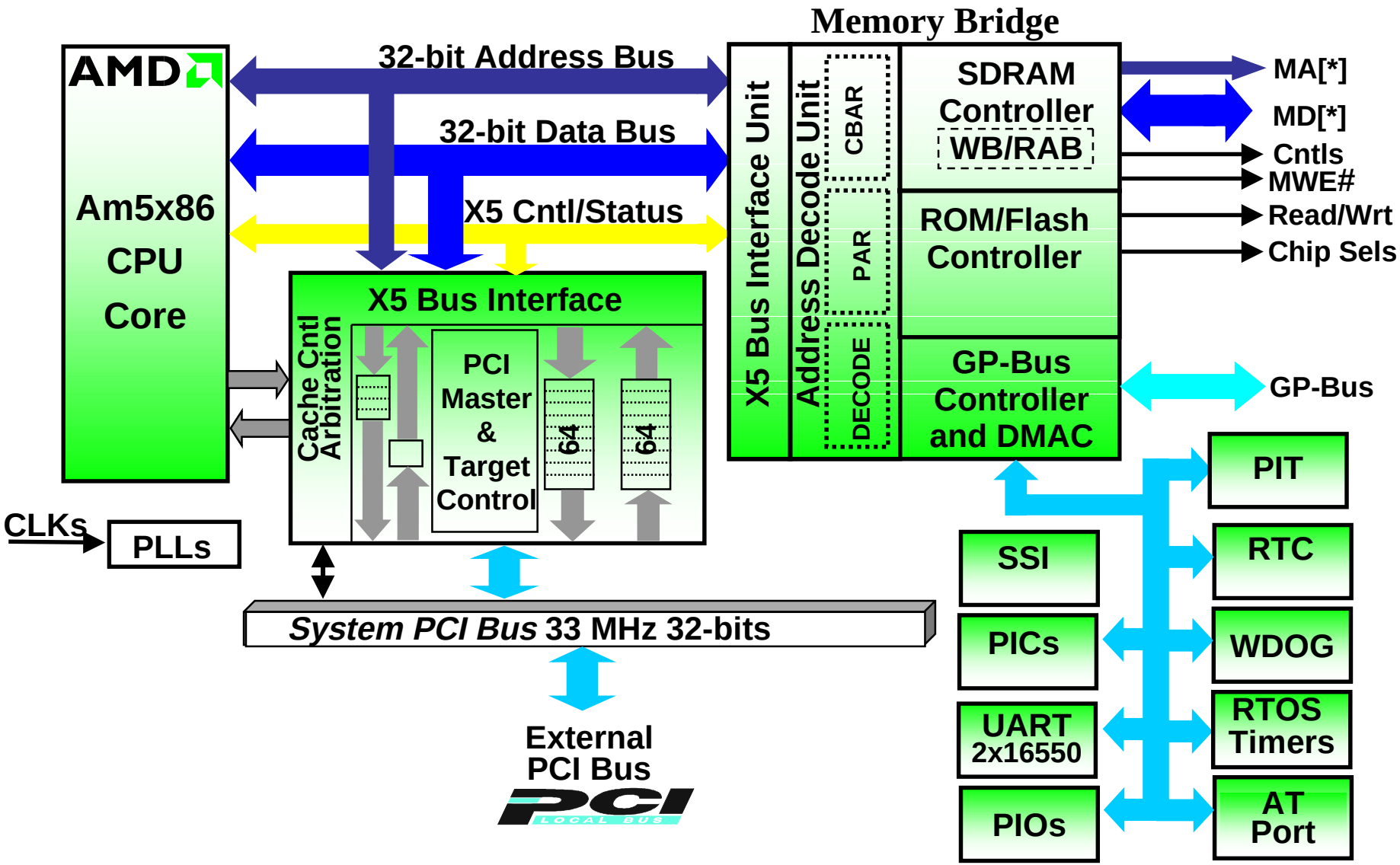


PC compatible CPU Reset sources: Port 92h, 60h/64h, Triple-Fault (shutdown)

System Resets

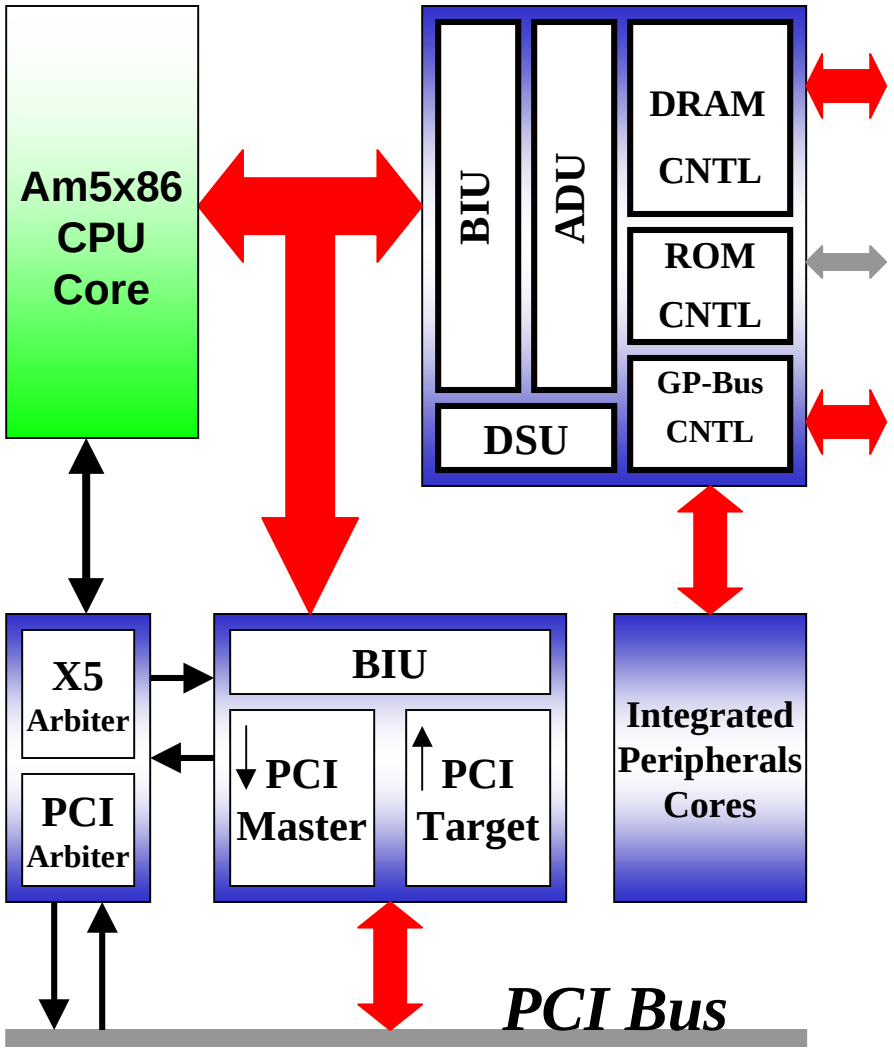
- ÉlanSC520 System Reset Sources
  - Signal from power supply (PWRGOOD)
  - Programmable Reset pin (PRGRESET)
  - Watchdog Timer
  - Configuration Register (SYS_RST)
  - ICE Reset
- CPU Soft Reset (SRESET) Sources
  - Shutdown triple bus fault detect (Special Cycle)
  - Port 92h, Port 60h/64h SCP
- All System Reset sources also reset the PCI Bus and GP-Bus
  - Each can be independently reset via configuration register write

ÉlanSC520 Internal Architecture



ÉlanSC520 System Busses

- **X5 Bus**
  - Internal only
  - 32-bits, 33 Mhz
  - X5 protocol
- **PCI Bus**
  - Internal and external
  - 32-bits, 33 MHz
- **GP-Bus**
  - Internal and external
  - 8/16-bits programmable
- **SDRAM Interface**
  - External only
  - 32-bits, 66 MHz



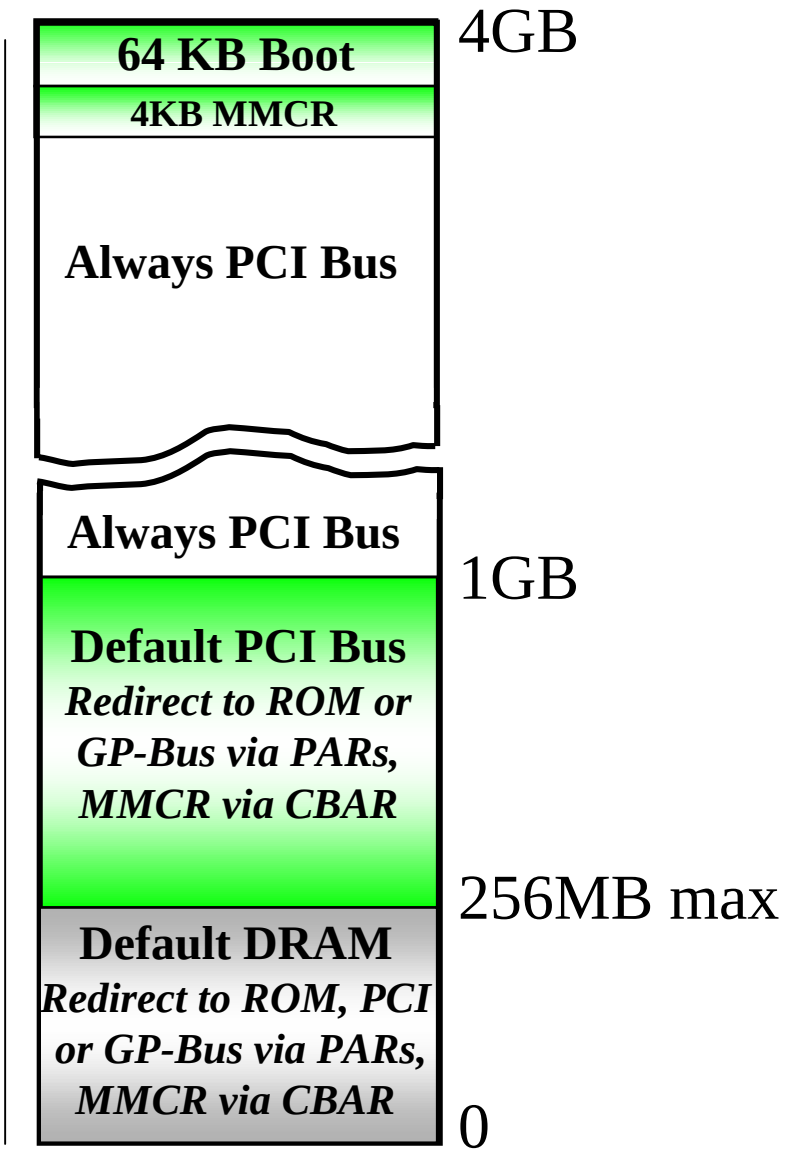
Systems in Silicon™

ÉlanSC520 Memory and I/O Space
Memory Bridge Bus Interface Unit

AMD

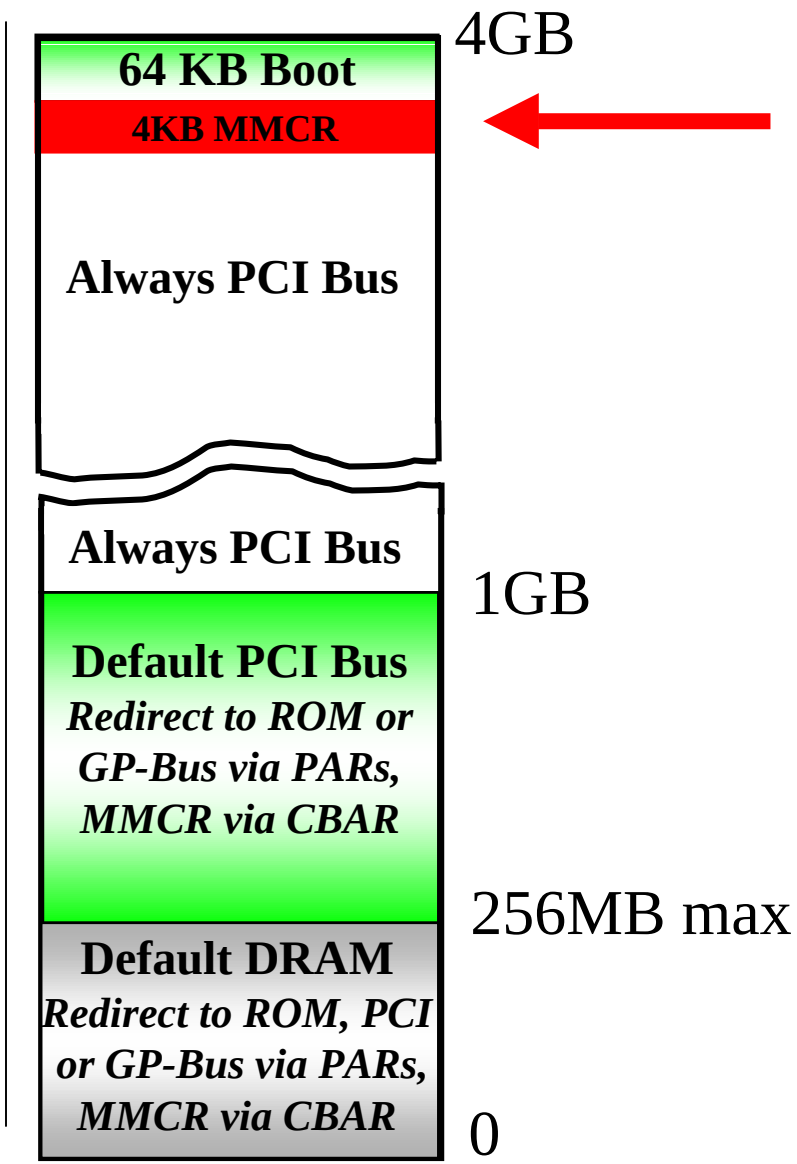
ÉlanSC520 Memory Space

- Up to 256 MB DRAM in linear memory space starting at 00000000h
- 64 KB “boot space” *always* enabled at FFFF0000h
  - *Can’t set attributes in this region*
- PAR registers provide common programming interface to define ROM and GP-Bus space
  - *Can be programmed for Windows Compatibility*
- All remaining space defaults to PCI Bus



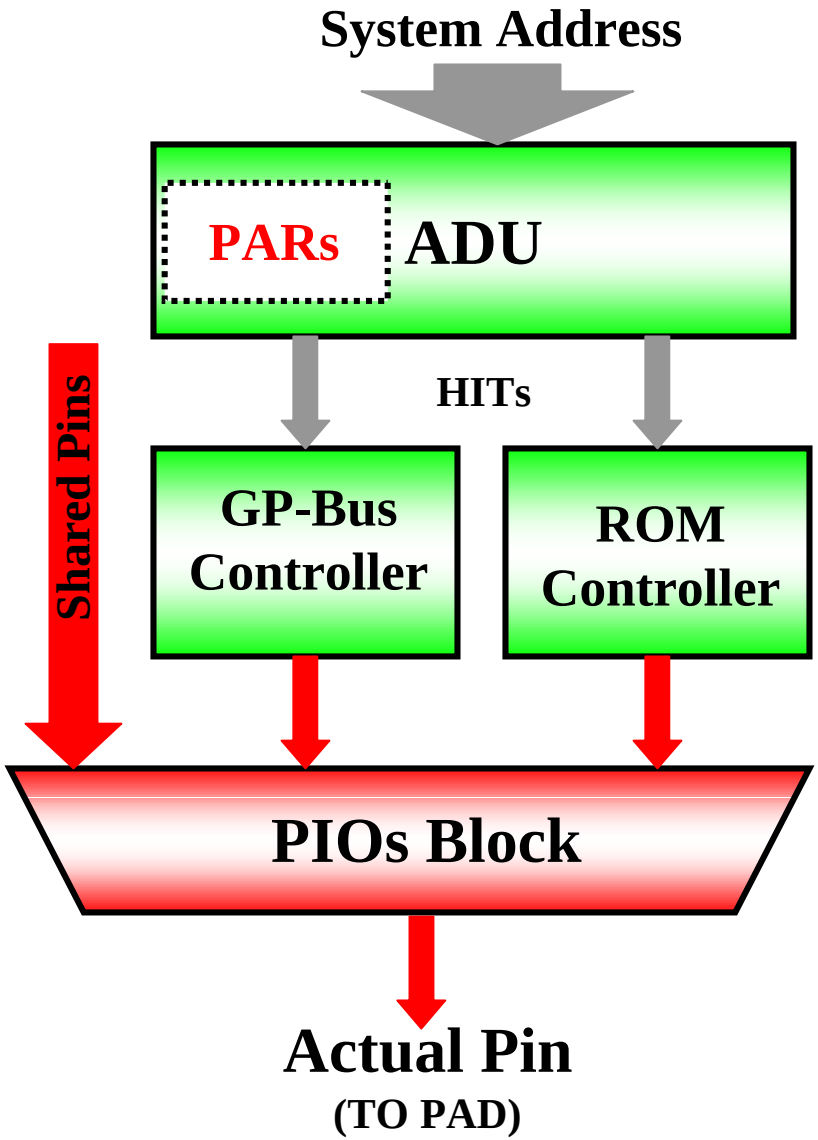
ÉlanSC520 Memory Space (cont'd)

- 4 KB "Memory Mapped Configuration Region" *always* enabled directly below boot region
- MMCR may be aliased anywhere in lower 1 GB with I/O mapped "CBAR"
  - *Cache must always be flushed after relocation!*
- DMA/PCI Bus masters access DRAM *only*

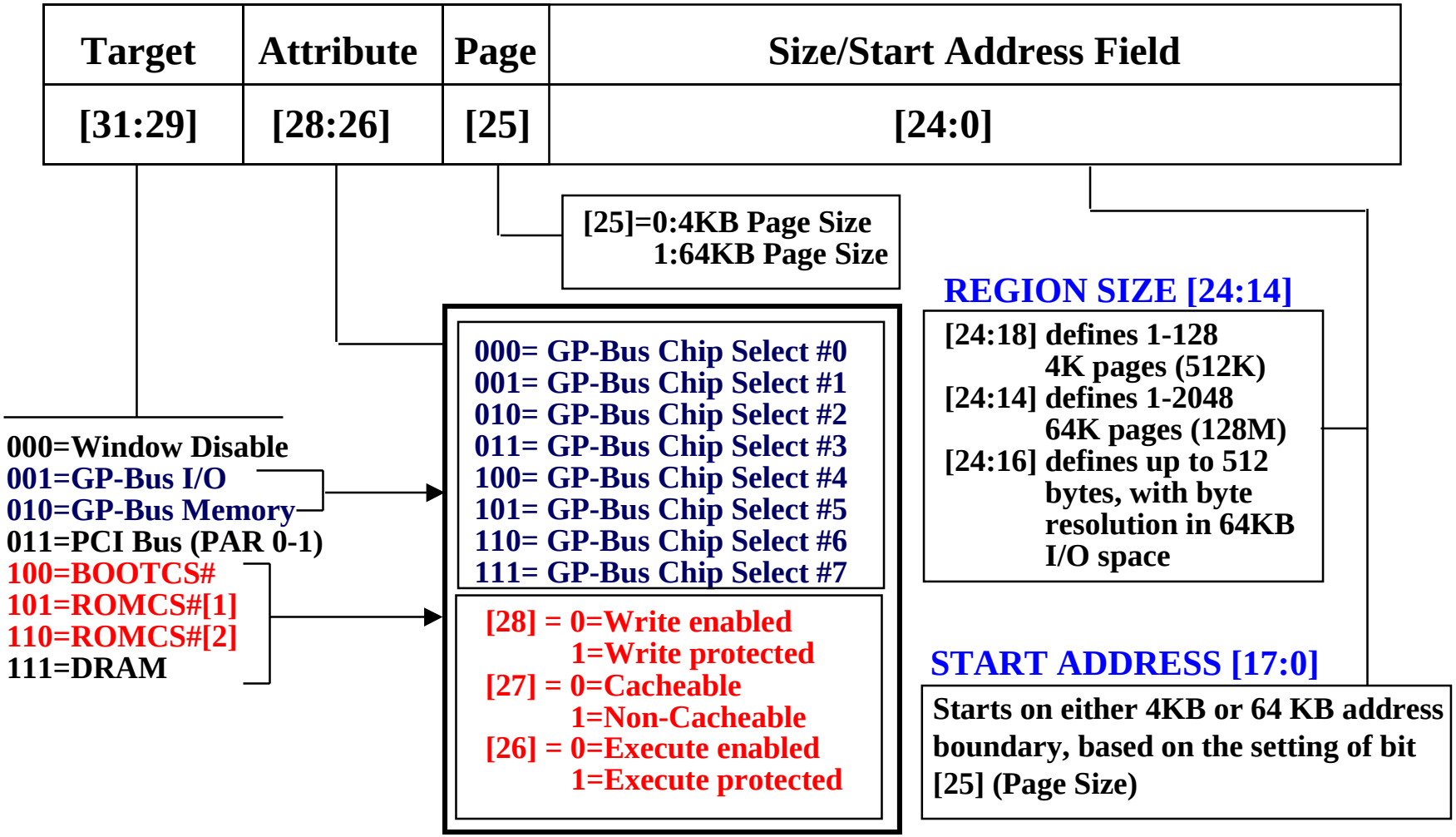


Chip Select Initialization

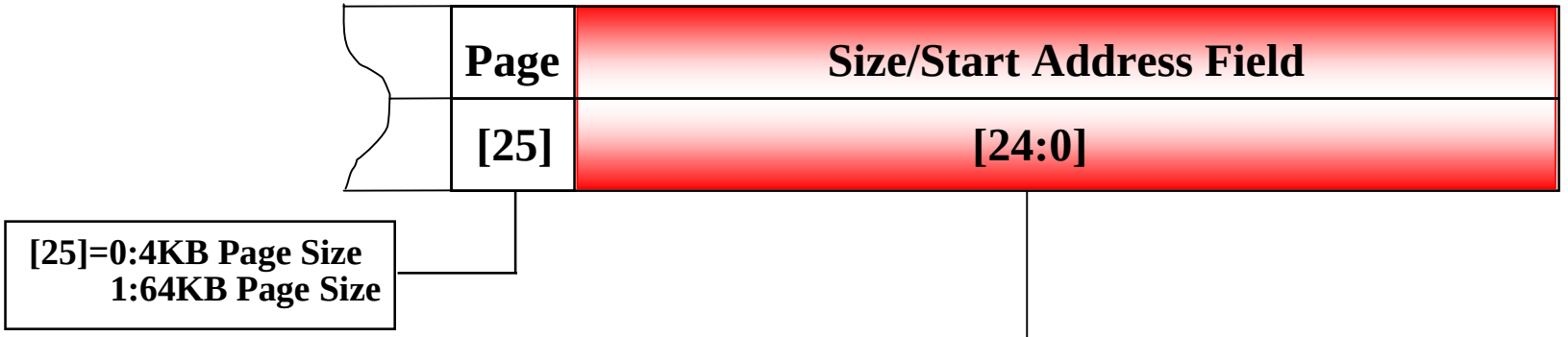
- PARs define the address space of the chip select, and the type (memory or I/O)
- Controller registers define the timing and width of the chip select (8/16/32-bits)
- PIOs define actual pin on ÉlanSC520



PAR Register Layout



Page, Size/Start Address Field



Memory Cycle PAGE=0	[24:18] defines up to 128 pages of 4KB each, on a 4KB boundary, for a 512KB maximum window size
	[17:0] defines actual start address, and compares to system address A[29:12]
Memory Cycle PAGE=1	[24:14] defines up to 2048 pages of 64KB each, on a 64KB boundary, for a 128MB maximum window size
	[13:0] defines actual start address, and compares to system address A[29:16]
I/O Cycles Only	[24:16] defines up to 512 bytes, with byte resolution in 64 KB I/O space
	[15:0] defines actual start address, and compares to system address A[15:0]

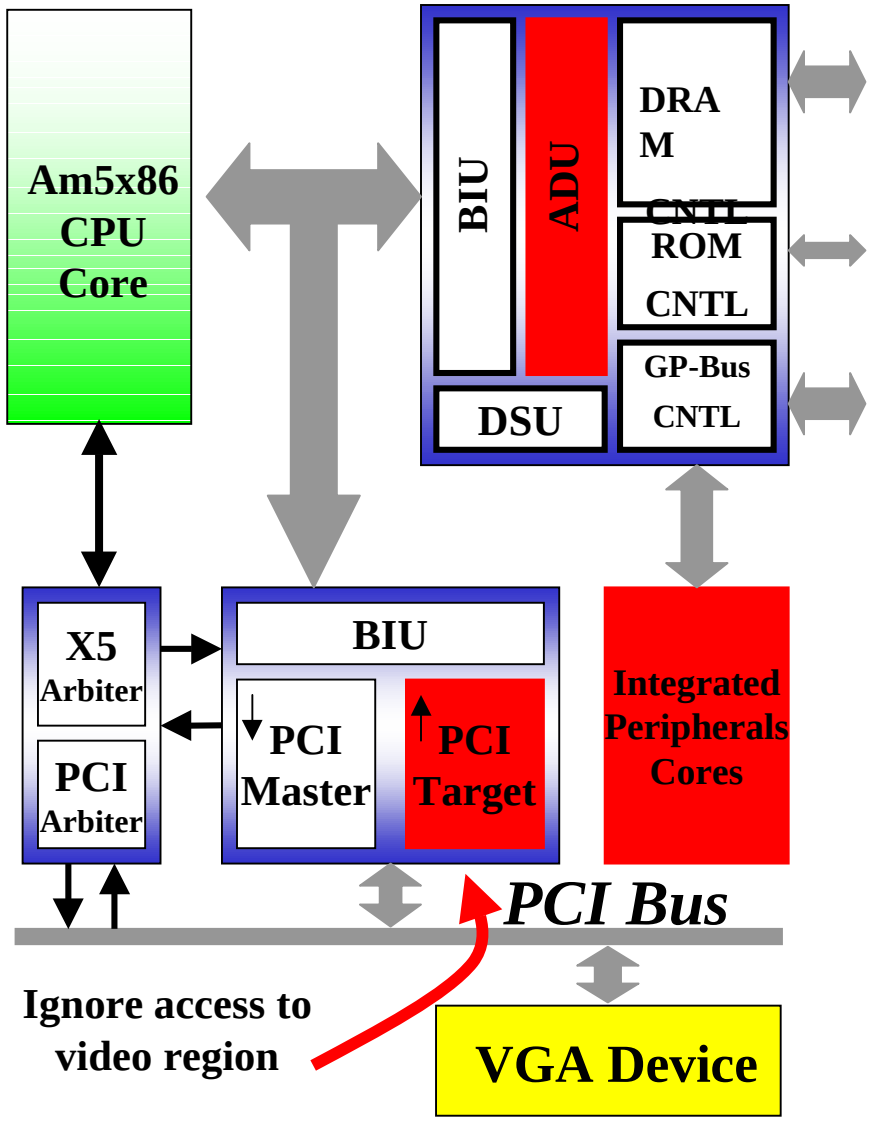
Systems in Silicon™

Attribute Field

- *Non-Execute Attribute*
  - Will force return of illegal op-code if CPU attempts to execute from marked region, resulting in an exception
- *Non-Cacheable Attribute*
  - Inhibits KEN# assertion to CPU for the region
  - **Flush cache after setting this!**
- *Write Protect Attribute*
  - SDRAM write cycle occurs but DQMs inactive
  - ROMWR# inhibited
  - Interrupt can optionally be generated

PC/AT Compatibility

- Integrated legacy PC/AT peripherals mapped in I/O space according to PC map
- PAR 0-1 can be used to redirect DRAM regions to PCI Bus
  - *Example: PCI VGA card at A0000h-AFFFFh*
- BIOS regions can also be redirected to ROM via PAR, instead of DRAM
- Interrupts, DMA channels can be routed to comply with PC/AT steering

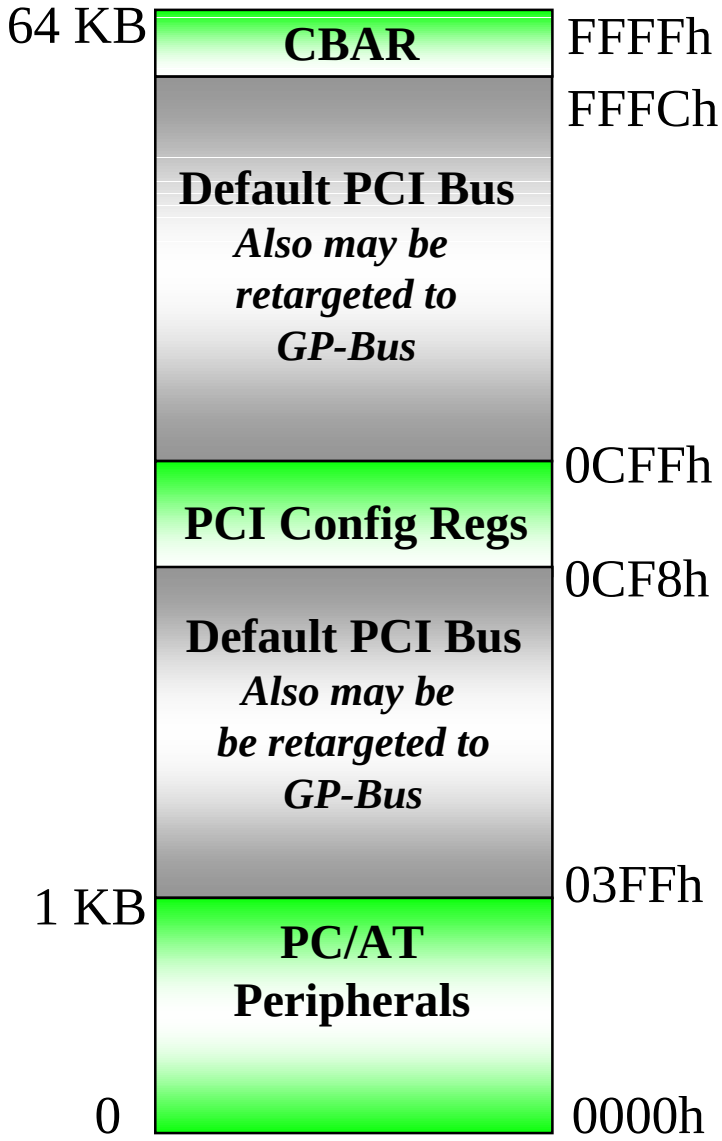


MMCR/ CBAR

- Memory Mapped Configuration Region (MMCR)
  - 4 KB space in memory where ElanSC520's non-PC/AT peripherals and configuration registers are mapped
    - Watchdog timer, S/W timer, SSI, General Purpose timers
  - Always accessible in upper memory below boot space (FFFEF000h-FFFEFFFFh)
  - May be aliased anywhere in lower 1 GB on 4KB boundary via CBAR
- Configuration Base Address Register (CBAR)
  - Used to alias MMCR in lower 1 GB region
  - I/O mapped at FFFCh-FFFFh (DWORD *only*)
  - Keyed to prevent accidental modification

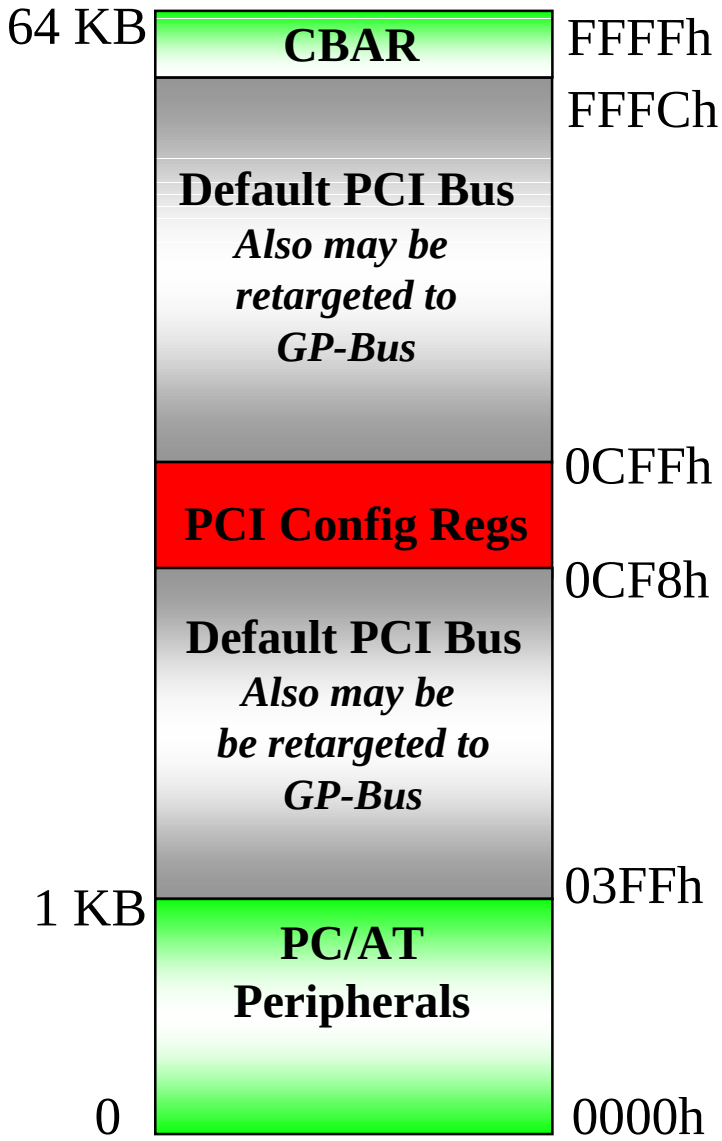
ÉlanSC520 I/O Space

- Only CPU has access to I/O mapped peripherals/registers
- Legacy peripherals are direct-mapped in PC/AT space
- Non-PC/AT peripheral cores memory mapped in MMCR
  - Watchdog Timer
  - Non-8254 PIT timers
  - SSI port
- Holes in 0000h-03FFh can optionally go to PCI Bus



ÉlanSC520 I/O Space

- PCI configuration space is indirect mapped at 0CF8h per PCI Specification (Mechanism #1)
- Unclaimed I/O is redirected to PCI Bus
  - Master abort if no target responds
- RTC/UARTs can be *disabled* and the space redirected to GP-Bus for external Super I/O



Systems in Silicon™

PCI Bus Host Bridge Arbitration Unit

AMD

Systems in Silicon™

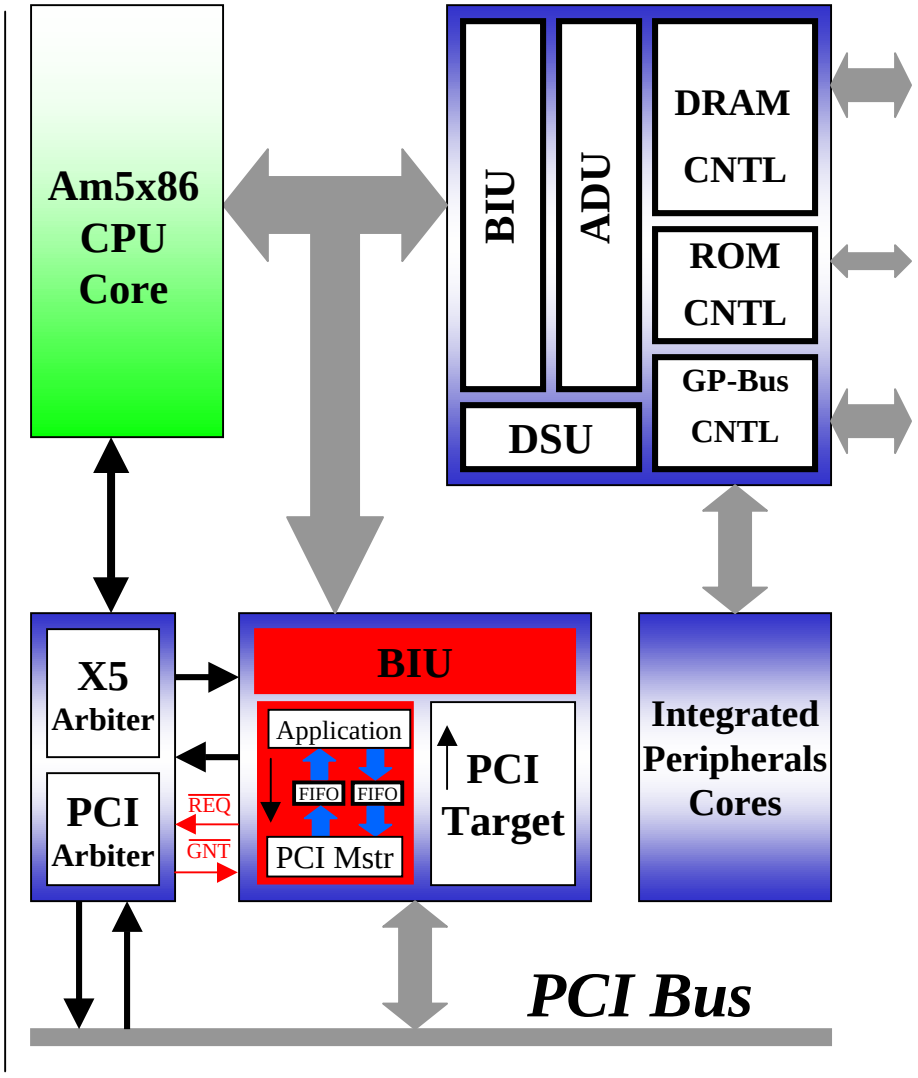
Host Bridge Overview

- Master side generates cycles on behalf of Am5x86 CPU only
  - Always single DWORD max (non-burst)
    - *CPU will not burst writes except for write-backs which won't go to PCI Bus (PCI Bus memory space is non-cacheable)*
    - *RDY# will be returned, even on multiple DWORD reads*
  - Internal configuration access not echoed to PCI Bus
- Target accepts cycles from PCI masters
  - memory only, within programmed DRAM region
  - accepts burst cycles
  - supports delayed transactions
  - contains 64 DWORD FIFO in both directions

AMD

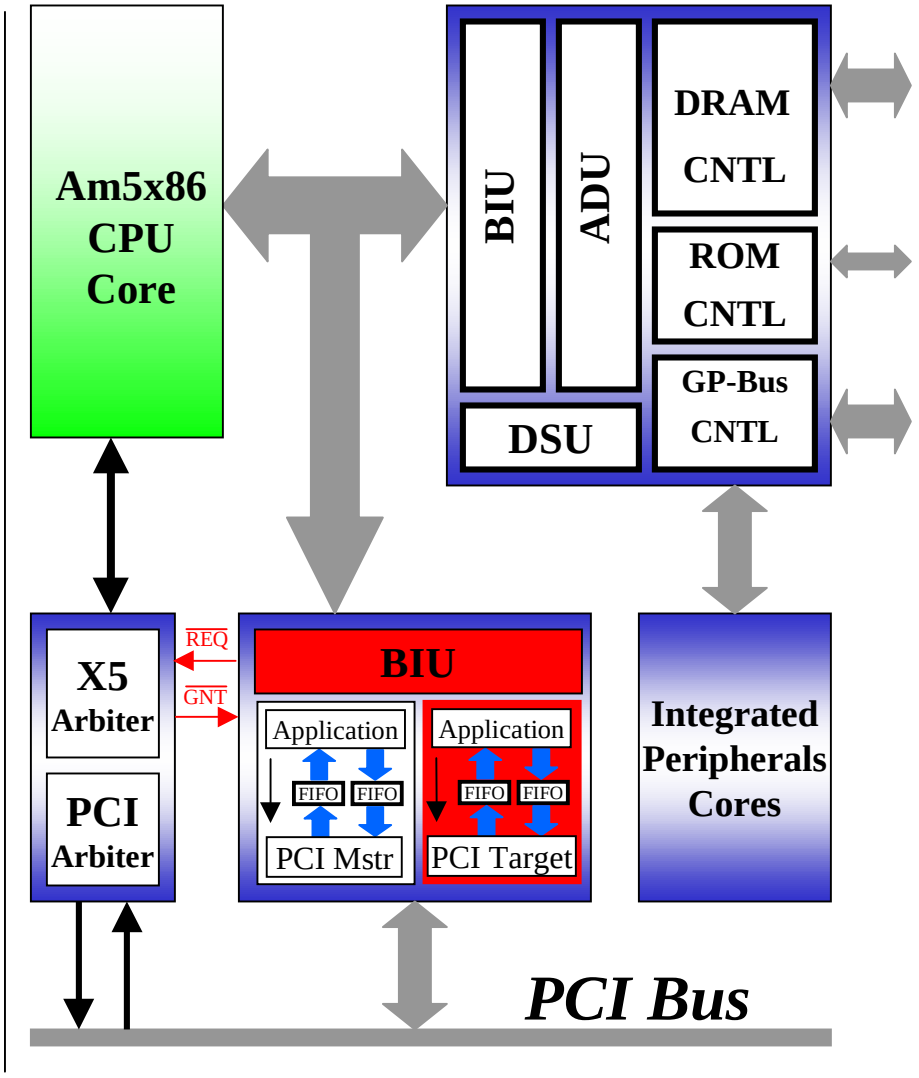
PCI Master Block

- PCI Configuration Space
- Converts X5 Bus cycle to PCI cycle
  - Requests bus from PCI Bus arbiter
  - Single cycles only
- Single level write posting buffer
- 2 level synchronizer between application layer and PCI Bus
- Address/data path for PCI AD[31:0] and separate X5 Bus address and data
- Retry options: 16, 64, 128 times before discarding



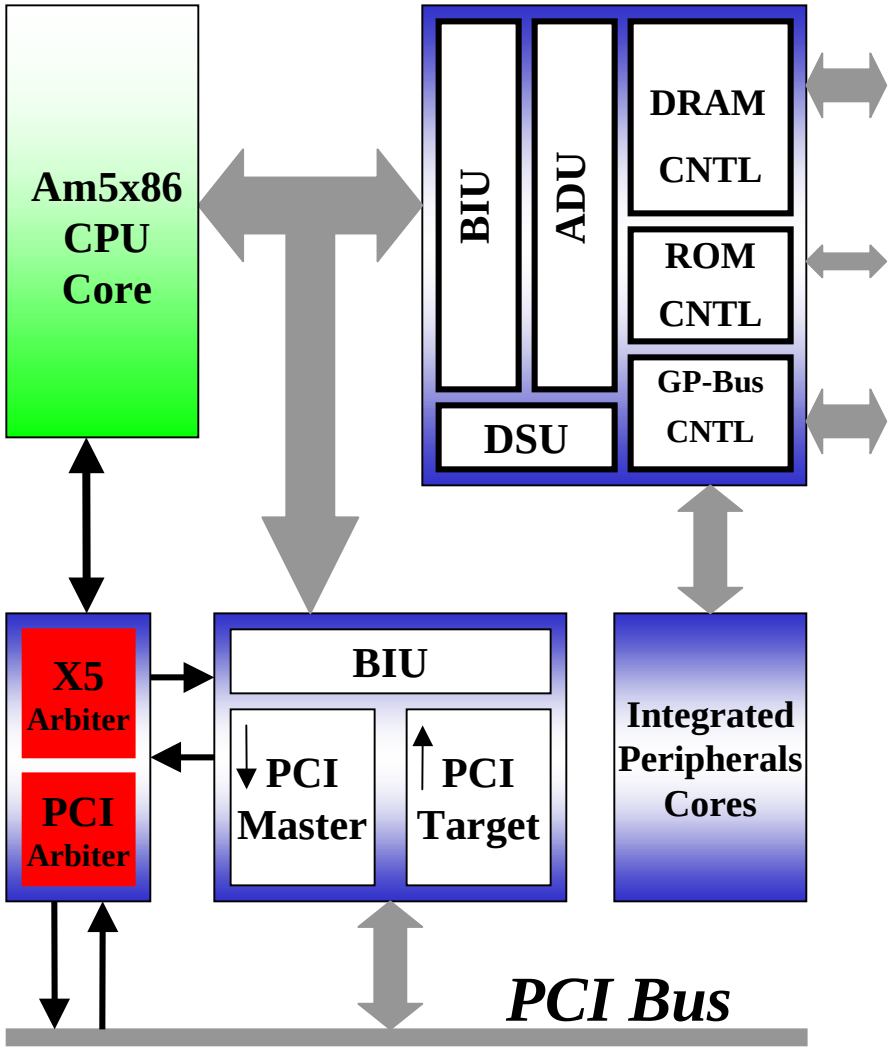
PCI Target Block

- Converts PCI cycles to X5 Bus cycles
  - Requests bus from X5 Bus arbiter
  - Complies to X5 protocol, 4 DWORD max per ADS#
- 64 DWORD FIFOs in each direction
- 2 level synchronizer between application layer and PCI Bus
- Delayed transaction support



Arbitration Overview

- Two separate arbiters
  - X5 Bus for CPU, DMA, and PCI Host Bridge
  - PCI Bus for external PCI masters and CPU
- Concurrent operation allows simultaneous (PCI peer to peer) and X5 Bus activity.
  - *Highest performance*
- Non-concurrent mode requires masters to gain ownership of both busses before starting transaction
  - *Lowest performance*



Systems in Silicon™

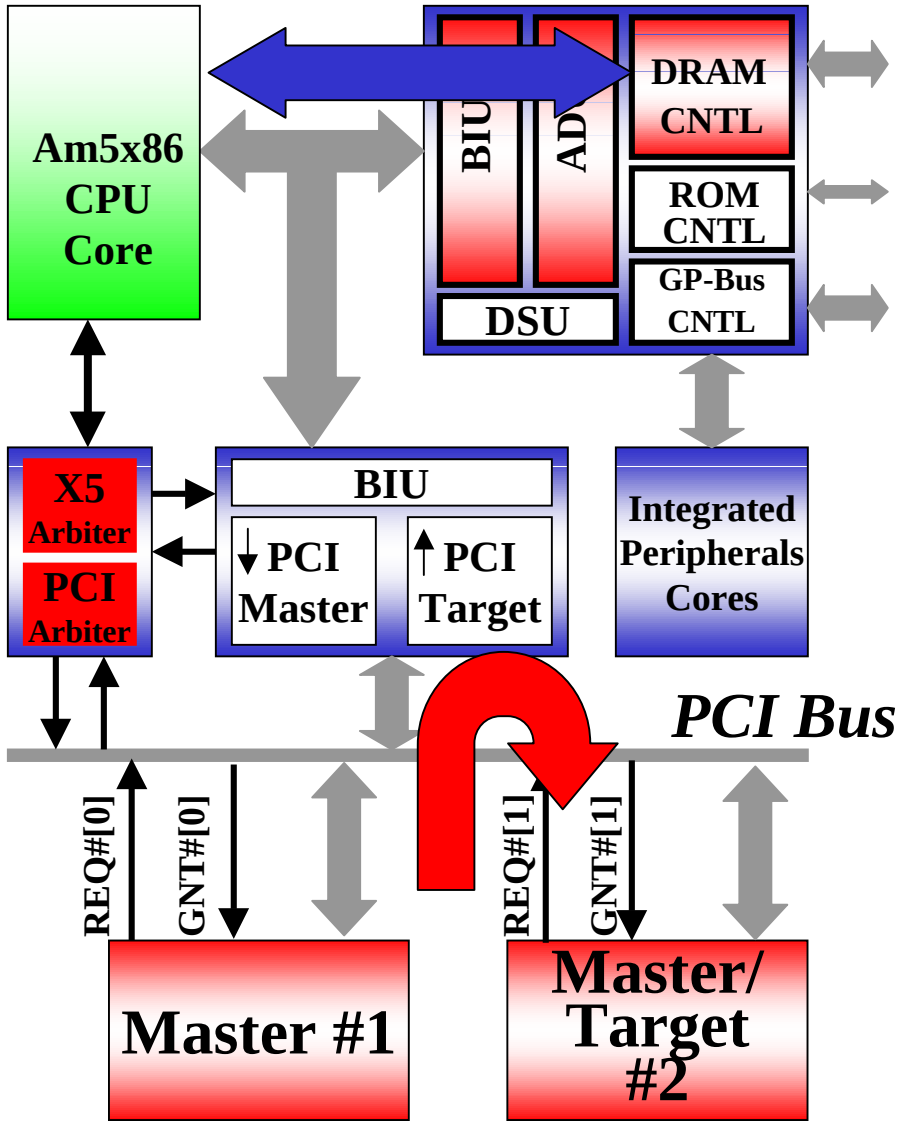
Arbitration Unit

- X5 CPU Bus Arbiter
  - Arbitrates between CPU, GPDMAC, and Host Bridge
  - Operates at 33 MHz in sync with CPU and X5 Bus
  - Participates in Dynamic Clock Change algorithm
- PCI Bus Arbiter
  - Arbitrates between CPU as PCI Bus Master and external masters
  - Operates at 33 MHz in sync with external PCI Bus clock
  - Supports five external PCI Bus masters

Concurrent Arbitration

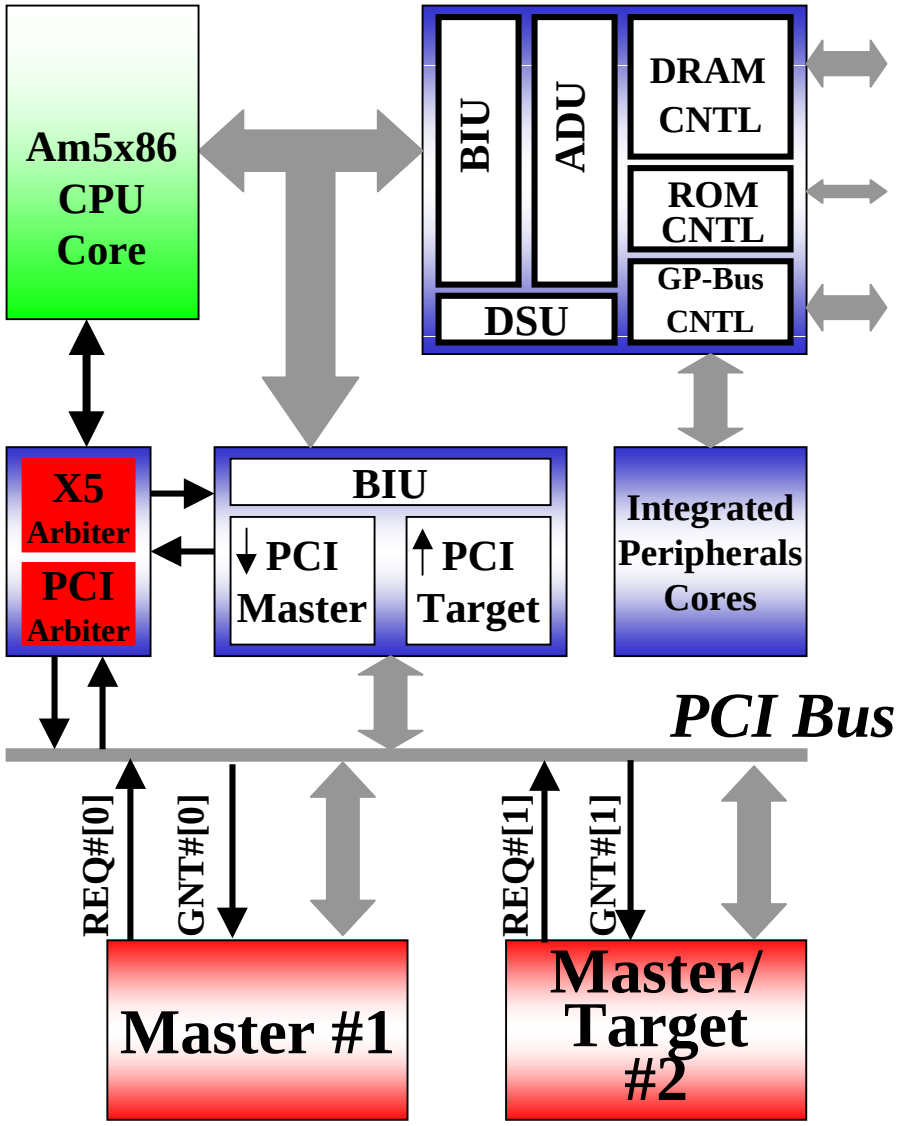
Concurrent operation allows simultaneous CPU Bus and PCI Bus cycles

- Peer to peer operation between two external PCI Bus agents.
  - Master #1 requests bus from PCI arbiter, which grants bus independent of any X5 Bus activity
- CPU access of DRAM, ROM or GP-Bus
  - CPU begins cycle without knowledge of PCI activity.
- DMA cycle between GP-Bus and DRAM
  - DMAC requests X5 Bus



Non-Concurrent Arbitration

- Any transfer requires that the bus master gain full ownership of both busses
  - Peer to peer PCI access requires PCI arbiter to gain ownership of X5 Bus *before* granting PCI master
- PCI arbiter must be programmed to park on CPU in this mode.
- Write posting must be disabled in this mode

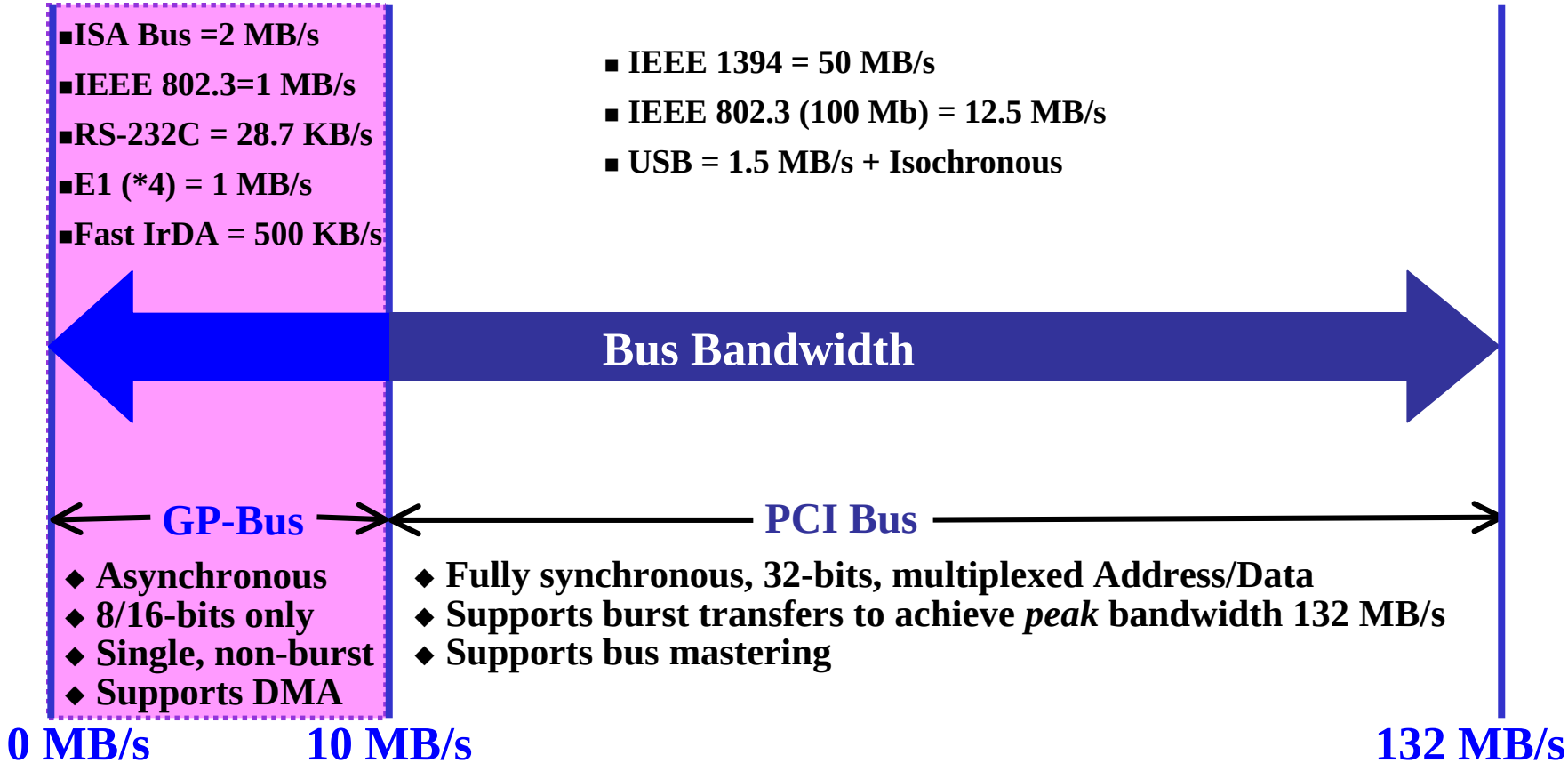


Systems in Silicon™

GP-Bus Controller
GP-Bus DMA Controller

AMD

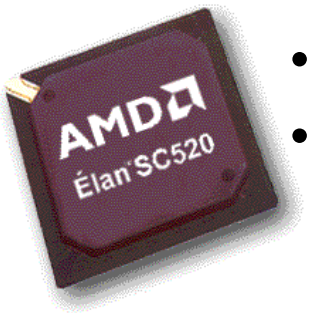
Bus Bandwidth Partitioning



Systems in Silicon™

GP-Bus Fact Sheet

- GP-bus is a 8/16-bit bus for interfacing “slower” peripherals
  - Internal Peripherals
  - External peripherals
- Internally interfaces to the X5 bus, and operates at 33 MHz
- Simple protocol to enable inexpensive interface logic
  - No Bus Mastering supported
  - No Burst cycles (easy interface, but lower performance)
- Only CPU can access GP-bus
- 32-bit CPU accesses are broken up
- Up to 8 chip selects with programmable space
- Up to four external DMA channels, target is always DRAM
- ROM devices can use SDRAM Data bus



GP-Bus and ISA Signals

	ISA Signal Name	GP-Bus Signal Name
Address Signals	SA19-SA0	GPA19-GPA0
	LA23-LA17	GPA23-GPA17
	(Not Supported)	GPA25-GPA24
Data Signals	SD15-SD0	GPD15-GPD0
Command Signals	MEMR_L	GPMEMRD_L
	MEMW_L	GPMEMWR_L
	IOR_L	GPIORD_L
	IOW_L	GPIOWR_L
Control Signals	MEMCS16_L	GPMEMCS16_L
	IOCHRDY	GPRDY
	REFRESH_L	(Not Supported)
	IOCHK	Supported through GPIRQ
	RSTDRV	GPRESET
	BALE	GPALE
	SBHE_L	GPBHE_L
IRQ/DMA Signals	IRQ	GPIRQ
	DRQ	GPDRQ
	DACK_L	GPDACK_L
	AEN	GPAEN
	TC	GPTC

Systems in Silicon™

GP-Bus Interfacing Simplicity

- Ease of interfacing (internal cores)
  - Enables smooth integration of Élan microcontroller peripherals (Z-bus)
  - Enables smooth integration of Am186CC peripherals (PCB-bus)
- Ease of interfacing (external devices) via user-defined programmable timing
- Control signals are like PC/AT ISA bus
  - ALE, BHE, MEMRD, MEMWR, IORD, IOWR, AEN, ….
  - RDY, MEMCS16, IOCS16, ….
  - GP-bus Programmable timing can also mimic ISA bus cycle timing
  - GP-bus Programmable timing can support fairly fast peripherals

Systems in Silicon™

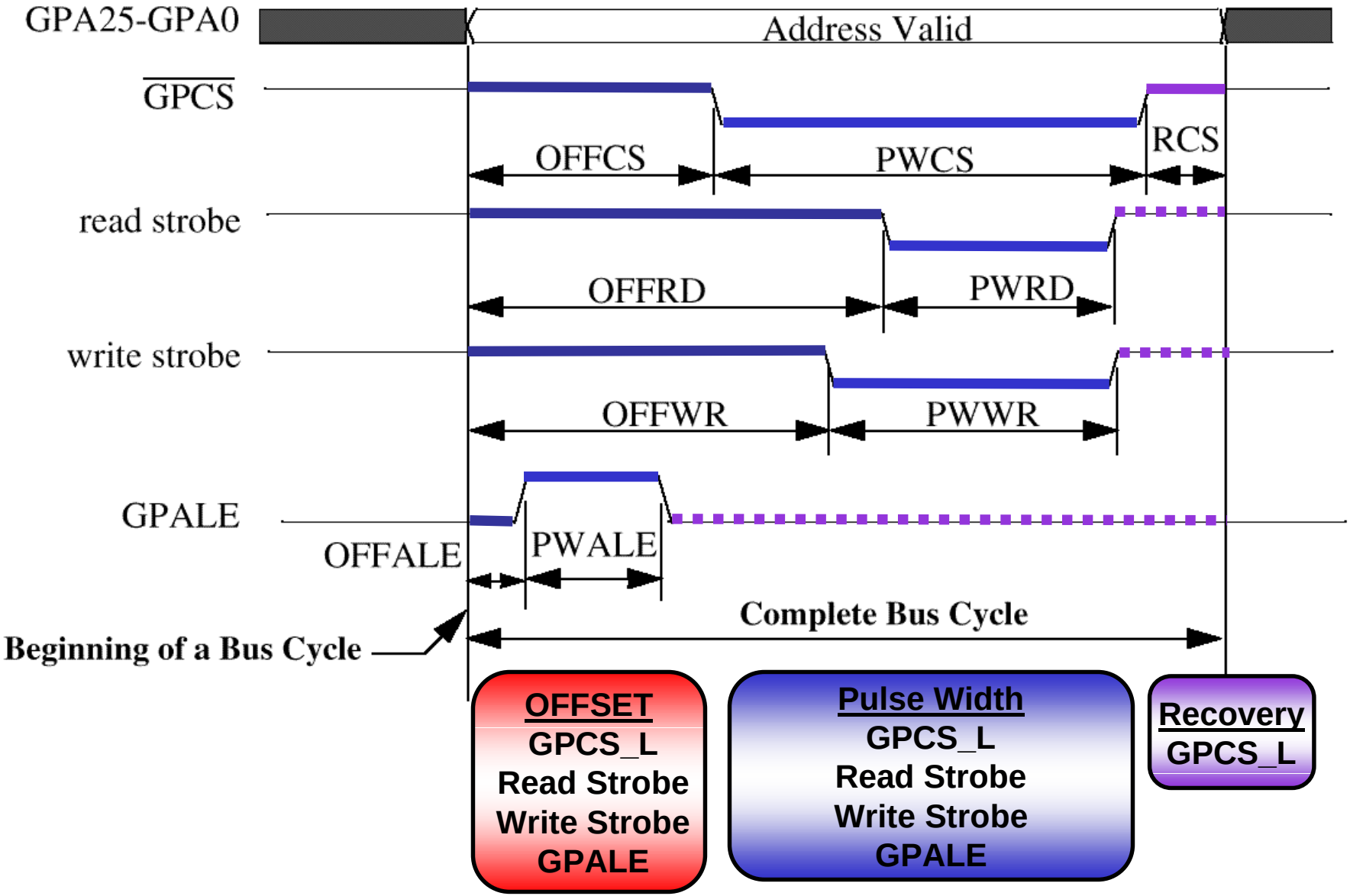
GP-Bus Programmable Timing

- Flexible interface through programmable timing parameters
  - setup time (Offset)
  - command duration (Pulse Width)
  - recovery time (only applicable to chip-selects)
    - Caveat: If not using any chip selects, user must still program the recovery time parameter

- Each of the 3 parameters is controlled by an 8-bit register
  - Time = (Reg_Val + 1) * 30 nS
  - Minimum cycle = (1 + 1 + 1) * 30 = **90 nS**
  - Maximum cycle = (256 + 256 + 256) * 30 = **23 µS**
- User can program timing for ISA Bus compatibility

AMD

GP-Bus Programmable Timing



GP-Bus Bandwidth

- Only the CPU can access GP-bus peripherals, and the minimum time between successive ADS assertions is 5 clocks
  - 4 clocks @ 33 MHz = 120 nS
    = 8.33 Mcycles/sec
    = 16.67 Mbytes/sec (raw bandwidth)
- Any overheads like code execution take away from the above raw bandwidth

GP-Bus Chip Selects

- Up to 8 external Chip select pins are available
  - Multiplexed with other pins
- Use PAR registers to set up
  - Space (Memory or I/O space)
  - Address Range (Start Address and Size)
- Use Pin Function and GP-bus registers to set up
  - Pin functionality
  - Optional qualification with command strobes
- Use GP-bus Timing registers to set up timing parameters
- Caveats
  - No GPCS pin can be asserted above 1 GB in Memory space
  - No GPCS pin can be asserted below 1 KB in I/O space
  - GP-bus is non-cacheable, and there is no support for write-protect violations or execution prevention

GP-Bus Bus Sizing

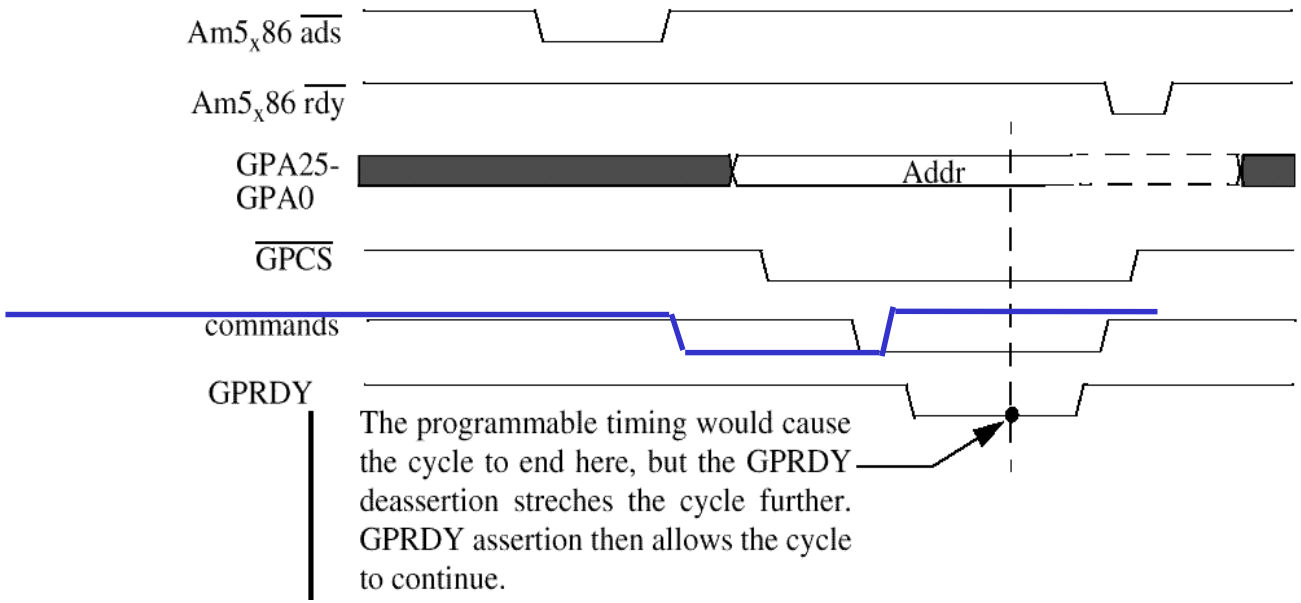
- GP-bus registers are used to program each device's size
  - Data width can be either 8-bit or 16-bit
- Dynamic Bus sizing
  - External devices can use GPMEMCS16 and GPIOCS16 pins to indicate size on a cycle-by-cycle basis
  - Overrides the programmed size settings for that bus cycle
- Recognition of the Sizing signals
  - GPMEMCS16 (or GPIOCS16) must be asserted at least 45 nS before command is deasserted

GP-Bus Wait State Control

- GP-bus timing registers are used to program each device's wait states (usually via the Pulse Width)
- Dynamic Wait State insertion
  - External Devices can use GPRDY pin to insert more wait states on a cycle-by-cycle basis
  - Overrides the programmed settings for that bus cycle
- Recognition of the Wait State signal (GPRDY)
  - Must be asserted at least 45 nS before command is deasserted
- Bus Hang
  - GP-bus can be infinitely hung if the GPRDY signal is left deasserted (low), resulting in a lock up

Effect of GPRDY on Cycle

- GPRDY can only stretch GP-Bus cycles, it cannot be used to provide early termination for the cycle
  - The control signals will always be asserted for a minimum of the entire period as programmed in the timing control registers, then additional delay may be inserted by the deassertion of GPRDY.



Systems in Silicon™

Sharing and Buffering GPD

- The ROM controller drives the GP-bus Address bus too
- ROM devices can use either the SDRAM data bus or the GP-bus's Data bus
  - (More info in the ROM controller section)

- The GPDBUFOE pin can be used to control transceivers
  - To resolve excessive loading on the GP-bus Data lines
  - To interface with 3V technology logic through transceivers

Systems in Silicon™

GP-Bus Echo Mode

- Echo mode is used to reflect accesses to internal GP-bus peripherals onto the external GP-bus
  - This is a debug aid we provide to the user
- Internal peripheral accesses are normally very fast, but when echo mode is on, these accesses adhere to the programmable timing parameters
  - Does not break user's desired conditions for external timing
  - Affects code execution timing
  - User must use GPAEN to prevent external peripherals from decoding "echoed" bus cycles

Systems in Silicon™

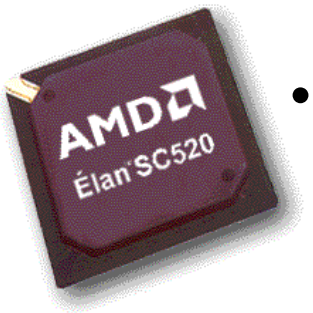
ROM Controller
SDRAM Controller

AMD

Systems in Silicon™

ROM Controller

- Flexible ROM/Flash interface
  - Supports 8/16-bit devices with data bus connected to GP-Bus
  - Supports 8/16/32-bit devices with data bus connected to SDRAM data bus
    - For XIP applications (2-1-1-1 with page mode devices)
    - Loading may impact SDRAM timing
  - Programmable timing supports slower devices as well as faster page mode (including new NVD Flash)
- PAR attributes support non-cacheable regions, write-protect regions, and non-execute regions
- Clocked from X5 Bus clock (33 MHz)

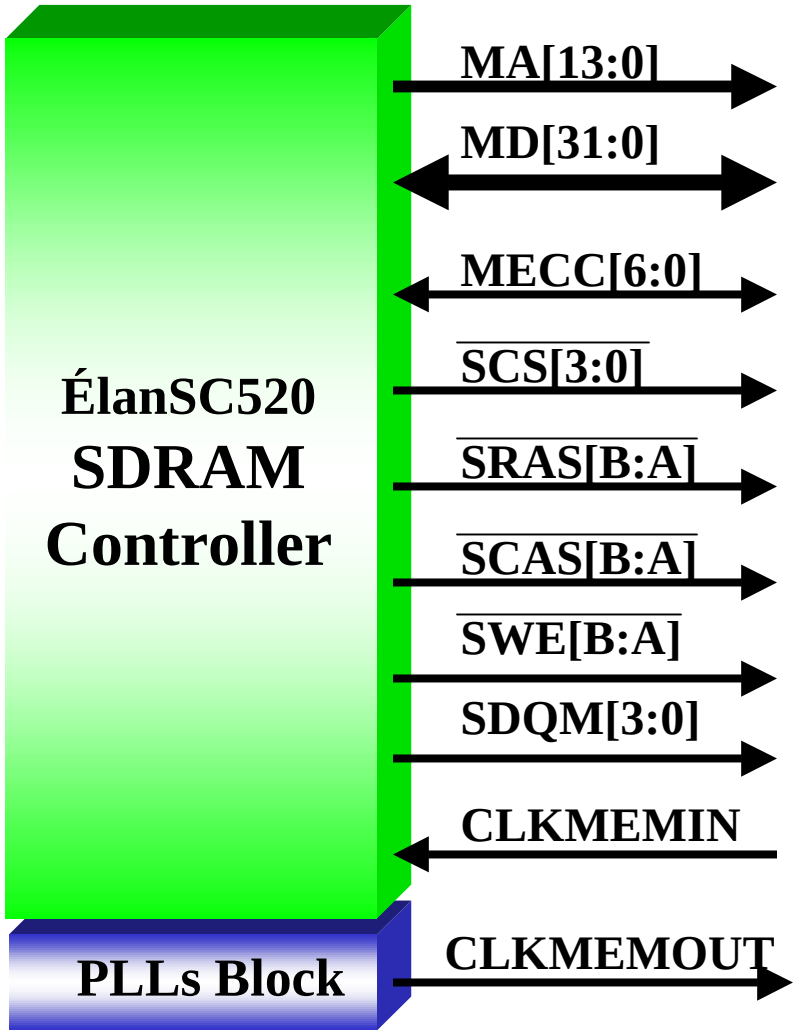


Systems in Silicon™

SDRAM Controller Overview

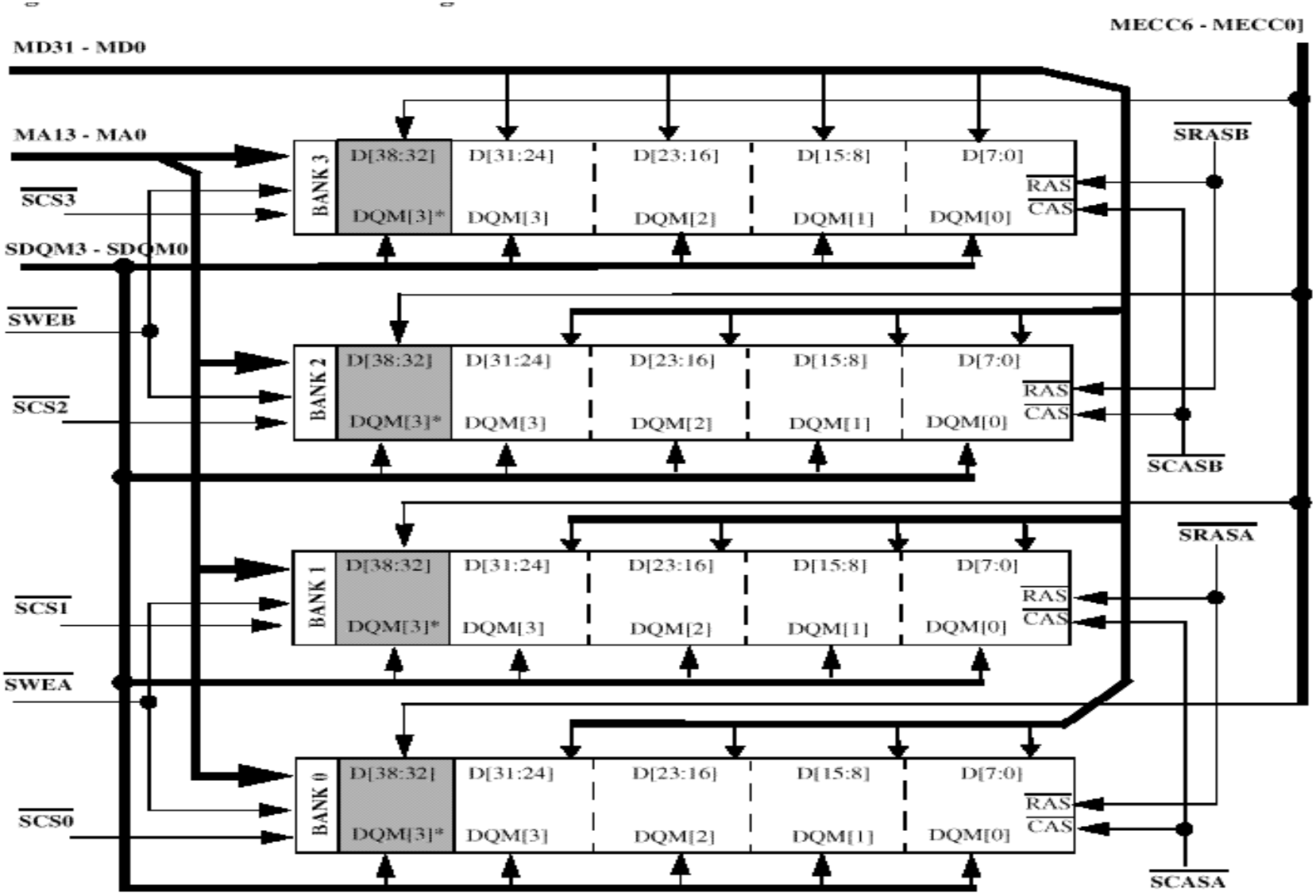
- Supports industry standard synchronous DRAMs
  - ÉlanSC520 interface is 66 MHz, we support faster speed SDRAMs but interface is still 66 MHz
- Supports up to four 32-bit banks for a total of 256 MB maximum
  - Independent size and symmetry per bank
- ECC optionally supported
- Refresh during reset optionally supported
- Performance features:
  - 32 rank write-buffer and 8 DWORD Read Ahead Buffer improves performance and optimizes DRAM interface bandwidth to accommodate multiple masters

SDRAM Controller Pins

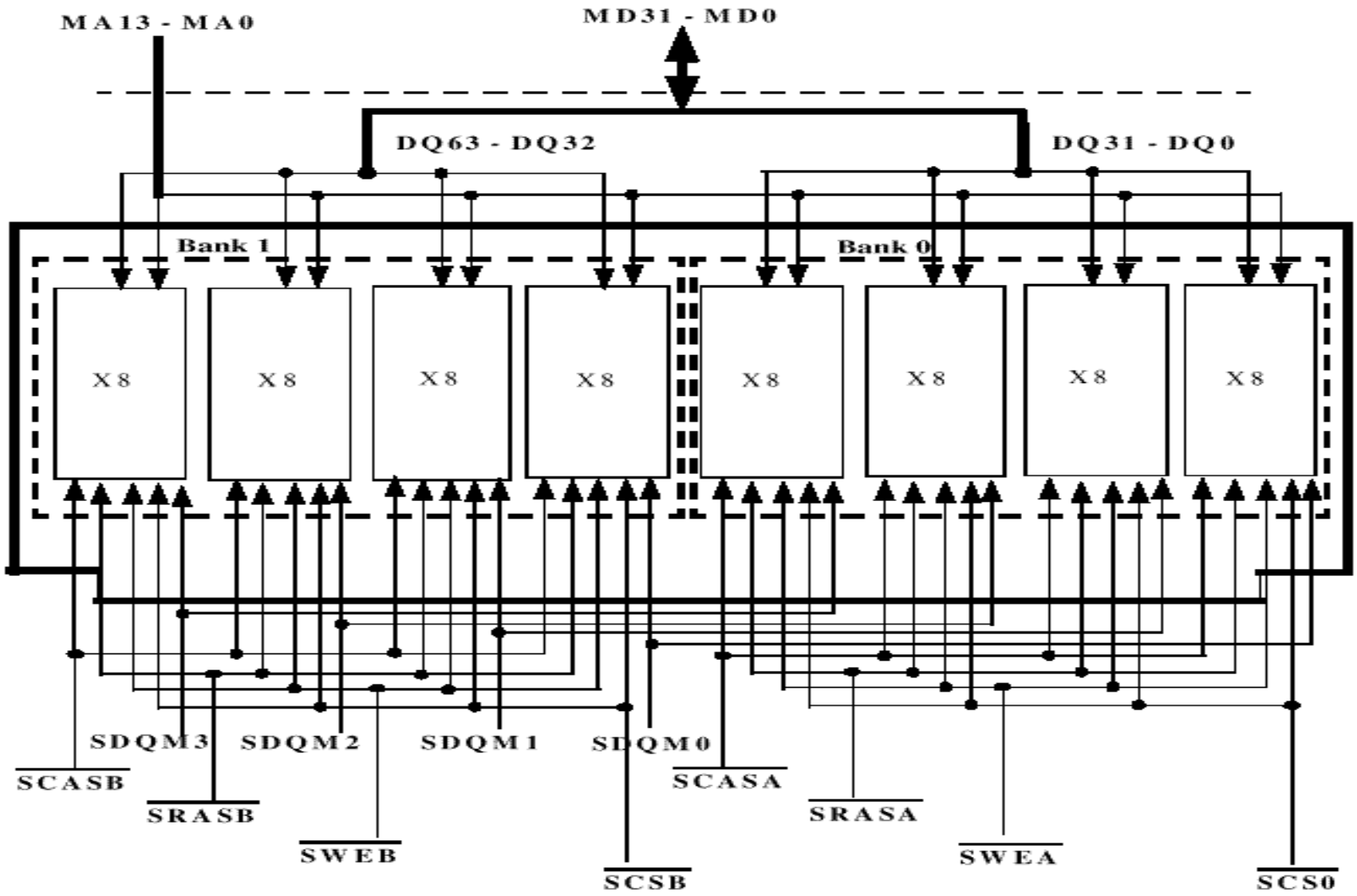


- MA[13:0]
  - multiplexed address bus
- MD[31:0], MECC[6:0]
  - 32-bit data, 7-bits for ECC
- $\overline{\text{SCS}}$[3:0]
  - SDRAM banks chip selects
- $\overline{\text{SRAS}}$[B:A]
  - Row Address Strobe
- $\overline{\text{SCAS}}$[B:A]
  - Column Address Strobe
- $\overline{\text{SWE}}$[B:A]
  - Write command
- SDQM[3:0]
  - Data mask per byte

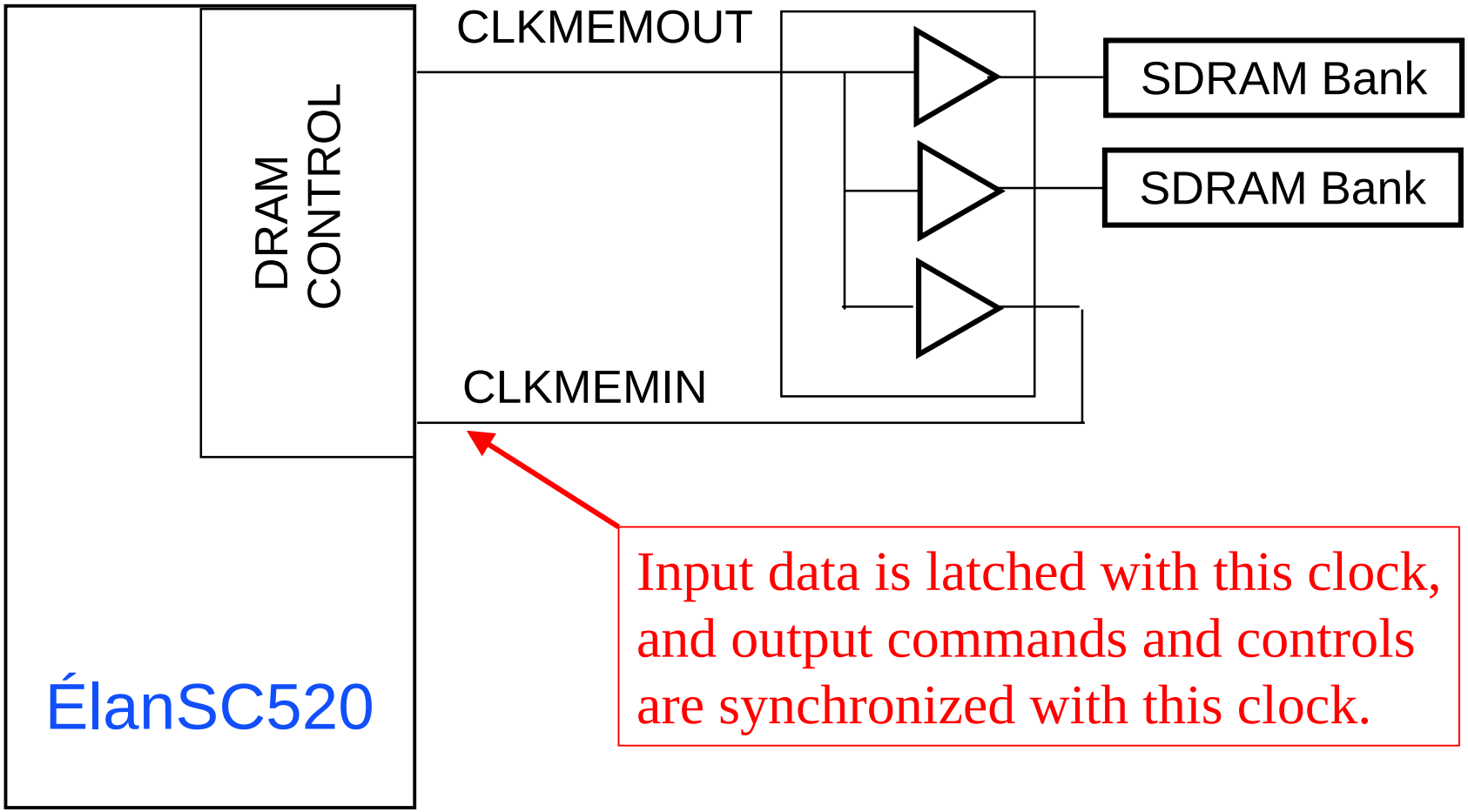
SDRAM Array in ElanSC520 System



SDRAM DIMM Connection



External Clock Routing



ECC Support

- Uses modified Hamming Code to generate 7-bit check word from the DWORD
  - Requires boot code to completely initialize all of DRAM to generate valid ECC that is stored in DRAM
- Single bit errors corrected, multiple bit detected
  - Corrected data given to master, not written to DRAM
  - Interrupt generated, address and bit position stored
  - Separate interrupt provided for multiple bit errors
- Sub-DWORD writes result in performance loss
  - Requires Read-Modify-Write to generate ECC
  - Write buffer hides this if it has empty ranks

SDRAM Refresh Options

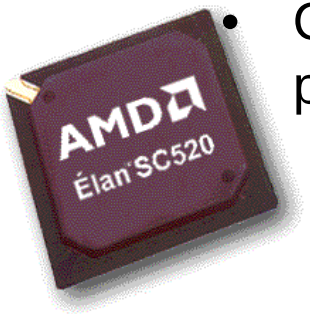
- "Auto-Refresh" analogous to CBR in async DRAMs
- Refresh rate is derived from 32 KHz clock
  - Flexible rate supports wide variety of devices
- Staggered refresh due to high current requirements
  - All internal SDRAM banks refreshed simultaneously
  - Only refresh enabled banks
- Optional refresh during programmable reset

DRAM Refresh Rates

Number of Rows	Refresh Rate		
	15.6us	31.2us	62.5us
256	4ms	8ms	16ms
512	8ms	16ms	32ms
1024	16ms	32ms	64ms
2048	32ms	64ms	128ms
4096	64ms	128ms	
8192	128ms		

Refresh Rate = Rows/Interval

Example: 4096 rows (12-bits) with 64 mS refresh requirement must be distributed every 15.6 µSec



SDRAM Timing Options

Systems in Silicon™

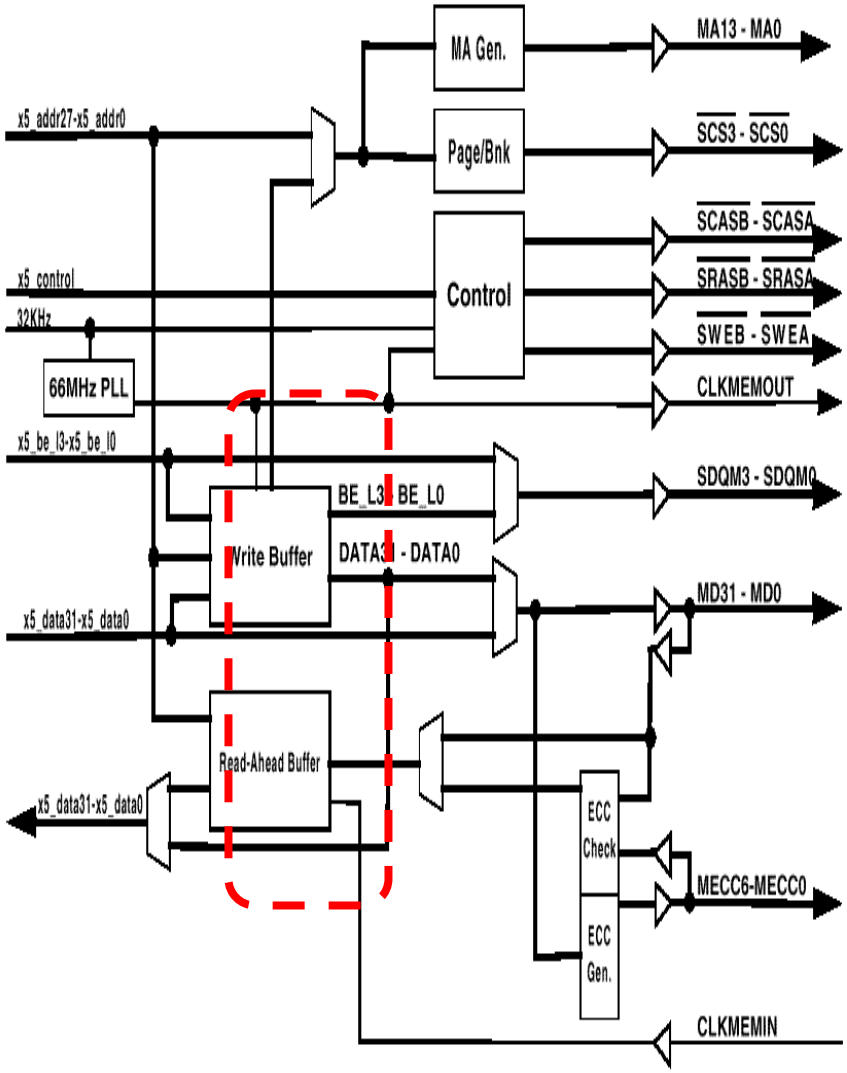
- ÉlanSC520 provides three programmable timing parameters:
  - CAS# Latency
    - 2 or 3 clocks (66 MHz)
    - Affects SDRAM device only
  - RAS# Precharge
    - 2, 3, 4, or 6 clocks (66 MHz)
    - Affects state machines only, not loaded into device.
  - RAS# to CAS# Delay
    - 2, 3, or 4 clocks (66 MHz)
    - Affects state machines only, not loaded into device.

- **CAS# Latency**
  - The number of clocks from the time the read command is issued until the *first* piece of data is available.
- **RAS# Precharge**
  - Minimum time period that must be met following a precharge command until a subsequent command to the same bank can be sent.
- **RAS# to CAS# Delay**
  - Minimum time between an ACTIVE command and a read or write command can be issued.

AMD

SDRAM Data Buffering

- Write Buffer and Read Ahead Buffer optimize SDRAM system bandwidth
- Separate arbiter in SDRAM Controller arbitrates between read, write, and refresh cycles
- Buffering and coherency allows SDRAM reads to be prioritized over writes



Systems in Silicon™

ÉlanSC520 Integrated GP-Bus Peripherals

AMD

Systems in Silicon™

ÉlanSC520 Integrated Peripherals

- Located on ÉlanSC520 internal GP-Bus
- Fast access times: 2 CPU wait states
- ÉlanSC520 provides:
  - PC/AT compatible peripherals and logic
  - Enhancements to these PC/AT peripherals
  - Additional Peripherals (non-PC/AT)

Systems in Silicon™

ÉlanSC520 PC/AT Peripherals

- ÉlanSC520 provides peripherals needed to maintain PC/AT Compatibility
  - Including PC/AT compatibility Logic (A20GATE, PORT-xx)
- Run DOS, Windows, RTOS, whatever runs on a PC
- ÉlanSC520 provides enhancements to each PC/AT core
  - PIC: More sources, Flexible routing, Pin configuration options
  - DMAC: Larger pages and counts, Routing, Buffer chaining
  - UARTs: Capable of using DMA, Faster baud rates
  - PIT: Clock input for DOS, Additional interrupt capabilities
  - RTC: NMI Enable bit has moved
- The extensions are memory-mapped (MMCR registers)

Systems in Silicon™

Non-PC/AT Peripherals

- ÉlanSC520 also provides additional non-PC/AT peripherals
- Useful for many communications and general embedded applications
  - General Purpose Timers
  - Watchdog Timer
  - SSI Port
  - Software Timer
  - PIOs
- These peripherals are memory-mapped (MMCR registers)

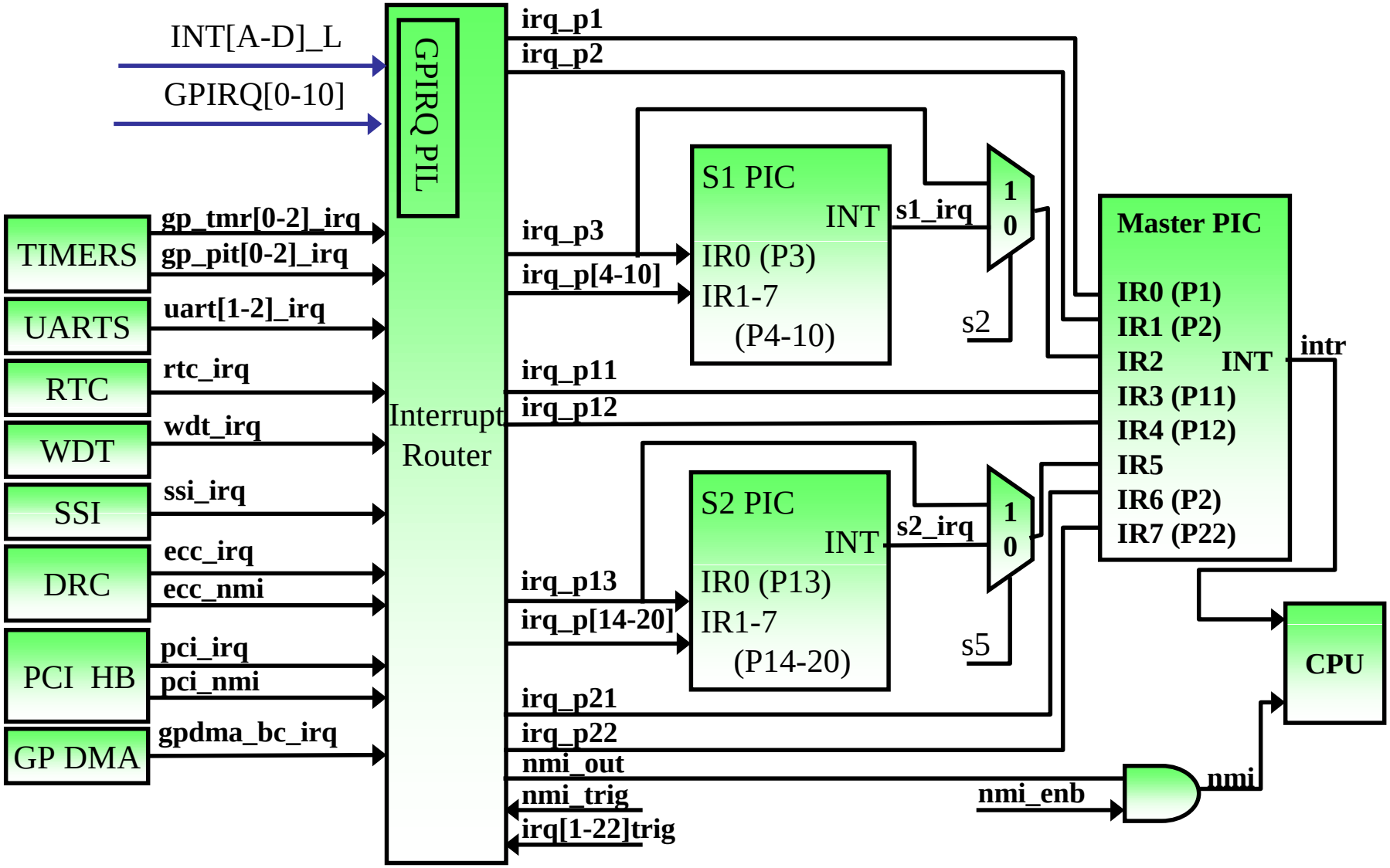
Systems in Silicon™

Interrupt Controller (PIC)

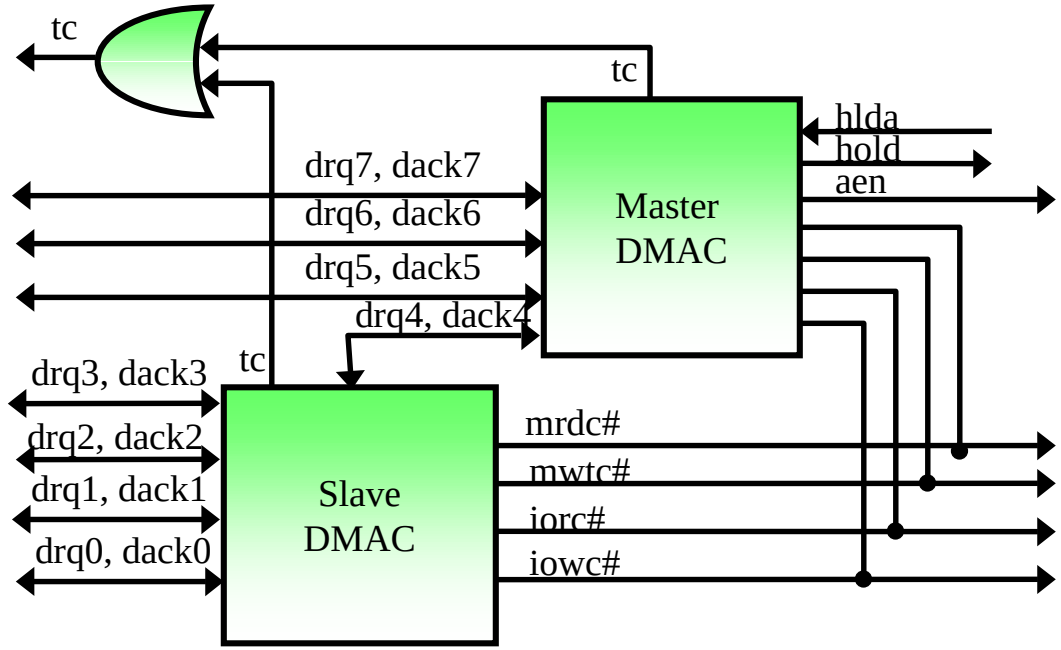
- Consists of three 8259s (i.e. 22 priority levels)
  - Slave-1 output feeds into Master's IR2 (with bypass)
  - Slave-2 output feeds into Master's IR5 (with bypass)
- Interrupt sources (31 total)
  - 16 internal sources
  - Up to 15 external sources
    - Programmable to be edge or level
    - Programmable polarity
- Flexible Routing (31 x 23 crossbar switch)
  - 31 interrupt sources can be routed into 22 priority levels, or into NMI
    - Any source can be routed to any priority of maskable interrupt
    - Any source can also cause NMI

AMD

PIC Block Diagram



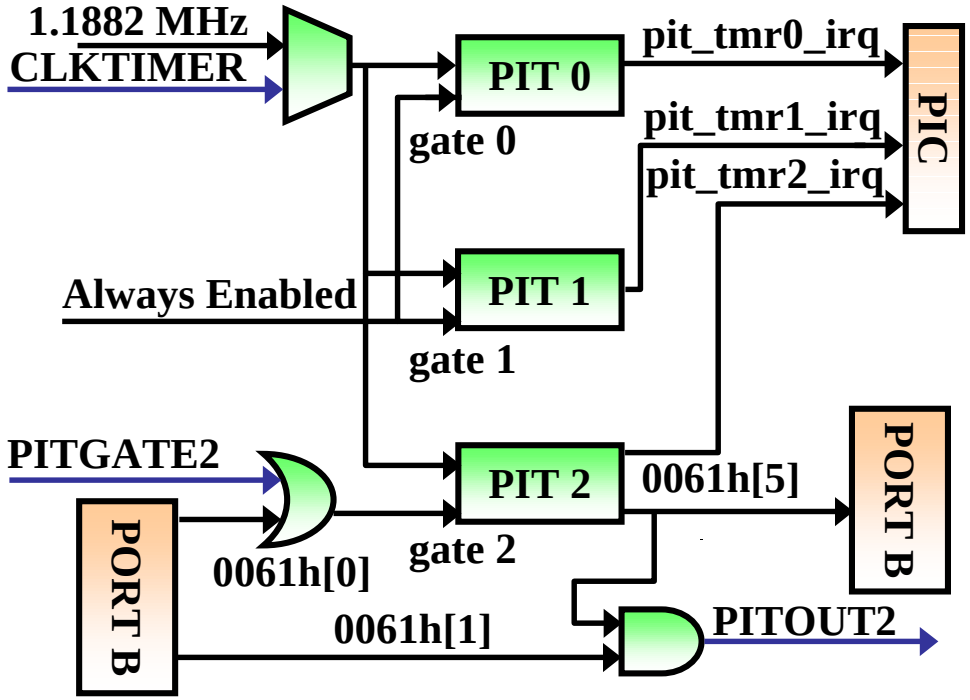
PC/AT DMAC


tc
tc
hlda
hold
aen
drq7, dack7
drq6, dack6
drq5, dack5
drq4, dack4
Master
DMAC
drq3, dack3
drq2, dack2
drq1, dack1
drq0, dack0
tc
Slave
DMAC
mrdc#
mwtc#
iorc#
iowc#

PC/AT Timers (PIT)

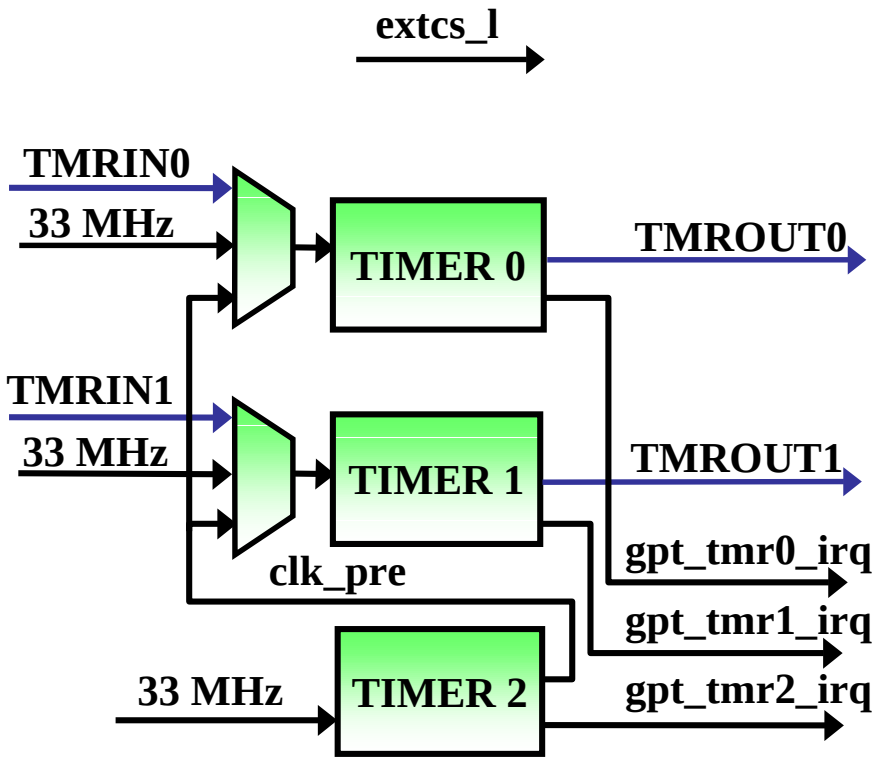
- PC/AT-compatible Programmable Interval Timer (PIT) that consists of 3 16-bit timers
- Clock to all three timers is
  - 1.1882 MHz or
  - External pin source if exact

    PC frequency is desired
- 3 independent interrupts
  - Superset of PC/AT
- PITOUT2 is like SPKR
- Various modes of operation



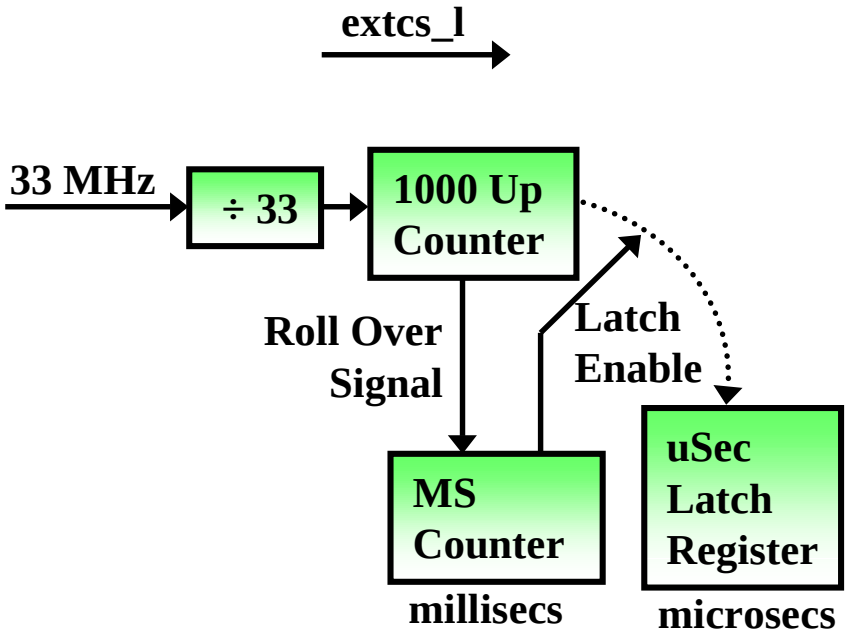
General Purpose Timers

- Imported from the 186 family
- Three 16-bit timers
  - Flexible cascading for 32-bit operation
  - Upto 120 nS resolution (33 MHz)
- Timer input and output pins provide ability to interface with off-chip hardware
  - Counting, PWM/PWD, etc.
- 3 independent interrupts
- Multiple internal modes



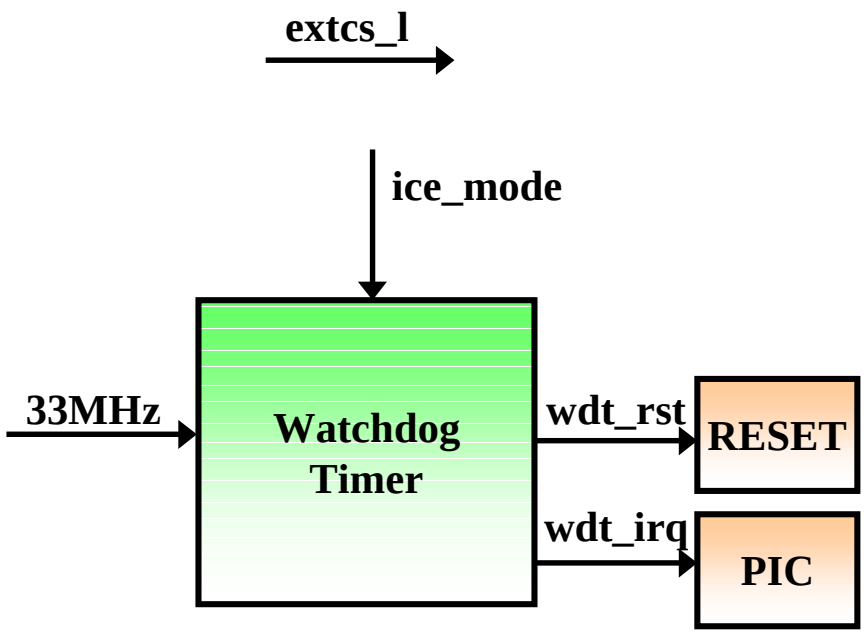
Software Timer (SWT)

- Software Timer eases the task of keeping system time
  - 1 uS resolution
  - O/S uses
  - Usable for performance monitoring
- Microsecond latch register that reports the last time the millisecond counter was read
- The 16-bit millisecond counter is reset to zero when it is read
- Both counters are zero upon reset
- No interrupts or pins



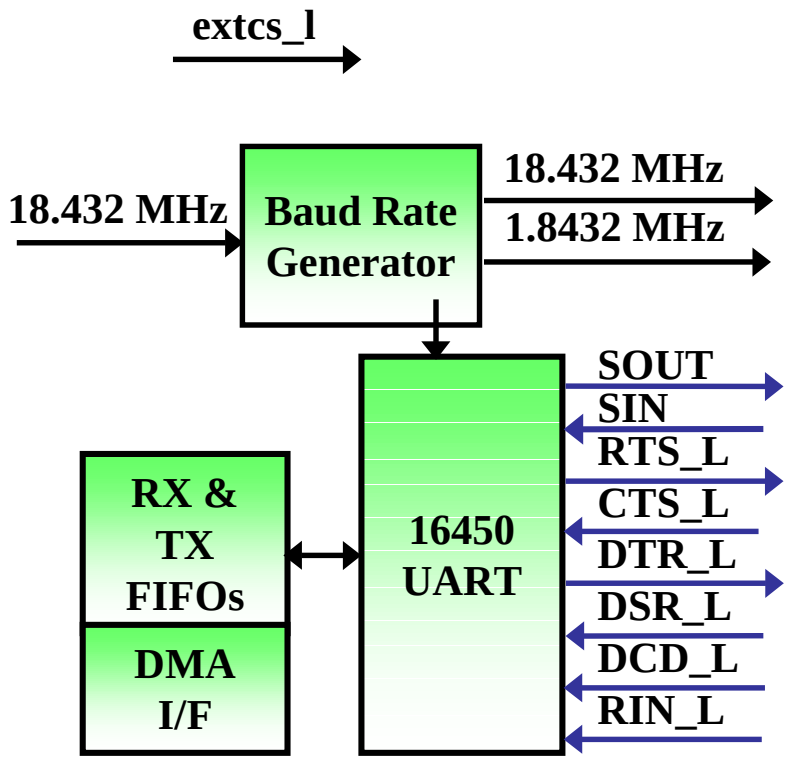
Watch Dog Timer (WDT)

- Used to regain control from runaway software
  - Programmable up to 32 secs
- Imported from the Am186CC
- Keyed sequences for writes to WDT configuration register
- Programmable to generate
  - System reset or
  - Interrupt
- Reset status flag readable for identification by boot code
- Stopped in ICE mode



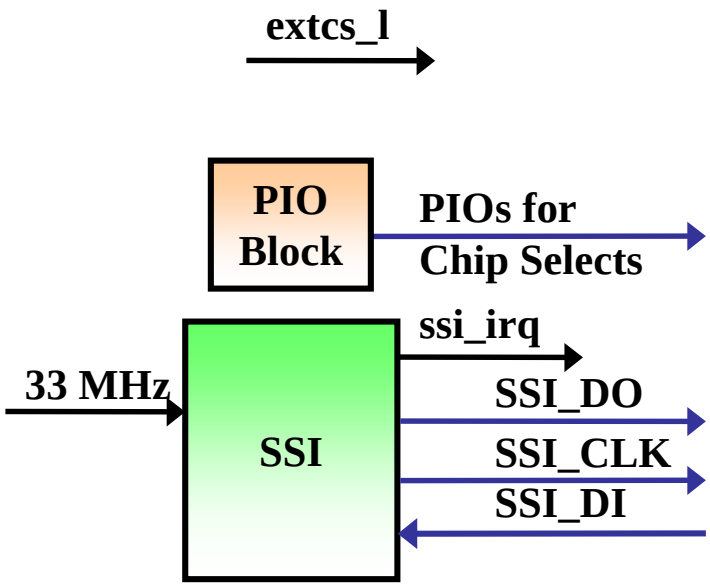
UARTs

- Two integrated 16450-16550 compatible UARTs
  - FIFOs can be disabled
- 8 pin modem capability (both)
- Enhancements over PC/AT
  - Goal to operate at up to 1.5 Mbits/s
  - Each UART can use the integrated GPDMAC (8-bit channels only)
- Can be individually disabled if using external UARTs
  - Interrupt routing still needed



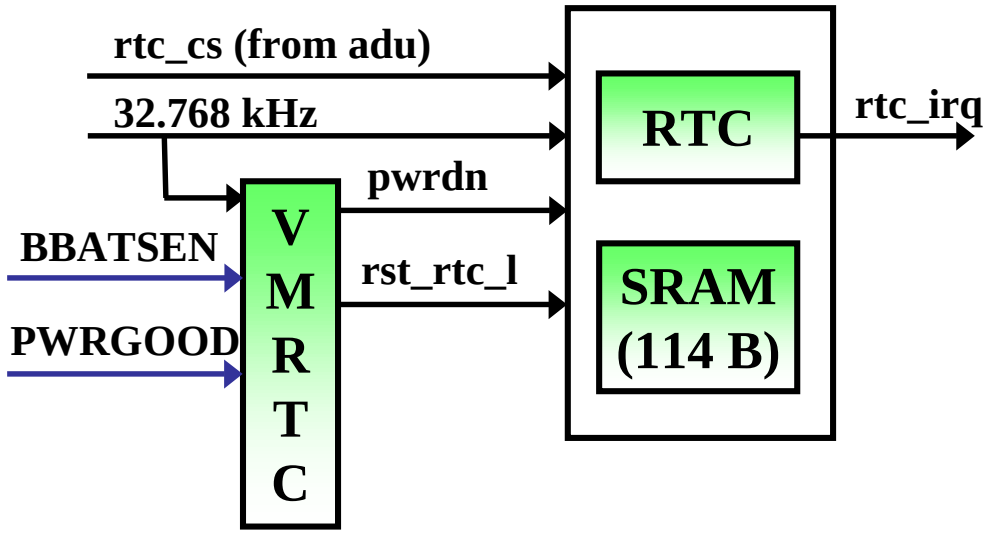
Synchronous Serial Interface

- Synchronous Serial Interface (SSI) compatible with SCP, SPI, and Microwire slave devices
- Flexible clocking and bit-order
- Full-duplex mode by using the TX+RX command
- Programmable for 4-wire or 3-wire interface
  - By connecting SSI_DO to SSI_DI
- Device enables via PIO pins
- Interrupt driven
- No DMA support



Real-Time Clock (RTC)

- RTC and RAM has battery backup capability
- Many configurations for Voltage Monitor (VMRTC)
- Many RTC conditions can cause interrupt
- Can be disabled to use external RTC
  - Interrupt routing still needed
- PC/AT compatible
  - Except for the NMI Enable Bit



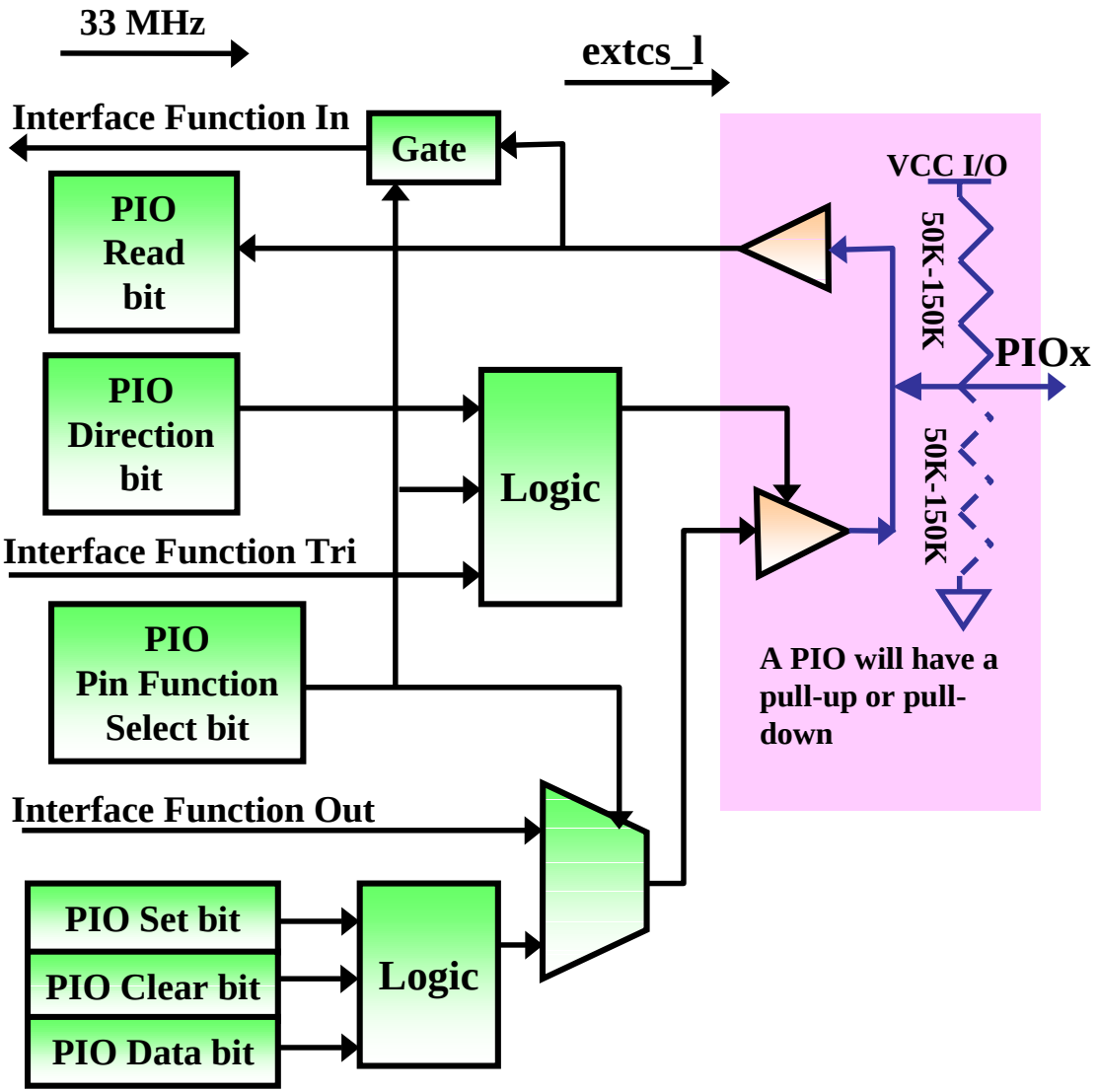
Systems in Silicon™

PC/AT Compatibility Logic

- PC/AT-compatible functions for control of
  - A20GATE
  - CPU Soft Reset
    - Ports 60h, 64h, 92h
  - Port 80h
- Port 80h, 60h/64h cycles echoed externally also, to maintain compatibility with legacy systems

Programmable I/O (PIO) Pins

- 32 PIOs
- Pins are multiplexed with other interface functions
- Better Software interface
  - Write, Set or Clear operation for outputs
  - Read side reads pin
- PU or PD according to Interface function need
- Initialization order is important



Systems in Silicon™

AMD Élan™SC520 Microcontroller Hardware Support

AMD

AMD Total Solution

Improve your time to market with a Total Solution from AMD and its partners.

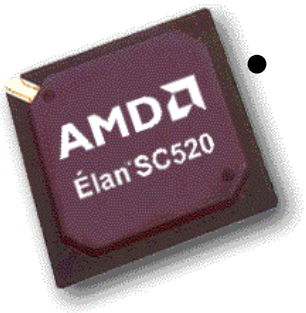
- Hardware Support
  - Customer Development Platforms
  - Reference Design
- CodeKit Software Packages
- Fusion Partners
- AMD Authorized Developers

Élan™SC520 Microcontroller Customer Development Platform

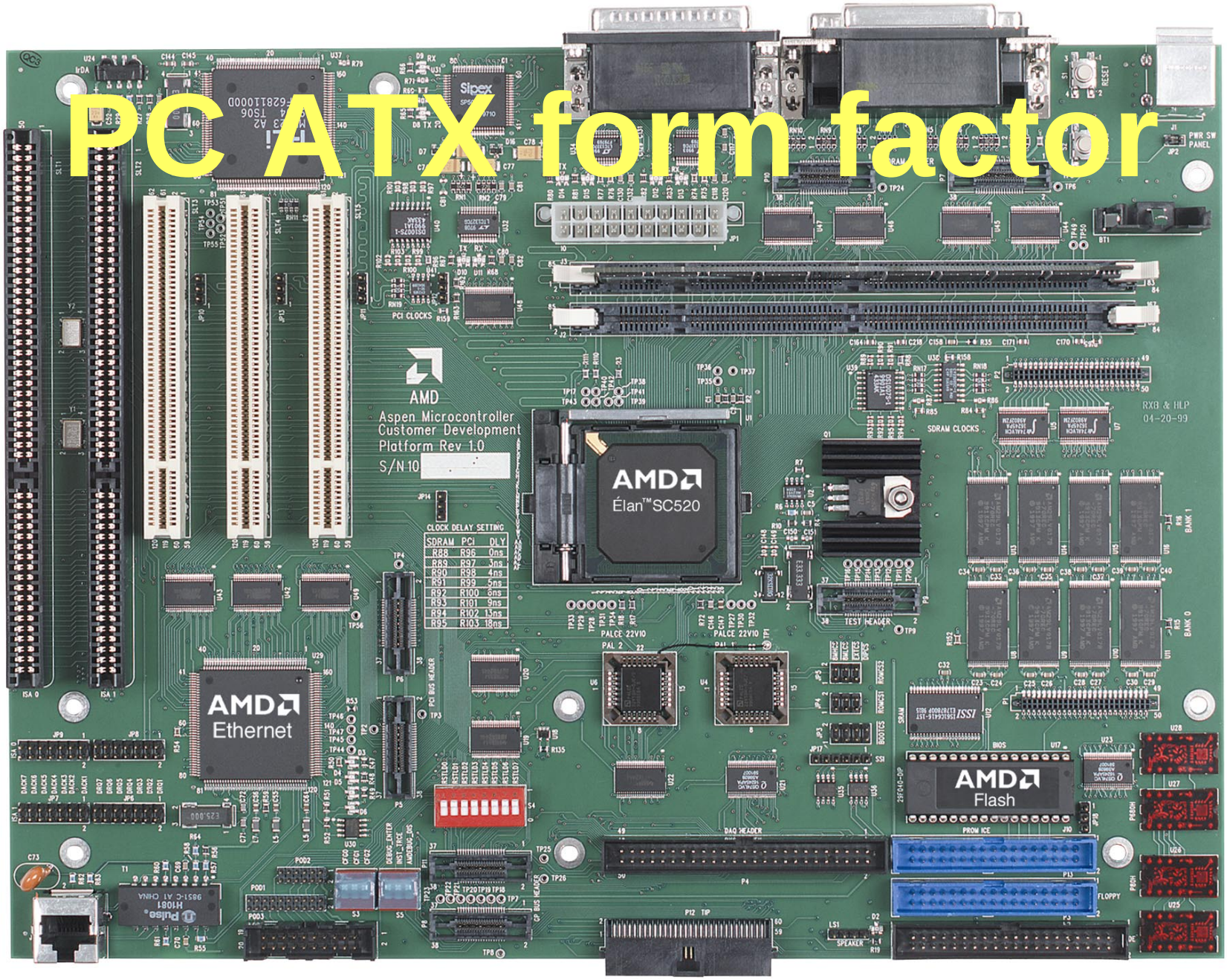
Systems in Silicon™

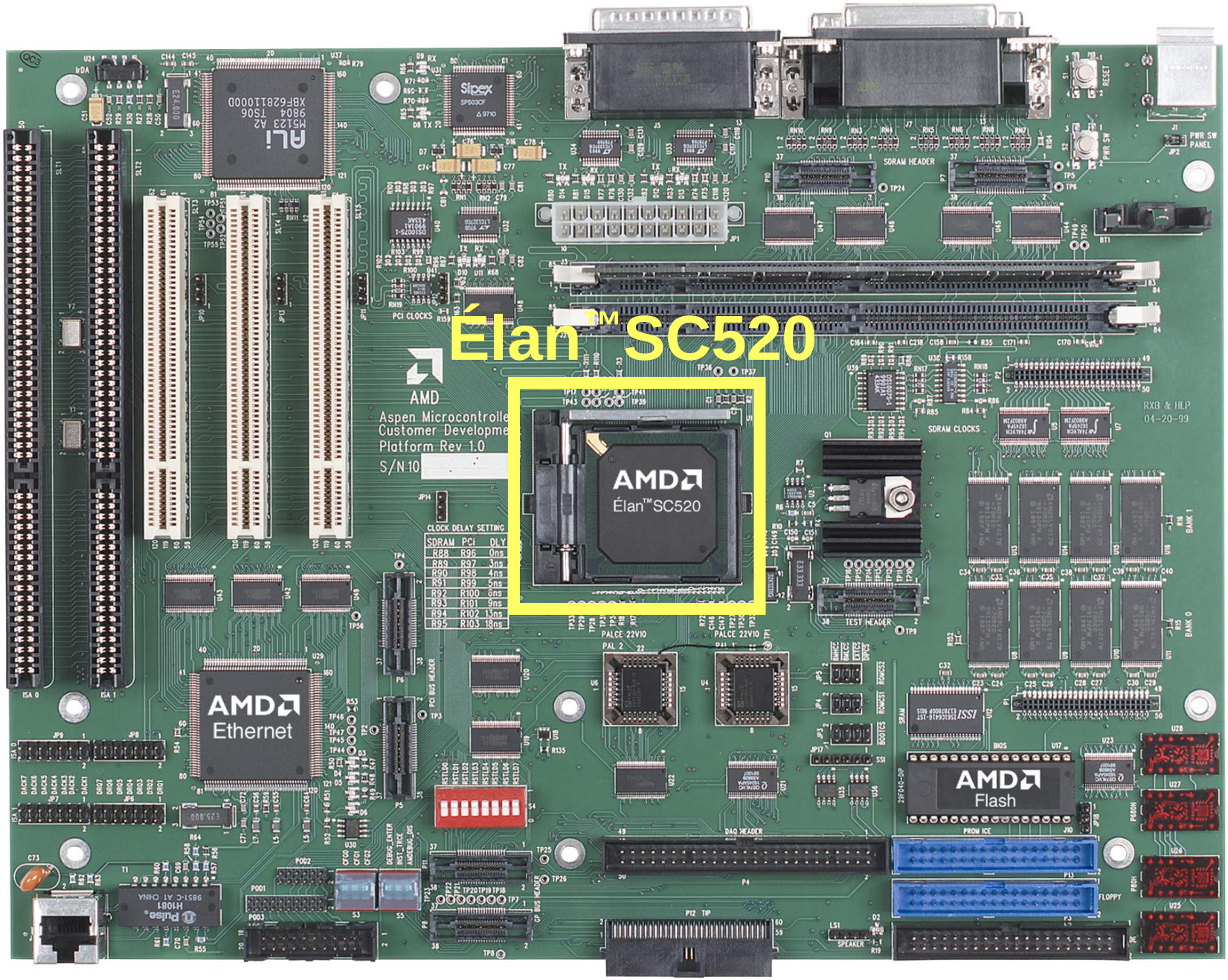
The **ÉlanSC520 Microcontroller CDP** is an excellent tool to begin hardware and software development.

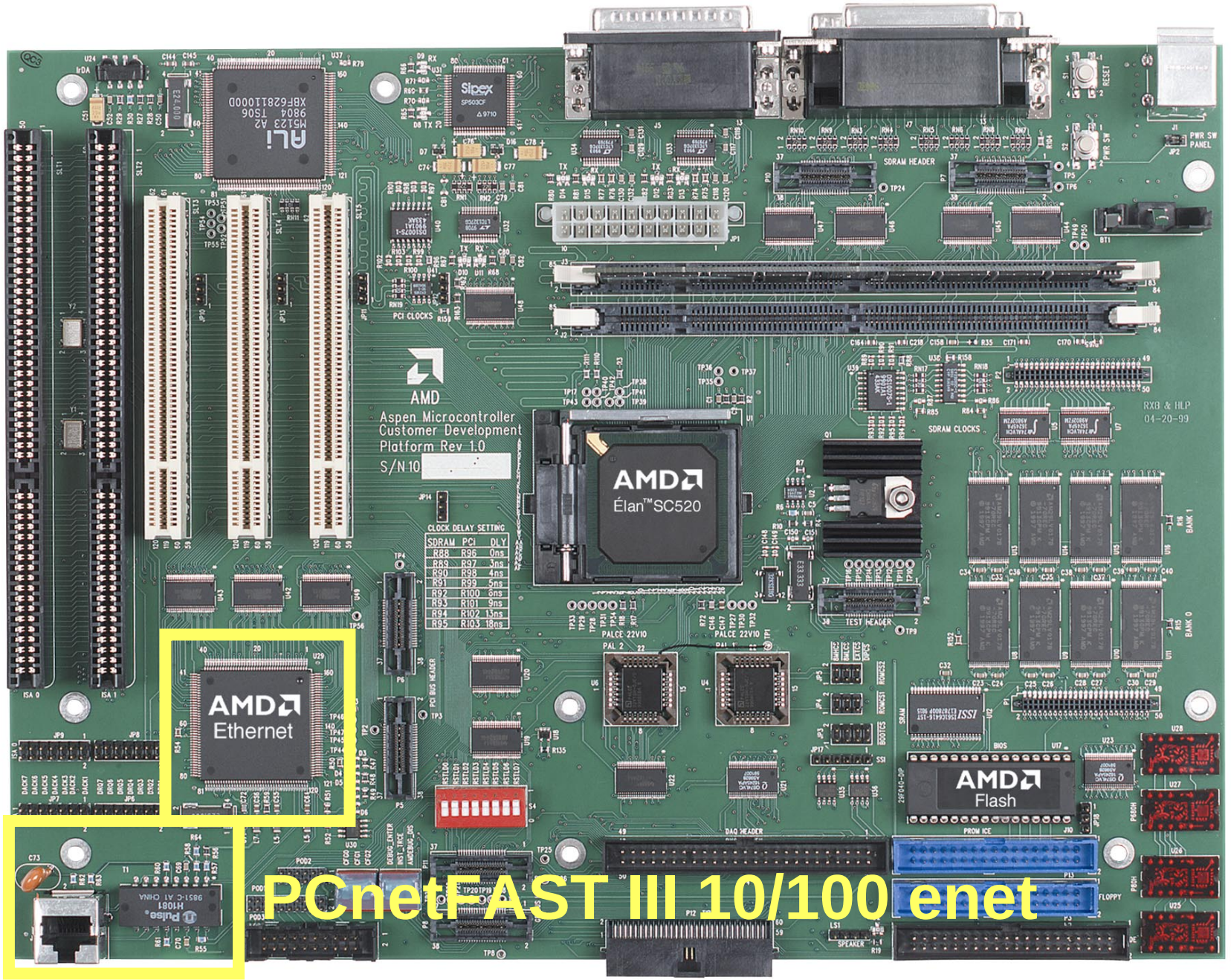
- Standard PC/AT form factor
- Expansion slots, ISA and PCI
- 10/100 Ethernet
- Debug and test ports
- Large Flash memory array
- Schematics / BOM / Documentation

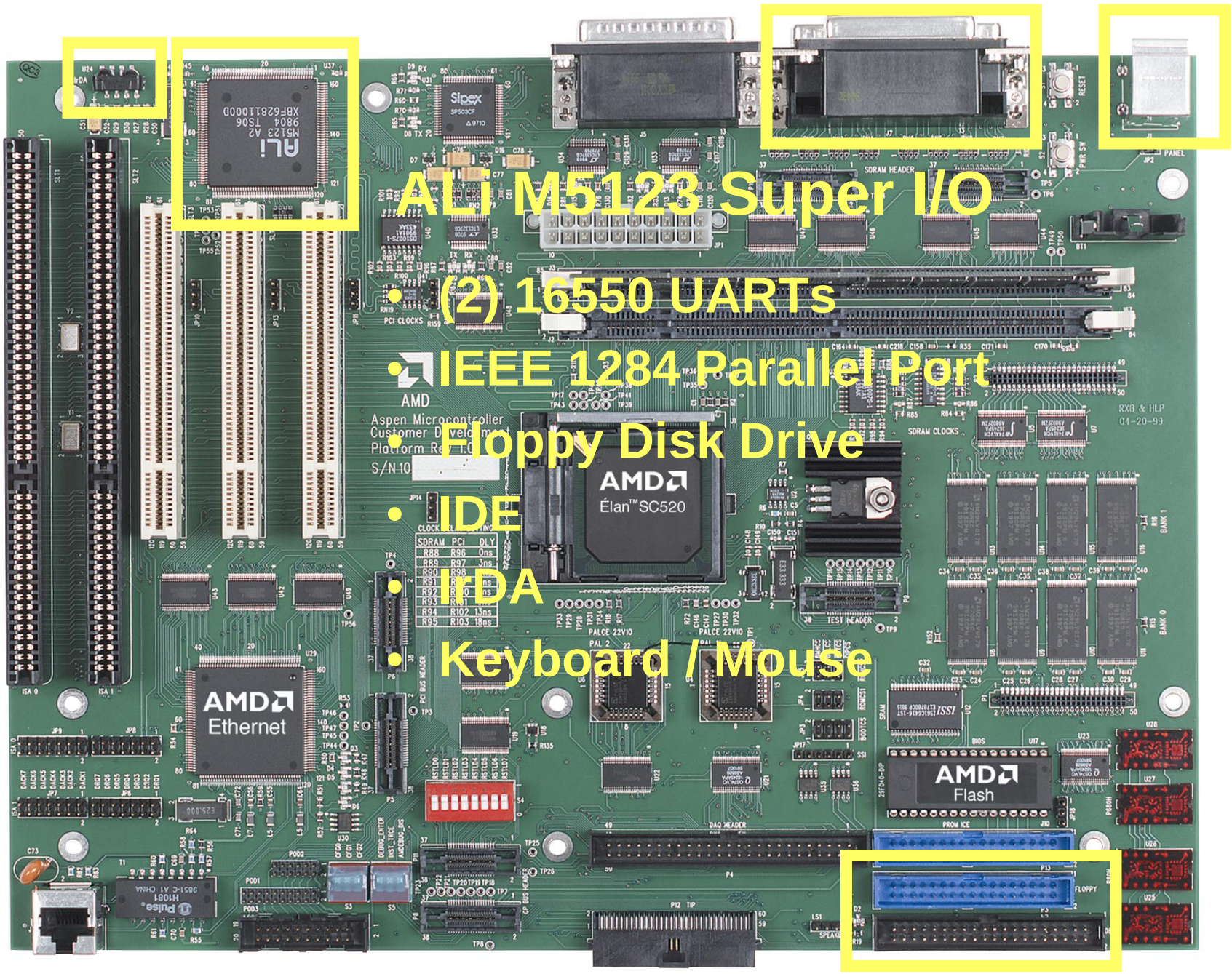


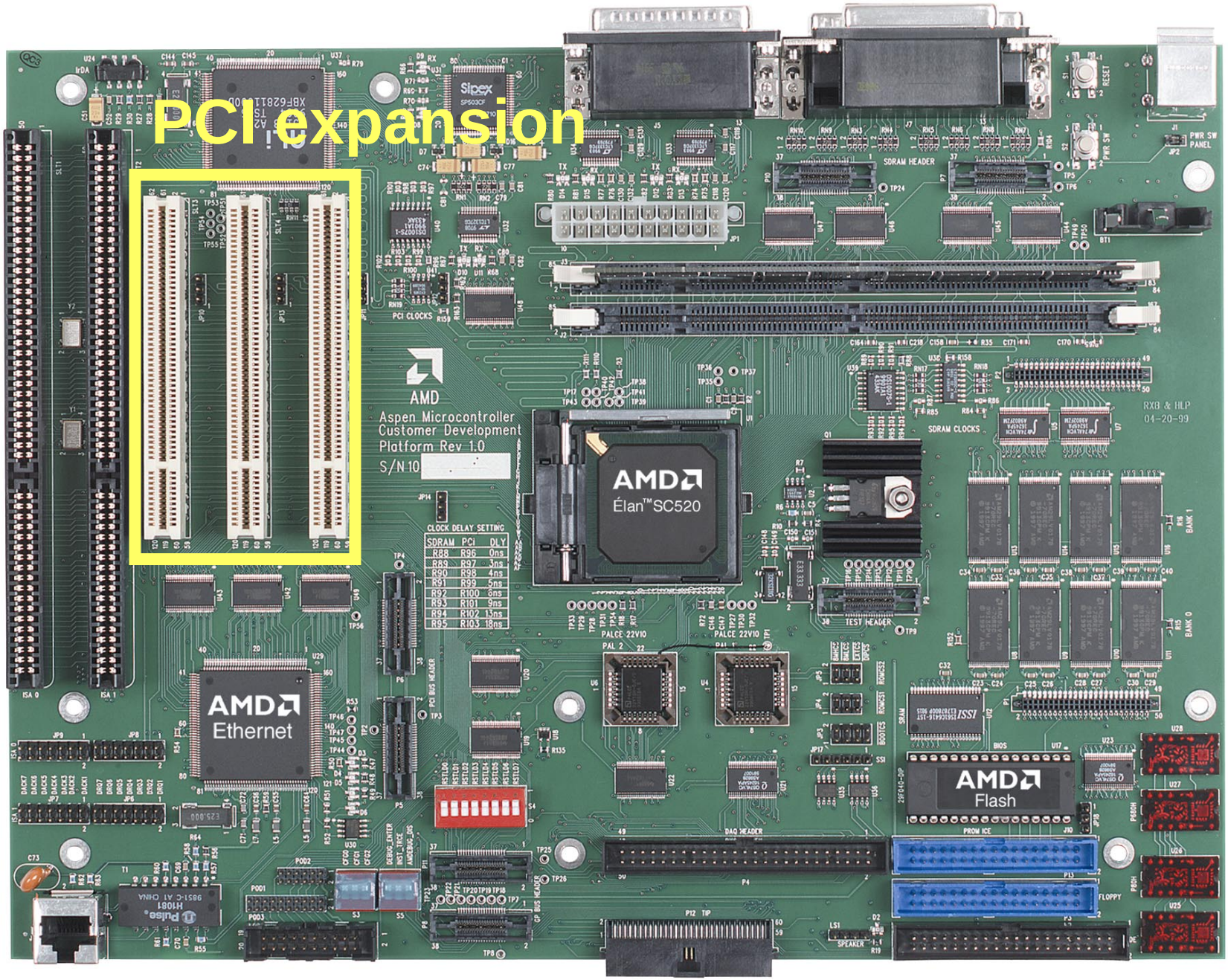
AMD

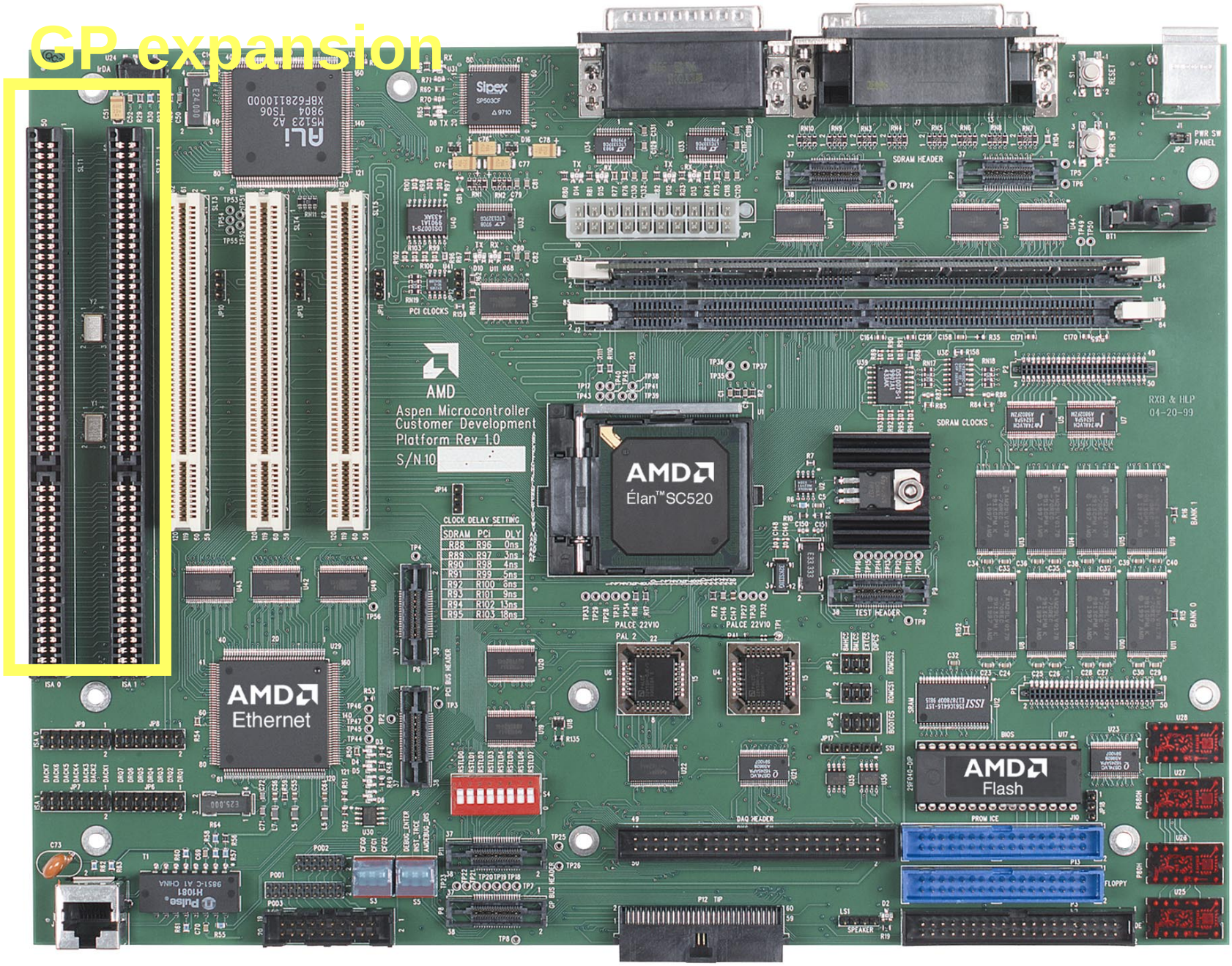

PC ATX form factor
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 8ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns

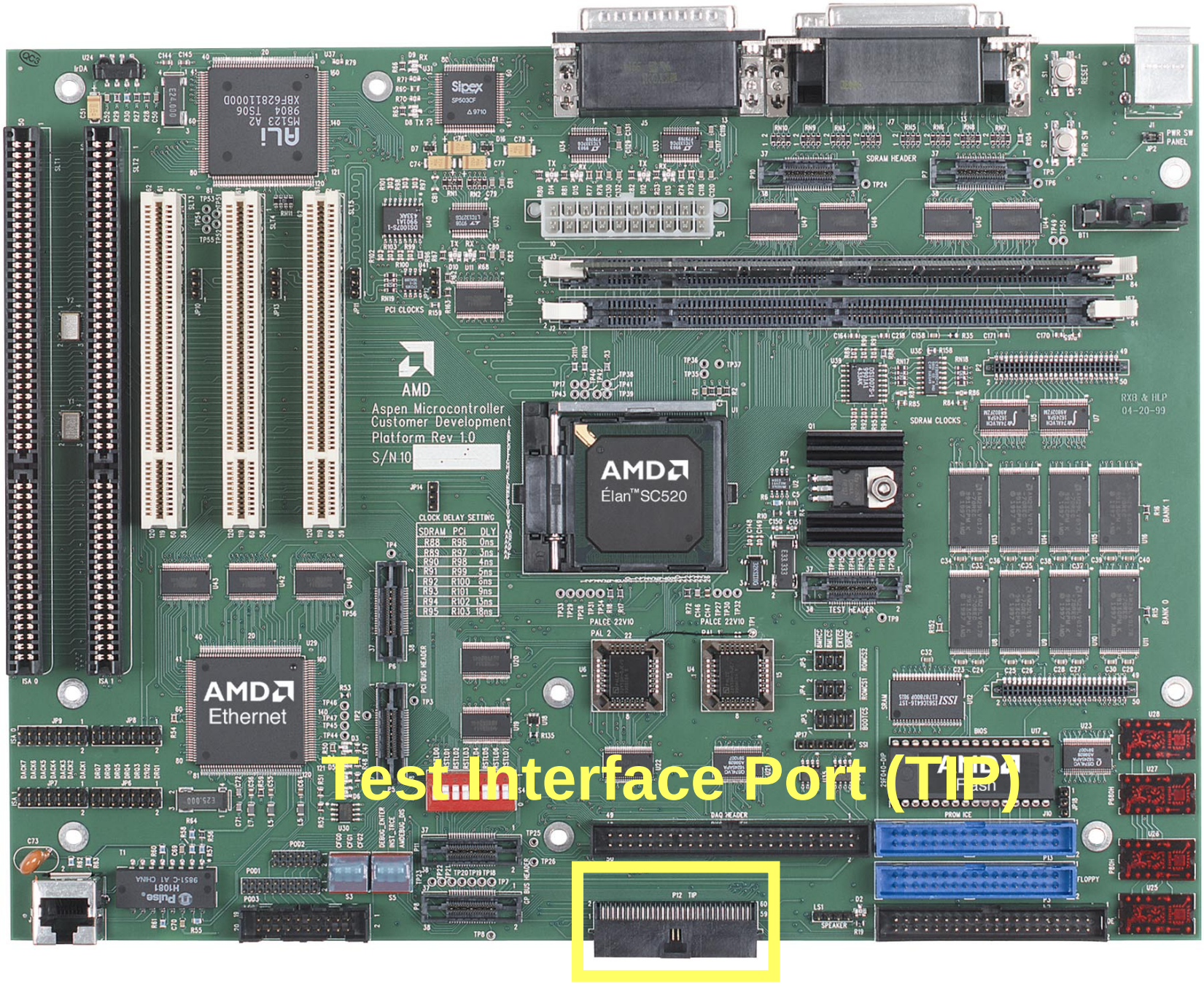

Élan™ SC520
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
AMD
Aspen Microcontroller
Customer Developme
Platform Rev 1.0
S/N 10
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
PWR SW PANEL
TEST HEADER
DAQ HEADER
FLOPPY
PROM ICE
SPEAKER
PALCE 22V10
RXB & HLP
04-20-99

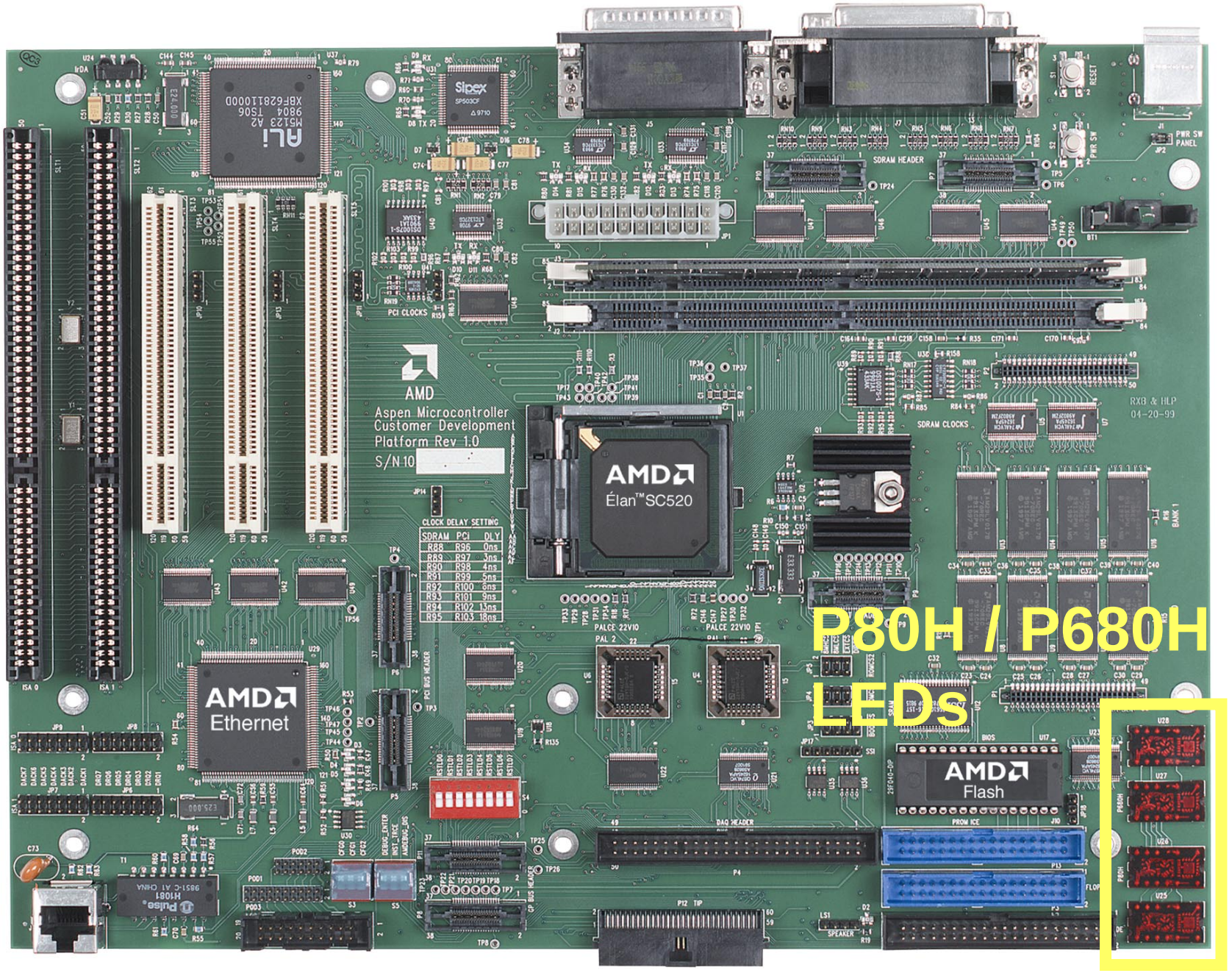

AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
PCnetFAST III 10/100 enet

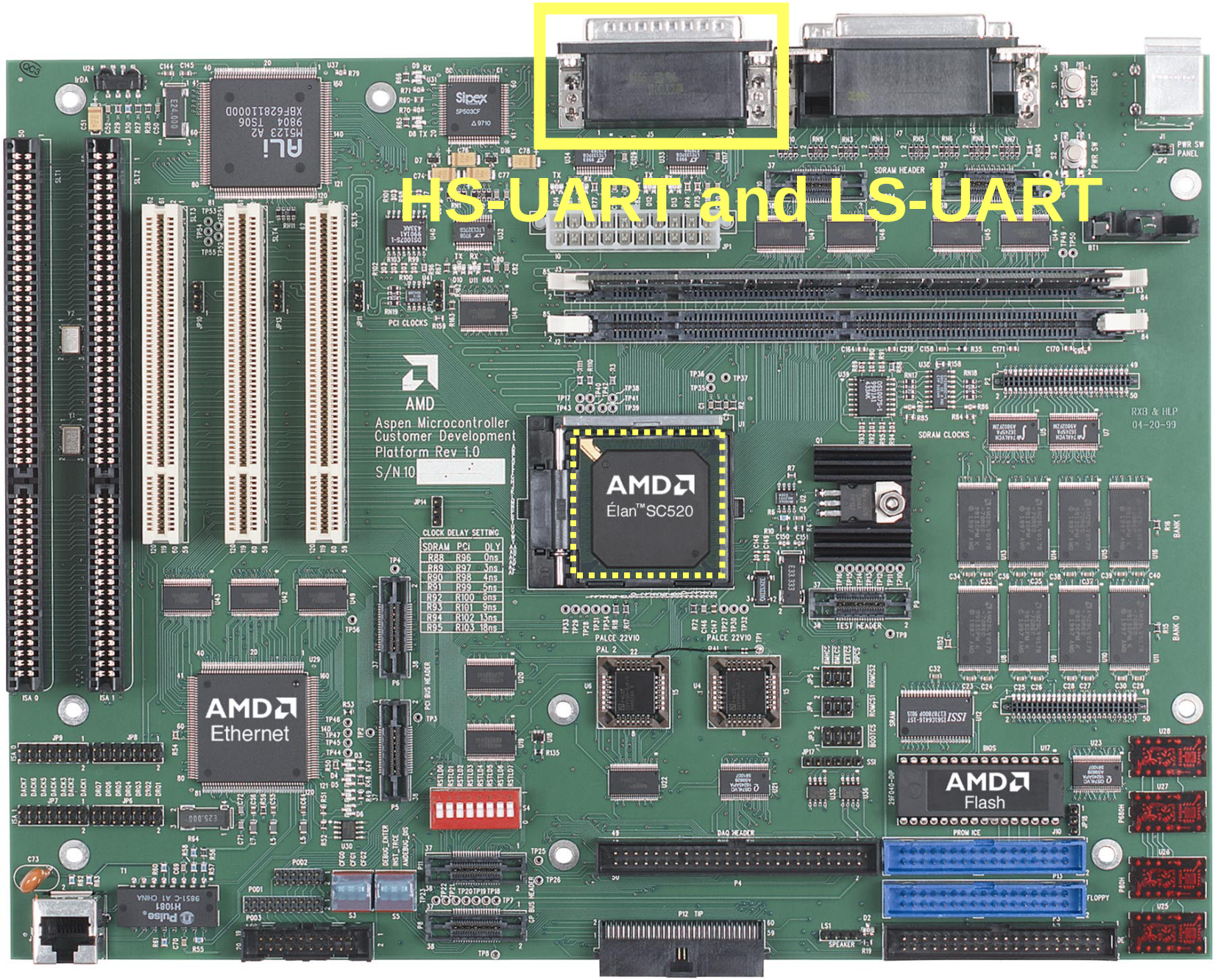

ALi M5123 Super I/O
• (2) 16550 UARTs
• IEEE 1284 Parallel Port
• Floppy Disk Drive
• IDE
• IrDA
• Keyboard / Mouse

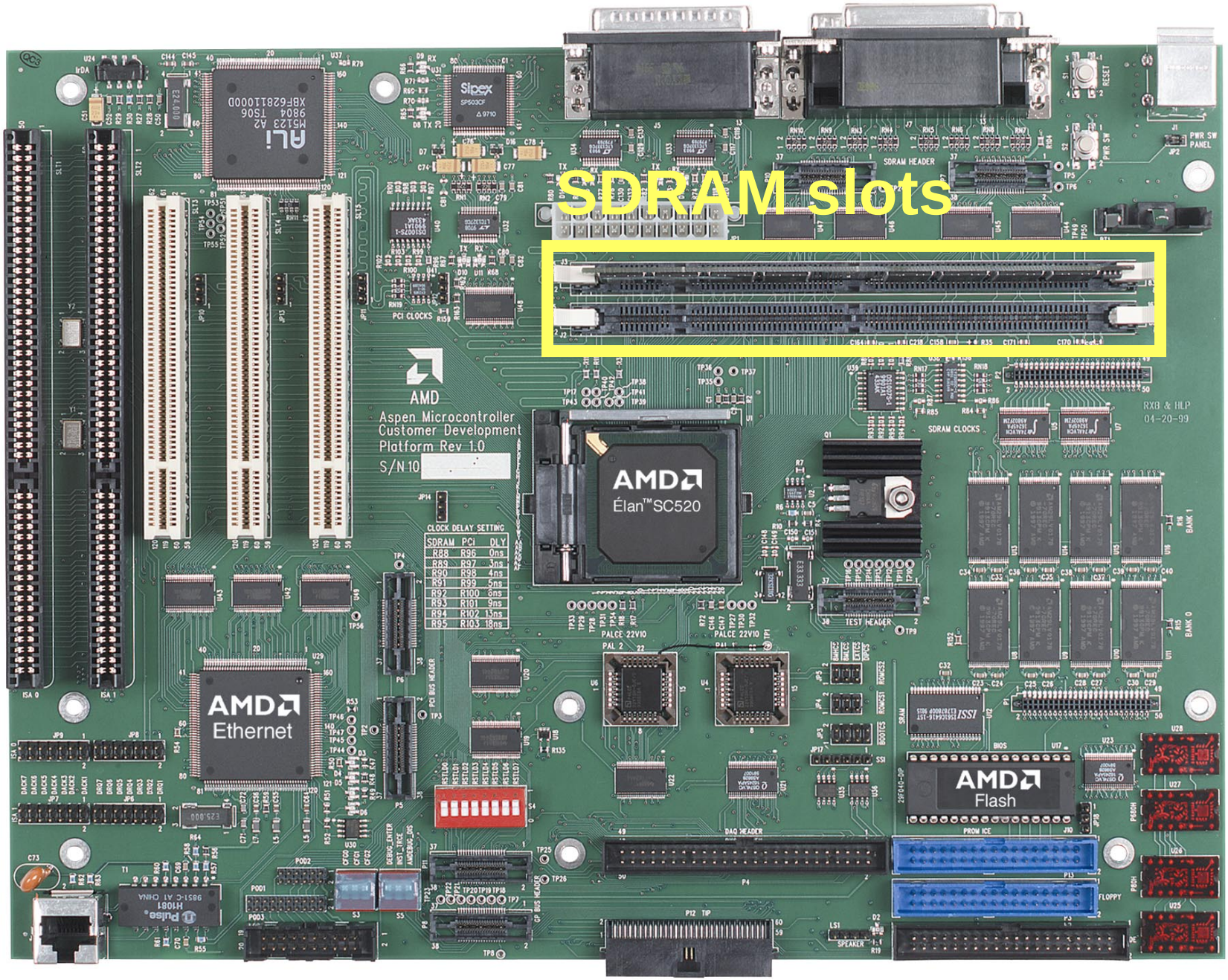

PCI expansion
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
PALCE 22V10
PAL 2
TEST HEADER
DAQ HEADER
PROM ICE
FLOPPY
SPEAKER
PWR SW PANEL
RESET
BANK 0
BANK 1
ISA 0
ISA 1
RXB & HLP
04-20-99

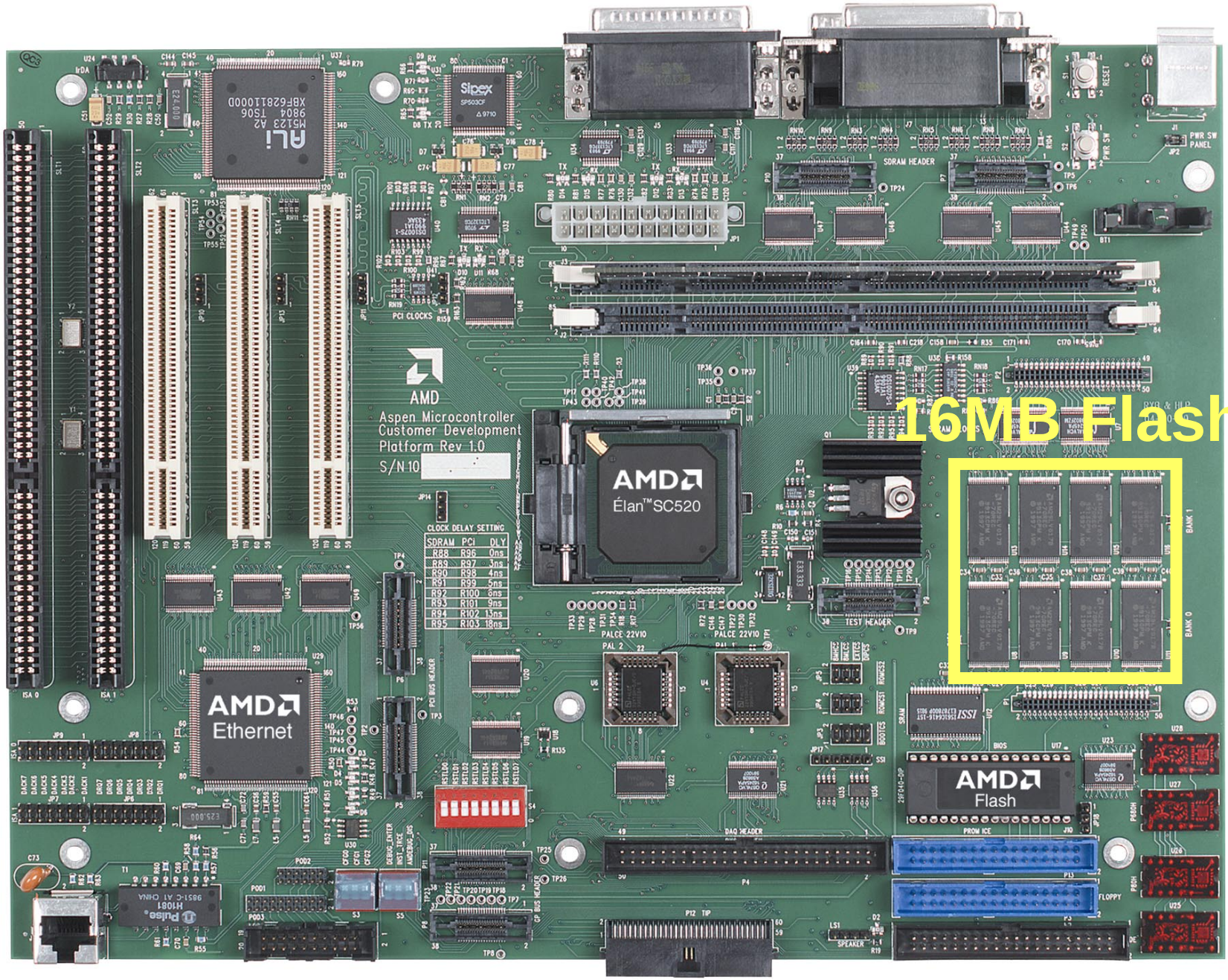

GP expansion
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns

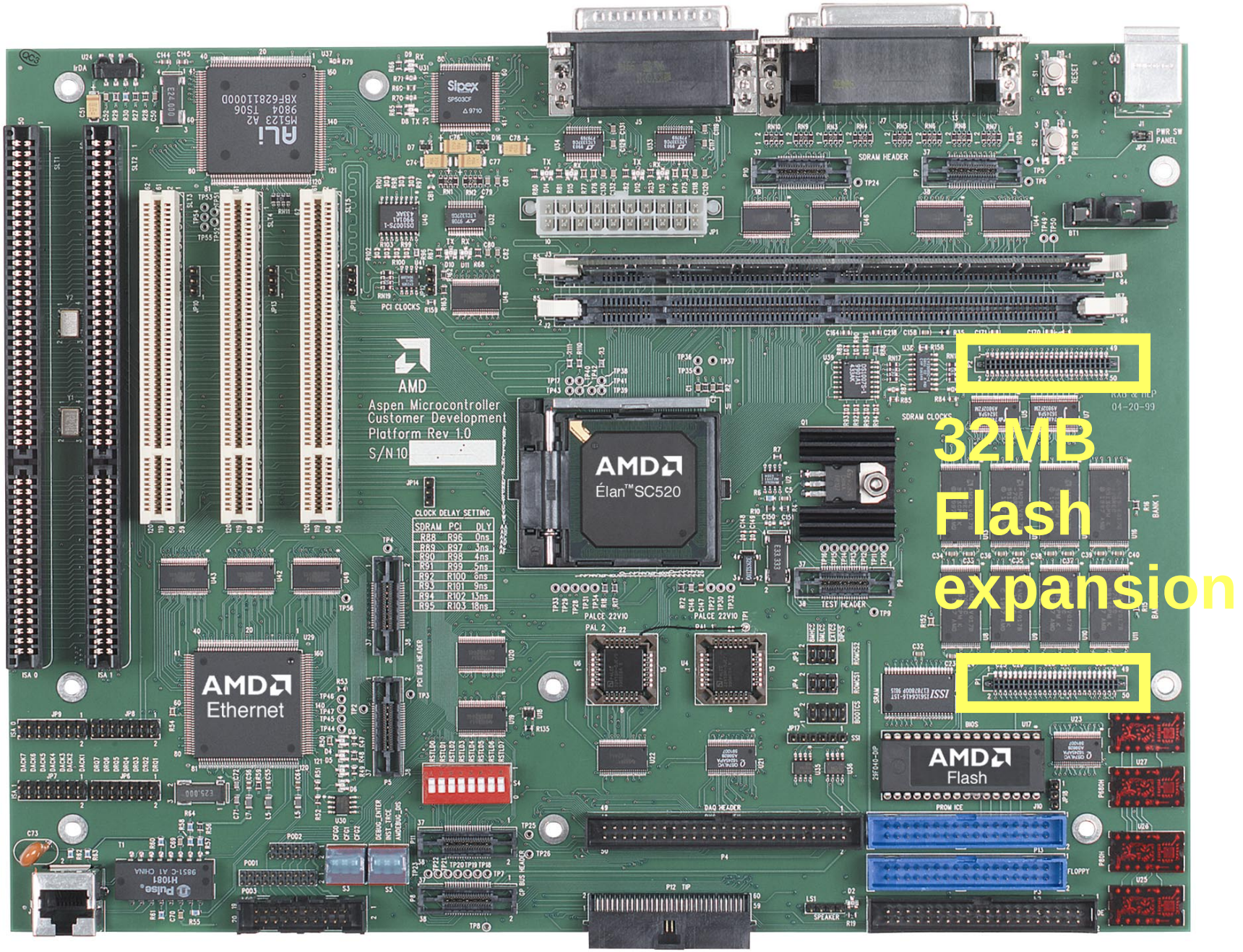

AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
Test Interface Port (TIP)

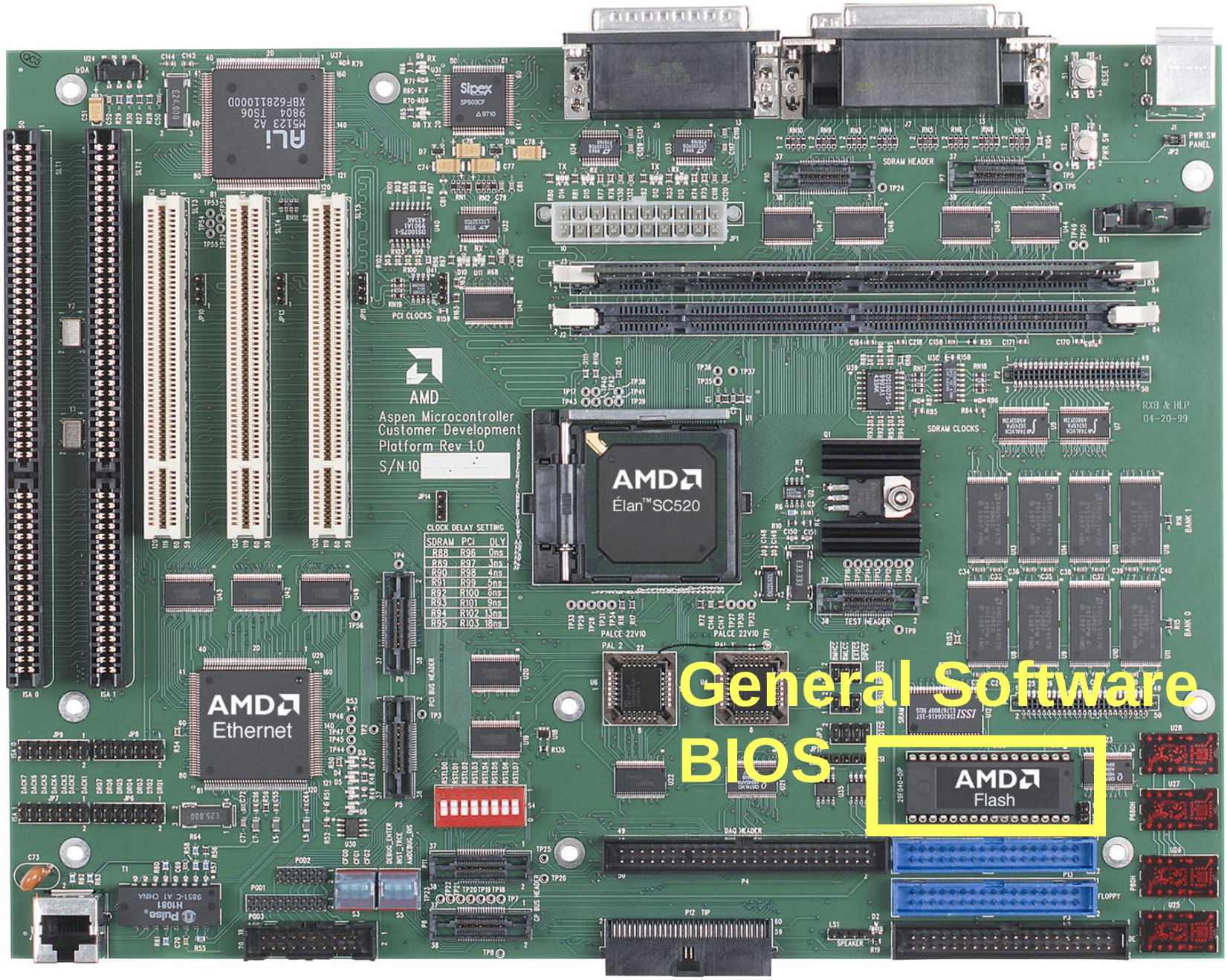

AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
P80H / P680H
LEDs

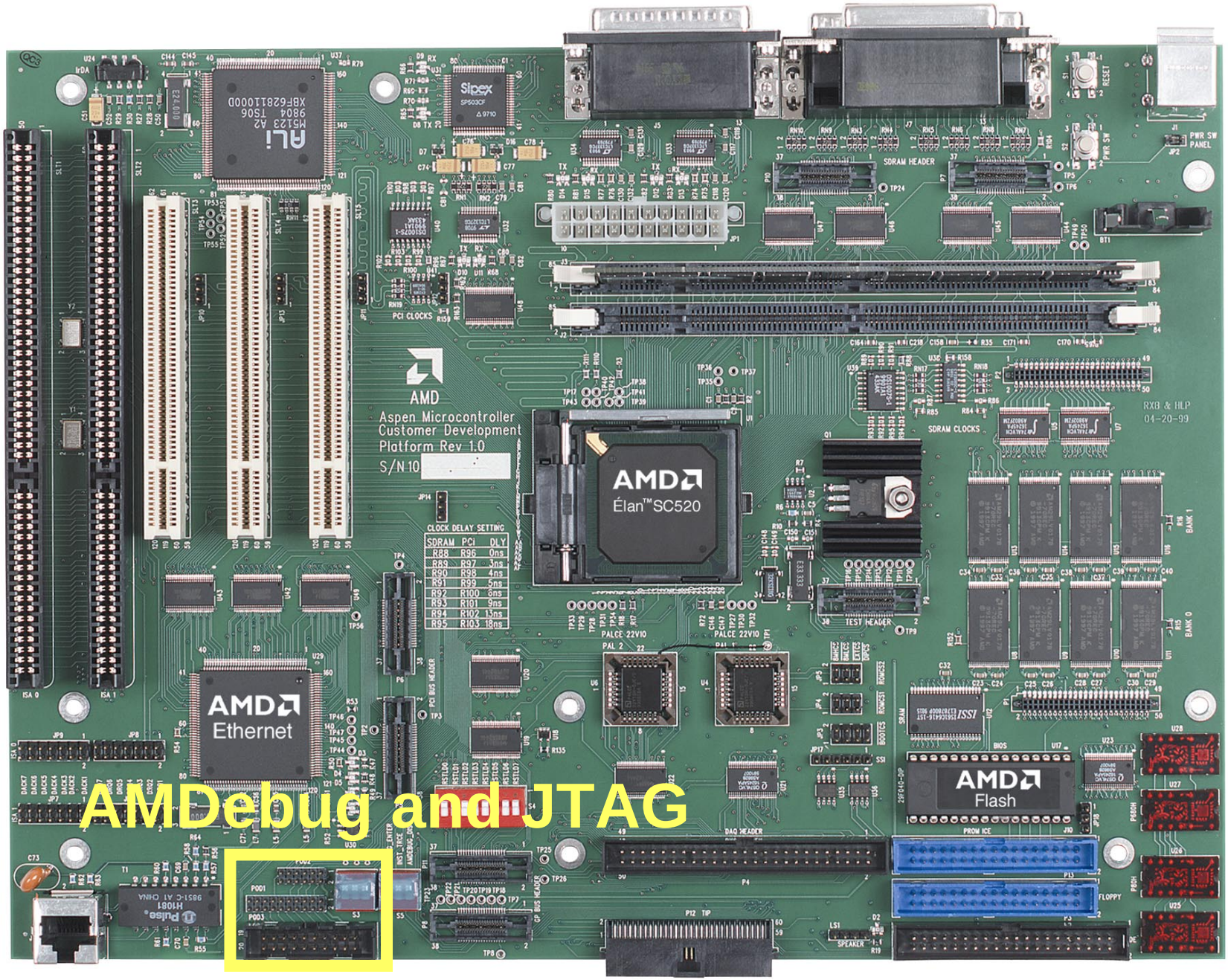

HS-UART and LS-UART
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
PALCE 22V10
PAL 2
TEST HEADER
DAQ HEADER
PROM ICE
FLOPPY
SPEAKER
PWR SW PANEL
RESET
BIOS
SRAM
BANK 0
BANK 1
ISA 0
ISA 1
PCI BUS HEADER
RXB & HLP
04-20-99

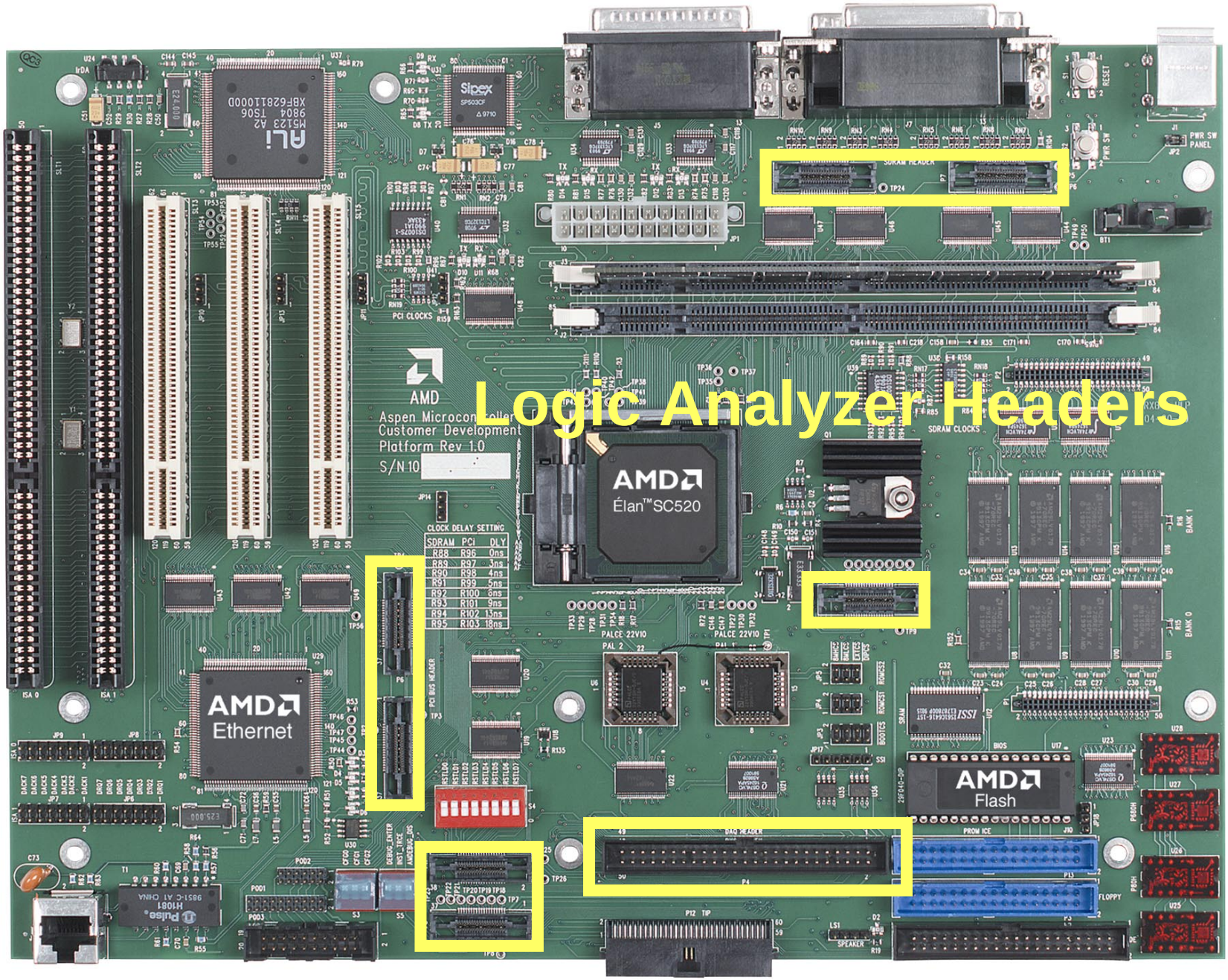

SDRAM slots
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
PALCE 22V10
PAL 2
TEST HEADER
DAQ HEADER
PROM ICE
FLOPPY
SPEAKER
PWR SW PANEL
RESET
BANK 0
BANK 1
BIOS
SRAM
ISA 0
ISA 1
RXB & HLP
04-20-99

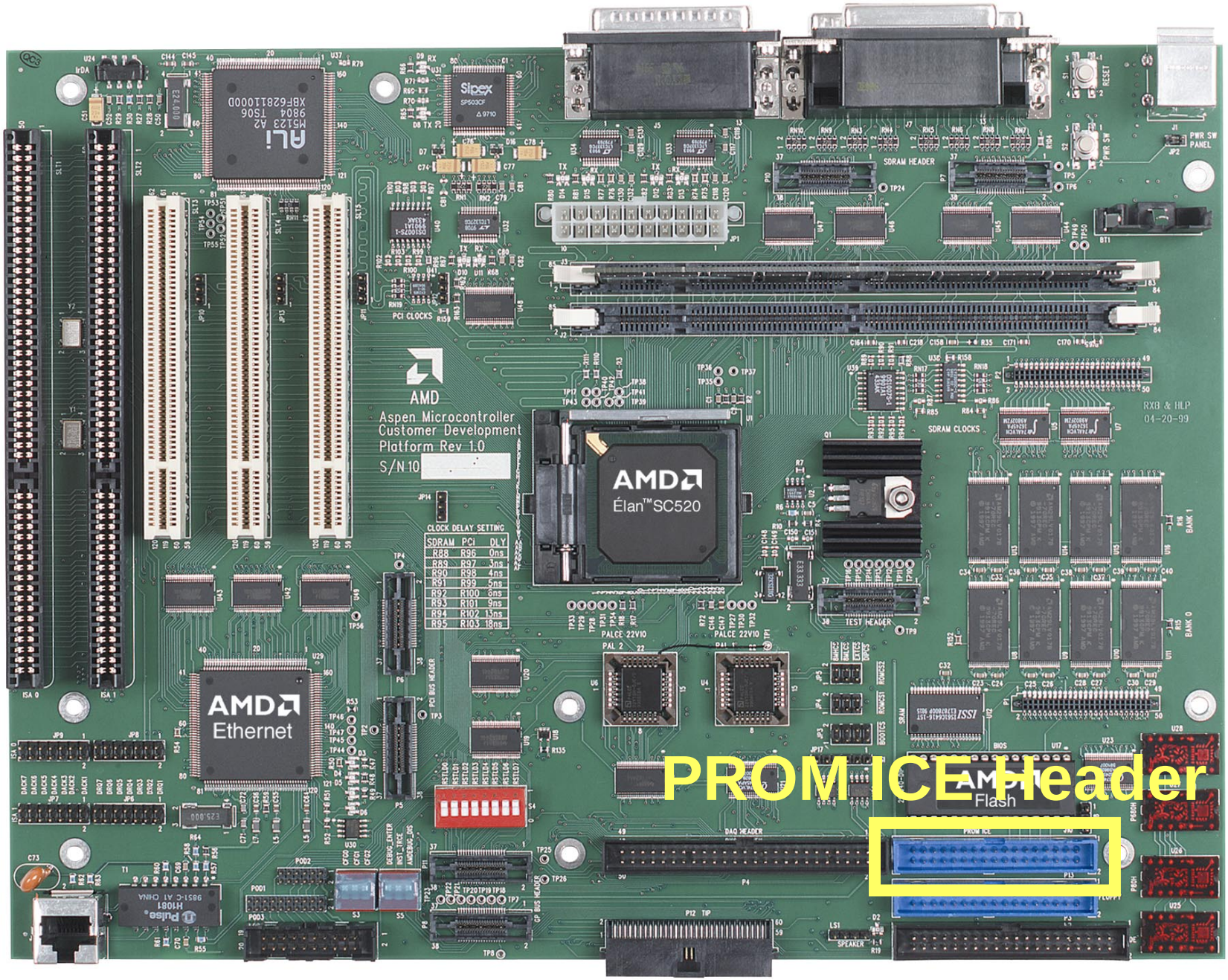

16MB Flash
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns


AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
32MB
Flash
expansion


AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
General Software
BIOS


AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N:10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
AMDebug and JTAG


Logic Analyzer Headers
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns


PROM ICE Header
AMD
Aspen Microcontroller
Customer Development
Platform Rev 1.0
S/N 10
AMD
Élan™SC520
AMD
Ethernet
AMD
Flash
SDRAM HEADER
SDRAM CLOCKS
PCI CLOCKS
CLOCK DELAY SETTING
SDRAM PCI DLY
R88 R96 0ns
R89 R97 3ns
R90 R98 4ns
R91 R99 5ns
R92 R100 6ns
R93 R101 9ns
R94 R102 13ns
R95 R103 18ns
PALCE 22V10
PAL 2
TEST HEADER
DAQ HEADER
PROM ICE
SPEAKER
PWR SW PANEL
RESET
BANK 0
BANK 1
BIOS
ISA 0
ISA 1
RXB & HLP
04-20-99

Systems in Silicon™

AMD Élan™SC520 Microcontroller Software Support

Systems in Silicon™

Software Overview

- Embedded BIOS
- RTOS Support, All with Ethernet Support
- CAD-UL Development Tools
- AMDebug™ Remote Monitor Tool
- System Utilities
- CodeKit™ Software

Systems in Silicon™

BIOS

- BIOS from General Software
  - Ported by AMD and GS
  - Full ÉlanSC520 Support
  - Upgradeable
  - Support for Board and MFG Diags
  - Support for CE Boot Loader
  - Board Level Monitor and Debug Support

Systems in Silicon™

RTOS Support

- RTOS Support
  - pSOS
  - VxWorks
  - QNX
  - RTXC
  - Windows CE
- All ports are native, (do not require a BIOS
- All ports have PCI Ethernet drivers and working TCP/IP stacks

Systems in Silicon™

CAD-UL Development tools

- Superb Tool
  - Works great with AMDebug (working now!)
  - Full support for AMC ICE
  - Full support for Serial Debugging (monitor based)
  - Full support for Embedded Trace Cache
  - Also has 16-bit tools
  - Fully integrated with pSOS development tools

Systems in Silicon™

AMDebug Remote Monitor

- REMON, complete monitor over AMDebug
  - Runs under Win32 (95/98/NT/W2000)
  - Low level system debug tool
  - Does not require any SW on target system
  - Provides flash programming utilities
  - Fully Scriptable

Systems in Silicon™

System Utilities

- Flash Programming
  - Via DOS
  - Via AMDebug
- EEPROM Programming
- System Configuration
- Board Diagnostics

Systems in Silicon™

CodeKit™ Software

- All EPD software for ÉlanSC520 delivered as CodeKits on website http://www.amd.com
  - Utilities
    - Configuration template
    - Remote Monitor
  - Drivers
    - PCnetFAST Ethernet