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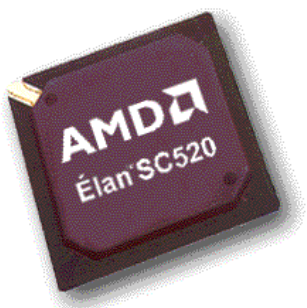
Converting Élan™SC400/410 Design to Élan™SC520



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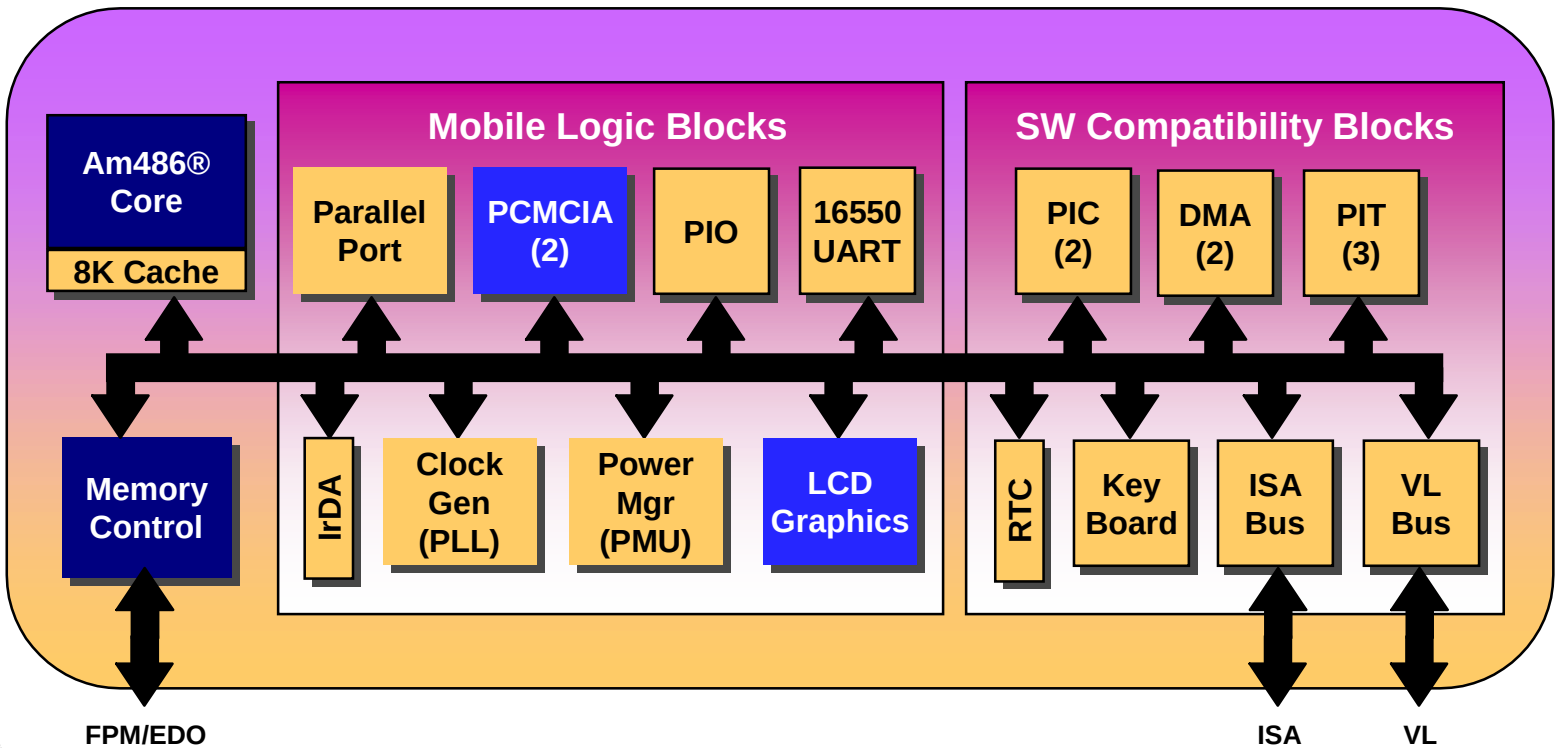
Élan™SC400/410 Block Diagram



Not featured in the ÉlanSC410

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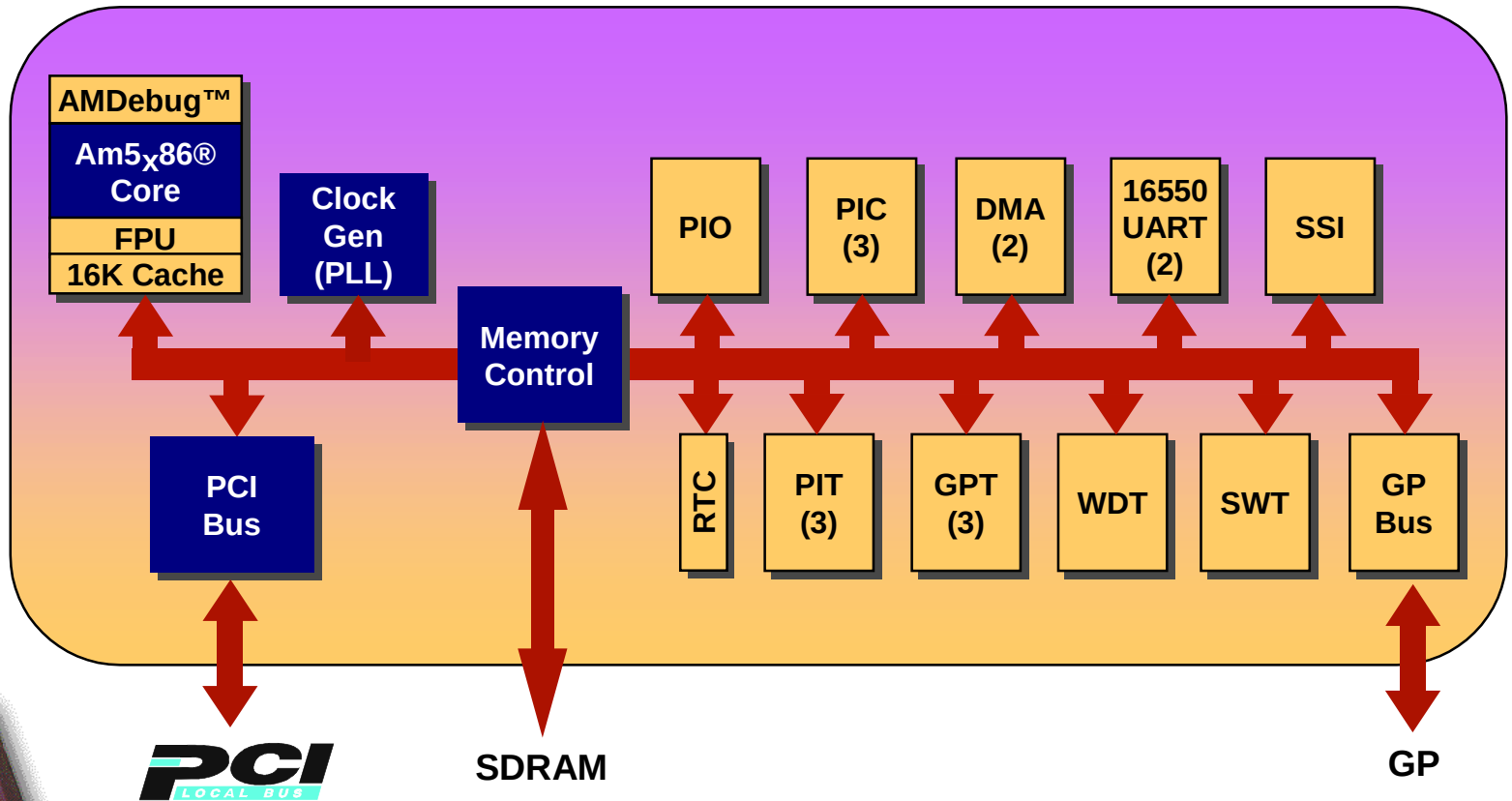
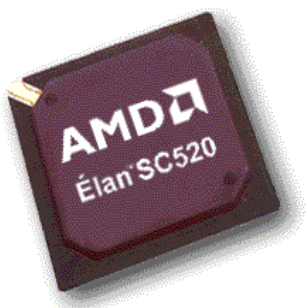
Élan™SC520 Microcontroller Block Diagram





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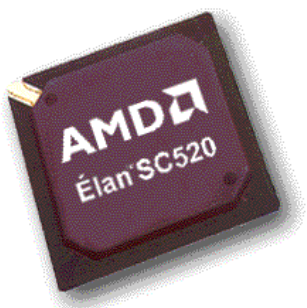
Advantage of SC520 over SC400



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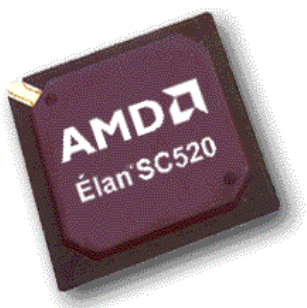
CPU Performance

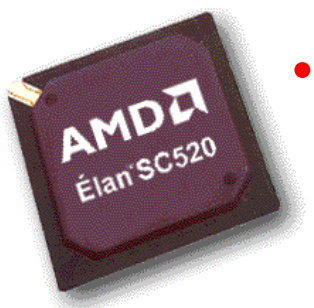
- Higher CPU clock speed of SC520
  - 133 MHz vs. 100 MHz
- Larger L1 cache size of SC520
  - 16 Kbyte vs. 8 Kbyte
- Floating point unit implemented in SC520, not in SC400

- SC520 has a higher performance CPU core than SC400!



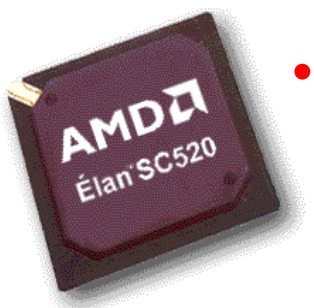
DRAM

- SC520 supports SDRAM
- SC400 supports FPM and EDO DRAM
- Performance
  - Page hit: 3-1-1-1 (66MHz) of SC520 vs. 4-2-2-2 (66MHz) of SC400
  - Read ahead buffer and write buffer (in SDRAM controller of 520) improve DRAM performance
  - SC520 supports ECC, SC400 doesn't
- Cost
  - SDRAM is more widely available than FPM/EDO
  - SDRAM is cheaper than FPM/EDO
- SC520 has a higher performance, lower cost DRAM solution than SC400!



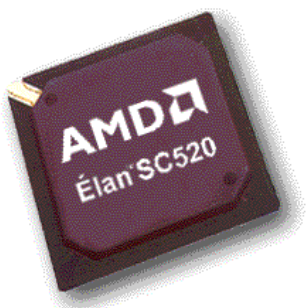
PCI vs. VESA

- SC520 supports 33 MHz, 32 bit PCI bus (2.2 compliant)
- SC400 supports 33 MHz, 32 bit VL-bus
- Peripheral availability
  - PCI bus has become the industrial standard while VL bus is obsolete
  - Peripheral chips with PCI interface is widely available
- Bus Mastering
  - VL-bus mastering is not supported on SC400
  - PCI bus controller of SC520 supports (up to 5) external bus masters
- SC520 systems can leverage much more standard peripheral chips than SC400



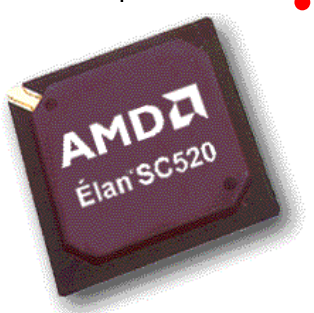
GP-Bus vs. ISA Bus

- SC520 has a general-purpose bus (GP bus) controller
- SC400 has an ISA bus controller
- Common
  - Both support 8 and 16 bit memory and I/O cycles
  - Both support dynamic bus sizing
  - Both support dynamic wait state for external devices
  - Neither supports bus mastering



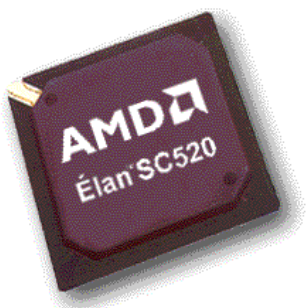
GP-Bus vs. ISA Bus (Continued)

- GP bus of SC520
  - 33.33 MHz maximum clock
  - 90 ns minimum bus cycle
  - Programmable bus interface timing
- ISA bus of SC400
  - 8.2944 MHz maximum clock
  - 362 ns minimum 16-bit bus cycle
    - 0-wait-state 16-bit memory bus cycle not supported on SC400
  - 723 ns minimum 8-bit bus cycle
- The GP-Bus of SC520 is faster and more flexible to accommodate various peripheral chips with ISA or general bus interface



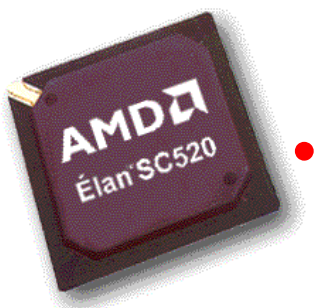
PC/AT Peripherals

- Both SC520 and SC400 provide PC/AT compatible peripherals
- SC520 provides enhancements to each PC/AT core
  - PIC: More sources, Flexible routing, Pin configuration options
  - DMAC: More channels available for external devices, Larger pages and counts, Routing, Buffer chaining
  - UARTs: One more UART than SC400, Capable of using DMA, Faster baud rates
  - PIT: Clock input for DOS, Additional interrupt capabilities
  - RTC: NMI Enable bit has moved



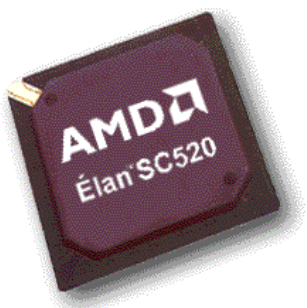
Additional Peripherals of SC520 – Useful for Embedded Applications

- Three general purpose 16-bit timers
  - Flexible cascading for 32-bit operation
  - Resolution: 4 clock periods @ 33MHz
- A software timer
  - Provides 1 us resolution
- A watchdog timer
- A synchronous serial interface (SSI)
  - Compatible with SCP, SPI and Microwire slave devices
- SC520 is more fitted for embedded applications



AmDebug Technology

- The AMDebug™ Technology built in SC520 offers a low-cost solution for the advanced debugging capabilities
  - Allows instruction tracing during execution from the Am5x86 CPU's internal cache
  - Uses an enhanced JTAG port for low-cost debugging
- SC520 systems are easier and cheaper to debug



Power Consumption

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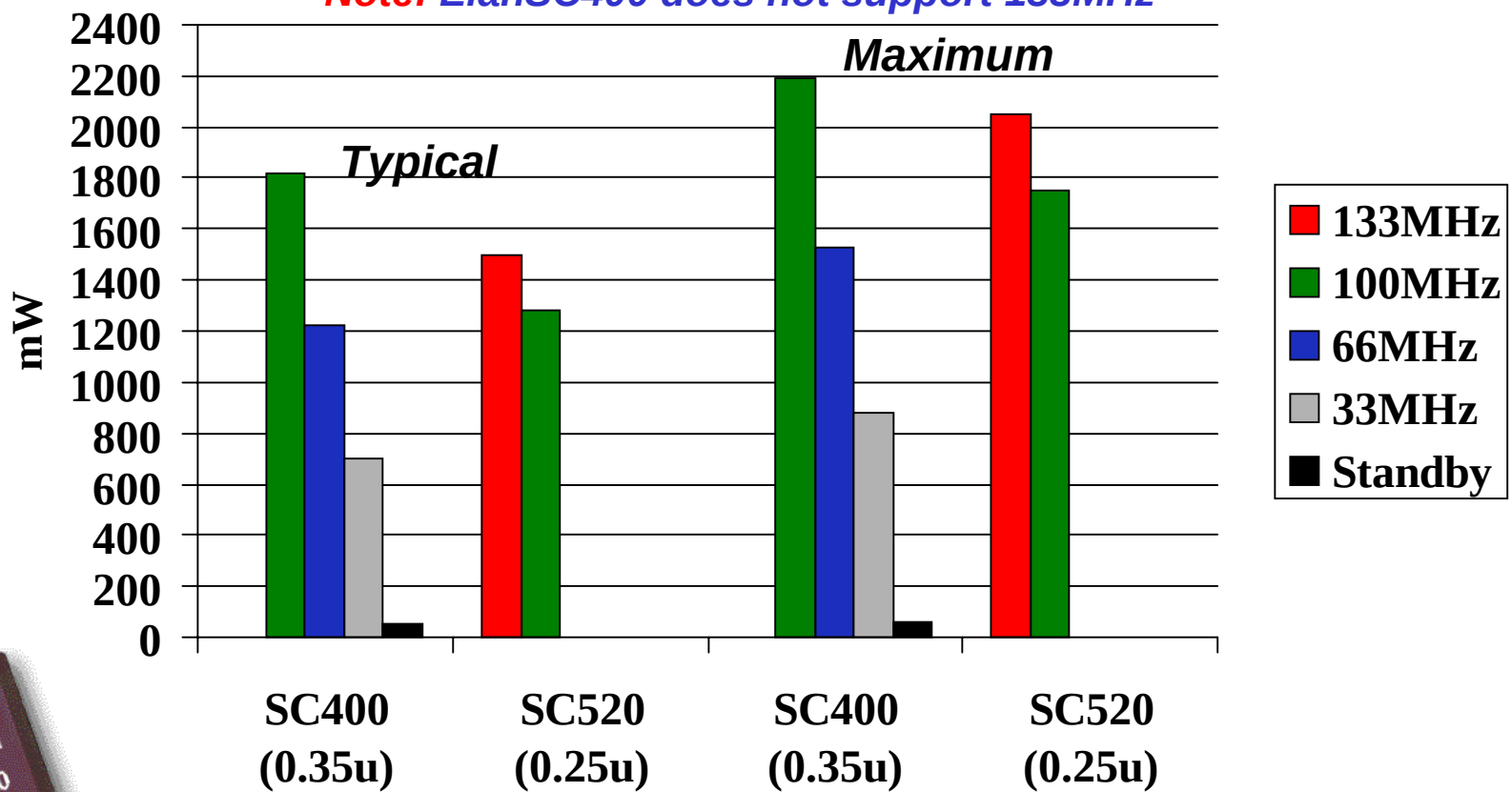
***Note:** ÉlanSC400 does not support 133MHz*



***Note:** ÉlanSC520 does not have PMU*

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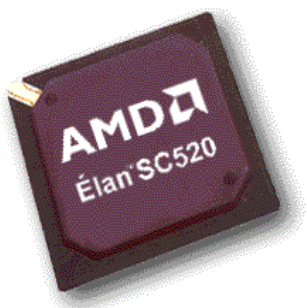
Disadvantage of SC520 to SC400



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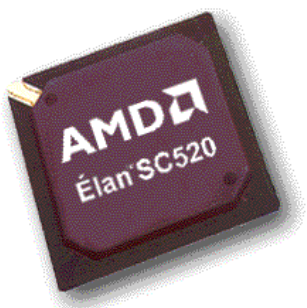
Power Management Unit (PMU)

- SC400/410 has a PMU
  - Seven modes of operation allow fine-tuning of power requirements for maximum battery life
  - Provides a superset of APM 1.2 features
- Solution for SC520 systems
  - SC520 is not designed for mobile applications
  - Some effort can be made to achieve some thermal control
    - Dynamic clock switching allows modification of CPU's core clock frequency under software control (from 133MHz to 100MHz)
    - Put CPU into Halt mode by executing HLT instruction
      - CPU will return to normal work mode upon receiving of interrupt
      - General Software is working on a new version of embedded BIOS including the implementation of this



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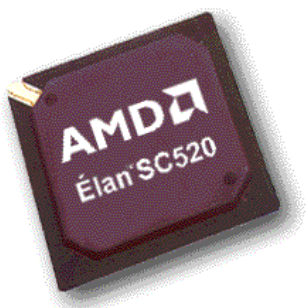
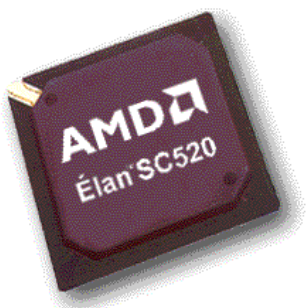
LCD Controller

- SC400 has a LCD controller (not available in SC410)
  - Unified memory architecture (UMA) allow sharing system DRAM
- Limitation
  - No VGA support
  - Not available when either 32-bit DRAM, 32-bit ROM, or the VL-bus is enabled
- Solution for SC520 systems
  - Use external LCD controller, though GP-bus or PCI bus



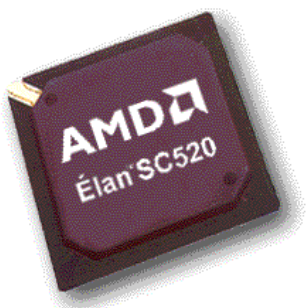
PCMCIA Controller

- SC400 integrated dual PC Card controller (not available in SC410)
- Limitation
  - The PC Card Socket B interface is shared with both the parallel port interface and some GPIO signals
  - The PC Card controller in SC400 is compliant with PCMCIA Standard Release 2.1
    - Do not support later PC Card Standards (1995, 1997),
    - Do not support 32-bit bus mastering interface (CardBus)
- Solution for SC520 systems
  - Use external PC Card (CardBus) controller, though PCI bus



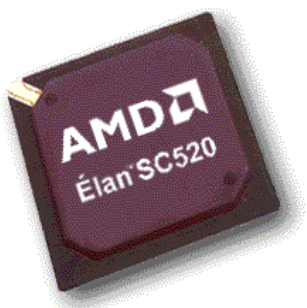
Infrared Port

- SC400/410 provide an infrared port
- Limitation
  - The UART can be used to drive either the standard 8-pin RS-232 interface or a 2-pin IrDA interface
  - IrDA and serial port cannot work simultaneously
- Solution for SC520 system:
  - Implement through external Super I/O chip or IrDA controller chip



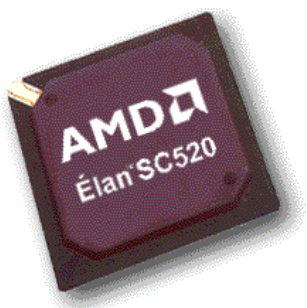
Keyboard Controller

- SC400/410 has a keyboard controller
  - Matrix keyboard support with up to 15 rows and 8 columns
  - Hardware support for software emulation of the System Control Processor (SCP) emulation logic
  - XT keyboard interface
- Limitation
  - Does not support AT keyboard
  - Matrix keyboard interface not available when either 32-bit DRAM, 32-bit ROM or the VL-bus is used
- Solution for SC520 system:
  - AT keyboard support implemented through external Super I/O chip or keyboard/mouse controller chip
  - A few keys can be interfaced with PIO



Parallel Port

- SC400/410 has a bi-directional parallel port
- Limitation
  - Pins shared with the second PC Card socket interface
- Solution for SC520 system:
  - Implement through external Super I/O chip
  - Emulate with PIO



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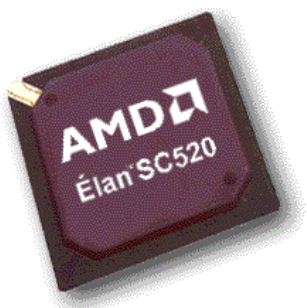
Super I/O & Keyboard/Mouse Controller Chips for ElanSC520



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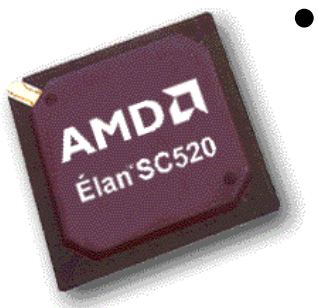
Super I/O Chips (ISA Interface)

- SMSC
  http://www.smsc.com/main/catalog/embioprod.html
- National Semiconductor
  http://www.national.com/parametric/0,1850,3085,00.html
  http://www.national.com/parametric/0,1850,3308,00.html
- ALi
  http://www.ali.com.tw
- ITE
  http://www.ite.com.tw
- Winbond
  http://www.winbond.com.tw



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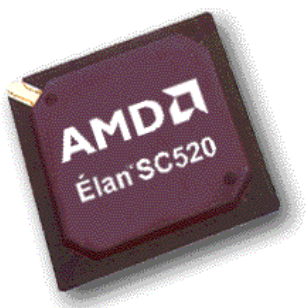
PC Card Controller Chips for ElanSC520



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PC Card Controllers

- Texas Instrument
  - PC Card (CardBus) Controllers, PCI interface

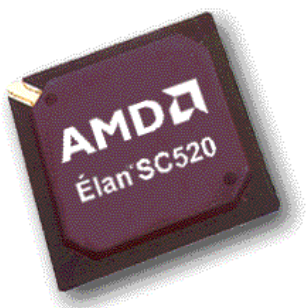
http://focus.ti.com/docs/browse/productnavigation.jhtml?familyId=381&tfsection=products&templateId=5

- Ricoh
  - PC Card (CardBus) Controllers, PCI interface

http://www.ricoh.co.jp/LSI/english/spec/assp/index.html

- O2Micro
  - PC Card (CardBus) Controllers, PCI interface

http://www.o2micro.com/products/prod_prodcard.html



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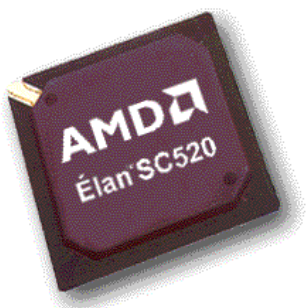
Graphic Controller Chips for ElanSC520



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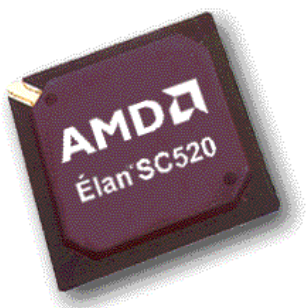
Graphic Controllers on GP-Bus

- EPSON LCD/CRT Controllers

http://www.erd.epson.com/vdc/html/products.htm

http://www.eea.epson.com/products/displayCategory?categoryId=EEA.IC.ASSP.Display_IC.LCD_Controllers

  - Easily interface to the GP-Bus of SC520
  - With or without embedded SRAM/SDRAM
  - Some has integrated USB slave controller



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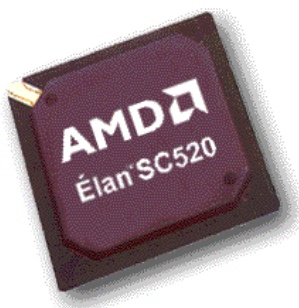
EPSON LCD/CRT Controllers

Part Number (Previous Part No.)	CPU Interface	Maximum Display Area	Display Memory	Target LCD Panels
S1D13305 (SED1335)	8-bit general bus	640 x 256 (black/white)	Max. 64 Kbyte SRAM	STN
S1D13503 (SED1353)	ISA	640 x 200 (256 Color)	Max. 128 Kbyte SRAM	STN (4/8/16 bits)
S1D13704 (SED1374)	ISA	240 x 160 (256 Color)	40 Kbyte Built-in SRAM	STN, TFT, D-TFD
S1D13705 (SED1375)	ISA	320 x 240 (256 Color)	80 Kbyte Built-in SRAM	STN, TFT, D-TFD
S1D13706 (SED1376)	ISA	160 x 240 (64K Color)	80 Kbyte Built-in SRAM	STN, TFT, D-TFD, HR-TFT
S1D13504 (SED1354)	ISA	800 x 600 (64K Color)	Max. 2 Mbyte DRAM (FPM/EDO)	STN (4/8/16 bits) TFT (16 bits), CRT
S1D13505 (SED1355)	ISA	800 x 600 (64K Color)	Max. 2 Mbyte DRAM (FPM/EDO)	STN (4/8/16 bits) TFT (16 bits), CRT
S1D13506 (SED1356)	ISA	800 x 600 (64K Color)	Max. 2 Mbyte DRAM (FPM/EDO)	STN, TFT, CRT, TV (NTSC, PAL)
S1D13806 (SED1386)	ISA	800 x 600 (64K Color) 1024 x 768 (256 Color)	1280 Kbyte Built-in SDRAM	STN, TFT, CRT, TV (NTSC, PAL)



Graphic Controllers on PCI Bus

- Tvia (former IGST)
  - Multimedia processors for STB, Internet Appliances, DTV, etc.
  - CyperPro families: 2010/50xx/53xx

    http://www.tvia.com/products/index.htm
- Silicon Motion
  - Low power 2D/3D graphic engine with embedded DRAM and multi-display support
  - Lynx family:

    http://www.siliconmotion.com/home.htm