ÉlanSC400 Microcontroller Evaluation Board User's Manual

Release 2.0

ADVANCED MICRO DEVICES

Élan™SC400 Microcontroller Evaluation Board User's Manual, Release 2.0

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About the Élan™SC400 Microcontroller Evaluation Board

Congratulations on your decision to design with the Élan™SC400 microcontroller. The ÉlanSC400 microcontroller for mobile computing applications utilizes the AMD *Systems in Silicon™* design philosophy—combining the industry-proven Am486® CPU core with a comprehensive set of peripherals in an advanced 0.35 micron process.

The ÉlanSC400 microcontroller evaluation board has been provided as a test and development platform for ÉlanSC400 microcontroller-based designs. Most of the microcontroller's features and options can be exercised on this board. Because there are numerous options and debug features available, this board is a much larger form factor than could be achieved with a dedicated set of features. This evaluation board can be used to experiment with design trade-offs, make power measurements, and develop firmware or software for the ÉlanSC400 microcontroller.

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Note: *Advanced Micro Devices does not assume any responsibility for the maintenance of this evaluation tool. Changes to the schematics will only be made if the board is required to go back through a CAD layout.*

Refer to the ÉlanSC400 Microcontroller documentation (listed on page xvi) for detailed information on the ÉlanSC400 microcontroller.

Overview of Features

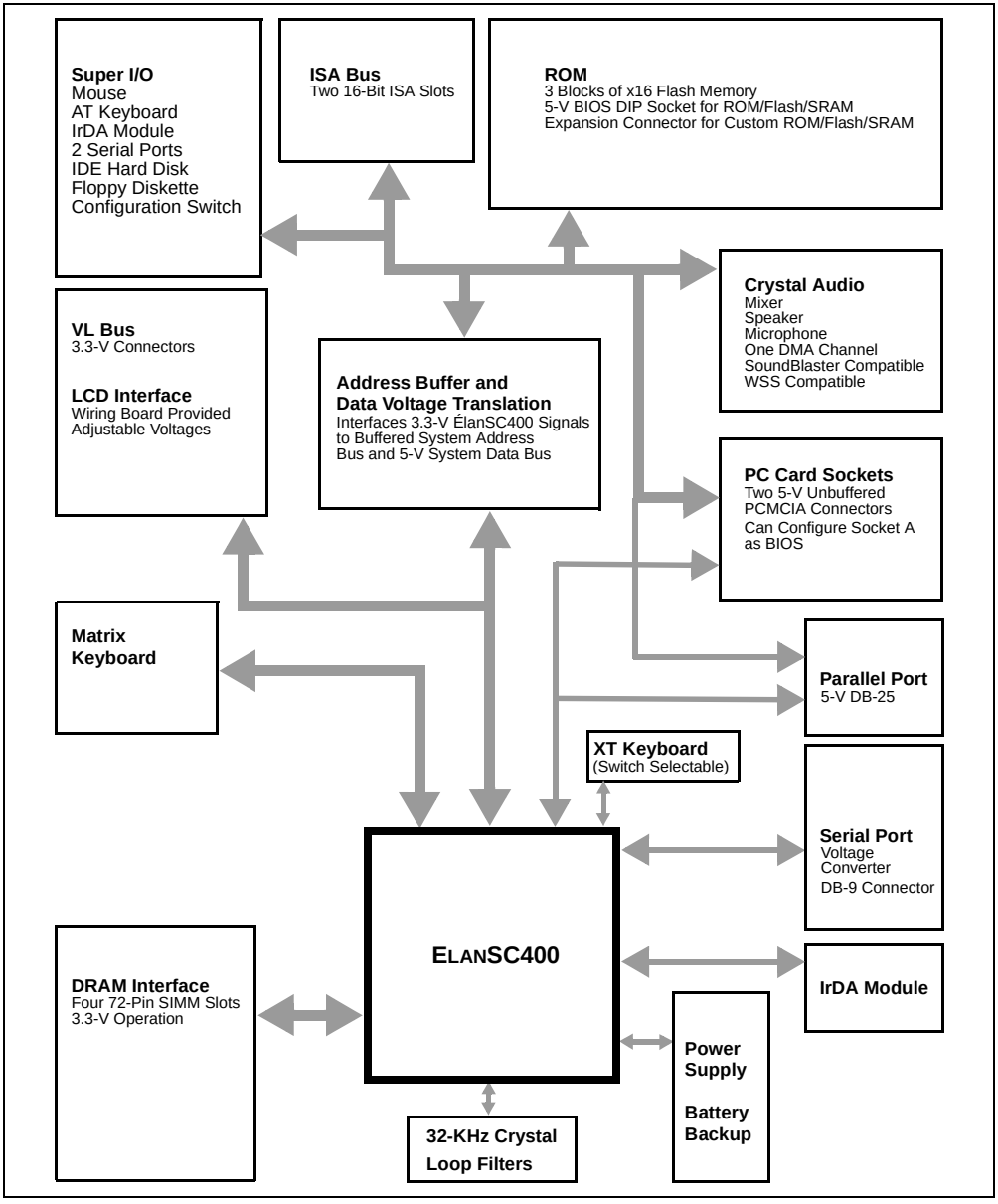

Figure 0-1. ÉlanSC400 Microcontroller Evaluation Board Overview

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Evaluation Board Features

This section describes the following features of the ÉlanSC400 microcontroller evaluation board:

- ÉlanSC400 Microcontroller
- DRAM
- Super I/O
- Bus Support
- PC Card
- Audio Support
- Power Management
- ROM
- Debugging

ÉlanSC400 Microcontroller

- Serial port connections:
  - One internal 16550-compatible port routed to a 9-pin D-shell connector.
  - One IrDA device for infrared serial communication (115 Kbps standard mode and 1.152 Mbps synchronous modes supported) routed to an IrDA transceiver.
- One parallel port connection from the ÉlanSC400 microcontroller (PC/AT, bidirectional, and EPP modes supported) routed to a 25-pin D-shell connector.
- Two unbuffered PC card 2.1-compliant sockets (standard and enhanced modes available).
- Two ISA bus connectors (for testing and development with 5-V ISA cards).
- 15-row, 8-column matrix keyboard controller.
- One keyboard connector: AT/XT switchable. (The ÉlanSC400 microcontroller provides the XT keyboard interface; AT control is from the Super I/O chip.)
- One LCD connection. (Note: since there is no one standard LCD connector, a daughter card is provided. You will need to adapt the cable for your particular LCD display.)
- 32-bit VESA local bus interface.

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DRAM

Four standard 72-pin DRAM SIMM sockets are provided. The following DRAM features are supported by the ÉlanSC400 microcontroller:

- 1-Mbyte through 64-Mbyte DRAM configurations
- 3.3-V DRAM only
- Fast Page mode (FPM) and Extended Data Out (EDO) DRAM
- Interleaving of FPM DRAM in paired banks

Super I/O

- Serial port connections:
  - Two Super I/O 16550-compatible ports routed to 9-pin D-shell connectors.
  - One IrDA device for infrared serial communication (115 Kbps standard mode only) routed to an IrDA transceiver.
- One IDE hard-disk-drive connector.
- One floppy-disk-drive connector.
- One keyboard connector: AT/XT switchable (Super I/O provides AT keyboard control; the XT interface is on the ÉlanSC400 microcontroller).
- One PS/2-style mouse connector.

Bus Support

- Two standard 16-bit ISA bus slot connectors provided. (Note that the board does not provide all ISA bus IRQs or DMAs at one time. These are routed via board jumpers to programmable pins on the ÉlanSC400 microcontroller.)
- 32-bit VESA local bus interface provided. A custom daughter card can be developed to test VL-bus devices. An example VL-bus VGA Card is available from AMD. The evaluation board provides non-standard VL-bus connectors because the ÉlanSC400 microcontroller's VESA local bus is 3.3 V only and standard VESA local bus cards operate at 5 V.

PC Card

- Two unbuffered PC Card sockets are provided.
- Support for 5-V cards and 12-V V_{PP} available for programming Flash memory cards.

Audio Support

- Audio interface supports testing of SoundBlaster, SoundBlaster Pro, and Windows Sound System software.
- Built-in microphone and speaker.

Power Management

- A power supply provided on the evaluation board converts PC 12-V and 5-V inputs to the following supply voltages:
  - Digital voltages: 3.3 V, 5 V, and Core V_{CC} (2.7 to 3.6 V adjustable)
  - LCD contrast voltages: $+V_{EE}$ and $-V_{EE}$ (10 to 40 V adjustable)
  - Analog V_{CC} (3.3 V)
- Power planes are isolated and jumpers are provided to measure current consumption.
  - ÉlanSC400 power planes are: V_{CC}, V_{CCCPU}, V_{CCMEM}, V_{CCSYS}, V_{CCLCD}, V_{CCBUS}, V_{CCPCM}, V_{CCRTC3}, V_{CCSER}, and AV_{CC}.
  - System planes are: V_{CCROM5}, $V_{CCDRAM3}$, V_{CCISA5}, V_{CCSER3}, $V_{CCPCMB5}$, V_{PPPCMB}, $V_{CCPCMA5}$, and V_{PPPCMA}.

The ÉlanSC400 microcontroller has the following power management features:

- SMI/NMI support.
- Programmable timers allow customizing of power management.
- Seven power modes provide efficient use of system power. (Hyper Speed, High Speed, Low Speed, Standby, Temporary Low Speed, Suspend, and Critical Suspend modes allowed.)

For testing power management features, the evaluation board provides a Suspend/Resume button and a DIP switch to toggle battery-low and ACIN signals.

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ROM

- Three Flash memory/ROM chip selects are supported by the ÉlanSC400 microcontroller.
- One 32-pin DIP socket is provided to allow for one of the following ROM, Flash, or SRAM devices:
  - 128K x 8, 256K x 8, or 512K x 8 Flash memory or EPROM (AMD's 29F010, 29F040, 28F010, or 28F020 Flash memory and 27C010, 27C020, or 27C040 EPROM parts are recommended)
  - 512K x 8 SRAM
- 12-V programming voltage is not supported.
- Six 2M x 8 TSOP Flash memory chips are provided for ROM development. These are configured in three selectable blocks of 2M x 16.
- ROM daughter card interface connectors are provided for custom ROM configurations.

Debugging

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- Headers for all signals (except the 32 KHz and loop filter signals) on the ÉlanSC400 microcontroller accessed through connectors and HP analyzer connectors (used with HP 01650-63203 termination adaptor).
- Port 80h LED display for tracking BIOS progress.
- Supports DOS Soft ICE tools and ROM ICE tools.
- Support for standard x86 application debugging tools.

ÉlanSC400 Microcontroller Evaluation Board Documentation

The *Élan™SC400 Microcontroller Evaluation Board User's Manual* provides information on the design and function of the evaluation board. The software shipped with the board is described in the README files and BIOS manuals included on diskette with your kit.

The included online documentation is in text or Adobe Acrobat (PDF) format. The latest Acrobat Reader is available from Adobe's site on the World Wide Web (currently at **http://www.adobe.com**).

About This Manual

Chapter 1, "Quick Start" helps you quickly set up and start using the ÉlanSC400 microcontroller evaluation board.

Chapter 2, "Board Functional Description" contains descriptions of the basic sections of the evaluation board: layout, microcontroller, Super I/O, ROMs, DRAM, VESA local and ISA bus interfaces, IrDA interface, serial and parallel ports, PC card, keyboards, mouse, drives, power measurement, and power management.

Chapter 3, "Product Support" provides information on: reaching and using the AMD Corporate Applications technical support services, product information and literature available through AMD's World Wide Web and FTP sites, and support tools for the E86 family.

Appendix A, "Evaluation Board Default Settings" summarizes the jumper and switch settings for the ÉlanSC400 microcontroller evaluation board when it is shipped.

Appendix B, "Verified Peripherals" contains a list of peripherals that have been verified to work on the ÉlanSC400 microcontroller evaluation board.

Appendix C, "Board Layout Suggestions" offers suggestions to minimize noise and noise coupling.

Appendix D, "Bill of Materials and Schematics" shows the bill of materials for the evaluation board, and the actual CAD schematics used to build the board.

Suggested Reference Material

For information on ordering the below literature, see Chapter 3, “Product Support”.

- *Élan™SC400 and ÉlanSC410 Microcontrollers Data Sheet*
  Advanced Micro Devices, order #21028
- *Élan™SC400 and ÉlanSC410 Microcontrollers Register Set Reference Manual*
  Advanced Micro Devices, order #21032
- *Élan™SC400 and ÉlanSC410 Microcontroller User’s Manual*
  Advanced Micro Devices, order #21030
- *FusionE86℠ Catalog*
  Advanced Micro Devices, order #19255
- *FusionE86℠ CD-ROM*
  Advanced Micro Devices, order #21058
- For current application notes and technical bulletins, see our World Wide Web page at **http://www.amd.com**.

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Documentation Conventions

The Advanced Micro Devices *Élan™SC400 Microcontroller Evaluation Board User's Manual* uses the conventions shown in Table 0-1 (unless otherwise noted). These same conventions are used in all the E86 family support product manuals.

Table 0-1. Notational Conventions

Symbol	Usage
Boldface	Indicates that characters must be entered exactly as shown, except that the alphabetic case is only significant when indicated.
Italic	Indicates a descriptive term to be replaced with a user-specified term.
`Typewriter face`	Indicates computer text input or output in an example or listing.
[ ]	Encloses an optional argument. To include the information described within the brackets, type only the arguments, not the brackets themselves.
{ }	Encloses a required argument. To include the information described within the braces, type only the arguments, not the braces themselves.
..	Indicates an inclusive range.
...	Indicates that a term can be repeated.
|	Separates alternate choices in a list — only one of the choices can be entered.
:=	Indicates that the terms on either side of the sign are equivalent.

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Chapter 1

Quick Start

This chapter provides information that helps you quickly set up and start using the ÉlanSC400 microcontroller evaluation board.

The ÉlanSC400 microcontroller evaluation board is shipped with evaluation BIOS' from Phoenix and SystemSoft, which have been configured specifically for this board. See "ROM Space (B10–B12)" starting on page 2-15 to select which BIOS is used at power-up. The BIOS contains the code that enables the ÉlanSC400 microcontroller evaluation board to function just like a standard AT-compatible PC, using AT-compatible displays, display adapters, and keyboards. Details on the BIOS can be found in the BIOS manuals shipped on diskette with your kit.

The ÉlanSC400 microcontroller evaluation board can run AT-compatible operating system software. You can start the system with either a bootable diskette or an ATA (IDE) hard disk drive that already has the operating system installed.

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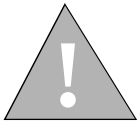
For information on how to:

- Set up the ÉlanSC400 microcontroller evaluation board, see page 1-2.
- Boot the ÉlanSC400 microcontroller evaluation board from a diskette, see page 1-6.
- Boot the ÉlanSC400 microcontroller evaluation board from a hard disk drive, see page 1-7.
- Troubleshoot installation problems, see page 1-8.

Setting Up the Evaluation Board



CAUTION: As with all computer equipment, the ÉlanSC400 microcontroller evaluation board may be damaged by electrostatic discharge (ESD). Please take proper ESD precautions when handling any board.

Warning: Read before using this evaluation board

Before applying power, the following precautions should be taken to avoid damage or misuse of the board:

- Make sure power supply connectors (from a standard AT system power supply) are plugged onto the board correctly. The grounds (usually black wires) *must* meet at the center of the two power supply connectors on the board. See "Power Supply and Measurement" on page 2-50.
- See "Board Block Diagram" on page 2-3 for connector positions.
- Check the diskette that was shipped with your kit for README or errata documentation. Read any such information carefully before continuing.

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For current application notes and technical bulletins, see the AMD World Wide Web page at **http://www.amd.com** and follow the link to Embedded Systems.

Installation Requirements

You need to provide the following items (in addition to the ÉlanSC400 microcontroller evaluation board from the kit). See Appendix B, “Verified Peripherals,” for a list of peripherals that are known to work with the ÉlanSC400 microcontroller evaluation board.

Required for all setups:

- A VGA monitor
- An ISA-bus VGA card
- A cable to connect the VGA monitor to the ISA-bus VGA card
- An AT-compatible keyboard
- A standard PC power supply

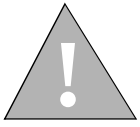
To boot from a floppy diskette:

- An AT-compatible 3.5" diskette drive
- A bootable 3.5" DOS diskette
- A standard 34-wire AT diskette drive cable

To boot from a hard disk drive:

- An ATA-compatible hard disk drive
- AT-compatible operating system (preinstalled on the hard disk drive)
- A standard 40-pin ATA HDD cable

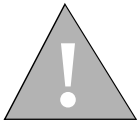
If you install both a floppy diskette drive and a hard disk drive, you can boot from either device. Only one boot image (floppy or hard disk) is required.



CAUTION: Use the configuration described here when you first start the ÉlanSC400 microcontroller evaluation board. Before using other features, read the appropriate sections in Chapter 2, “Board Functional Description.”

Board Installation

Note: *See Figure 2-2 on page 2-3 for a block diagram of the board. See Figure 2-3 on page 2-4 for the a layout diagram of the board, including connector locations referenced in this section.*



DANGER: Make sure the power supply and the VGA monitor are *not* plugged into an electrical outlet during the following steps.

1. Remove the board from the shipping carton. Visually inspect the board to verify that it was not damaged during shipment. The board contains several jumpers. The following steps assume all jumpers are in the factory default configuration (settings are listed in Appendix A, "Evaluation Board Default Settings").
2. If you are installing a diskette drive, perform the following steps:
   a. Inspect the 34-wire, diskette-drive cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1. Most cables have a connector for the board at one end and two or more connectors along the length. There may be two different drive connectors at each location to accomodate different drive types.
   b. Connect one end of the diskette-drive cable to the 34-pin connector at location P14 on the ÉlanSC400 microcontroller evaluation board (with wire 1 oriented towards the power supply module). If there is a twist in one span of the cable, connect the opposite end to the board.
   c. Connect another connector on the diskette-drive cable to the diskette drive, just as you would for a standard PC installation. If there is a twist in the cable, the position you use determines whether the drive responds as A or B (typically drive A connects to the end of the cable, beyond the twist). The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.
   d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the diskette drive just as you would for a standard PC installation.

3. If you are installing a hard disk drive, perform the following steps:

   a. Inspect the 40-wire IDE cable that you are providing. The red wire along one edge of the ribbon cable indicates wire 1.

   b. Connect one end of the 40-wire IDE cable to the hard drive just as you would for a standard PC installation. The connector's orientation should be indicated in the drive documentation, or marked near the connector on the drive. Usually wire 1 is oriented towards the drive's power cable connector.

   c. Connect the other end of the 40-wire IDE cable to the 40-pin connector P12 on the ÉlanSC400 microcontroller evaluation board (with wire 1 oriented towards the power supply module).

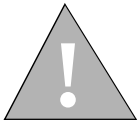
   d. Find one of the 4-wire power connectors from the PC power supply and attach it to the 4-pin connector on the hard drive just as you would for a standard PC installation.

4. Insert an ISA-bus VGA card into either of the ISA slots on the ÉlanSC400 microcontroller evaluation board. The ISA slots are labeled P33 and P34.

5. Connect the VGA monitor cable from the monitor to the D-connector on the ISA-bus VGA card just as you would for a standard PC.

6. Connect the keyboard to the keyboard connector at location P6.

7. Connect the connectors (usually marked P8 and P9) from the standard PC power supply into the board's power connectors at P1 and P2. P8 connects to P1 (the six pins closest to the corner of the board); P9 to the other six pins. *Make sure the black ground wires from P8 and P9 meet in the middle of the board's P1 and P2 connectors.*

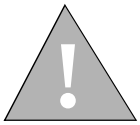


DANGER: Failure to verify the power supply connections will result in total destruction of the ÉlanSC400 microcontroller evaluation board.

Starting from Diskette

Use the following steps to start the ÉlanSC400 microcontroller evaluation board from a bootable diskette:

1. Make sure you have installed the evaluation board correctly as described in "Setting Up the Evaluation Board" on page 1-2.



DANGER: Failure to verify the power supply connections will result in total destruction of the ÉlanSC400 microcontroller evaluation board.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. Insert a bootable DOS diskette (not included) in the disk drive.
4. Apply power to the ÉlanSC400 microcontroller evaluation board by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on.

   The power supply fan should start running, and the port 80h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying BIOS messages.

5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system's date, time, startup drive, and other options.

   For more information on each included BIOS, see the corresponding BIOS manual. BIOS manuals are included in Adobe Acrobat format on the diskette shipped with your kit.

6. Save and exit the setup utility.
7. The system should now boot from the DOS diskette just like a standard PC. If you encounter any problems, see "Installation Troubleshooting" on page 1-8.

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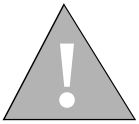
Starting from an IDE Hard Drive

Use the following steps to start up the ÉlanSC400 microcontroller evaluation board from an IDE hard drive on which you have preinstalled an operating system (while it was connected to another PC):

1. Make sure you have installed the evaluation board correctly as described in "Setting Up the Evaluation Board" on page 1-2.



DANGER: Failure to verify the power supply connections will result in total destruction of the ÉlanSC400 microcontroller evaluation board.

2. Plug the VGA monitor into an electrical outlet and turn it on.
3. If a diskette drive is installed, make sure it is empty.
4. Apply power to the ÉlanSC400 microcontroller evaluation board by connecting the PC power supply to an electrical outlet. If the power supply is equipped with a switch, turn it on.

   The power supply fan and hard disk should start running, and the port 80h LEDs should start to display power-on self-test (POST) status codes. Then the speaker should beep and the monitor should start displaying BIOS messages.

5. The first time you start the system, the BIOS might display a message reporting a CMOS error or some other BIOS configuration problem. Follow the instructions shown on the screen to enter the Setup utility. Once you are in the Setup utility, you can set the system's date, time, startup drive, and other options.
6. In the BIOS setup utility, configure Drive C for the proper number of heads, cylinders and sectors. For most hard disk drives, you can select Autoconfigure to let the BIOS do this automatically.

   For more information on each included BIOS, see the corresponding BIOS manual. BIOS manuals are included in Adobe Acrobat format on the diskette shipped with your kit.

7. Save and exit the setup utility.
8. The system should now boot using the operating system on the hard disk. If you encounter any problems, see "Installation Troubleshooting" on page 1-8.

Installation Troubleshooting

Table 1-1. Installation Troubleshooting

Problem	Solution
The Port 80h LED readout is blank after I turn on the power supply.	Check power supply connections at P1 and P2.
The Port 80h LED readout is stuck at 00. I see nothing on the VGA monitor and do not hear any beeps from the speaker. I do not hear the head synchronization on the diskette drive (if attached).	Ensure processor reset by pressing the Reset button, SW7. Make sure the Reset jumper, P42, is *not* connected. Make sure section CFG0 on switch SW3 is Off. Make sure CFG1 on SW3 is set correctly: Off if JP36 is set to "BIOS", and On if JP36 is set to "X16". See page 2-16.
I hear a beep on the speaker but see nothing on the VGA monitor.	Check that the monitor is plugged in and turned on. Check that the monitor is correctly connected to the ISA-bus VGA card. Check that the VGA card is correctly seated in the ISA slot.
I get the startup message on the monitor but it says there's a battery problem or CMOS checksum error and the system doesn't finish booting.	Follow the BIOS instructions to run the Setup utility to configure the CMOS RAM and save settings.
I configured the CMOS RAM and saved my settings, but settings are lost the next time I turn on the evaluation board.	Make sure a fresh 3.0-V 20-mm coin cell is installed correctly in the BT1 battery holder.
I don't hear any sound from the diskette drive and the system does not boot from a diskette.	Check that the 34-wire cable to the diskette drive is properly connected at both the drive end and the board end (board connector P14). Check that the CMOS setup indicates that drive A is a 3.5-inch, 1.44-Mbyte drive.

Table 1-1. Installation Troubleshooting (Continued)

Problem	Solution
I hear the diskette being accessed but get an error message “Non System disk” or “Drive A not found.”	Check that the diskette in the drive is indeed bootable, just as you would on a standard PC. Make sure the diskette drive is connected properly to the last connector on the cable.
I get a “Missing Keyboard” error message on the monitor during boot-up.	Check that keyboard is properly connected. Check that SW1 is set to the “C2” position (switch is depressed towards the AT label on the board).
I have installed a hard disk with a preinstalled operating system, but the evaluation board won’t access the hard disk.	Check that the 40-wire IDE cable is properly connected at both the drive end and the board end (board connector P12). Check that the CMOS setup is configured correctly for your drive. Make sure the evaluation board will start from a bootable diskette in drive A. Then try to do a directory listing of drive C. If the directory listing of C works, the drive is functioning and there is a problem with the drive’s boot block or system image. (Note that some operating systems will display an error if you list an empty directory.) Make sure the drive functions properly on a different system. Note, however, that the mapping of logical to physical sectors on a hard drive can vary from one BIOS to another, so your hard drive might work on another computer but not be readable by the BIOS on the ÉlanSC400 microcontroller evaluation board. In that case, you should boot from diskette and reformat the hard drive while it is attached to the ÉlanSC400 microcontroller evaluation board. See your DOS documentation for how to reformat your hard drive.
There is a problem you cannot resolve.	Check that the board is set to its default settings (see Appendix A, “Evaluation Board Default Settings”). Contact the AMD Technical Support Hotline (see Chapter 3, “Product Support”).

Chapter 2

Board Functional Description

The ÉlanSC400 microcontroller evaluation board provides a test and development platform for ÉlanSC400 microcontroller-based designs. Read the following sections to learn more about the board:

See the appendices for information about default board settings, verified peripherals, board layout suggestions, and the bill of materials and schematics.

Overview of Features

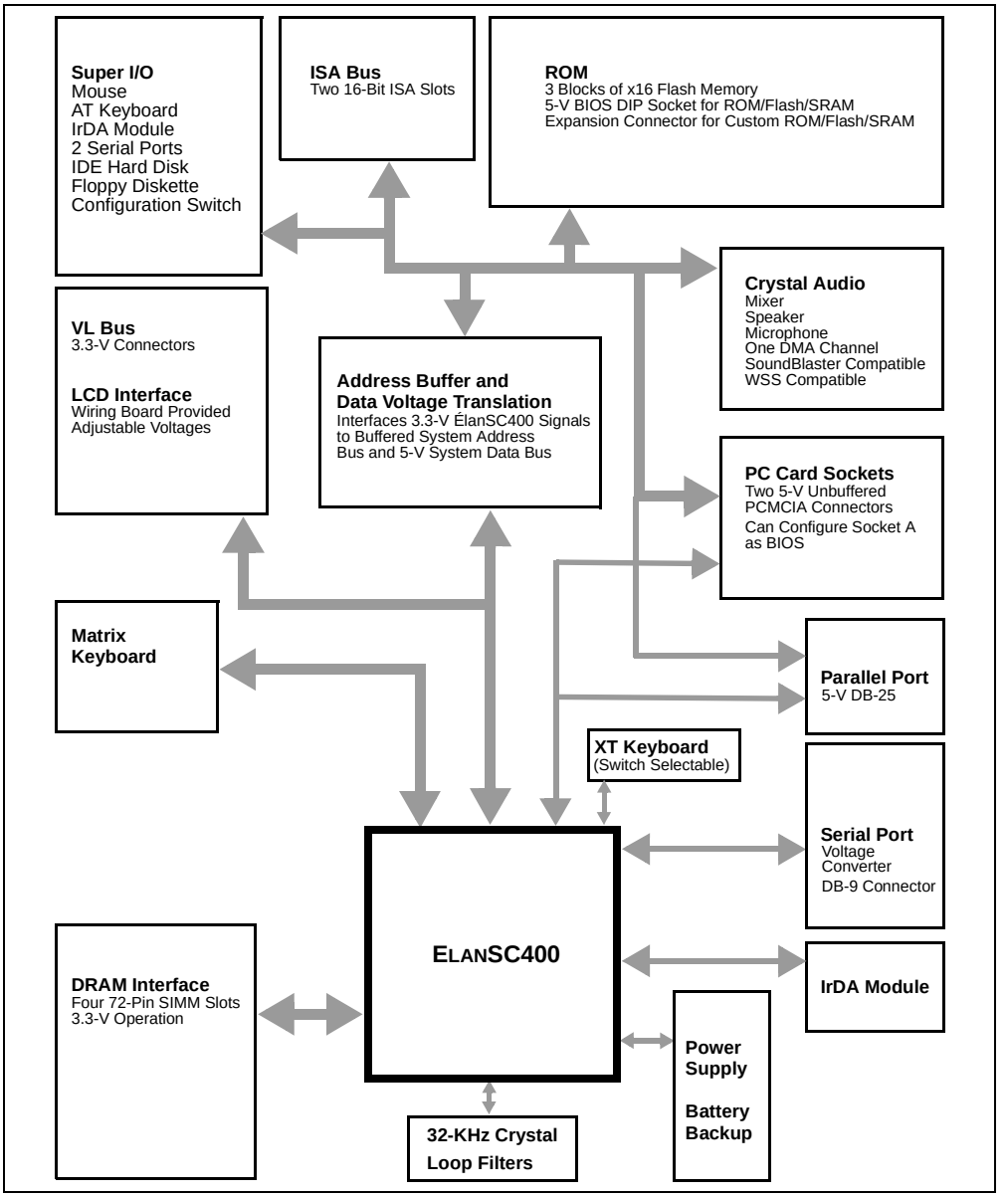


Figure 2-1. ÉlanSC400 Microcontroller Evaluation Board Overview (Duplicate)

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Board Block Diagram

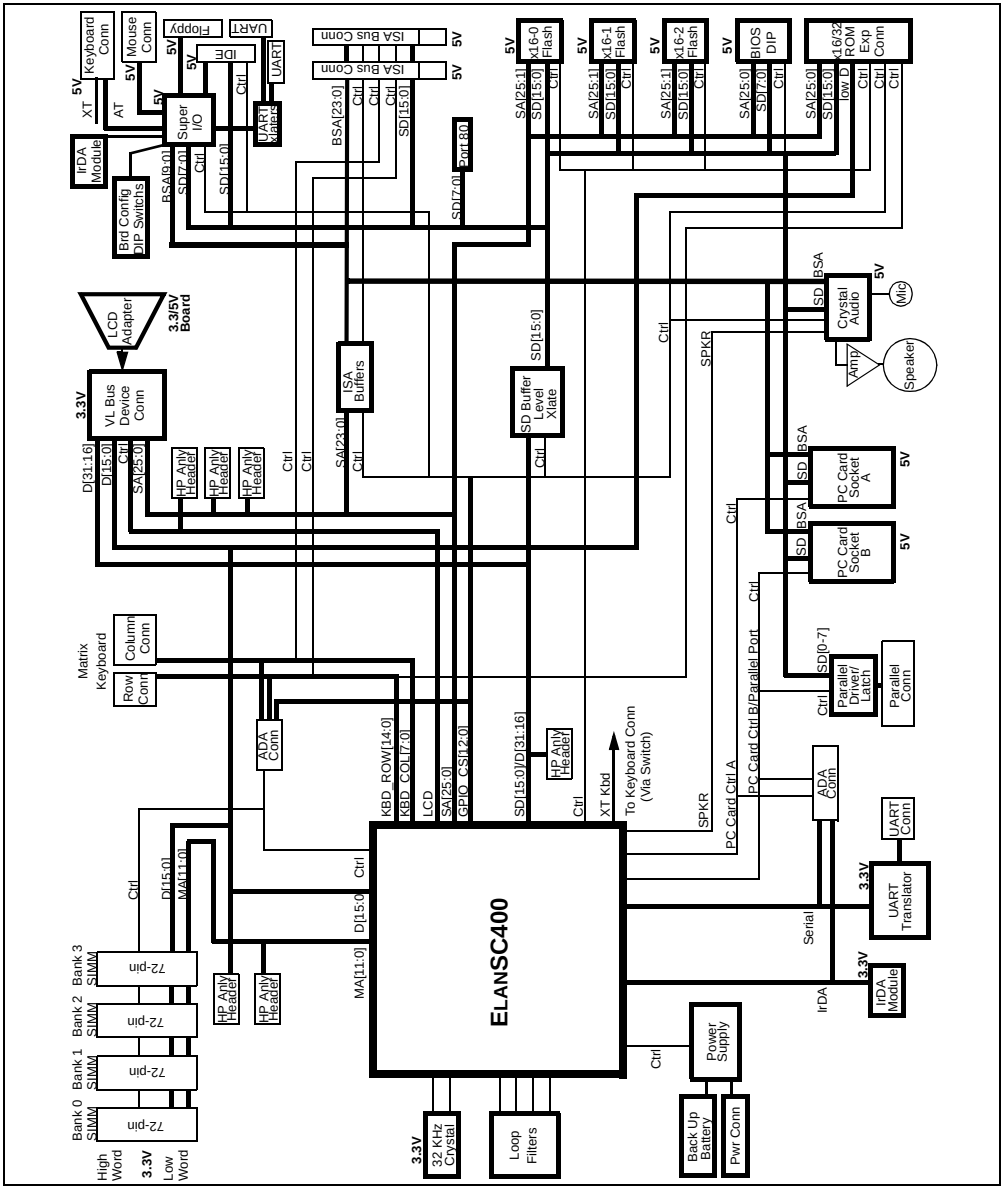

Figure 2-2. ÉlanSC400 Microcontroller Evaluation Board Block Diagram

Board Layout

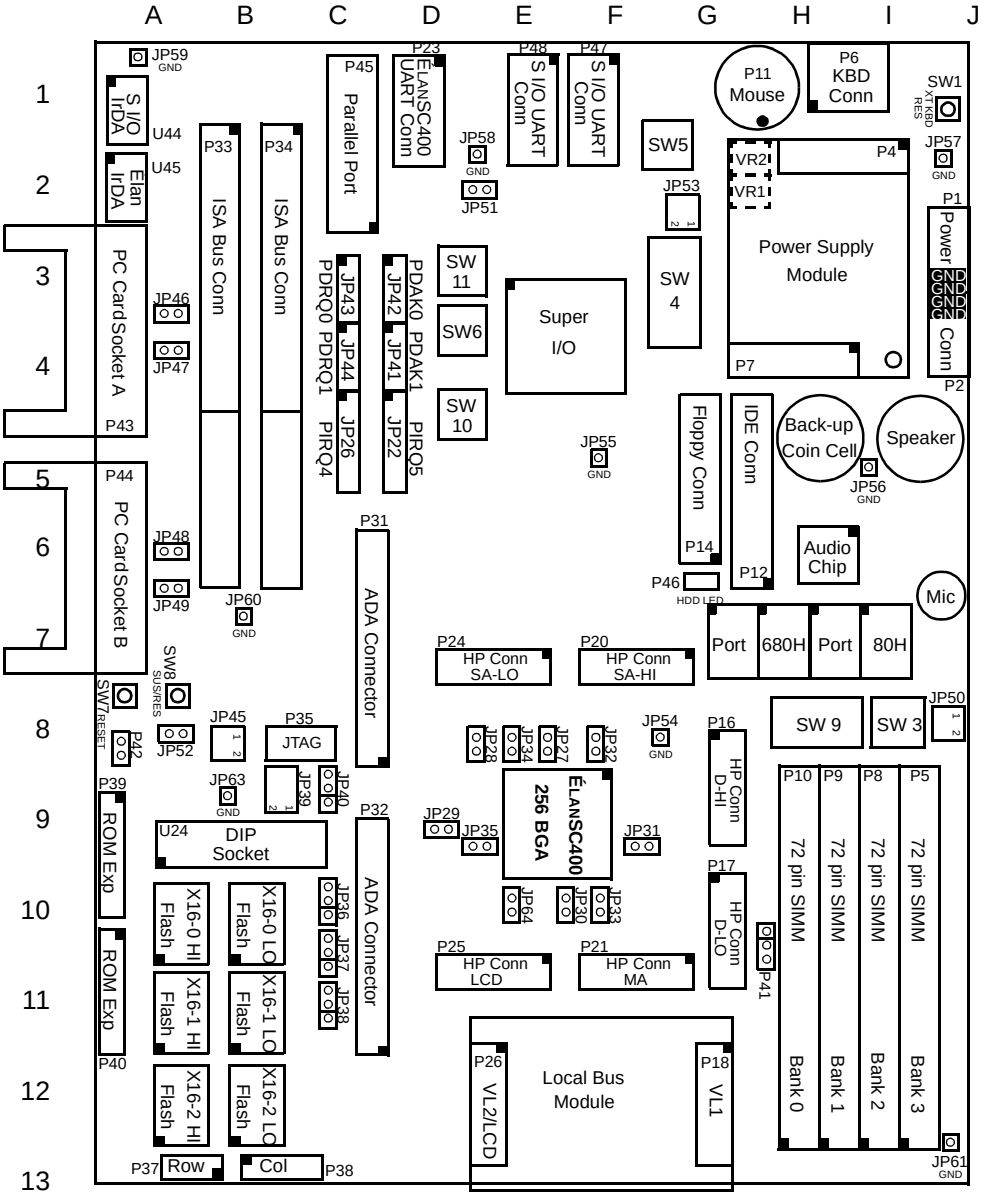

Figure 2-3. ÉlanSC400 Microcontroller Evaluation Board Layout

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Table 2-1. Board Jumpers, Switches, and Adjustments

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
JP22	KBDCOL4 (PIRQ5)	Used to route ÉlanSC400 microcontroller programmable PIRQ5 to IRQ 3–7, 9–12, 14, or 15 on the ISA bus connectors.	D4–D5	Sheet 10	page 2-28
JP26	KBDCOL3 (PIRQ4)	Used to route ÉlanSC400 microcontroller programmable PIRQ4 to IRQ 3–7, 9–12, 14, or 15 on the ISA bus connectors.	C4–C5	Sheet 10	page 2-28
JP27	V_{CC}CPU	ÉlanSC400 microcontroller CPU V_{CC}. Enables current measurement for microcontroller CPU power pins (2.7–3.6-V DC).	E8	Sheet 2	page 2-50
JP28	AV_{CC}	ÉlanSC400 microcontroller Analog V_{CC}. Enables current measurement for microcontroller analog power plane driving internal PLLs and oscillator circuit.	D8–E8	Sheet 2	page 2-50
JP29	V_{CC}RTC	ÉlanSC400 microcontroller RTC V_{CC}. Enables current measurement for microcontroller RTC power plane driven by 3.3-V AV_{CC} or 3-V cell.	D9	Sheet 2	page 2-50
JP30	V_{CC}	ÉlanSC400 microcontroller V_{CC}. Enables current measurement for microcontroller core power pins (3.3-V DC).	E10–F10	Sheet 2	page 2-50

Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
JP31	V_{CC}MEM	ÉlanSC400 microcontroller memory interface V_{CC}. Enables current measurement for microcontroller memory interface power pins (3.3-V DC).	F9–G9	Sheet 2	page 2-50
JP32	V_{CC}BUS	ÉlanSC400 microcontroller Bus V_{CC}. Enables current measurement for microcontroller SD bus power pins (3.3-V DC).	F8	Sheet 2	page 2-50
JP33	V_{CC}LCD	ÉlanSC400 microcontroller LCD V_{CC}. Enables current measurement for microcontroller LCD and VESA local bus power pins (3.3-V DC).	F10	Sheet 2	page 2-50
JP34	V_{CC}PCM	ÉlanSC400 microcontroller PC Card V_{CC}. Enables current measurement for microcontroller PC Card Socket A and Socket B interface power pins (3.3-V DC).	E8	Sheet 2	page 2-50
JP35	V_{CC}SER	ÉlanSC400 microcontroller serial port V_{CC}. Enables current measurement for microcontroller serial port power pins (3.3-V DC).	D9–E9	Sheet 2	page 2-50

Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
JP36	$\overline{\text{ROMCS0}}$	ROM Chip select 0. Used to configure $\overline{\text{ROMCS0}}$ to the DIP socket or to Flash memory block x16-0. *(SW3 must also be configured.)*	C10	Sheet 8	page 2-16
JP37	$\overline{\text{ROMCS1}}$	ROM Chip select 1. Used to configure $\overline{\text{ROMCS1}}$ to the DIP socket or to Flash memory block x16-1.	C10–C11	Sheet 8	page 2-16
JP38	$\overline{\text{ROMCS2}}$	ROM Chip select 2. Used to configure $\overline{\text{ROMCS2}}$ to the DIP socket or to Flash memory block x16-2.	C11	Sheet 8	page 2-16
JP39	ROMP31	$\overline{\text{ROMWR}}$ and address routing for DIP socket device	B9–C9	Sheet 8	page 2-18
JP40	ROMP29	$\overline{\text{ROMWR}}$ and address routing for DIP socket device	C9	Sheet 8	page 2-18
JP41	$\overline{\text{PDACK1}}$	With SW10, used to route ÉlanSC400 microcontroller programmable $\overline{\text{PDACK1}}$ to $\overline{\text{DACK}}$ 0–3, 5–7 on the ISA bus connectors.	D4	Sheet 10	page 2-30
JP42	$\overline{\text{ISADACK}}$	With SW6, used to route ÉlanSC400 microcontroller programmable $\overline{\text{PDACK0}}$ to $\overline{\text{DACK}}$ 0–3, 5–7 on the ISA bus connectors.	D3	Sheet 10	page 2-30

Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
JP43	ISADRQ	With SW6, used to route ISA DRQ 0–3, 5–7 from ISA bus connectors to ÉlanSC400 microcontroller programmable PDRQ0.	C3	Sheet 10	page 2-30
JP44	PDRQ1	With SW10, used to route ISA DRQ 0–3, 5–7 from ISA bus connectors to ÉlanSC400 microcontroller programmable PDRQ1.	C4	Sheet 10	page 2-30
JP45	$\overline{\text{PPWE}}$ $\overline{\text{CD\_B}}$	Used to disable the parallel port buffer control signal when using PC Card Socket B	B8	Sheet 14	page 2-39
JP46	V_{CC}PCMA5	Used to measure current in 5-V V_{CC} PC Card Socket A system power plane.	A3–A4	Sheet 19	page 2-50
JP47	V_{PP}PCMA	Used to measure current in 12-V V_{PP} PC Card Socket A system power plane.	A4	Sheet 19	page 2-50
JP48	V_{CC}PCMB5	Used to measure current in 5-V V_{CC} PC Card Socket B system power plane.	A6	Sheet 19	page 2-50
JP49	V_{PP}PCMB	Used to measure current in 12-V V_{PP} PC Card Socket B system power plane.	A6	Sheet 19	page 2-50
JP50	V_{CC}DRAM3	DRAM V_{CC}. Enables user to measure current being used by the DRAM (3.3-V DC). Two jumpers are needed to support the maximum load (3.84 A).	G8–H8	Sheet 20	page 2-50

Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
JP51	V_{CC}SER3	System serial port V_{CC}. Enables current measurement for system serial port power plane (3.3 V DC).	D2–E2	Sheet 20	page 2-50
JP52	V_{CC}ROM5	ROM V_{CC}. Enables current measurement for ROM system power plane (5 V).	C9	Sheet 20	page 2-50
JP53	V_{CC}ISA5	System ISA V_{CC}. Enables current measurement for ISA system power plane (5 V). Two jumpers are needed to support the maximum load (~5 A).	F2–G2	Sheet 20	page 2-50
JP54	GND	Ground post.	G8	Sheet 21	page 2-55
JP55	GND	Ground post.	F5	Sheet 21	page 2-55
JP56	GND	Ground post.	I5	Sheet 21	page 2-55
JP57	GND	Ground post.	J2	Sheet 21	page 2-55
JP58	GND	Ground post.	D2–E2	Sheet 21	page 2-55
JP59	GND	Ground post.	A1	Sheet 21	page 2-55
JP60	GND	Ground post.	B7	Sheet 21	page 2-55
JP61	GND	Ground post.	J13	Sheet 21	page 2-55
JP63	GND	Ground post.	B9	Sheet 21	page 2-55
JP64	V_{CC}SYS	ÉlanSC400 microcontroller ISA V_{CC}. Enables current measurement for microcontroller ISA bus power pins (3.3-V DC).	E10	Sheet 2	page 2-50
SW1	RSTDRVXT	XT Keyboard reset.	J1	Sheet 18	N/A

Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
SW3	CFG2–CFG0	Used to configure boot ROM pinstrap options.	I8	Sheet 4	page 2-22
SW4	ACIN, $\overline{BL2}$–$\overline{BL0}$, MKBDEN, DCFGx	Switches for power management test, matrix keyboard enable, board diagnostics	G3	Sheet 21	page 2-54
SW5	AT/XT	Used to select Super I/O AT or ÉlanSC400 microcontroller XT keyboard interface.	F1–G2	Sheet 18	page 2-44
SW6	$\overline{PDACK0}$ /PDRQ0	Used to select either floppy or ISA bus for programmable DMA channel 0.	D3–E4	Sheet 10	page 2-33
SW7	RESET	Used to reset (reboot) the system.	A7–A8	Sheet 4	page 2-53
SW8	SUSRES	Used to force ÉlanSC400 microcontroller to suspend mode and to resume.	A7–B8	Sheet 4	page 2-53
SW9	KBDROW 0–6	Used to enable either full DRAM interface or matrix keyboard	H8	Sheet 7	page 2-25
SW10	$\overline{PDACK1}$ /PDRQ1	Used to select either audio or ISA bus for programmable DMA channel 1.	D4–E5	Sheet 10	page 2-34
SW11	PIRQ2	Used to select either audio or PS/2 mouse for programmable PIRQ 2.	D3–E3	Sheet 10	page 2-45

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Table 2-1. Board Jumpers, Switches, and Adjustments (Continued)

Part	Signal	Description	Reference in Figure 2-3	See App. D schematics on	For more info., see
VR1	V_{EE}	Used to adjust both V_{EE}POS and V_{EE}NEG. Enable in software and measure on LCD interface card.	G2–H2	N/A	page 2-46
VR2	V_{CC}CPU	Used to adjust CPU V_{CC}. Measure on JP27.	G2–H2	N/A	page 2-50

Board Restrictions

- A number of functions are limited by or limit the use of the matrix keyboard because of shared signals. See “Matrix Keyboard (B13)” on page 2-41.
- Only two ISA bus IRQs and DMAs can be used at any one time. Using both ISA bus DMAs disables the Super I/O floppy and the Crystal audio device.
- The mouse port is unavailable if audio IRQ is enabled and vice versa.
- The parallel port is unavailable if PC Card Socket B is enabled and vice versa.
- The local bus is unavailable if the LCD interface is enabled and vice versa.

Board Features

The remainder of this chapter describes the features of the ÉlanSC400 microcontroller evaluation board. The number in parenthesis following each heading indicates the part’s location in Figure 2-3 on page 2-4. In addition, other locations or jumpers referenced can be found in the figure.

ÉlanSC400 Microcontroller (E9)

The ÉlanSC400 microcontroller contains an Am486 CPU core providing up to 33-Mhz bus operation, 105-Mbps burst mode, internal PLLs capable of multiplying the clock speed to 100 MHz, and a 16- or 32-bit wide data path.

The ÉlanSC400 microcontroller exclusively integrates several of the standard PC/AT peripherals. The ÉlanSC400 microcontroller controls:

- One 16550-compatible serial port
- IrDA infrared interface
- One EPP parallel port
- Two 82365-compatible PC Card sockets
- ISA bus
- Matrix and XT keyboard
- LCD Display Interface
- 3.3-V VESA local bus

The chip is a 292-pin BGA, marked U14 on the board. See Figure 2-4 on page 2-13 for a block diagram of the ÉlanSC400 microcontroller.

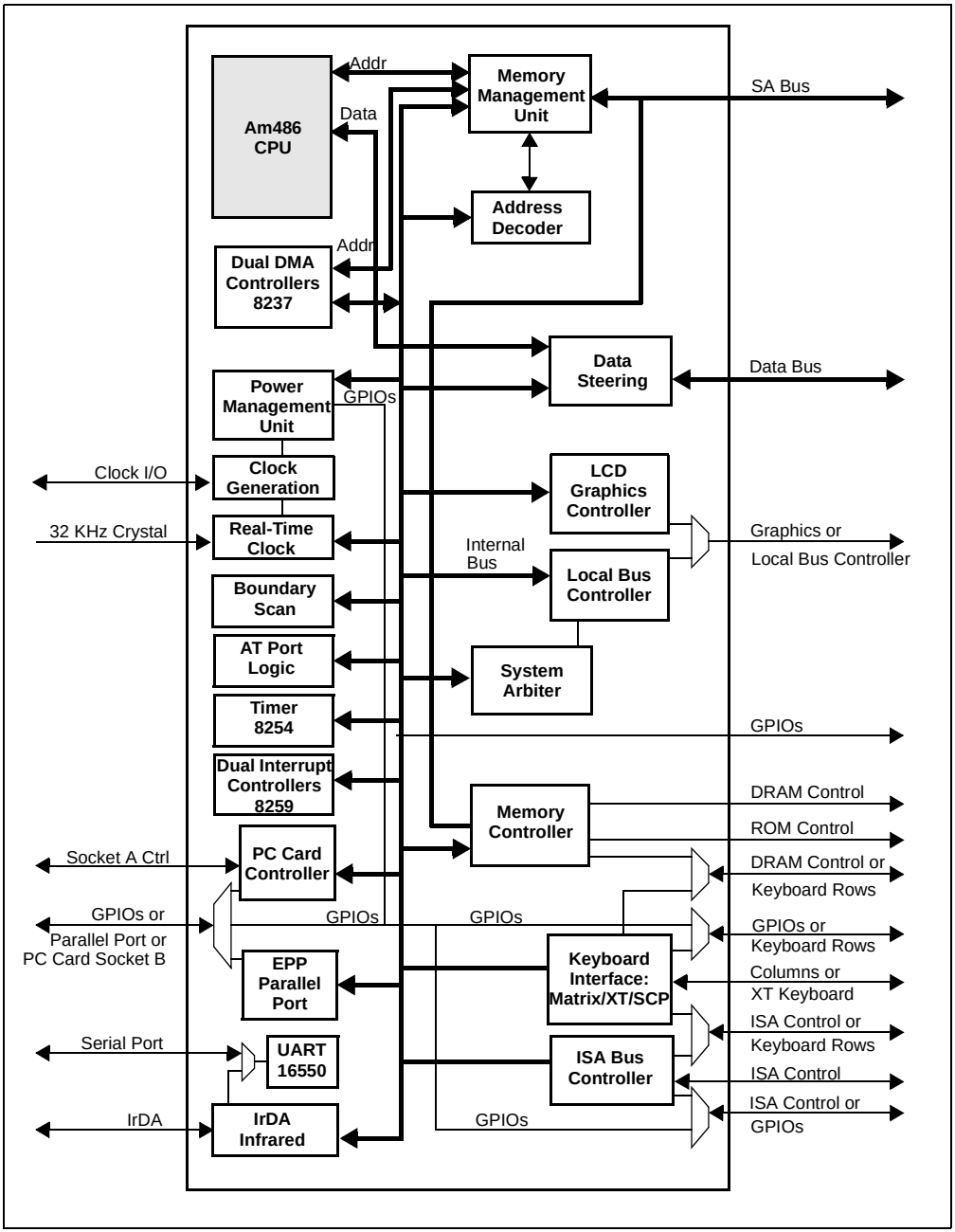

Figure 2-4. ÉlanSC400 Microcontroller Block Diagram

Super I/O (E3)

The Super I/O governs all devices except audio that are not under the direct control of the ÉlanSC400 microcontroller. It is provided on the board for debugging purposes and provides an environment more like a desktop PC for development. The Super I/O controls:

- Two 16550-compatible serial ports
- IrDA infrared interface
- IDE hard drive interface
- Floppy disk interface
- AT keyboard
- PS/2 mouse
- Chip select for port 80h and port 680h LED readouts.

Crystal Audio Interface (H6)

The ÉlanSC400 microcontroller evaluation board includes a Crystal digital audio chip, marked U54 on the board, plus a microphone, amplifier, and speaker to allow testing of software that requires SoundBlaster, SoundBlaster Pro, or Windows Sound System compatibility.

One audio DMA channel is provided, which shares programmable DMA channel 1 with the ISA bus via switch SW10. See “ISA Bus DMA Versus Crystal Audio I/O (SW10)” on page 2-34. Programmable DMA channel 1 is not available when the matrix keyboard is in use.

Audio interrupts share microcontroller PIRQ2 with the PS/2 mouse and the matrix keyboard interface. See “PS/2 Mouse (H1)” on page 2-45.

The microcontroller SPKR output is routed to the audio chip for mixing with digital audio output.

ROM Space (B10–B12)

The ÉlanSC400 microcontroller provides three ROM/Flash memory chip selects to the system to control three independent ROM/Flash memory spaces. The ÉlanSC400 microcontroller evaluation board provides one 32-pin DIP socket and six AMD 29F016 2M x 8 Flash memory parts soldered to the board. The DIP socket can be configured to accept up to 512-Kbyte of 8-bit-wide ROM, EPROM, Flash memory, or SRAM devices. The soldered-down Flash memory devices are configured in three banks of 2M x 16 words.

The E4FLASH utility included on diskette with your kit allows you to program, verify, and read back the Flash memory devices on the evaluation board. For details, see the text file documentation for that utility.

You can boot the system from either of two BIOS images from different vendors. One BIOS is installed in the DIP socket, the other is programmed into bank 0 of the soldered-on Flash memory. Documentation for each provided BIOS is included on diskette in Adobe Acrobat (PDF) format.

This section discusses the following:

ROM/Flash Chip Select Routing (JP36, JP37, and JP38)

Three jumper blocks (JP36, JP37, and JP38) allow you to route any of the three ROM chip selects from the ÉlanSC400 microcontroller to the DIP socket or to one of the blocks of x16 Flash memory.

Note: *Never set more than one chip select jumper (JP36, JP37, or JP38) to the "DIP" position. For example, a conflict will occur if you set both JP36 and JP37 to select the DIP socket. Such a conflict will cause improper operation and might damage the memory device or the microcontroller.*

You can route one, two, or all three chip selects to x16 Flash memory. When routed to x16 Flash memory, each chip select enables a different pair of Flash memory chips (labeled x16-0, x16-1, or x16-2 on the board).

JP36: $\overline{\text{ROMCS0}}$ Routing

The jumper block JP36 lets you route $\overline{\text{ROMCS0}}$ to the chip select of the DIP socket or to Flash memory block 0 (x16-0). Figure 2-5 shows the valid JP36 configurations.

Note: *If you move jumper JP36 to change $\overline{\text{ROMCS0}}$ routing, you must reconfigure segment CFG1 on switch SW3 to set the correct boot ROM interface width. Set CFG1 off (8 bit) for the DIP socket. Set CFG1 on (16 bit) for Flash memory block x16-0. If you disconnect JP36, you must configure the board to boot from PC Card A or install a custom boot ROM expansion device on P39 and P40. See "Boot ROM Configuration (SW3)" on page 2-22.*

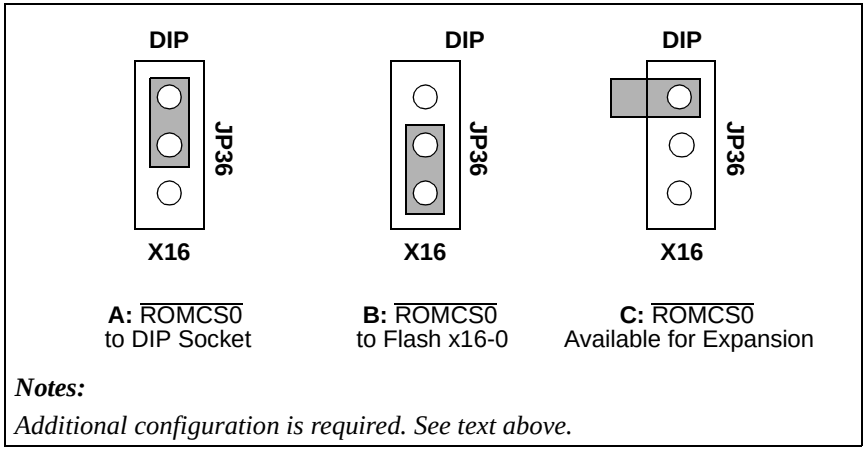

Figure 2-5. JP36 Jumper Positions (C10)

JP37: $\overline{\text{ROMCS1}}$ Routing

The jumper block JP37 lets you route $\overline{\text{ROMCS1}}$ to the chip select of the DIP socket or to Flash memory block 1 (x16-1). If JP37 is not connected, $\overline{\text{ROMCS1}}$ is available for use by the custom ROM expansion connectors P39 and P40. Figure 2-6 shows the valid JP37 configurations. Configure the $\overline{\text{ROMCS1}}$ data bus width in software via CSC Index 25h[2–1]. See the microcontroller documentation for configuration details.

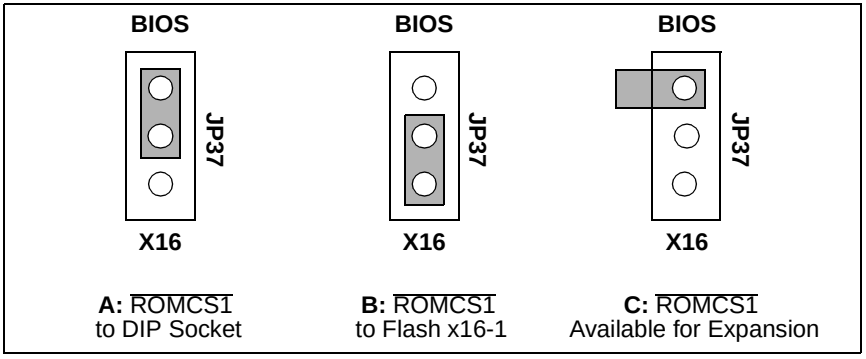

Figure 2-6. JP37 Jumper Positions (C10–C11)

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JP38: $\overline{\text{ROMCS2}}$ Routing

The jumper block JP38 lets you route $\overline{\text{ROMCS2}}$ to the chip select of the DIP socket or to Flash memory block 1 (x16-2). If JP38 is not connected, $\overline{\text{ROMCS2}}$ is available for use by the custom ROM expansion connectors P39 and P40. Figure 2-6 shows the valid JP38 configurations. Configure the $\overline{\text{ROMCS2}}$ data bus width in software via CSC Index 27h[2–1]. See the microcontroller documentation for configuration details.

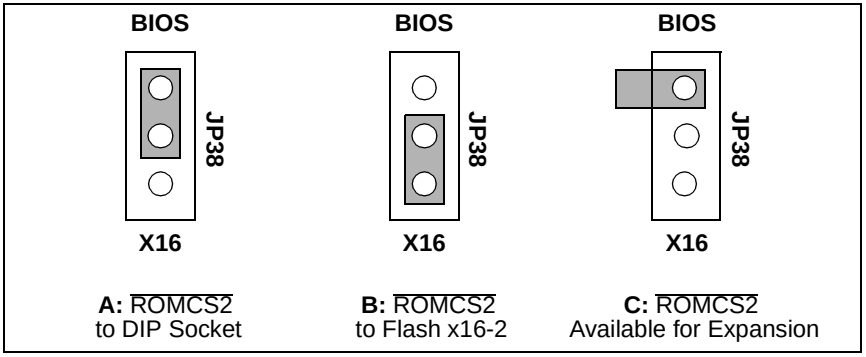

Figure 2-7. JP38 Jumper Positions (C11)

Device Selection for the DIP Socket (JP39 and JP40)

The 8-bit DIP ROM socket on the ÉlanSC400 microcontroller evaluation board can be used to support various Flash memory, EPROM, or SRAM devices. Densities supported are shown in Table 2-2. This table also shows how to configure jumpers JP39 and JP40 so they route signals to the socket correctly for each different device type's pinout. Pinouts for the various devices supported are shown in Table 2-3 on page 2-19.

Table 2-2. DIP ROM Device Selection

Device	JP39	JP40
Flash memory 128K x 8	1-2	1-2
Flash memory 256K x 8	1-2	1-2
Flash memory 512K x 8	1-2	1-2
EPROM 128K x 8	NC	1-2
EPROM 256K x 8	NC	1-2
EPROM 512K x 8	3-4	1-2
SRAM 512K x 8	5-6	2-3

Note: *Only 5-V V_{CC} devices can be used. Programming is not supported for devices requiring 12-V V_{PP}.*

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Table 2-3. Pinouts for ROM, Flash Memory, and SRAM

Pin	ROM			Flash Memory			SRAM
	128Kx8	256Kx8	512Kx8	128Kx8	256Kx8	512Kx8	512Kx8
1	V_{PP}	V_{PP}	V_{PP}	V_{PP}/NC	V_{PP}	A18	A18
2	A16	A16	A16	A16	A16	A16	A16
3	A15	A15	A15	A15	A15	A15	A14[1]
4	A12	A12	A12	A12	A12	A12	A12
5	A7	A7	A7	A7	A7	A7	A7
6	A6	A6	A6	A6	A6	A6	A6
7	A5	A5	A5	A5	A5	A5	A5
8	A4	A4	A4	A4	A4	A4	A4
9	A3	A3	A3	A3	A3	A3	A3
10	A2	A2	A2	A2	A2	A2	A2
11	A1	A1	A1	A1	A1	A1	A1
12	A0	A0	A0	A0	A0	A0	A0
13	D0	D0	D0	D0	D0	D0	D1
14	D1	D1	D1	D1	D1	D1	D2
15	D2	D2	D2	D2	D2	D2	D3
16	GND	GND	GND	GND	GND	GND	GND
17	D3	D3	D3	D3	D3	D3	D4
18	D4	D4	D4	D4	D4	D4	D5
19	D5	D5	D5	D5	D5	D5	D6
20	D6	D6	D6	D6	D6	D6	D7
21	D7	D7	D7	D7	D7	D7	D8
22	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/$\overline{P}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CS}$

Notes:

1. The evaluation board uses a non-standard address pinout for SRAM. See the following text.

Table 2-3. Pinouts for ROM, Flash Memory, and SRAM (Continued)

Pin	ROM			Flash Memory			SRAM
	128Kx8	256Kx8	512Kx8	128Kx8	256Kx8	512Kx8	512Kx8
23	A10	A10	A10	A10	A10	A10	A10
24	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
25	A11	A11	A11	A11	A11	A11	A11
26	A9	A9	A9	A9	A9	A9	A9
27	A8	A8	A8	A8	A8	A8	A8
28	A13	A13	A13	A13	A13	A13	A13
29	A14	A14	A14	A14	A14	A14	$\overline{WE}$
30	NC	A17	A17	NC	A17	A17	A17
31	$\overline{PGM}$	$\overline{PGM}$	A18	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	A15[1]
32	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

Notes:

1. The evaluation board uses a non-standard address pinout for SRAM. See the following text.

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JP39: $\overline{ROMWR}$ and Address Routing

The three-position jumper block JP39 selects the signal to route to pin 31 on the DIP socket (see Figure 2-8 on page 2-21). Pin 31 is different for different part types and densities. As seen in Table 2-3, pin 31 is Address 18 on the 512K x 8 ROM, and it is write enable for Flash memory.

For 128K x 8 and 256K x 8 EPROMs, pin 31 is the Program pin. For these devices JP39 should not be connected on the ÉlanSC400 microcontroller evaluation board because the board does not support the 12-V V_{PP} used by these devices.

For SRAM only, the ÉlanSC400 microcontroller evaluation board deviates from the standard address pinout (shown in Table 2-3 above) to simplify jumper settings. For SRAM, SA15 remains connected to DIP pin 3, and SA14 is routed to DIP pin 31. (Effectively, the two SRAM address pins are reversed.) This works because SRAM byte read and write order is not critical, and the data is volatile. Nonstandard addressing will *not* work for EPROM or Flash memory.

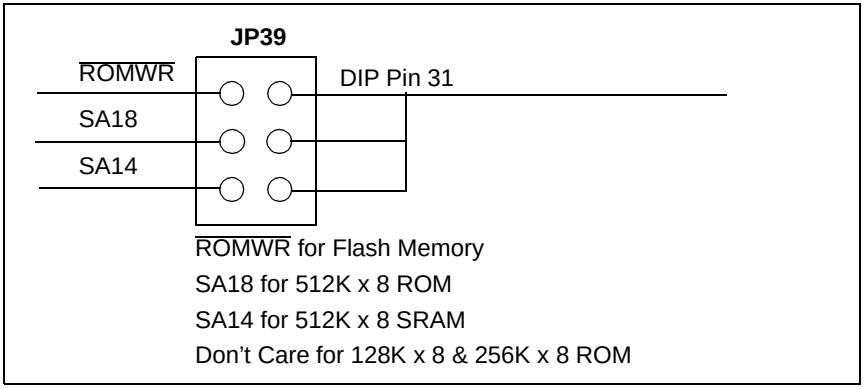

Figure 2-8. JP39 Jumper

JP40: More ROMWR and Address Routing

The two-position jumper at JP40 selects the signal to route to pin 29 on the DIP socket (see Figure 2-9). Pin 29 is different for different types of part. As seen in Table 2-3, pin 29 is Address 14 for ROM and Flash memory parts, or it is the Write Enable for the 512K x 8 SRAM.)

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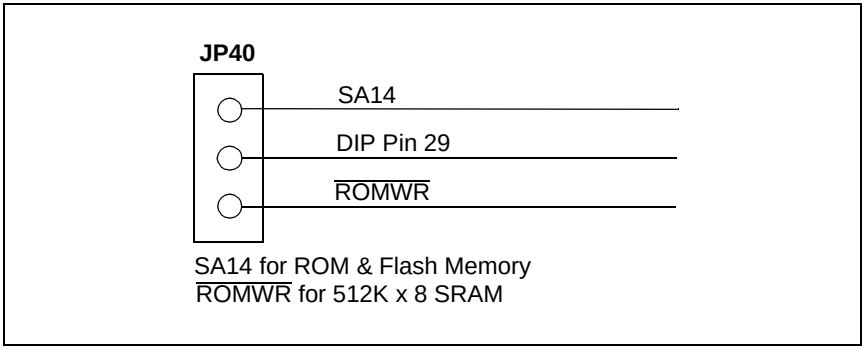


Figure 2-9. JP40 Jumper

Boot ROM Configuration (SW3)

The ÉlanSC400 microcontroller asserts the $\overline{\text{ROMCS0}}$ chip select to fetch its first instruction after reset. Normally $\overline{\text{ROMCS0}}$ is routed to the BIOS DIP socket on the evaluation board, but it can also be routed to different devices on the board or redirected within the microcontroller to PC Card Socket A.

The boot ROM configuration is controlled by switch SW3 (location I8 on the board layout, Figure 2-3 on page 2-4). The three SW3 segments (individual switches) that are used are marked CFG0, CFG1, and CFG2 on the board. (See Figure 2-10.)

Note: *If you move jumper JP36 to change $\overline{\text{ROMCS0}}$ routing on the board (see page 2-16), you must set CFG1 to select the correct boot ROM data width. See "Boot ROM Width (SW3 CFG0 and CFG1)" on page 2-23.*

CFG2 lets you select PC Card Socket A as the boot device. See "PC Card Boot Option (SW3 CFG2)" on page 2-23.

These switches are connected to ÉlanSC400 microcontroller configuration pins, also called "pin straps." During normal operation these pins act as memory address lines, but during reset the microcontroller latches the state of the pins and uses this information to set parameters for the BIOS boot device. This is necessary because the boot device must be selected before the system can fetch code to execute.

When a CFG switch on SW3 is set to 0 (off), the configuration pin's weak internal pull-down resistor causes a 0 to latch at reset. When a switch is set to 1 (on), the switch connects the pin to a pull-up resistor that causes a 1 to latch at reset.

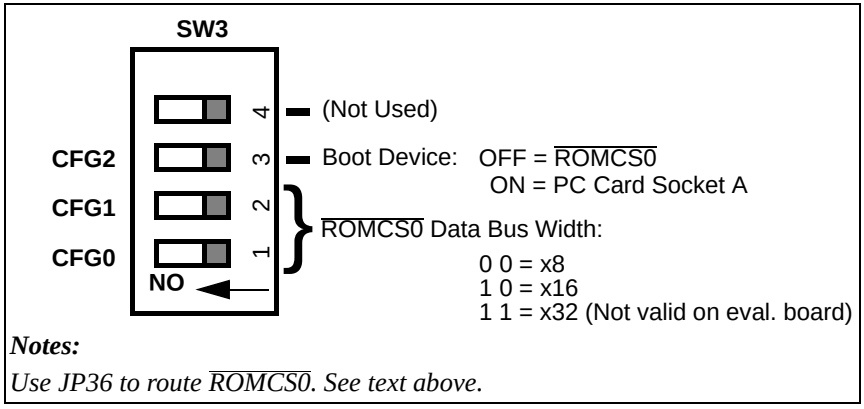


Figure 2-10. Boot Configuration Switch (SW3)

Boot ROM Width (SW3 CFG0 and CFG1)

The ÉlanSC400 microcontroller CFG0 and CFG1 pin straps are used to configure the boot ROM data bus width to x8, x16, or x32. The evaluation board does not support x32 ROM data, so you should never select x32 mode. In a design that uses x32 mode, $\overline{\text{R32BFOE}}$ would be asserted for $\overline{\text{ROMCS0}}$. Table 2-4 shows the possible data width settings.

On the evaluation board, CFG0 and CFG1 are set via SW3. However, it is never necessary to change CFG0 (it should always be off).

Select the x8 configuration (CFG1 off) when booting from the ROM DIP socket. Select x16 (CFG1 on) when booting from Flash memory bank x16-0. If you configure the board to boot from another device (PC Card or custom ROM expansion daughter board), be sure to set the data width correctly for that device.

Table 2-4. Boot ROM Data Width

CFG1 (segment 2)	CFG0 (segment 1)	$\overline{\text{ROMCS0}}$ Data Width	$\overline{\text{R32BFOE}}$
0 (off)	0 (off)	x8	Disabled
0 (off)	1 (on)	x8	Disabled
1 (on)	0 (off)	x16	Disabled
1 (on)[1]	1 (on)	x32	Enabled

Notes:

1. Although the ÉlanSC400 microcontroller supports x32 ROM, this board does not. Do not set both CFG0 and CFG1 to on.

PC Card Boot Option (SW3 CFG2)

The ÉlanSC400 microcontroller provides the option of selecting PC Card Socket A as the boot ROM. To select this option, set the SW3 switch marked CFG2 to on. To restore the normal $\overline{\text{ROMCS0}}$ pin chip select, set CFG2 to off.

When booting from PC Card A, the boot data width (CFG0 and CFG1 on SW3) must be set to x8 or x16, depending on the device being used. The PC Card interface does not support the x32 data width.

The ability to boot from a PC Card makes it possible to manufacture devices using unprogrammed Flash memory, and then program in the latest firmware when the product ships. In the field, a service technician can boot the device using diagnostic firmware contained on a PC Card simply by moving a jumper or switch and pressing

reset. This feature is especially useful for upgrading firmware. Replacing a chip or upgrading from software might render the device unusable because of a simple bent pin or untimely power loss. An upgrade boot ROM on a PC Card is immune to these pitfalls.

When selecting or designing a PC Card boot device, be sure to read the section about PC Card control in the microcontroller user's manual memory management chapter. In particular, the PC Card boot memory device should be linear (not ATA), and should only decode the address space that it actually has memory for. Such a card will alias its contents throughout the PC Card address space. This is desirable because a card that does not alias and is less than 64-Mbyte will have no way to hook the PC Card boot vector at 3FFFFF0h.

In the BIOS or execute-in-place (XIP) boot code, the first access beyond the current segment causes A25–A20 to be asserted. To continue operation above 1 Mbyte, but outside of the top 64 Kbyte, the boot code must first enter Protect mode, set up an MMS window, and point the MMS window to the $\overline{\text{ROMCS0}}$ device.

Also, if your design uses the PC Card Socket A power control pin functions (PCMA_VCC, PCMA_VPP1, PCMA_VPP2), your PC Card boot code must take certain steps before changing these pins from their default GPIO functions (GPIO15, GPIO_CS14, and GPIO_CS13). First, enable the PC Card controller via CSC D0h[1], and then set PC Card Index 02h[4] to enable the PC Card Socket A power control registers. After this is done, CSC 39h[5] may be set to enable GPIO15–GPIO_CS13 as PC Card Socket A power control pins.

This sequence ensures that the PC Card A power control is enabled before the GPIO15–GPIO_CS13 pins are switched to their power control function. Otherwise PC Card A power would be lost as soon as CSC 39h[5] was set. (These GPIO pins' default states match the PC Card power configuration for PCMA V_{CC} enabled.)

When changing register bits, always use a read/modify/write operation to preserve the state of other bits in the register. Figure 2-20 on page 2-37 shows example read/modify/write code that configures CSC register indexes for two other features (programmable DMA and IRQ), but the same technique can be applied to any register index you need to modify. (For PC Card indexes, use index register 03E0h and data register 03E1h.)

DRAM Main Memory (I10)

The ÉlanSC400 microcontroller evaluation board comes with two 72-pin, 3.3-V, 60-ns, non-parity, self-refresh, FPM DRAM SIMMs installed on the board. The evaluation board requires DRAMs with access times of 70 ns or less (for 33 MHz operation). The SIMMs are a standard pinout but operate at only 3.3 V.

Use only 3.3-V SIMMs when changing the DRAM configuration. Also, you must not use 1-bit DRAMs on the ÉlanSC400 microcontroller evaluation board because of the loading restrictions associated with 32 loads. Please refer to “Board Block Diagram” on page 2-3 to ensure correct installation. Install the first SIMM into Bank 0 (socket P10), the second into Bank 1 (socket P9), the third in Bank 2 (socket P8), and the fourth in Bank 3 (socket P5).

When the board is shipped, all four SIMM sockets are enabled for x32 DRAM. If you want to use the microcontroller’s matrix keyboard interface and internal graphics controller, you must turn off segments 1–7 of switch SW9 on the board to limit the DRAM to two banks of x16 memory. This is necessary because the matrix keyboard interface shares pins with the high-word $\overline{\text{CAS}}$ and bank 2 and 3 $\overline{\text{RAS}}$ signals, and because the graphics controller cannot be used when any x32 data bus is enabled.

Turning off switch SW9 segments 1–4 limits the DRAM interface to the low word (x16) by disconnecting $\overline{\text{CASL2}}$, $\overline{\text{CASL3}}$, $\overline{\text{CASH2}}$, and $\overline{\text{CASH3}}$. Segments 5 and 6 disable banks 2 and 3 by disconnecting $\overline{\text{RAS2}}$, and $\overline{\text{RAS3}}$. Segment 7 disconnects MA12. These signals are shared with matrix interface signals KBDROW0–KBDROW6. (SW9 segment 8 is not used.)

See the ÉlanSC400 microcontroller documentation for information about detecting and configuring DRAM. The BIOS provided will automatically detect the amount of DRAM installed, but because this is an evaluation BIOS, it will not select all configurations of DRAM.

ISA Bus Interface (B1–B6)

The ÉlanSC400 microcontroller evaluation board is populated with two standard ISA bus connectors for developers who need to use ISA devices in their development systems. These ISA bus connectors have certain limitations because of other components on the evaluation board, shared signals on the ÉlanSC400 microcontroller, and ISA bus signals that are not supported by the ÉlanSC400 microcontroller. To make the evaluation board as flexible as possible, switches and jumpers are provided on the board so you can selectively assign certain signals to the ISA bus connectors.

Note: *The switches and jumpers on the evaluation board only change the routing of signals between various pins and connectors. Software must still configure the ÉlanSC400 microcontroller to enable or disable the appropriate signal functions on the shared pins.*

When the system boots, the BIOS programs all ISA signals that share pins with other functions on the ÉlanSC400 microcontroller to be ISA signals. This gives the most flexibility to the ISA bus connectors.

Keep in mind that the following signals are shared with the matrix keyboard controller. The BIOS defaults to enable these for use on the ISA bus, but if you enable the matrix keyboard controller, these signals will not be available at the ISA bus.

- PIRQ7
- PIRQ6
- PIRQ5
- PIRQ4
- PIRQ3
- $\overline{\text{MCS16}}$
- $\overline{\text{SBHE}}$
- BALE
- PIRQ2
- PDRQ1
- $\overline{\text{PDACK1}}$

2.0

There are several standard ISA signals that are not supported on the ÉlanSC400 microcontroller. We have added components to the board to accommodate those that are necessary. The standard ISA signals *not* supported are:

- $\overline{0WS}$ – Zero Wait State

  Not necessary to support; ISA will work without this signal.

- $\overline{MASTER}$ – Bus Master Enable

  ISA bus mastering is not supported in the ÉlanSC400 microcontroller.

- $\overline{REF}$ – Refresh

  DRAM refresh is not echoed to the ISA bus so the signal is not necessary to disable ISA accesses during DRAM refresh.

- $\overline{IOCHCHK}$ – I/O Channel Check

  Rarely used ISA signal that causes an NMI.

- $\overline{SMEMR}$ – Memory Read for ISA accessed in lowest 1 Mbyte of Memory
- $\overline{SMEMW}$ – Memory Write for ISA accessed in lowest 1 Mbyte of Memory

  These two signals are necessary for the ISA bus connectors because many cards use them instead of the $\overline{MEMR}$ and $\overline{MEMW}$ signals. These are generated with a programmable logic part on the board; they are simply the qualification of SA[25:20] as low with $\overline{MEMR}$ and $\overline{MEMW}$.

- SYSCLK—8-MHz System Clock
- 14MHz—14-MHz clock

  These two signals are generated on the board with oscillators.

DMA and IRQ Routing

The ÉlanSC400 microcontroller provides internal interrupt request (IRQ) and direct memory access (DMA) functions traditionally provided by discrete 8259 programmable interrupt controller (PIC) and 8237 DMA controller (DMAC) devices. However, to minimize pin count (and thus system cost), only two of the seven possible PC/AT compatible DMA channels are available externally to the ÉlanSC400 microcontroller, and at most there are eight possible IRQ inputs, of which two can be routed to the ISA connectors on the evaluation board.

Software can control which internal interrupt level or DMA channel the external IRQ or DMA pins are used for inside the ÉlanSC400 microcontroller. This is done via two configuration status and control (CSC) register ports, 22h and 23h. For example, the evaluation board BIOS normally programs these registers so the programmable pins PDRQ0 and $\overline{\text{PDACK0}}$ are routed internally to DMA channel 2, which is used for the floppy disk controller in a typical PC/AT system.

On the ÉlanSC400 microcontroller evaluation board, the two available PIRQ signals can be routed separately to any of the eleven ISA bus IRQ pins. The two DMA channels are normally used for the floppy diskette and audio interfaces, but you can switch either channel to the ISA bus instead. When used for ISA, either programmable DMA channel can be routed by jumpers to any of the seven ISA bus DMA channels.

The following sections explain how to route these signals physically on the evaluation board, but your software will also have to configure CSC registers 22h and 23h appropriately to route the signals within the ÉlanSC400 microcontroller.

IRQs

The ÉlanSC400 microcontroller pins PIRQ4 and PIRQ5 can be routed to the ISA bus. There are two large jumper blocks (JP22 and JP26) that are used to route each of these signals to the specific ISA bus IRQ that is needed. Figure 2-11 and Figure 2-12 on page 2-29 show the layouts of the IRQ routing jumper blocks.

Note that these programmable IRQs on the ÉlanSC400 microcontroller are not available when the matrix keyboard is used.

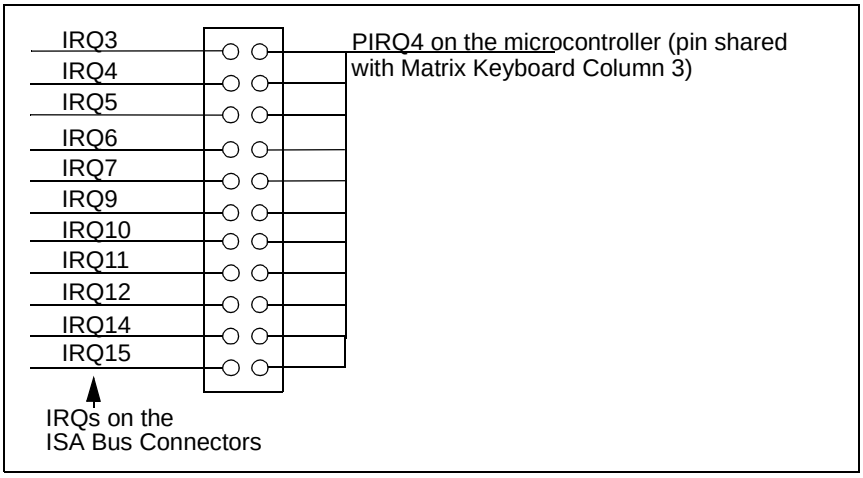


Figure 2-11. PIRQ4 Jumper Block (JP26)

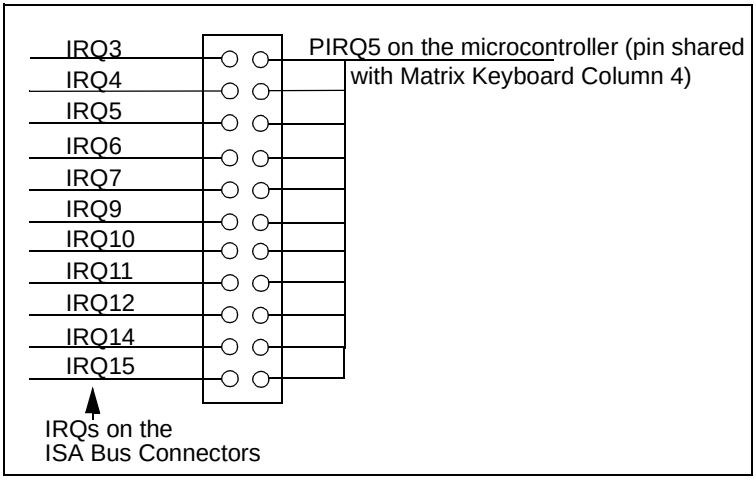


Figure 2-12. PIRQ5 Jumper Block (JP22)

DMAs

There are four large jumper blocks (JP41 and JP44, JP42 and JP43) that are used to route either of the ÉlanSC400 microcontroller DMA channels to the specific ISA bus DMA channel that is needed. The microcontroller DMA channel signals are PDRQ0, $\overline{\text{PDACK0}}$, PDRQ1, and $\overline{\text{PDACK1}}$.

To use DMA channel 0 for an ISA device, you must first switch it from the floppy diskette drive controller (Super I/O chip) to the ISA bus. See “ISA Bus DMA Versus Floppy Diskette Drive (SW6)” on page 2-33 for more information.

To use DMA channel 1 for an ISA device, you must first switch it from the audio device (Crystal chip) to the ISA bus. See “ISA Bus DMA Versus Crystal Audio I/O (SW10)” on page 2-34 for more information.

Note that programmable DMA channel 1 on the ÉlanSC400 microcontroller is not available when the matrix keyboard is used.

To select the ISA DMA channel to be supported by either programmable DMA channel, you must populate *two* jumpers. One jumper routes the DRQ signal for a channel, and the other jumper routes $\overline{\text{DACK}}$.

Figures 2-13 through 2-16 on the following pages show the jumper block layouts for routing the $\overline{\text{PDACK1}}$, PDRQ1, $\overline{\text{PDACK0}}$, and PDRQ0 signals.

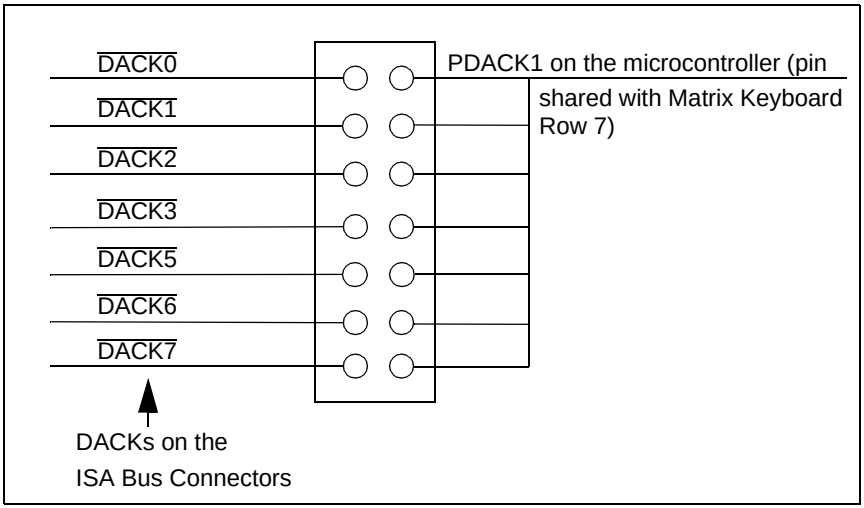


Figure 2-13. PDACK1 Jumper Block (JP41)

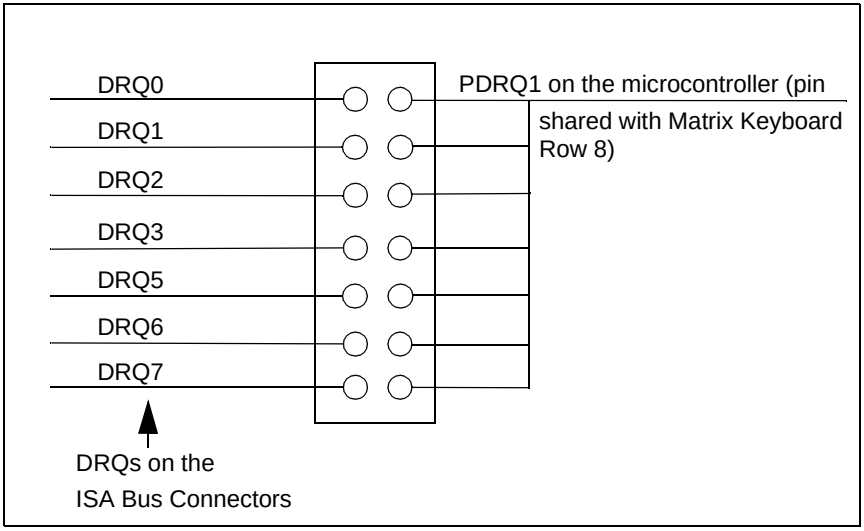


Figure 2-14. PDRQ1 Jumper Block (JP44)

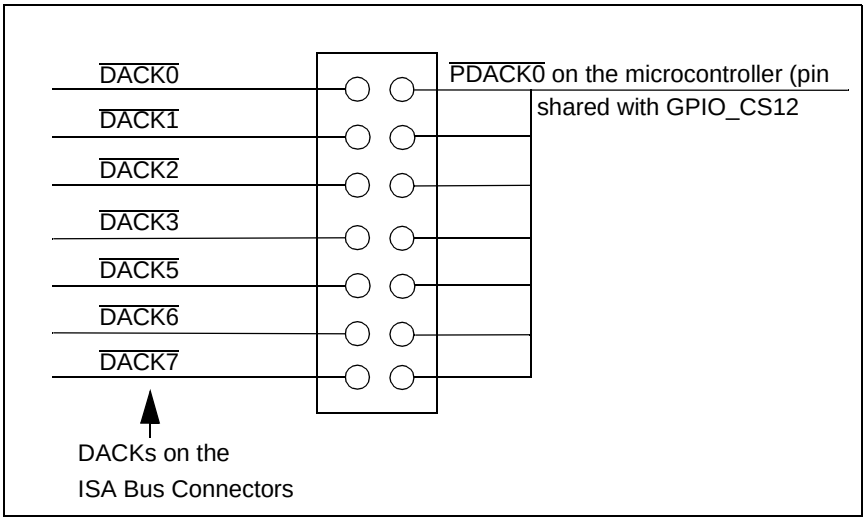


Figure 2-15. PDACK0 Jumper Block (JP42)

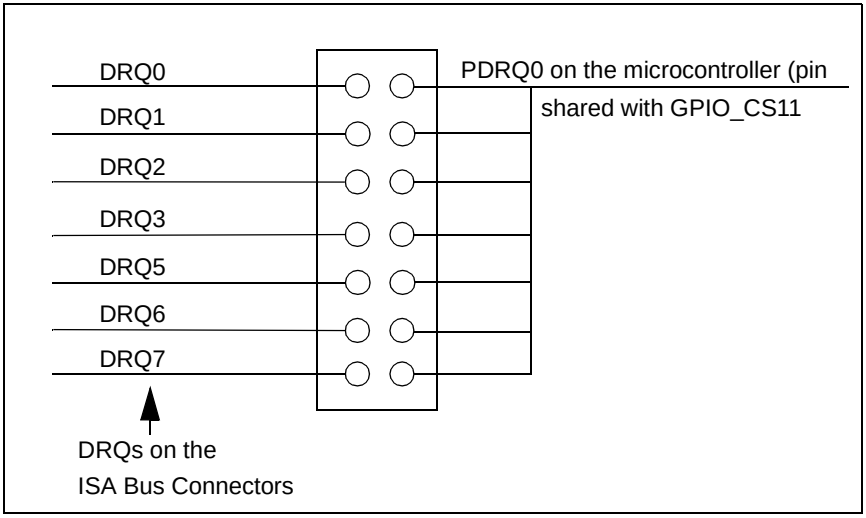


Figure 2-16. PDRQ0 Jumper Block (JP43)

2.0

ISA Bus DMA Versus Floppy Diskette Drive (SW6)

Switch SW6 must be set to allow the ISA bus to use the ÉlanSC400 microcontroller DMA signals that are normally used by the Super I/O floppy diskette controller. These signals are PDRQ0 and $\overline{\text{PDACK0}}$. See Figure 2-17.

To switch PDRQ0 and $\overline{\text{PDACK0}}$ to the ISA bus, push switch SW6 to position "C2". To switch these signals back to the Super I/O diskette interface, select position "C1". (You can route this channel to any ISA DMA channel. See "DMAs" on page 2-30.)

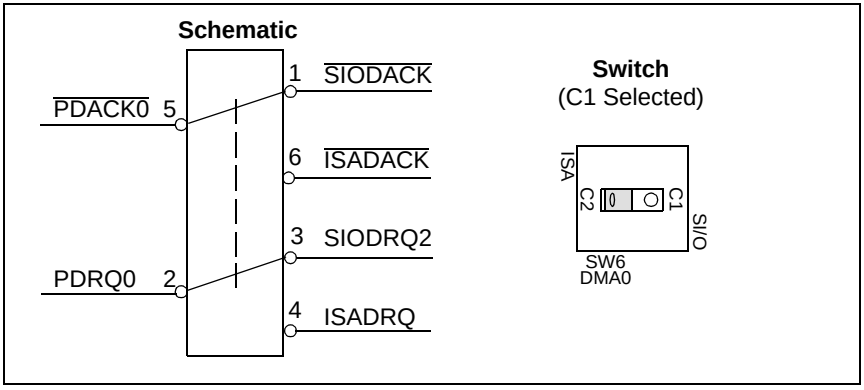


Figure 2-17. Programmable DMA 0 Switch (SW6)

ISA Bus DMA Versus Crystal Audio I/O (SW10)

Switch SW10 must be set to allow ISA bus to use the ÉlanSC400 microcontroller DMA signals that are normally used by the Crystal audio device. These signals are PDRQ1, and $\overline{\text{PDACK1}}$. See Figure 2-18.

To switch PDRQ1 and $\overline{\text{PDACK1}}$ to the ISA bus, push switch SW10 to position "C2". To switch these signals back to the audio interface, select position "C1". (You can route this channel to any ISA DMA channel. See "DMAs" on page 2-30.)

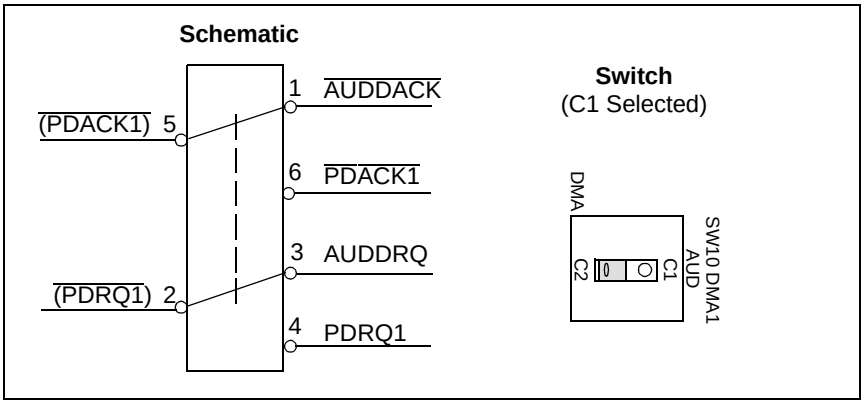


Figure 2-18. Programmable DMA 1 Switch (SW10)

Example IRQ and DMA Configuration

This section shows how to configure the ÉlanSC400 microcontroller evaluation board for an example ISA audio card that uses ISA signals IRQ11, DMA1 (for recording), and DMA3 (for simultaneous playback). (This ISA audio card would replace the evaluation board's onboard audio interface.) In this example, both of the available programmable DMA channels (four pins) and one PIRQ pin will be routed to the required ISA bus pins. Furthermore, the appropriate CSC registers will be programmed to associate these PIRQ and programmable DMA pins with the correct IRQ and DMA signals in the ÉlanSC400 microcontroller.

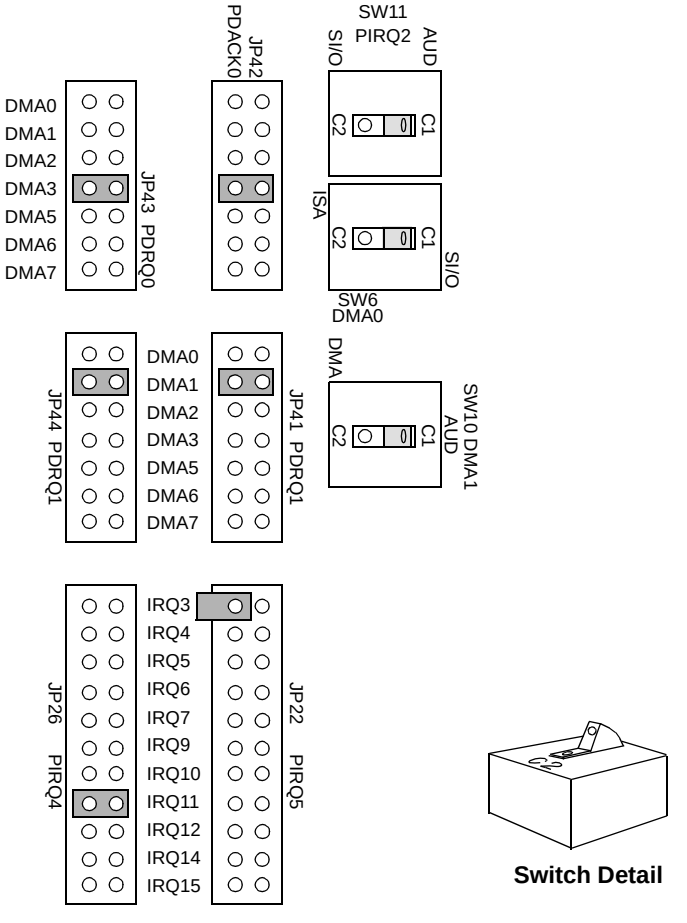
Only one IRQ pin is needed, so either PIRQ4 or PIRQ5 can be routed to the ISA bus. This example routes pin PIRQ4 to ISA IRQ11. Both programmable DMA channels are needed, so it is unimportant which one is routed to a particular ISA DMA channel. This example uses programmable DMA channel 1 for ISA DMA1 and programmable DMA 0 for ISA DMA 3.

For the example just described, the following configuration steps are appropriate:

1. Route PIRQ4 to ISA IRQ11 by moving the jumper on the PIRQ4 jumper pin block (JP26) to the position marked “IRQ11” on the board.
2. Change SW6 from its default position C1, (marked “SI/O” on the board) to its C2 position (marked “ISA”). Change the switch by rocking it towards the desired position. This makes programmable DMA channel 0 available for routing to the ISA bus.
3. Route PDRQ0 to ISA DRQ3 by moving the jumper on the PDRQ0 jumper block (JP43) to the position marked “DMA3” on the board.
4. Route $\overline{\text{PDACK0}}$ to ISA $\overline{\text{DACK3}}$ by moving the jumper on the $\overline{\text{PDACK0}}$ jumper block (JP42) to the position marked “DMA3” on the board. (The positions marked next to JP43 also apply to JP42. See Figure 2-19 on page 2-36)
5. Change SW11 from its default position C1, (marked “AUD” on the board) to its C2 position (marked “DMA”). This makes programmable DMA channel 1 available for routing to the ISA bus.

   Since this disables the onboard audio device, you can also change SW11 from its default position C1, (marked “AUD” on the board) to its C2 position (marked “DMA”). This is not necessary for ISA DMA, but it makes the Super I/O mouse interface available.
6. Route PDRQ1 to ISA DRQ1 by moving the jumper on the PDRQ1 jumper block (JP44) to the position marked “DMA1” on the board.
7. Route $\overline{\text{PDACK1}}$ to ISA $\overline{\text{DACK1}}$ by moving the jumper on the $\overline{\text{PDACK1}}$ jumper block (JP41) to the position marked “DMA1” on the board.

   Figure 2-19 on page 2-36 shows how the jumpers and switches are configured after these steps.



ISA Jumper and Switch Layout
(Example Settings Shown)

Notes:

This example does not route PIRQ5 to the ISA bus, so jumper JP22 is shown in its storage (disconnected) position.

Figure 2-19. Example ISA Jumper and Switch Configuration

Now that the PIRQ and programmable DMA pins needed for this example are routed to the correct pins on the ISA bus, you need to do some internal signal routing within the ÉlanSC400 microcontroller to complete the process.

8. In your software, use a read/modify/write operation to change CSC Index D6h[3–0] to a value of xxxx1011b, where x represents bits whose value you must preserve. In this case you must preserve bits 7–4 to maintain the current PIRQ5 routing setting.

   You can use the SDB (simple debugging) utility included on diskette with your kit to temporarily change individual CSC register values.

9. In your software, use a read/modify/write operation to change CSC Index DBh[5–0] to a value of xx010100b, where x represents bits whose value you must preserve. In this case you must preserve bits 7–6 to maintain the current IrDA DMA routing. Bits 5–0 set the routing for both programmable DMA channels.

The following source code example performs the internal signal routing that is required by this example configuration:

```
        ...
MOV     AL,     0D6h    ;Select CSC Index 0D6h (programmable IRQ routing)
OUT     22h,    AL
IN      AL,     23h     ;Read current PIRQ internal routing
AND     AL,     0F0h    ;Clear *only* the bits to be changed
OR      AL,     0Bh     ;Set *only* configuration bits for PIRQ 4
OUT     23h,    AL      ;Write the new value to the configuration register

MOV     AL,     0DBh    ;Select CSC Index 0DBh (programmable DMA routing)
OUT     22h,    AL
IN      AL,     23h     ;Read current PDMA internal routing
AND     AL,     0C0h    ;Clear *only* the bits to be changed
OR      AL,     14h     ;Set *only* the configuration bits for PDMA 0 and 1
OUT     23h,    AL      ;Write the new value to the configuration register
        ...
```

Figure 2-20. Example IRQ and DMA Configuration Code

Many audio or network cards for non-plug-and-play systems have driver installation programs that auto-detect the presence of their hardware and warn the user of possible conflicts with other hardware in their system. Such utilities will not work properly until you route the required PIRQ or programmable DMA signals in hardware and software as described in this section (using the ISA IRQ and DMA signals appropriate for the device). After the signals are routed properly, the driver installation program will be able to auto-detect the resources that are routed to its ISA card and use this information to configure the software driver for the device.

Serial Ports (D1, E1, and F1)

The ÉlanSC400 microcontroller evaluation board includes the following serial ports. You can configure each port using the DOS-based SETE4SER utility that is included on diskette with your kit. **SETE4SER /S** displays the current serial port configuration. For details, see the text file documentation for that utility.

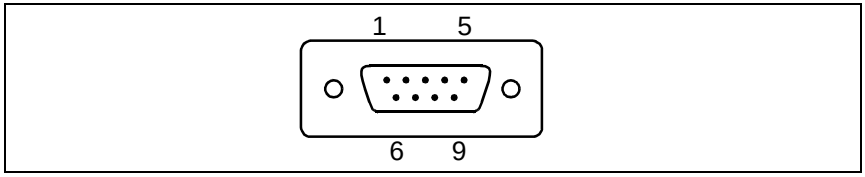


Figure 2-21. Serial Port Connector Pins (P23, P47, P48)

ÉlanSC400 Microcontroller Serial Port (D1)

The evaluation board has one standard 8-pin serial port driven by the ÉlanSC400 microcontroller 16550A UART. The UART for the serial interface powers up in 16450 mode (storage for one byte transmit/receive) but can be set to 16550 mode (with 16-byte FIFO) or IrDA mode (see "IrDA Interface (A1 and A2)" on page 2-39).

The serial port is available on a 9-pin D-shell connector at location P23 (see Figure 2-21). Its location is marked "SERIAL" on the evaluation board.

Super I/O Serial Ports (E1 and F1)

The evaluation board's Super I/O device includes two 16550-compatible serial ports that can also be used. These are routed to two 9-pin D-shell connectors at locations P47 (marked "SI/O SER1" on the board) and P48 (marked "SI/O SER2"). See Figure 2-21.

Do not enable the Super I/O serial ports when the matrix keyboard interface is enabled. The matrix keyboard interface shares pins on the ÉlanSC400 microcontroller with PIRQ7 and PIRQ3, which are used for Super I/O serial ports 1 and 2, respectively. Interrupt conflicts will occur if a Super I/O serial port is enabled at the same time as the matrix keyboard interface.

IrDA Interface (A1 and A2)

ÉlanSC400 Microcontroller IrDA Interface (A2)

The ÉlanSC400 microcontroller supports infrared data transfers via its IrDA interface. The serial data transmission rates include all of the UART bit rates (up to 115 Kbps) and the board supports a 1.152 Mbps synchronous mode.

The ÉlanSC400 microcontroller IrDA interface on the board is available from an IrDA LED module at U45.

Super I/O IrDA Interface (A1)

The Super I/O supports infrared data transfers via its IrDA interface. The serial data transmission rates include all of the UART bit rates (up to 115 Kbps) but, unlike the ÉlanSC400 microcontroller, the board does not support a 1.152 Mbps synchronous mode. The Super I/O shares UART2 between its IrDA port and its serial port 2.

The Super I/O IrDA interface on the board is available from an IrDA LED module at U44.

Parallel Port (C1)

The parallel port feature of the ÉlanSC400 microcontroller cannot be enabled at the same time as PC Card Socket B because these features use shared pins on the microcontroller. To enable the parallel port, you need to configure jumper JP45 and program the microcontroller accordingly. Table 2-5 shows valid configurations for jumper JP45:

Table 2-5. JP45 Configuration

Function	JP45 Position
Parallel port available	Pins 1–2
PC Card Socket B available	Pins 3–4
GPIO31–GPIO21 available	No connection

By default, the ÉlanSC400 microcontroller evaluation board BIOS and JP45 are configured to support PC Card Socket B.

If you change JP45 to enable the parallel port, you will also need to change the software configuration. You can configure the parallel port using the DOS-based SETE4PAR utility that is included on diskette with your kit. For details, see the text file documentation for that utility.

You can also configure the port by modifying the ÉlanSC400 microcontroller CSC registers in software. See the microcontroller documentation for details.When changing register bits, always use a read/modify/write operation to preserve the state of other bits in the register. Figure 2-20 on page 2-37 shows example read/modify/write code that configures CSC register indexes for two other features (programmable DMA and IRQ), but the same technique can be applied to any CSC index you need to modify.

Figure 2-22 and Table 2-6 show the parallel port pinouts.

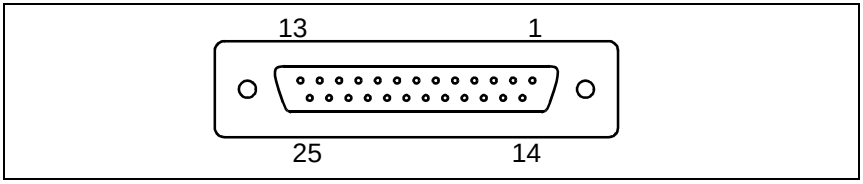


Figure 2-22. Parallel Port Socket (P45)

Table 2-6. Parallel Port Pin/Signal Table

Pin	Signal
1	$\overline{\text{STRB}}$
2–9	PD0–PD7
10	$\overline{\text{ACK}}$
11	BUSY
12	PE
13	SLCT
14	$\overline{\text{AFDT}}$
15	$\overline{\text{ERROR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{SLCTIN}}$
18–25	GND

PC Card (A3–A7)

The ÉlanSC400 microcontroller evaluation board provides two unbuffered PC Card sockets controlled by the PC Card controller in the ÉlanSC400 microcontroller.

PC Card Socket A can be selected as the BIOS location for the system. See “PC Card Boot Option (SW3 CFG2)” on page 2-23.

PC Card Socket B is normally enabled on the board. It must be disabled via jumper JP45 if you need to use the parallel port or GIPO31–GPIO21. See “Parallel Port (C1)” on page 2-39.

The two unbuffered PC Card sockets demonstrate the functionality of a non-buffered, low-cost PC Card implementation using the ÉlanSC400 microcontroller. Since there is no buffering, hot-swapping (changing cards with power applied) is not recommended on these sockets.

The power consumed by the PC Cards can be measured through JP46–JP49.

Matrix Keyboard (B13)

The ÉlanSC400 microcontroller controls a 15-row, 8-column matrix keyboard that can be supported by either interrupts or polling. Locations P37 and P38 are provided for connecting a 14-row x 8-column keyboard (the keyboard row 14 signal is used in its Suspend/Resume function).

The connector pin locations and functions are shown in Figure 2-23, Table 2-7, and Table 2-8 on page 2-43. The ÉlanSC400 microcontroller evaluation board has been tested with Fujitsu matrix keyboard model #N860-1406-T001. This keyboard connects directly to the row and column connectors provided.

Many of the control lines used by the matrix keyboard are shared by the ISA bus, DRAM, Flash memory, and XT Keyboard controllers on the ÉlanSC400

microcontroller. All of these functions are either limited by or limit the use of the matrix keyboard. Observe the following interactions when using the matrix keyboard:

- You must set segments 1–7 of switch SW9 to off before connecting a matrix keyboard. This disables the high word of x32 DRAM and DRAM banks 2 and 3, which share signals with the matrix keyboard. See “DRAM Main Memory (I10)” on page 2-25 for details.
- You must set SW4 segment 5 (marked MKBDEN) to off before connecting a matrix keyboard. See “Floppy Versus Matrix Keyboard (SW4 segment 5)” on page 2-49.
- You must set switch SW5 to AT before connecting a matrix keyboard. See “XT Keyboard (H1–I1)” on page 2-44.
- The matrix keyboard shares KBDROW9 (PIRQ2) with the PS/2 mouse or the audio interface, whichever is enabled by switch SW11. See “PS/2 Mouse (H1)” on page 2-45.
- The matrix keyboard shares several signals with the ISA bus controller. These are listed in “ISA Bus Interface (B1–B6)” on page 2-26.

Figure 2-23 below shows the matrix keyboard connectors. Table 2-7 and Table 2-8 on page 2-43 show the matrix keyboard connector pinouts.

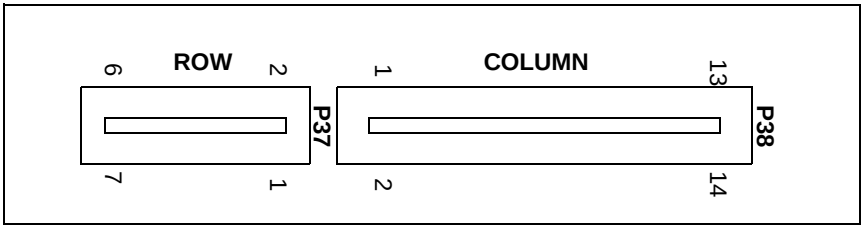


Figure 2-23. Matrix Keyboard Ribbon Connectors (P37, P38)

Table 2-7. Matrix Keyboard Row Connector Table

Pin	Signal
1	KBDCOL6
2	KBDCOL5
3	KBDCOL4
4	KBDCOL3
5	KBDCOL2
6	KBDCOL1
7	KBDCOL0

Table 2-8. Matrix Keyboard Column Connector Table

Pin	Signal
1	KBDROW0
2	KBDROW1
3	KBDROW2
4	KBDROW3
5	KBDROW4
6	KBDROW5
7	KBDROW6
8	KBDROW7
9	KBDROW8
10	KBDROW9
11	KBDROW10
12	KBDROW11
13	KBDROW12
14	KBDROW13

XT Keyboard (H1–I1)

The ÉlanSC400 microcontroller contains an XT keyboard interface that is compatible with the IBM PC-XT keyboard and operates at clock speeds up to 250 kHz. To operate an XT keyboard, insert the keyboard connector into the 5-pin DIN (P6) on the evaluation board and set SW5 to the “C1” position (switch is depressed towards the XT label on the board). This will route the keyboard clock and data signals to the XT clock and data lines. See Figure 2-24.

The XT keyboard interface cannot be used at the same time as the matrix keyboard interface. The XT keyboard shares signals with matrix keyboard columns 0 and 1.

Note: *This interface is not supported by the Phoenix BIOS. To select the startup BIOS, see “ROM/Flash Chip Select Routing (JP36, JP37, and JP38)” on page 2-16. To see what BIOS is selected, view the messages displayed at startup.*

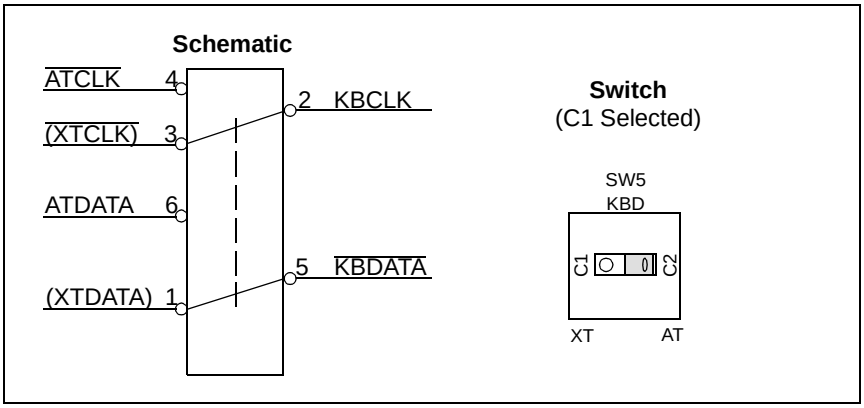


Figure 2-24. SW5 Switch

AT Keyboard (H1–I1)

If an AT keyboard is being used, the same 5-pin DIN external connector (P6) is implemented as for an XT keyboard, but SW5 must be set to “C2” (switch is depressed towards the AT label on the board).This will route the keyboard clock and data signals to the bidirectional AT clock and data lines on the Super I/O. This is the default when the board is shipped.

PS/2 Mouse (H1)

A PS/2 port has been provided on the evaluation board for a PS/2-style mouse. This device is driven by the keyboard controller internal to the Super I/O.

The Super I/O mouse interface interrupt, SIOIRQ12, is routed to the ÉlanSC400 microcontroller programmable PIRQ2 pin (KBDROW9). This pin is shared with matrix keyboard row 9.

PIRQ2 is also shared via switch SW11 with the Crystal audio interface. To switch PIRQ2 to the mouse, push switch SW11 to position “C2”. To switch this signal back to the audio interface, select position “C1”. See Figure 2-25.

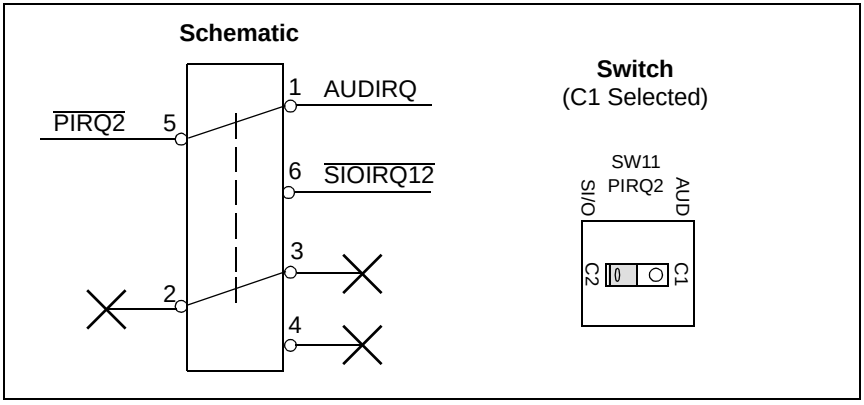


Figure 2-25. SW11 Switch

VL Bus Interface (E12)

The ÉlanSC400 microcontroller incorporates a VESA local (VL) bus operable at up to 33 MHz (3.3-V only). The bus is 32-bits wide and supports burst mode transfers. The VESA local bus shares signal lines with the LCD controller, so either a VL device or an LCD device may be operated at any one time. Locations P18 and P26 are for the VL daughter card.

Note: *A standard VESA local bus connection is not provided because the ÉlanSC400 microcontroller’s VESA local bus is not 5 V. An example 3.3-V VL-Bus VGA interface is available from AMD.*

LCD Display Interface (E12)

The ÉlanSC400 microcontroller incorporates an LCD display interface. This interface shares signals with the VL bus, so they cannot both be used at the same time.

The LCD graphics controller also cannot be used if the x32 DRAM data bus is enabled. Make sure all segments of switch SW9 are turned off. See "DRAM Main Memory (I10)" on page 2-25 for details.

The ÉlanSC400 microcontroller evaluation board kit includes an LCD interface card that plugs into connector P26 (shown at location E12 in the evaluation board layout, Figure 2-3 on page 2-4).

Before connecting any LCD display, check the display's V_{EE} supply voltage and power-up timing specification. The following paragraphs explain how to adjust these values on the evaluation board to help ensure safe and proper operation of the LCD panel.

Install a bare LCD interface card (one with no LCD panel attached) on the evaluation board; then use software to enable and power up the ÉlanSC400 microcontroller graphics controller (CSC Index DDh and Graphics Index 50h). Graphics Index 50h includes settings for power-up delays, be sure to program adequate delays for your display. See the ÉlanSC400 microcontroller documentation for information about graphics controller initialization and power management.

With LCD power enabled, adjust potentiometer VR1 on the evaluation board's power module to supply the correct voltage. You can measure V_{EE}POS on pin 1 of the LCD interface card's header. VR1 adjusts the amplitude of both V_{EE}POS and V_{EE}NEG. It is located on the underside of the power module near the mouse connector (shown at position G2–H2 in the board layout, Figure 2-3 on page 2-4).

Note: *There are two potentiometers at this location, VR1 is farthest from the corner of the module. The potentiometer on the corner of the module (VR2) adjusts V_{CC}CPU. If you accidentally change VR2, be sure to measure V_{CC}CPU (at JP27) afterwards to make sure it is still correct.*

The LCD interface card can be adapted to a variety of LCD display panels. If you will be using several different displays, you can construct custom cables that mate to the interface card's 34-pin header. See Figure 2-26. If you will use only one display, you can route the LCD wiring through the provided strain relief holes and connect directly to the solder pads on the bottom of the interface card.

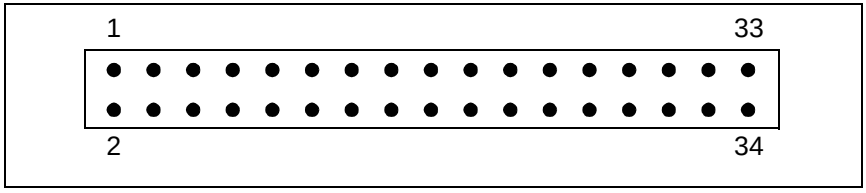


Figure 2-26. LCD Interface Card Header Pattern

Note: *The holes next to the header do not connect to any signals.You can use them for strain relief, or to mount a custom connector whose pins you can then wire to the appropriate solder pads on the header.*

Table 2-9 lists pin numbers and signal descriptions for the LCD interface card header. For more information about the ÉlanSC400 microcontroller's LCD control signals, see the ÉlanSC400 microcontroller documentation.

2.0

Table 2-9. LCD Interface Card Header Pins and Signals

Pin	Signal	Description
1	V_{EE}POS	**+10-V to +40-V Supply**. (Mirror of V_{EE}NEG) Adjust via VR1 on power module. See board layout, Figure 2-3 on page 2-4, location G2–H2.
2	CONTPOS	**Positive contrast voltage**. Adjust via VR1 *on the LCD interface card* (not on the power module).
3, 4	V_{CC}LCD5	**+5-V supply voltage for LCD.**
5, 6, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29	GND	**System ground.**
8	LCDD0	**LCD panel data bit 0**. When driving 4-bit single-scan panels, bits 3–0 form a nibble-wide LCD data interface.

Table 2-9. LCD Interface Card Header Pins and Signals (Continued)

Pin	Signal	Description
10	LCDD1	**LCD panel data bit 1**.
12	M	**LCD Panel AC Modulation** is the AC modulation signal for the LCD. AC modulation causes the LCD panel drivers to reverse polarity to prevent an internal DC bias from forming on the panel.
14	LCDD2	**LCD panel data bit 2**.
16	LC	**LCD Panel Line Clock** is activated at the start of every pixel line. Commonly referred to by LCD data sheets as CL1 or CP1.
18	LCDD3	**LCD panel data bit 3**.
20	SCK	**LCD Panel Shift Clock** is the nibble/byte strobe used by the LCD panel to latch a nibble or byte of incoming data. Commonly referred to by LCD panels as CL2 or CP2.
22	LCDD4	**LCD panel data bit 4**.
24	FRM	**LCD Panel Line Frame Start** is asserted by the microcontroller at the start of every frame to indicate to the LCD panel that the next data clocked out is intended for the start of the first scan line on the panel. Some panels refer to this signal as FLM or S (scan start up).
26	LCDD5	**LCD panel data bit 5**.
28	LCDD6	**LCD panel data bit 6**.
30	LCDD7	**LCD panel data bit 7**.
32	V_{CC}LCD3	**+3.3-V supply voltage for LCD.**
33	V_{EE}NEG	**–10-V to –40-V Supply**. (Mirror of V_{EE}POS) Adjust via VR1 on power module. See board layout, Figure 2-3 on page 2-4, location G2–H2.
34	CONTNEG	**Negative contrast voltage**. Adjust via VR2 *on the LCD interface card* (not on the power module).

2.0

IDE Hard Drive (G5–H5)

The ÉlanSC400 microcontroller evaluation board contains a standard 40-pin connection for an IDE drive at P12. The Super I/O controls the IDE hard drive on the evaluation board. For details on how to connect an IDE hard drive to the ÉlanSC400 microcontroller evaluation board, see “Board Installation” on page 1-4.

The IDE interface has a buffered data bus. The Super I/O IDE SIOIRQ14 is routed to the ÉlanSC400 microcontroller on PIRQ0.

Floppy Disk Drive (G5)

The Super I/O uses its own floppy disk controller (FDC) to support the system’s 3.5" floppy disk drive. This drive can be installed with a standard 34-pin connector.

Floppy Versus Matrix Keyboard (SW4 segment 5)

The floppy interrupt IRQ6 is routed to the ÉlanSC400 microcontroller on PIRQ6, which shares a pin with the matrix keyboard’s KBD_COL5 signal.

For matrix keyboard code development, set SW4 segment 5 (marked MKBDEN) to off. This disables the floppy IRQ from the ÉlanSC400 microcontroller’s PIRQ6, and makes KBD_COL5 available to the matrix keyboard.

While MKBDEN on SW4 is turned off, the Super I/O chip is configured to share PIRQ1 between the floppy disk and the AT keyboard. This is achieved via Super I/O pin GP1027 ($\overline{\text{MATFDEN}}$). This signal goes low when floppy disk IRQ is required, connecting SIOIRQ6 to PIRQ1 and briefly disabling AT keyboard input. When $\overline{\text{MATFDEN}}$ is High, its normal state, the AT keyboard drives PIRQ1 as usual.

Power Supply and Measurement

The ÉlanSC400 microcontroller has many different power planes for operating different parts of the system. Each of these planes derives its voltage from the power supply module. This module takes the 5 V and 12 V from a standard PC power supply and provides the following supply voltages:

- Digital voltages: 3.3 V, 5 V, and Core V_{CC} (2.7 to 3.6 V adjustable)
- LCD contrast voltages: $+V_{EE}$ and $-V_{EE}$ (10 to 40 V adjustable)
- Analog V_{CC} (3.3 V)

V_{EE} and V_{CC}CPU can be adjusted via variable resistors VR1 and VR2 on the underside of the power module. See Figure 2-3 on page 2-4 for locations.

To ensure proper functionality of the power module, the PC power supply sockets must be inserted correctly onto the board.

CAUTION: It is important that the ground wires of one connector are adjacent to the ground wires of the other. See Figure 2-27.

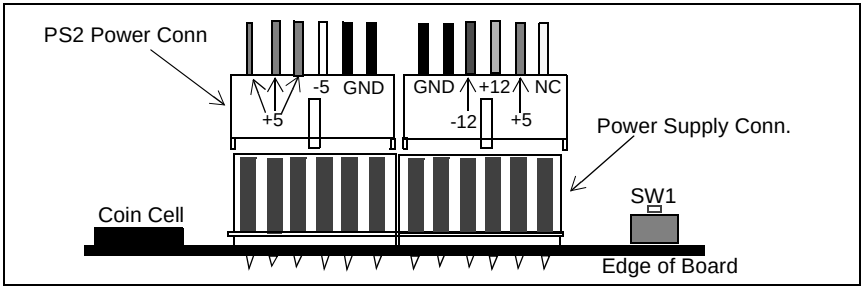


Figure 2-27. Ground Wire Connections

The evaluation board enables for measurement of current flow in separate V_{CC} planes for power budget analysis. Table 2-10 and Table 2-11, beginning on page 2-51, summarize the connections to the V_{CC} jumpers.

Note: *To test current, first be sure to turn off system power; then remove the jumper to test and connect a current meter in its place before powering up. Otherwise the system will not work.*

Table 2-10. Power Measurement Connectors: Controller Power Planes

Part	Signal	Description	Reference in Figure 2-3 on page 2-4
JP27	V_{CC}CPU	ÉlanSC400 microcontroller CPU V_{CC}. Enables current measurement for ÉlanSC400 microcontroller CPU power pins (2.7–3.6-V DC).	E8
JP28	AV_{CC}	ÉlanSC400 microcontroller Analog V_{CC}. Enables current measurement for ÉlanSC400 microcontroller analog power plane driving internal PLLs and oscillator circuit.	D8–E8
JP29	V_{CC}RTC	ÉlanSC400 microcontroller RTC V_{CC}. Enables current measurement for ÉlanSC400 microcontroller RTC power plane driven by 3.3-V AV_{CC} or 3-V cell.	D9
JP30	V_{CC}	ÉlanSC400 microcontroller V_{CC}. Enables current measurement for ÉlanSC400 microcontroller core power pins (3.3-V DC).	E10–F10
JP31	V_{CC}MEM	ÉlanSC400 microcontroller memory interface V_{CC}. Enables current measurement for ÉlanSC400 microcontroller memory interface power pins (3.3-V DC).	F9–G9
JP32	V_{CC}BUS	ÉlanSC400 microcontroller Bus V_{CC}. Enables current measurement for ÉlanSC400 microcontroller SD bus power pins (3.3-V DC).	F8
JP33	V_{CC}LCD	ÉlanSC400 microcontroller LCD V_{CC}. Enables current measurement for ÉlanSC400 microcontroller LCD and VESA local bus power pins (3.3-V DC).	F10
JP34	V_{CC}PCM	ÉlanSC400 microcontroller PC Card V_{CC}. Enables current measurement for ÉlanSC400 microcontroller PC Card Socket A and socket B interface power pins (3.3-V DC).	E8
JP35	V_{CC}SER	ÉlanSC400 microcontroller serial port V_{CC}. Enables current measurement for ÉlanSC400 microcontroller serial port power pins (3.3-V DC).	D9–E9

Table 2-11. Power Measurement Connectors: System Power Planes

Part	Signal	Description	Reference in Figure 2-3 on page 2-4
JP46	V_{CC}PCMA5	Used to measure current in 5-V V_{CC} PC Card Socket A system power plane.	A3–A4
JP47	V_{PP}PCMA	Used to measure current in 12-V V_{PP} PC Card Socket A system power plane.	A4
JP48	V_{CC}PCMB5	Used to measure current in 5-V V_{CC} PC Card Socket B system power plane.	A6
JP49	V_{PP}PCMB	Used to measure current in 12-V V_{PP} PC Card Socket B system power plane.	A6
JP50	V_{CC}DRAM3	DRAM V_{CC}. Enables user to measure current being used by the DRAM (3.3-V DC). Two jumpers are needed to support the maximum load (3.84 A).	G8–H8
JP51	V_{CC}SER3	System serial port V_{CC}. Enables current measurement for system serial port power plane (3.3-V DC).	D2–E2
JP52	V_{CC}ROM5	ROM V_{CC}. Enables current measurement for ROM system power plane (5-V).	C9
JP53	V_{CC}ISA5	System ISA V_{CC}. Enables current measurement for ISA system power plane (5-V). Two jumpers are needed to support the maximum load (~5 A).	F2–G2
JP64	V_{CC}SYS	ÉlanSC400 microcontroller ISA V_{CC}. Enables current measurement for microcontroller ISA bus power pins (3.3-V DC).	E10

Power Management

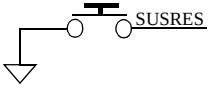
The ÉlanSC400 microcontroller offers unparalleled power management in its class. In addition to low operating current, seven power management modes are available: Hyper Speed, High Speed, Low Speed, Standby, Temporary Low Speed, Suspend, and Critical Suspend. Refer to the *Élan™SC400 and ÉlanSC410 Microcontrollers User's Manual*, order #21030, for an in-depth discussion of these modes.

Table 2-12 and the following sections describe evaluation board features for testing power management.

Table 2-12. Power Management Connectors

Part	Signal	Description	Reference in Figure 2-3
SW4	ACIN, $\overline{BL2}$–$\overline{BL0}$	Switches for testing ÉlanSC400 microcontroller power management	F3–G4
SW8	SUSRES	Used to force ÉlanSC400 microcontroller to suspend mode and to resume.	A7–B8

Suspend/Resume (SW8)



SW8 is a push-button, normally open switch. Pressing this button grounds the ÉlanSC400 microcontroller SUSRES pin, which can be configured to control the microcontroller's Suspend mode.

The ÉlanSC400 microcontroller evaluation board BIOS configures SUSRES (via CSC Index 50h) to let you toggle between the High Speed and Suspend modes. If you press the Suspend/Resume button after the system has powered up, the system will enter the Suspend mode. If you press the Suspend/Resume button again, the system will return to High Speed mode.

ACIN and Battery Low Detects (SW4)

The ÉlanSC400 microcontroller has several inputs that are used by the PMU to efficiently adjust the power level within the microprocessor. Segments 1–4 of switch SW4 allow you to control these signals. See Figure 2-28 and the following sections.

ACIN (SW4 Segment 1)

ACIN (active High) can be used to indicate that the system is connected to a permanent AC power source. Software can configure the ACIN signal so that, when asserted, it effectively disables the High-Speed mode timer. This forces the system to remain in High or Hyper Speed modes constantly unless the Suspend mode is activated. You can test software that uses ACIN by switching segment 1 of switch SW4 to the off position, which asserts it to High. (3.3 V indicates assertion for this signal.)

$\overline{BL0}$–$\overline{BL2}$ (SW4 Segments 2–4)

The $\overline{BL0}$–$\overline{BL2}$ (active Low) signals can be used to indicate low-battery voltage conditions of various degrees. Software can configure the PMU to monitor these signals and, when it detects a low-battery condition, force the system to a lower power mode if no AC source is detected. You can test software that uses these signals by switching segments 2–4 of SW4 for $\overline{BL}$(0:2), respectively, to the on position, which asserts them to Low. (0 V indicates assertion for these signals.)

2.0

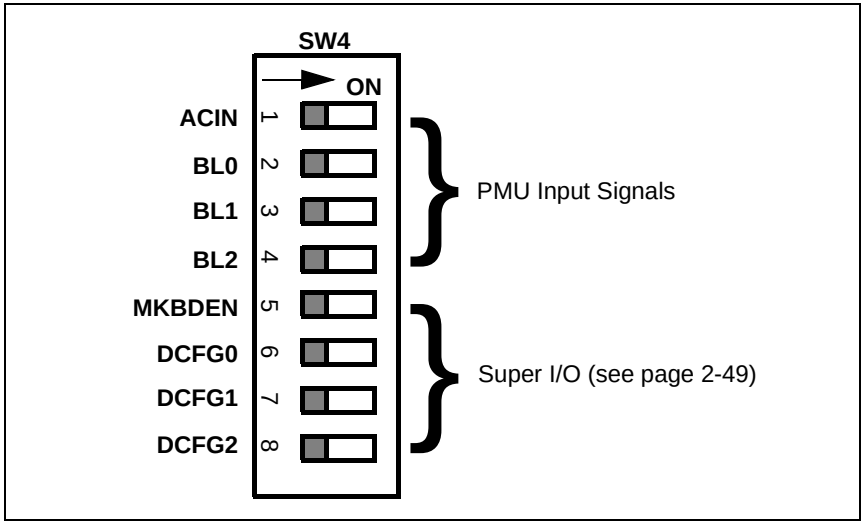


Figure 2-28. Diagnostics Switch (SW4)

Miscellaneous

The following tables and figures describe miscellaneous features of the ÉlanSC400 microcontroller evaluation board.

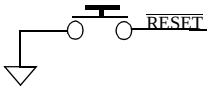
Table 2-13. Ground Connectors

Part	Signal	Description	Reference in Figure 2-3 on page 2-4
JP54	GND	Ground post.	G8
JP55	GND	Ground post.	F5
JP56	GND	Ground post.	I5
JP57	GND	Ground post.	J2
JP58	GND	Ground post.	D2–E2
JP59	GND	Ground post.	A1
JP60	GND	Ground post.	B7
JP61	GND	Ground post.	J13
JP63	GND	Ground post.	B9

Table 2-14. Miscellaneous Connectors

Part	Signal	Description	Reference in Figure 2-3 on page 2-4
SW7	RESET	Used to reset (reboot) the system.	A7–A8

Reset (SW7)



SW7 is a push-button, normally open switch. Pressing this button grounds the ÉlanSC400 microcontroller $\overline{\text{RESET}}$ signal and resets the board to default settings.

Chapter 3

Product Support

This chapter provides information on reaching and using the AMD Corporate Applications technical support services, product information and literature available through AMD's World Wide Web and FTP sites, and support tools for the E86 family.

2.0

AMD Corporate Applications Technical Support Services

Technical support for the E86 family of microcontrollers and corresponding support products is available via e-mail, online (BBS and WWW), or through telephone or fax. For non-technical support, see “Product Support” on page 3-4.

E-Mail Support

Please include your name, company, telephone number, AMD product requiring technical support, and question or problem in all e-mail correspondence.

In the USA and Canada, send mail to:

`lpd.support@amd.com`

In Europe and the UK, send mail to:

`euro.tech@amd.com`

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Online Support

AMD offers technical support on our WWW site, and through our bulletin board services. See “Product Support” on page 3-4 for more on what our WWW and FTP sites have to offer.

WWW Technical Support

Got to AMD’s home page at **http://www.amd.com** and click on “Support” for the latest AMD technical support phone numbers, software, and Frequently Asked Questions.

Bulletin Board Support

Country	Number
UK and Europe	44-(0) 1276-803-211

Telephone and Fax Support

Telephone assistance is available in the U.S. from 8:00 A.M. to 5:00 P.M. Pacific time, Monday through Friday (except major holidays). In Europe, assistance is available during U.K. business hours. Contact the hotlines at one of the following telephone or fax numbers.

Direct Dial Numbers

Country	Number
USA and Canada	Tel.: (408) 749-5703 Fax: (408) 749-4753
Far East Asia	Fax: (852) 2956-0599
Germany	Tel.: 089 4505 3199
Japan	Tel.: (03) 3346-7550 Fax: (03) 3346-9828
UK and Europe	Tel.: 44-(0) 1276-803-299 Fax: 44-(0) 1276-803-298

Toll-Free Numbers

Country	Number
USA and Canada	Tel.: (800) 222-9323
France	Tel.: 0800-908-621
Italy	Tel.: 1678-77224
Japan	Tel.: 0031-11-1163

Product Support

AMD's WWW and FTP sites are described below. Questions, requests, and input concerning these sites can be sent via E-mail to **webmaster@amd.com**.

In addition, AMD's literature support and third-party development support products are described.

WWW Site

A subset of the AMD WWW pages, the Embedded Processor section is frequently updated and includes general product information, as well as technical documents such as data sheets, application notes, and technical bulletins. To access these files, go to the AMD home page at **http://www.amd.com** and click on "Embedded Processors."

The "Embedded Processors" page is divided into six sections:

- "What's New" lists new products and new contents.
- "Product Overviews" briefly describes all the microprocessors and microcontrollers in the E86 family.
- "Technical Documentation" provides the *Available Literature List* of datasheets, application notes, user's manuals, and promotional literature, and describes how to order these documents. Many are also available online in PDF form. (For details on accessing the Literature Ordering Center, see "Literature Support" on page 3-5.)
- "Support & Tools" provides information about the tools that support our processors, and lists contact information for technical and sales support.

FTP Site

In addition to the documentation on our WWW pages, AMD provides software through an anonymous FTP site. To download the software, ftp to **ftp.amd.com** and log on as "anonymous" using your e-mail address as a password. Or via your web browser, go to **ftp://ftp.amd.com**. Software relating to the E86 family can be found in the **/pub/epd/e86/** directory.

Literature Support

Documentation can be ordered by phone or e-mail.

Telephone

Country	Number
USA and Canada	Toll-free: (800) 222-9323 Direct: (512) 602-5651
Far East Asia	Fax: (852) 2956-0588
France	Toll-free: 0800-908-621
Germany	Direct: 089 4505 3199
Italy	Toll-free: 1678-77224
Japan	Direct: (03) 3346-7550
UK and Europe	Direct: 44-(0) 1276-803-299

E-Mail

2.0

Please include your name, company, telephone number, and complete mailing address with your literature request.

In the USA and Canada, send mail to:

`AMDlit@gomez.amd.com`

In Europe and the UK, send mail to:

`euro.lit@amd.com`

Third-Party Development Support Products

The FusionE86^{SM} Program of Partnerships for Application Solutions provides the customer with an array of products designed to meet critical time-to-market needs. Products and solutions available from the AMD FusionE86 partners include emulators, hardware and software debuggers, board-level products, and software development tools, among others. The *FusionE86^{SM} Catalog*, order #19255, and the *FusionE86^{SM} CD-ROM*, order #21058, describe these solutions.

In addition, mature development tools and applications for the x86 platform are widely available in the general marketplace.

Appendix A

Evaluation Board Default Settings

This chapter lists the default settings of the ÉlanSC400 microcontroller evaluation board when it is shipped.

2.0

Table A-1. Microcontroller Power Plane Jumpers Default Settings

Location	Pins Set	Signal
JP27	1–2	V_{CC}CPU
JP28	1–2	AV_{CC}
JP29	1–2	V_{CC}RTC
JP30	1–2	V_{CC}
JP31	1–2	V_{CC}MEM
JP32	1–2	V_{CC}BUS
JP33	1–2	V_{CC}LCD
JP34	1–2	V_{CC}PCM
JP35	1–2	V_{CC}SER
JP64	1–2	V_{CC}SYS

Table A-2. System Power Plane Jumpers Default Settings

2.0

Location	Pins Set	Signal
JP46	1–2	V_{CC}PCMA5
JP47	1–2	V_{PP}PCMA
JP48	1–2	V_{CC}PCMB5
JP49	1–2	V_{PP}PCMB
JP50	1–2, 3–4	V_{CC}DRAM3
JP51	1–2	V_{CC}SER3
JP52	1–2	V_{CC}ROM5
JP53	1–2, 3–4	V_{CC}ISA5

Table A-3. Miscellaneous Jumpers Default Settings

Location	Pins Set	Function
JP22	NP	Selects PIRQ5
JP26	NP	Selects PIRQ4
JP41	NP	Selects $\overline{\text{PDACK1}}$
JP42	NP	Selects $\overline{\text{PDACK0}}$
JP43	NP	Selects PDRQ0
JP44	NP	Selects PDRQ1
JP45	3–4	Enables PC card socket B

Notes:

An NP indicates that the jumper is not populated.

Table A-4. ROM Device Jumpers Default Settings

Location	Pins Set	Function
JP36	2–3	Routes $\overline{\text{ROMCS0}}$ to DIP Socket
JP37	1–2	Routes $\overline{\text{ROMCS1}}$ to Flash memory x16-1
JP38	1–2	Routes $\overline{\text{ROMCS2}}$ to Flash memory x16-2
JP39	1–2	Selects devices in DIP socket as Flash memory
JP40	1–2	Selects device in DIP socket as Flash memory/EPROM

Table A-5. Switch Default Settings

Switch Segment	Setting	Function
SW3-1	Off	CFG0 = 0: x8 or x16 boot ROM
SW3-2	Off	CFG1 = 0: x8 boot ROM
SW3-3	Off	CFG2 = 0: Boot on $\overline{\text{ROMCS0}}$
SW4-1	Off	Sets ACIN active
SW4-2	Off	Sets $\overline{\text{BL0}}$ inactive
SW4-3	Off	Sets $\overline{\text{BL1}}$ inactive
SW4-4	Off	Sets $\overline{\text{BL2}}$ inactive
SW4-5	On	Disables matrix keyboard
SW4-6	On	Sets DIAG CFG0 to 0
SW4-7	On	Sets DIAG CFG1 to 0
SW4-8	On	Sets DIAG CFG2 to 0
SW5	C2	Enables AT keyboard
SW6	C1	Routes programmable DMA channel 0 to Super I/O
SW9-1	On	Enables $\overline{\text{CASL2}}$ to DRAM
SW9-2	On	Enables $\overline{\text{CASL3}}$ to DRAM
SW9-3	On	Enables $\overline{\text{CASH2}}$ to DRAM
SW9-4	On	Enables $\overline{\text{CASH3}}$ to DRAM
SW9-5	On	Enables $\overline{\text{RAS2}}$ to DRAM
SW9-6	On	Enables $\overline{\text{RAS3}}$ to DRAM
SW9-7	On	Enables MA12 to DRAM
SW10	C1	Routes programmable DMA channel 0 to audio
SW11	C1	Routes programmable IRQ2 to Super I/O

2.0

Appendix B

Verified Peripherals

This a list of peripherals that have been verified to work on the ÉlanSC400 microcontroller evaluation board.

Table B-1. Verified Peripherals

Peripheral	Manufacturer	Model #
Floppy Drive	TEAC	FD-235HF
Hard Drive	Maxtor	7541A
	Quantum	ProDrive LPS series
	Western Digital	Caviar series
Power Supply	Senstron	SQH-4154
	Likom	PSA-2054C
AT Keyboard	Chicony	KB-5911
AT/XT Keyboard	Keytronic	EO3600QL-C
Matrix Keyboard	Fujitsu	#N860-1406-T001
VGA Monitor	CTX	6439
	Mitsubishi	15FS
	NEC MultiSync	3D
	NEC MultiSync	5FGE
Video Card	Trident	TVGA 9000I
PCMCIA	SunDisk ATA	
	AMD	D Series Flash cards
	Various SRAM cards	

2.0

Appendix C

Board Layout Suggestions

The following suggestions concern the ÉlanSC400 microcontroller evaluation board layout strategy for the 32-kHz oscillator, the PLLs, and the power supplies. The goal is to minimize noise and noise coupling associated with the way the board is laid out. Special care is needed to minimize board leakages which can be fatal to pins that are sensitive to leakage currents, such as the two crystal oscillator pins, XTAl1 and XTAL2.

32-kHz Oscillator

Prudent board layout for the 32-kHz oscillator suggests the following precautions:

- The crystal capacitor locations on the evaluation board are not populated and not necessary in a finished design. They were included for testing purposes only.
- Route the area around the oscillator by hand.
- Keep the two traces, XTAL1 and XTAL2, as short as possible.
- Keep all noisy signals (e.g., PLL filters and other clocking signals) as far away from XTAL1 and XTAL2 as possible. XTAL1 is much more sensitive to noise coupling than XTAL2.
- Minimize parasitic capacitance between XTAL1 and XTAL2; even a few picofarads can potentially cause the oscillation frequency to be off target.

Phase-Locked Loops

Board layout considerations for the four PLLs suggest the following precautions:

- The loop filter signals are all close to one corner of the chip. Place the loop filter components as close as possible to this corner.
- Route the area around the loop filters first, and by hand. Keep the traces as short as possible and keep them as far away as possible from each other and from other clocking signals.
- As with the oscillator, keep all noisy signals as far away as possible, even on the inner layers.

- For additional protection, put an Analog V_{CC} power plane directly under the loop filter circuit.
- See the microcontroller data sheet for loop filter component recommendations. C2 in the PLL circuit filters high-frequency noise. (See Figure C-1.) The C1 and R values adjust lock time and jitter. Larger RC values reduce jitter in the PLL but increase lock time (the time required for the loop filter voltage to stabilize after reset). As RC values get larger, the LF voltage will tend to remain unstable long after reset.

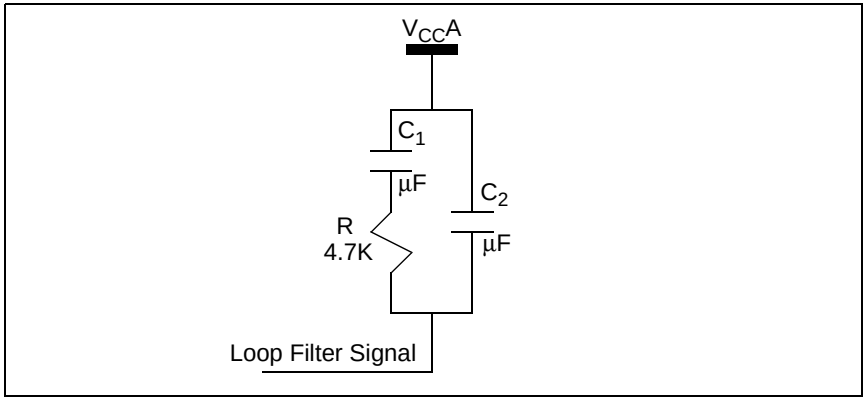


Figure C-1.PLL Schematic

Power Supplies

Board layout considerations for the power supplies suggest the following precautions:

- Bring the analog V_{CC} and digital V_{CC} on separate conductors from the output of the voltage regulator to the ÉlanSC400 microcontroller. If you use traces instead of power planes, make sure they are thick and wide.
- Filter the analog V_{CC} with an RLC second-order low-pass filter (e.g., R= 10 Ω, L=47 µH, C=33 µF).
- Since the digital V_{CC} carries much more current than the analog V_{CC}, a second order LC low-pass filter should be used instead (i.e., the series resistor should be removed).
- A small capacitor in the order of a few nanofarads can be added in parallel to the large filter capacitor to suppress high-frequency noise.
- Isolate the analog ground plane from the digital ground plane on the board, and connect them after decoupling.

Appendix D

Bill of Materials and Schematics

The bill of materials for the ÉlanSC400 microcontroller evaluation board begins on page D-2.

The actual schematics used to build the ÉlanSC400 microcontroller evaluation board begin on page D-8.

2.0

Board Bill of Materials (BOM)

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM

Item	Quantity	Reference	Part	Package	Description
1	1	BT1	3.0 COIN CELL	TH	Keystone 103 or 106
2	9	C1,C5,C10,C14,C18,C22, C26,C30,C48,C212	0.001 uF	805	
3	11	C2,C6,C11,C15,C19,C23, C27,C31,C44,C208,C209, C213	0.01 uF	805	
4	105	C3,C7,C9,C12,C16,C20,C24, C28,C32,C34,C35,C36,C37,C 49,C62,C63,C64,C65,C66,C67 ,C68,C69,C70,C71,C72,C73,C 74,C75,C76,C77,C78,C79,C80 ,C81,C82,C83,C84,C85,C86,C 87,C88,C89,C90,C91,C93,C95 ,C96,C97,C98,C99,C100,C101 ,C102,C103,C104,C105,C106, C107,C108,C109,C110,C111, C112,C113,C114,C115,C116,C 117,C118,C119,C120,C121,C1 22,C130, C131,C132,C133,C134,C135, C136,C156,C167,C171,C174, C175,C176,C177,C178,C179, C180,C182,C185,C186,C187, C188,C189,C190,C194,C195, C202,C203,C206,C207,C210, C211,C214	0.1 uF	805	
5	2	C4,C13	33 uF	DCASE, 16 V	
6	34	C8,C40,C126,C127,C128,C12 9,C139,C140,C141,C142, C145,C146,C147,C148,C149, C150,C151,C152,C153,C154, C157,C158,C159,C160,C161, C162,C165,C168,C169,C172, C181,C192,C198,C201	10 uF	CCASE, 16 V	

Notes:

An asterisk (*) indicates parts that are not populated.

2.0

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM (Continued)

Item	Quantity	Reference	Part	Package	Description
7	11	C17,C21,C25,C29,C33,C123, C124,C125,C137,C138,C193, C215	1 uF	A CASE, 16 V	
8	2	C38,C39	*CAP NP	805	
9	1	C41	330 pF	805	
10	2	C42,C43	470 pF	805	
11	1	C45	15 pF	805	
12	1	C46	33 pF	805	
13	3	C47,C183,C184	22pf	805	
14	14	C50,C51,C52,C53,C54,C55,C 56,C57,C58,C59,C60,C61, C199,C200	0.33 uF	805	
15	2	C94,C92	6.8 uF	A CASE, 10 V	
16	6	C155,C163,C164,C166,C170, C173	4.7 uF	C CASE, 16 V	
17	2	C143,C144	4.7 uF	E CASE, 50 V	
18	2	C191,C204	2700 pF	805	
19	2	C197,C196	1000 pF	805	
20	1	C205	1.0 uF	1206	
21	1	D1	BAT54C	SOT-23	PHILLIPS BAT54C
22	1	D2	BAT54	SOT-23	PHILLIPS BAT54
23	2	JP26,JP22	HEADER 11X2	TH	
24	16	JP27,JP28,JP29,JP30,JP31,JP3 2,JP33,JP34,JP35,P42, JP46,JP47,JP48,JP49,JP51, JP52,JP64	HEADER 2	TH	
25	5	JP36,JP37,JP38,JP40,P41	HEADER 3	TH	
26	1	JP39	HEADER 3X2	TH	
27	4	JP41,JP42,JP43,JP44	HEADER 7X2	TH	
28	3	JP45,JP50,JP53	HEADER 2X2	TH	
29	10	JP54,JP55,JP56,JP57,JP58,JP5 9,JP60,JP61,JP62,JP63	HEADER 1	TH	

Notes:

An asterisk (*) indicates parts that are not populated.

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM (Continued)

Item	Quantity	Reference	Part	Package	Description
30	1	LS1	SPEAKER	TH	ISL-8032VT
31	3	L1,L2,L3	INDUCTOR	1206	TDK CB70-1206
32	2	P1,P2	PC POWER CONN	TH	Burndy GTC6R-1
33	2	P4,P7	COND26	TH	AMP 1-534206-3
34	4	P5,P8,P9,P10	72-PIN SIMM	TH	Molex 15-82-0762
35	1	P6	KYBD CONN	TH	AMP 212044-1
36	1	P11	MOUSE CONN.	TH	AMP 750329-2
37	1	P12	IDE CONN 40	TH-40	SHRD HEADER 2X20
38	1	P14	FDD CONN.	TH-34	SHRD HEADER 2X17
39	6	P16,P17,P20,P21,P24,P25	HP CONN	TH-2x10-SHRD	3M:2520-6003UB
40	4	P18,P26,P39,P40	COND50	SMT-2x25	AMP 104652-5
41	3	P23,P47,P48	SERIAL PORT	TH	AMP 745410-1
42	2	P31,P32	ADA CONN	TH-2x25-SHRD	
43	2	P33,P34	ISA AT CONN	TH	AMP 645169-3
44	1	P35	HEADER 5X2	TH	
45	1	P37	CON7	TH-7	Molex 5597 39-51-3074
46	1	P38	CON14	TH-14	Molex 5597 39-51-3144
47	2	P43,P44	PCMCIA CONN.	TH	AMP 535653-1
48	1	P45	PARALLEL PORT	TH	AMP 745967-7
49	1	P46	*HEADER 2	TH	
50	2	RS2,RS1	RSHORT		
51	2	R1,R2	10	805	
52	4	R86,R87,R89,R90	10	1206	
53	5	R3,R14,R20,R73,R173	0	805	

Notes:

An asterisk (*) indicates parts that are not populated.

2.0

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM (Continued)

Item	Quantity	Reference	Part	Package	Description
54	66	R4,R5,R6,R7,R21,R22,R23,R24,R25,R50,R51,R57,R58, R59,R60,R61,R62,R63,R64, R65,R66,R67,R70,R71,R74, R78,R79,R110,R111,R133, R134,R135,R136,R137,R138, R139,R142,R143,R145,R146, R147,R148,R149,R150,R151, R152,R162,R163,R164,R165, R166,R167,R168,R169,R170, R171,R176,R177,R178,R183, R185,R187,R188,R189,R190, R191	10K	805	
55	4	R8,R9,R10,R11	330	805	
56	1	R12	150K	805	
57	4	R13,R19,R140,R182	100K	805	
58	11	R15,R16,R17,R18,R123,R124, R125,R126,R129,R130, R179	4.7K	805	
59	3	R26,R72,R75	*0	805	
60	46	R27,R28,R29,R30,R31,R32,R33,R34,R35,R36,R37,R38, R39,R40,R41,R42,R43,R44, R45,R46,R47,R48,R49,R53, R54,R55,R56,R76,R77,R80, R81,R82,R83,R84,R113, R114,R115,R116,R117,R118, R119,R120,R121,R122,R131, R132	1M	805	
61	19	R52,R68,R95,R96,R101,R102, R103,R104,R105,R106, R107,R108,R109,R153,R154, R155,R158,R159,R160	1K	805	
62	2	R85,R88	47	1206	
63	4	R91,R92,R93,R94	*4.7K	805	
64	5	R97,R98,R99,R100,R144	*10K	805	
65	1	R112	220	805	
66	3	R127,R141,R180	2.2K	805	

Notes:

An asterisk (*) indicates parts that are not populated.

2.0

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM (Continued)

Item	Quantity	Reference	Part	Package	Description
67	1	R128	100	805	
68	2	R156,R157	*1K	805	
69	1	R161	3.3K	805	
70	1	R175	47K	805	
71	1	R181	6.8K	805	
72	2	R186,R184	22K	805	
73	1	SP1	*SPARE20	SOIC-20	
74	1	SP2	*SPARE14	SOIC-14	
75	3	SW1,SW7,SW8	PBNO	SMT	C&K KT11P2SM
76	1	SW3	SW DIP-4	TH	C&K BD04
77	2	SW9,SW4	SW DIP-8	TH	C&K BD08
78	4	SW5,SW6,SW10,SW11	SW DPDT	TH	Grayhill 76SD01
79	24	S1,S2,S3,S4,S5,S6,S7,S8,S9,S10,S11,S12,S13,S14,S15,S16,S17,S18,S19,S20,S21,S22,S23,S24	SHORT		
80	16	TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP12,TP13,TP14,TP15,TP16	TESTPT		
81	1	U6	Super I/O	PQFP-160	National PC87306VUL
82	2	U7,U8	74ACT245	SOIC-20	
83	7	U9,U12,U13,U19,U34,U43,U49	74ACT244	SOIC-20	
84	1	U11	74ALVC164245	SSOP-48	TI SN74ALVC164245 DLR
85	1	U14	E4_292	BGA-292	AMD ElanSC400
86	1	U17	LTC1327	SSOP-28	RS232-3V
87	6	U22,U23,U37,U38,U39,U40	29F016	TSOP-48	AM29F016EC
88	1	U24	29F040	32 DIP Socket	AM29F040PC
89	1	U29	PALCE20V8H-7PC	24 DIP Socket	AMD PALCE20V8H-7PC

Notes:

An asterisk (*) indicates parts that are not populated.

Table D-1. ÉlanSC400 Microcontroller Evaluation Board BOM (Continued)

Item	Quantity	Reference	Part	Package	Description
90	4	U30,U31,U32,U33	Hex Display	TH	TI -TIL311
91	1	U36	74ACT04	SOIC-14	
92	1	U41	74ACT32	SOIC-14	
93	1	U42	74ACT08	SOIC-14	
94	2	U44,U45	TFDS6000	SMT	Temic TFDS6000 "D"
95	2	U46,U53	TC7SH32FU	SSOP5-P-A	Toshiba
96	1	U47	74ACT373	SOIC-20	
97	1	U48	74ACT02	SOIC-14	
98	2	U50,U51	LTC1349	SSOP-28	RS232-5V
99	1	U52	74ACT125	SOIC-14	
100	1	U54	Pcmcia Pwr	SSOP-28	MIC2563A-1
101	1	U55	74ACT240	SOIC-20	
102	1	U56	LTC1478	SOIC-16	LINEAR TECH
103	1	U57	CS 4236B	TQFP-100	Crystal 4236B-KQ
104	1	U58	LTC1477	SOIC-8	LINEAR TECH
105	1	U60	LM4861M	SOIC-8	National Semiconductor
106	1	X1	32.768 KHz CRYSTAL	SMT	Ecliptek ECPSM29T
107	1	X2	MICROPHONE	TH-2	Panasonic WM-54BT
108	1	Y1	24MHz OSC	SMT	Ecliptek 23EC2500ETT-24MHz-G
109	1	Y2	8.00MHz OSC	SMT	Ecliptek 23EC2500ETT-8.0MHz-G
110	1	Y3	14.318MHz OSC	SMT	Ecliptek 23EC2500ETT-14.318MHz-G
111	1	Y4	16.93440Mhz	SMT	Cal Crystal CCL-SM3B14F

Notes:

An asterisk (*) indicates parts that are not populated.

Schematics

The schematics that follow are the actual CAD schematics used to build the ÉlanSC400 microcontroller evaluation board. These schematics are useful for understanding and modifying the evaluation board. Since the evaluation board incorporates many different possible configurations for the ÉlanSC400 microcontroller, these schematics are not a good place to start for actual ÉlanSC400 microcontroller-based designs.

ElanSC400 Verification Board Schematics

Table of Contents

Rev 1.0: Original design

Rev 1.1:
Sh. 11: Corrected CAD for ISA Bus connector.

Rev 2.0:
Sh.2: Added 0.01uF & 0.001uF caps to ElanSC400 power planes.
Added pads to bottom of board for caps near SC400 socket.
Sh.3: Removed VCC5 from analyzer headers.
Removed RESET# from analyzer header P19.
Added GND to NI-1 & NI-2 connectors.
Added RESET# to NI-2 connector.
Sh.4: Changed SW5 & SW6 from an Omron B3S1000 to a C&K KT11P2SM.
Changed LFx circuit from a one component to three component design.
Added GND to P27 for RESET#.
Sh.6: Added VL device VDD & VEE controls to P20.
Added VCC5 to P23.
Sh.7: Changed RS1-RS7 to sets of 0 ohm resistors.
Sh.8: Changed pull-ups on BIOSCS#, DIAGCS#, & X16CS# from VCCROM5 to VCC3.
Sh.9: Added ROMID2 to P42.
Sh.10: Added KBDROW10 (BALE) to buffer U24.
Sh.11: Added buffered ISABALE to ISA connector P34 & P35.
Changed SA20-25 on U9 to buffered BSA20-25.
Changed pull-ups on IOCHRDY, KBDROW12 (MCS16#), & IOCS16# from VCCISA5 to VCC3.
Sh.12: Changed VCC for U22 from VCCISA5 to VCC3.
Changed pull-ups on PCMCIA card detects for slot A & slot B from VCCISA5 to VCC3.
Sh.13: Added work-around for SC400 IrDA errata to invert TXD & RXD.
Sh.14: Changed pull-ups on PPOEN# & PPWE# from VCCISA5 to VCC3.
Added pull-ups to VCC3 on STRB#, AFDT#, INIT#, & SLCTIN#.
Sh.15: Added ROMID2 to U10.
Sh.18: Changed P12 from an AMP right angle 749265-1 to an AMP vertical 750329-2.
Added circuit to translate 5 volt input to the SC400 to 3.3 volts.
Sh.19: Changed circuit for PSLVEE to support VL-bus devices also.
Sh.20: Changed position & pinout of P6 & P7 for power supply module.
Added circuit for support of an external back-up battery.
Added bulk caps for P5VOLT, P12VOLT, VCCCPU, VCCANLG3, VEEPOS, & VEENEG.

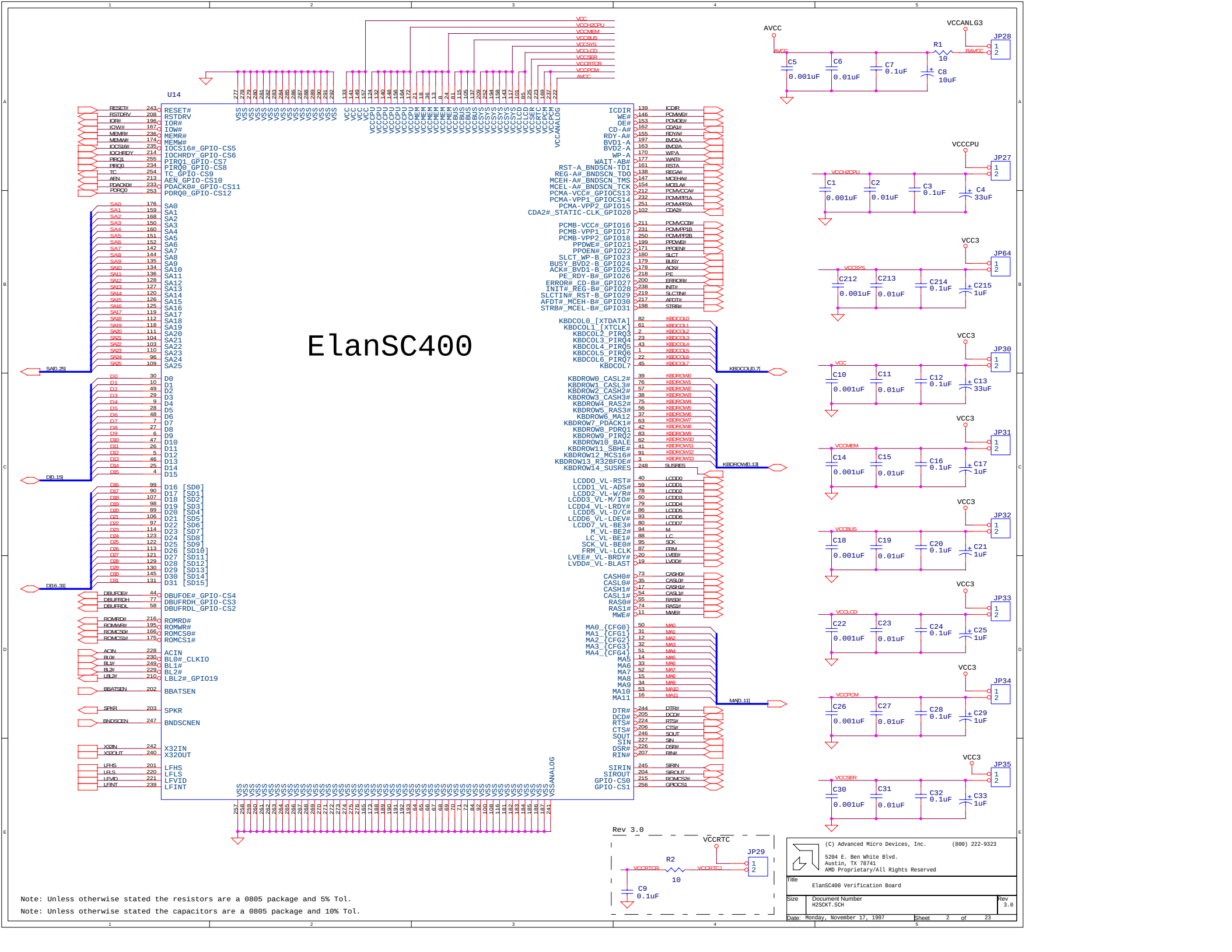
Rev 3.0:
Sh.2: Removed cap C87 from VCCH2CPU and cap C92 from AVCC.
Removed 1.2uH and 47uH inductosr from VCCCPU and VCCANLG3 respectively.
Removed off page connector from VCCRTC3.
Added JP24 and respective circuity.
Renamed SDA and SCL to ROMCS2# and GPIOCS1 respectively and removed SDA and SCL from pin name.
Add VCC current jumper JP23, .1uF cap, and 10 ohm resistor to VCCRTC.
Sh.3: Removed header JP22.
Added CLK8MHz signal to conn P19.
Added BNDSCEN signal to header P38.
Connected IOR#, IOW#, MEMR#, and MEMW# to conns P36, P25, P8, and P16 respectively.
Sh.4: Removed buzzer circuit.
Removed header P28.
Replaced 510pF, .01uF, and .22uF caps with 470pF, .001uF, and .01uF caps respectively.
Sh.5: Removed 0 ohm resistors R41 - R46.
Sh.7: Removed S12 and changed VCCISA5 to VCCSUSP.
Removed 10K resistors R103, R104, R125, and R126.
Replaced two HD151015 buffers with one 74ALVC164245 buffer.
Replaced zero value resistors with 8-dip switch.
Added two 244 buffers.

Rev 3.0: Cont.
Sh.8: Removed header JP36.
Removed ROM-2.
Removed DIAGCS# signal from headers.
Replaced JP31-JP33 3 X 2 headers with 3 X 1 headers.
Changed App Flash names to X16-0, -1, -2.
Changed ROM-1 name to DIP.
Added off page connector to X16CS# signals.
Sh.9: Added four 29F016 flash chips.
Added off page connectors for X16CS# signals.
Sh.11: Removed short shape S25 and S26 from VCCISA5.
Renamed 8MHz and 14MHz signals to CLK8MHz and CLK14MHz
Sh.12: Added a 244 buffer.
Sh.13: Removed IrDA tranceivers and circuity.
Added TFDS6000 tranceivers and circuity from SC450 IrDA port design.
Sh.15: Removed short shape S7 from VCCISA5.
Sh.16: Removed header JP3 and plug P4 from P12Volt and VCCISA5.
Removed IDE & FDD power conn.
Sh.18: Removed diode D5 and 1K resistor from 74ACT125 and added TC7SH32FU.
Added 2.2K and 100 ohm resistor, .1uF cap, and a switch
between RSIDRV off page connector and P5 KYBD CONN.
Sh.20: Removed header P3 and diodes D3 and D2.
Removed power on LED and R26.
Moved VCC current jumper circuit to H2SCKT.SCH page.
Sh.21: Removed all verification testing pullups.
Added spare 04 inverter to VCCISA5.
Sh.22: Added audio driver with respective circuity for audio capability to the board.
Sh.23: Added microphone, and speaker with respective circuity for audio capability.

Title: ElanSC400 Verification Board

Size	Document Number	Rev
	H2.SCH	3.0

Date: Wednesday, September 10, 1997 Sheet 1 of 23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VCCSYS
VCCLCD
VCCSER
VCCRTCR
VCCPCM
AVCC
VCCANLG3
JP28
R1
10
C5
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C6
0.01uF
C7
0.1uF
C8
10uF
VCCCPU
JP27
C1
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C2
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C4
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JP35
C30
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KBDROW[0..13]
MA[0..11]
Rev 3.0
VCCRTC
JP29
R2
10
C9
0.1uF
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.
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Austin, TX 78741
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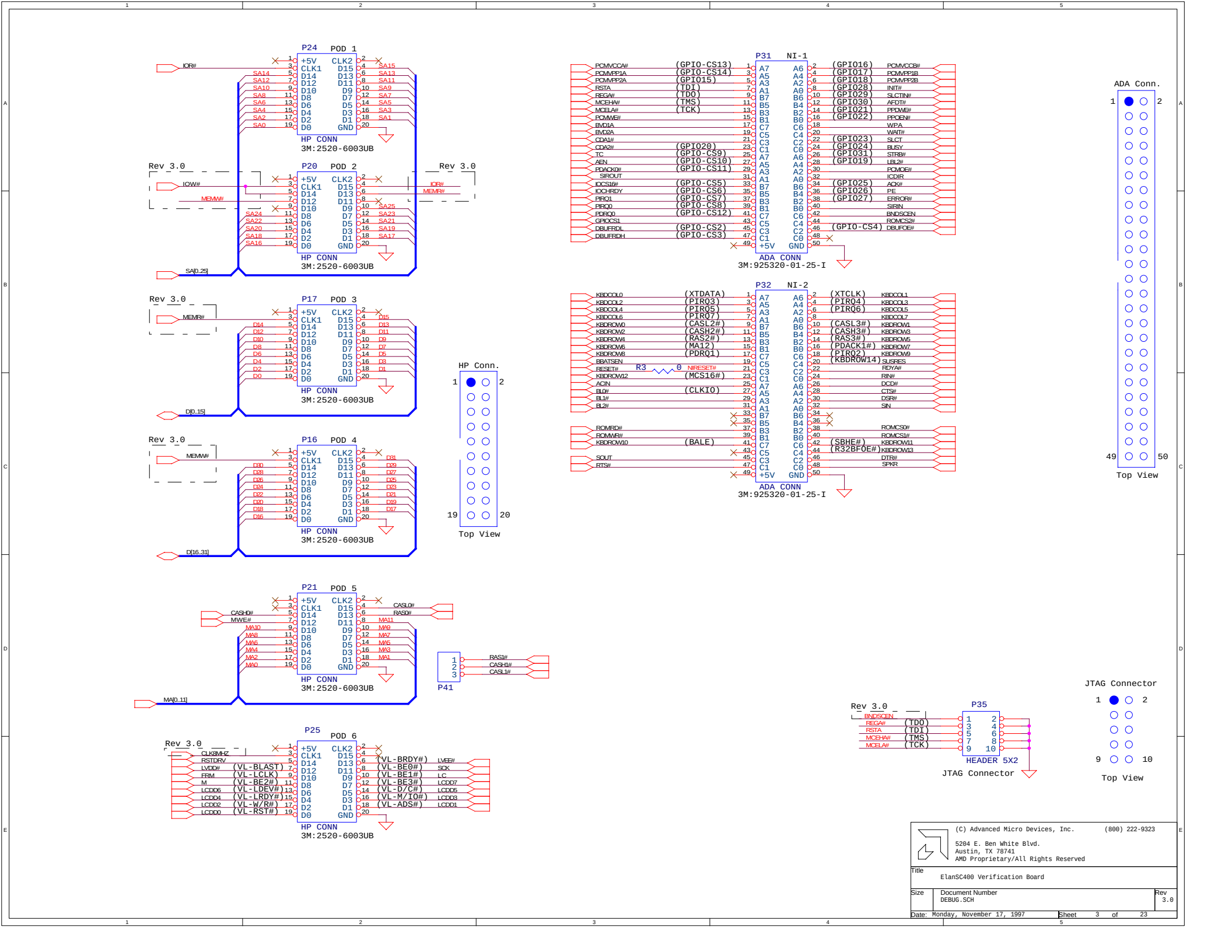
Title
ElanSC400 Verification Board
Size
Document Number
H2SCKT.SCH
Rev
3.0
Date: Monday, November 17, 1997
Sheet 2 of 23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Rev 3.0
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P16 POD 4
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ADA CONN
3M:925320-01-25-I
P32 NI-2
HP Conn.
Top View
ADA Conn.
P41
P35
HEADER 5X2
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DEBUG.SCH
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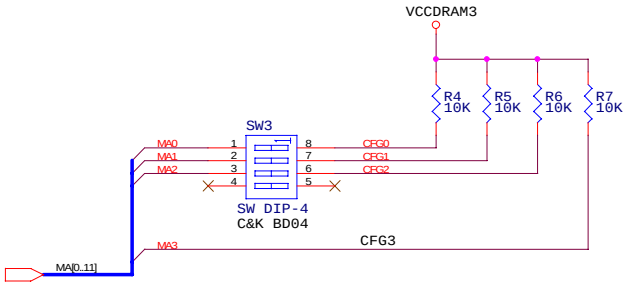
Sheet 3 of 23

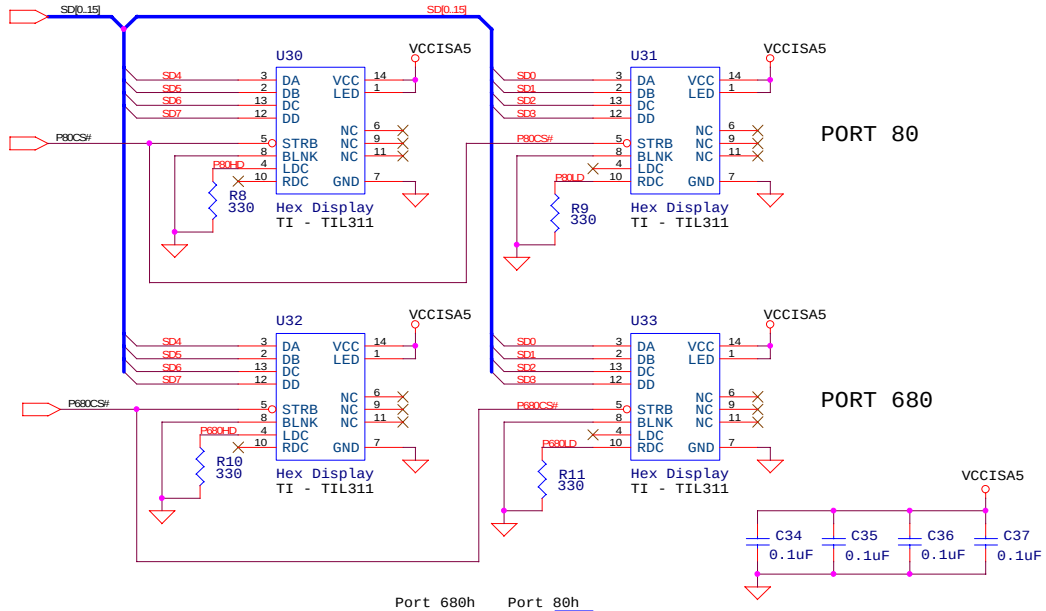


SC400 PIN STRAP OPTIONS

CFG1 CFG0 Configuration
0 0 x8 ROMCS0# ROM Interface
1 0 x16 ROMCS0# ROM Interface
1 1 x32 ROMCS0# ROM Interface

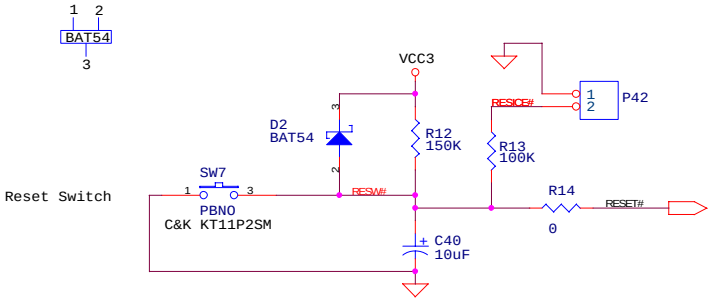
CFG2 Configuration
0 Enable ROMCS0# decode on the ROMCS0# pin.
1 Enable ROMCS0# decode to access PCMCIA socket A.

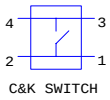
CFG3 Configuration
NOT IN USE.

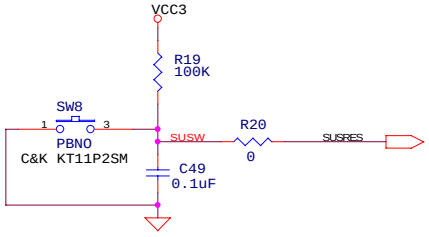


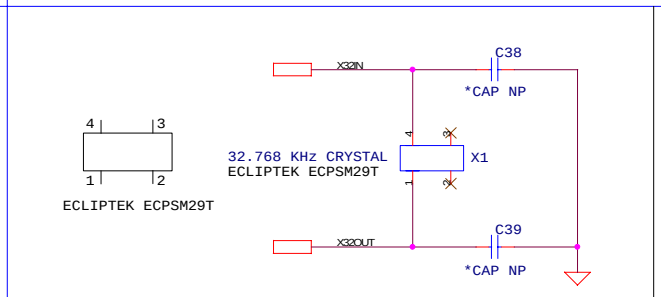
NOTE:
Place the 680h displays before the 80h displays if possible. See diagram.

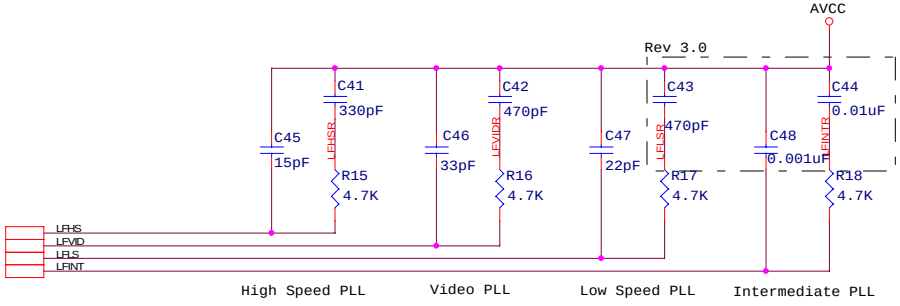
Port 680h		Port 80h	
U32	U33	U30	U31





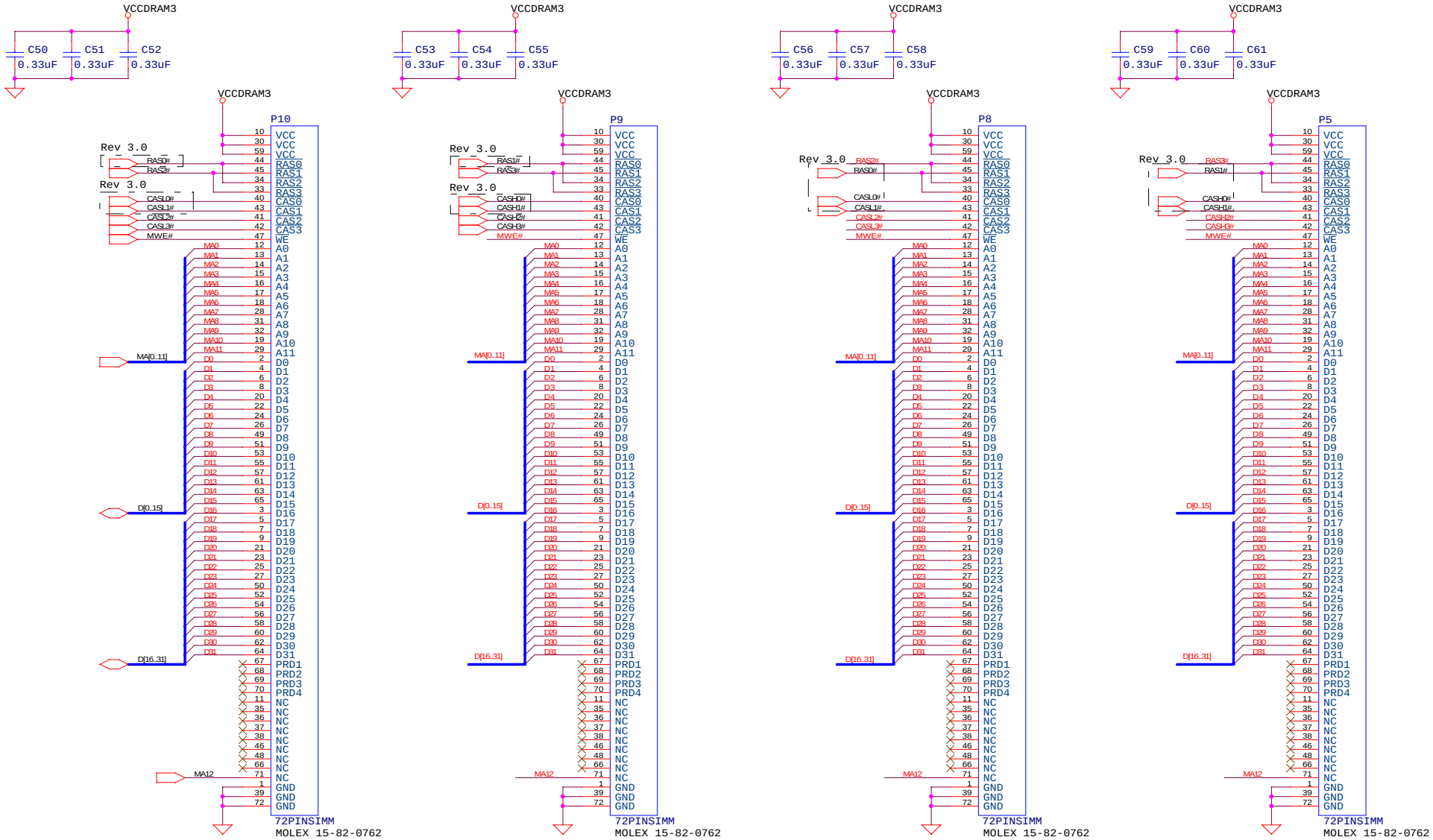






Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: Elan SC400 Verification Board
Size: Document Number: XTAL.SCH Rev: 3.0
Date: Monday, November 17, 1997 Sheet 4 of 23



3.3 Volt SIMMS Only

NOTE:
Using 4Mx4 DRAM in a 64MB system will exceed the loading requirements of the MWE# and MA signals. ElanSC400 will need to be programmed to support this configuration.

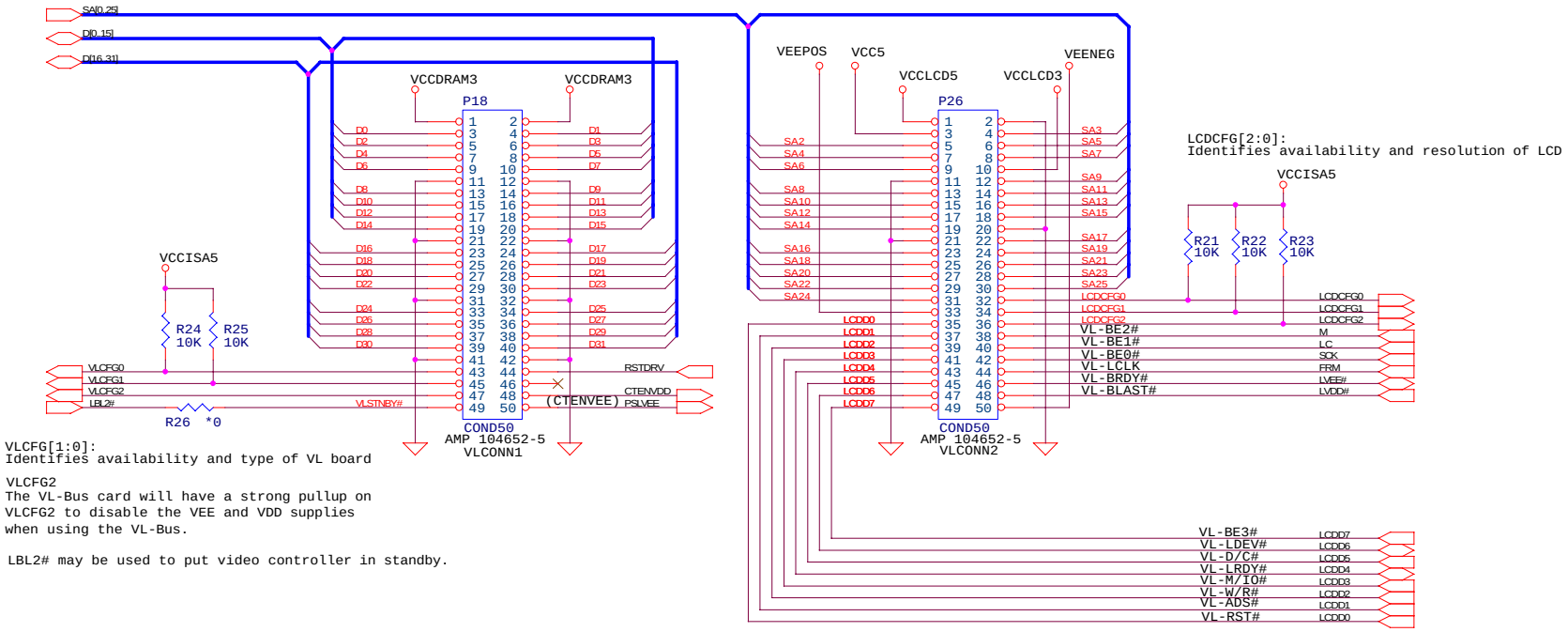
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size | Document Number: DRAM.SCH | Rev: 3.0

Date: Monday, November 17, 1997 | Sheet 5 of 23

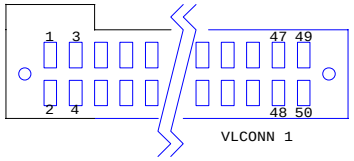


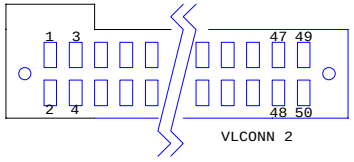
LCDCFG[2:0]:
Identifies availability and resolution of LCD

VLCFG[1:0]:
Identifies availability and type of VL board

VLCFG2
The VL-Bus card will have a strong pullup on
VLCFG2 to disable the VEE and VDD supplies
when using the VL-Bus.

LBL2# may be used to put video controller in standby.





Edge of Board

VLCFG[1:0]:
Identifies availability and type of VL board

VLCFG2
The VL-Bus card will have a strong pullup on
VLCFG2 to disable the VEE and VDD supplies
when using the VL-Bus.

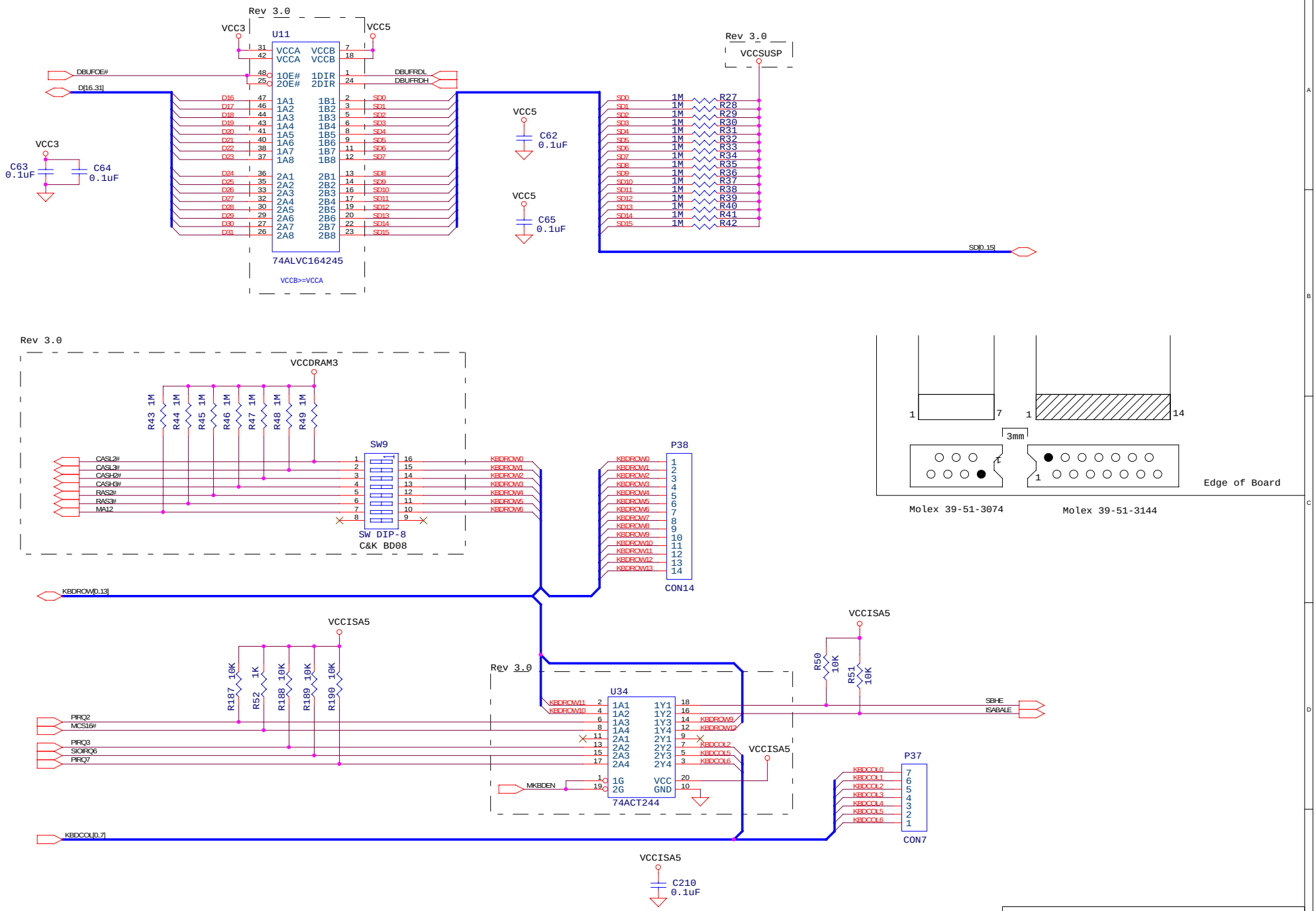
LBL2# may be used to put video controller in standby.

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Title: ElanSC400 Verification Board

Size	Document Number	Rev
	VLCONN.SCH	3.0

Date: Monday, November 17, 1997 Sheet 6 of 23



Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

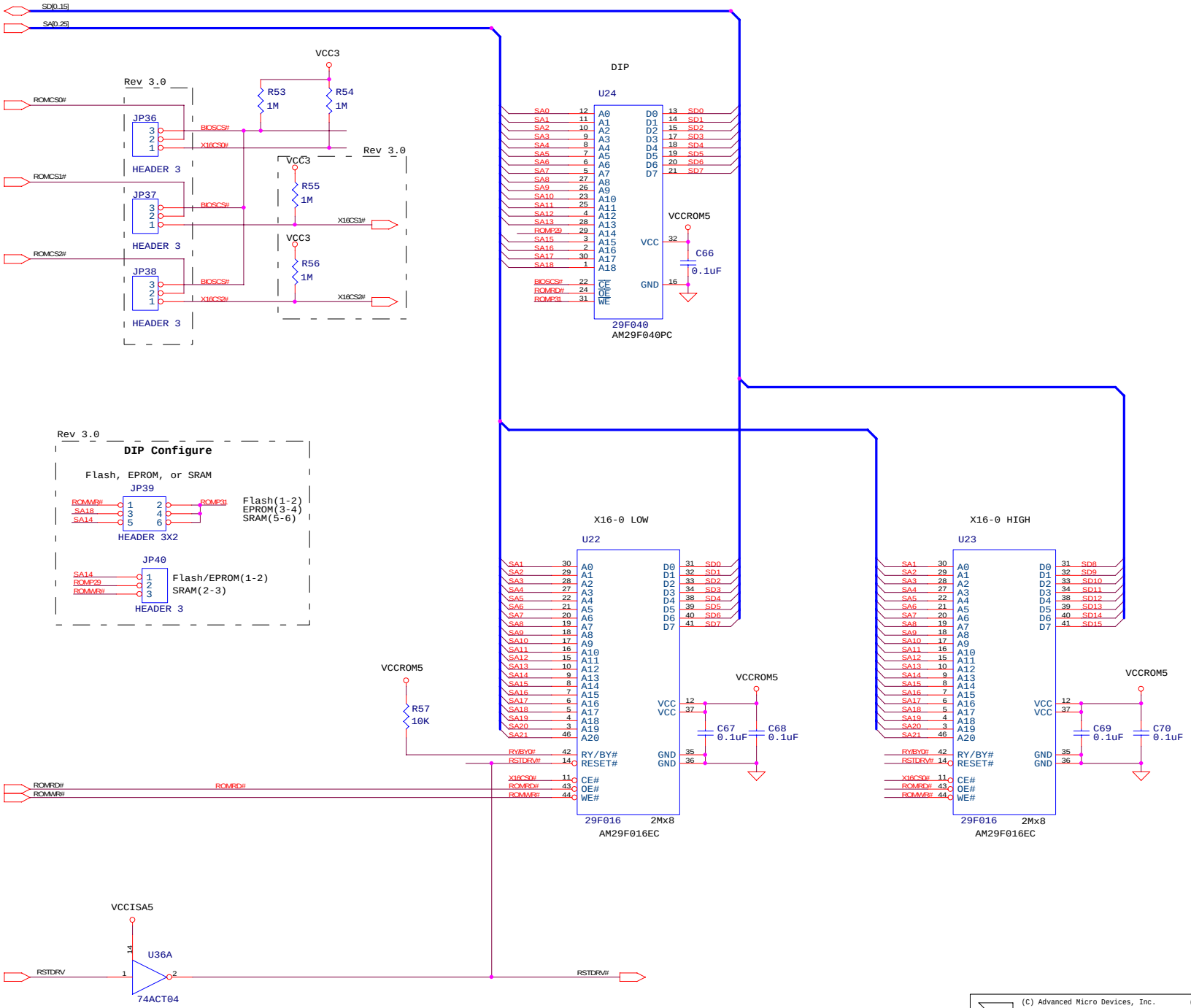
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

NOTE: Buffer U34 is used to provide the appropriate connections for either matrix keyboard use or ISA and Super I/O use. It is not needed for normal operation.

Title: ElanSC400 Verification Board

Size	Document Number	Rev
	DATABUFF.SCH	3.0

Date: Monday, November 17, 1997 Sheet 7 of 23



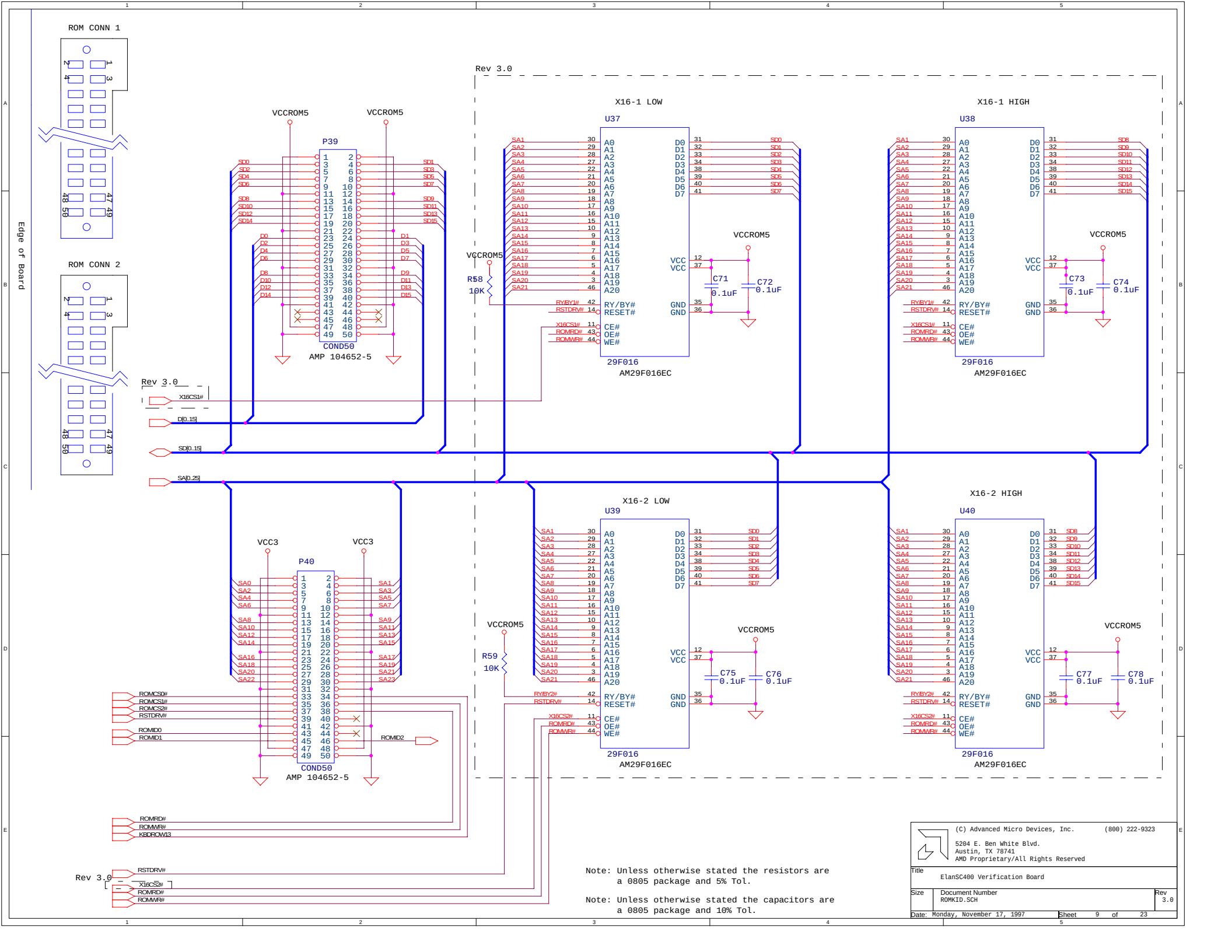
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

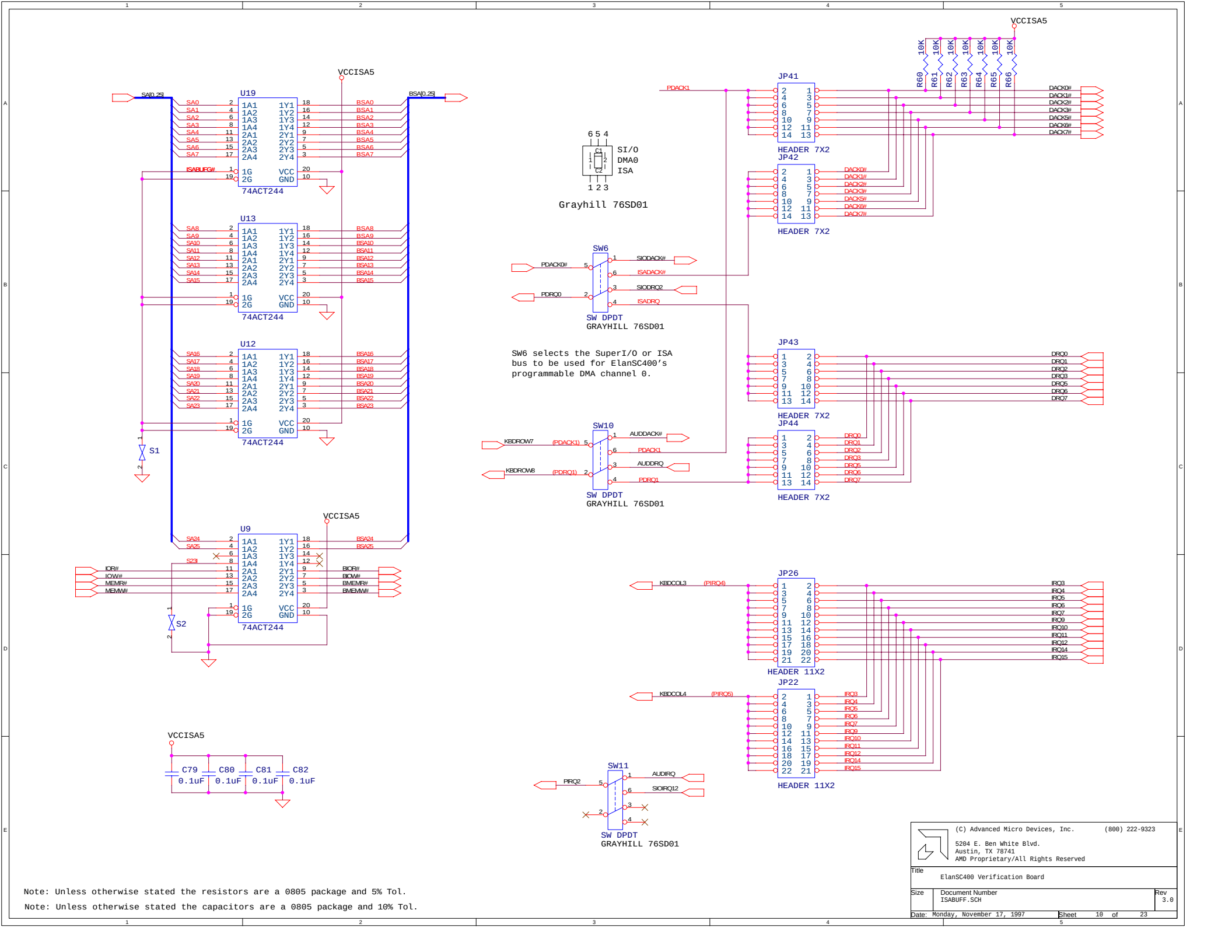
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size | Document Number: ROM.SCH | Rev: 3.0

Date: Monday, November 17, 1997 Sheet 8 of 23


ROM CONN 1
ROM CONN 2
Edge of Board
Rev 3.0
X16-1 LOW
X16-1 HIGH
X16-2 LOW
X16-2 HIGH
U37
U38
U39
U40
29F016
AM29F016EC
P39
P40
COND50
AMP 104652-5
VCCROM5
VCC3
R58
R59
10K
C71
C72
C73
C74
C75
C76
C77
C78
0.1uF
X16CS1#
D[0..15]
SD[0..15]
SA[0..25]
ROMCS0#
ROMCS1#
ROMCS2#
RSTDRV#
ROMID0
ROMID1
ROMID2
ROMRD#
ROMWR#
KBDROW13
X16CS2#
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.
(C) Advanced Micro Devices, Inc. (800) 222-9323
5204 E. Ben White Blvd.
Austin, TX 78741
AMD Proprietary/All Rights Reserved
Title
ElanSC400 Verification Board
Size
Document Number
ROMKID.SCH
Rev
3.0
Date: Monday, November 17, 1997
Sheet 9 of 23



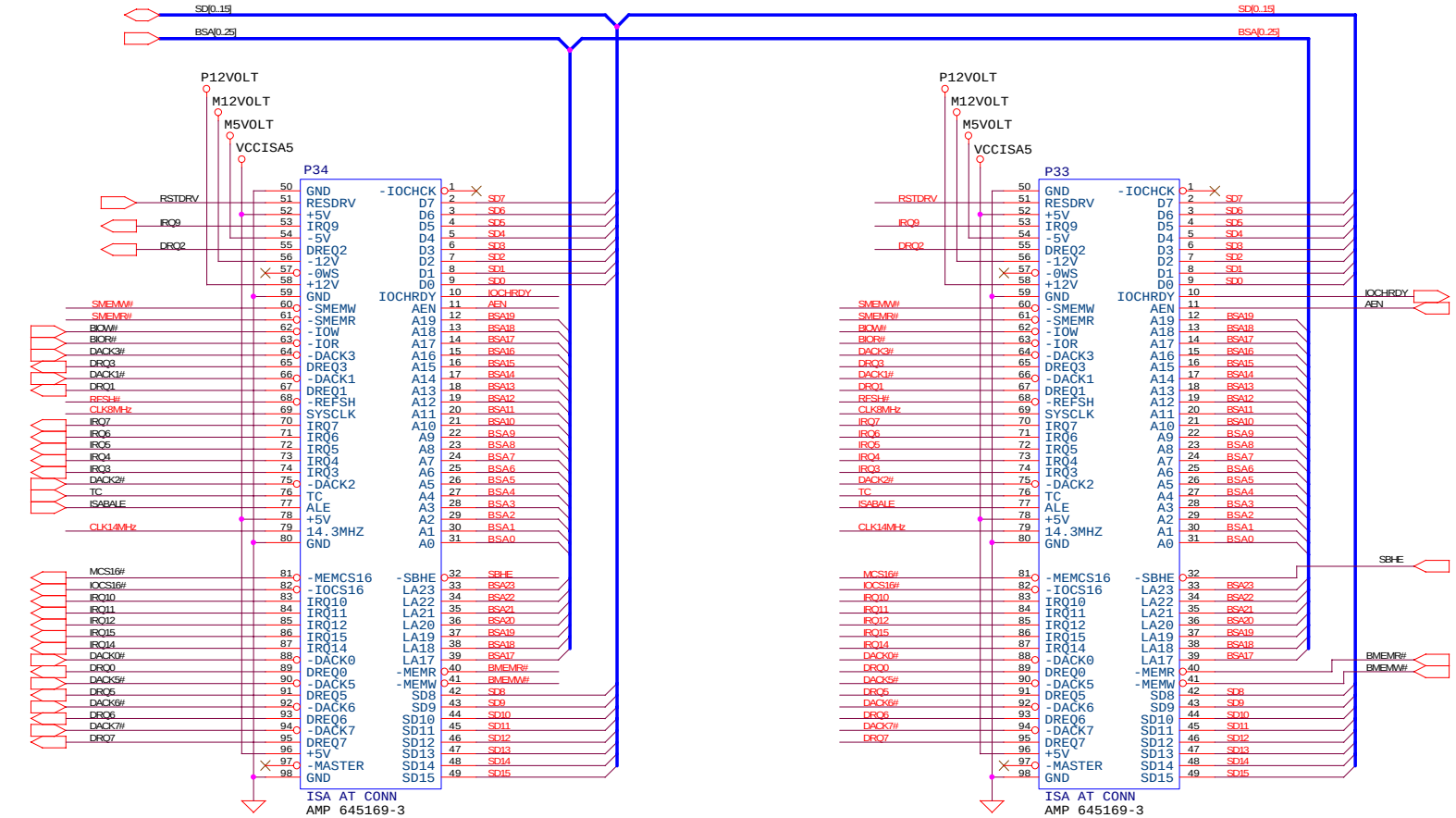
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

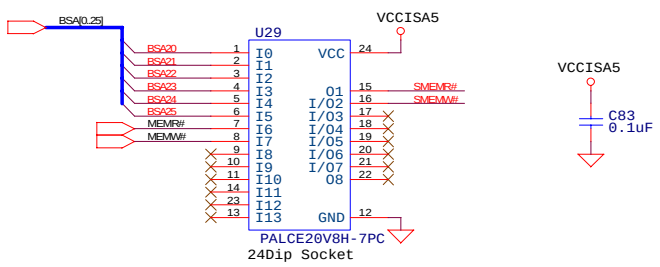
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

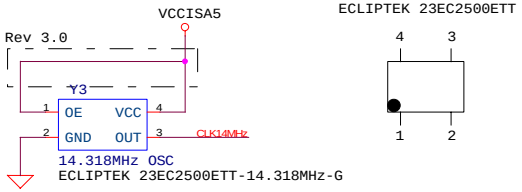
Title: ElanSC400 Verification Board

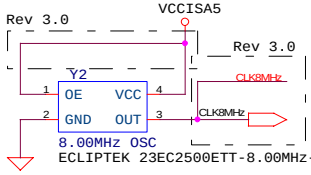
Size | Document Number: ISABUFF.SCH | Rev: 3.0

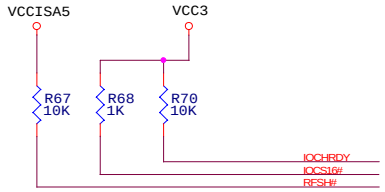
Date: Monday, November 17, 1997 | Sheet 10 of 23











PAL equations

SMEMR# = /BSA20 * /BSA21 * /BSA22 * /BSA23 * /BSA24 * /BSA25 * /MEMR#

SMEMW# = /BSA20 * /BSA21 * /BSA22 * /BSA23 * /BSA24 * /BSA25 * /MEMW#

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

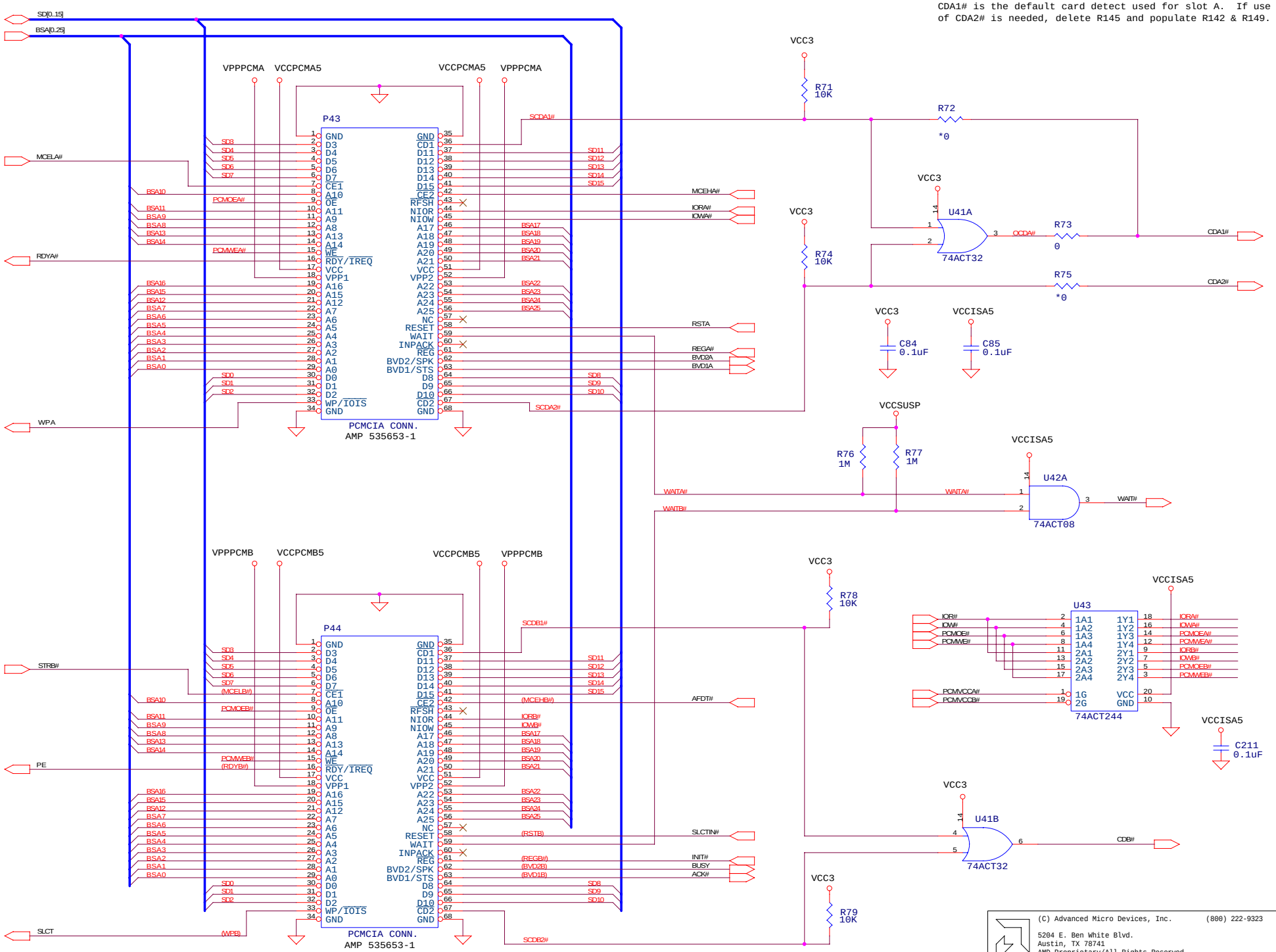
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size | Document Number: ISACONN.SCH | Rev: 3.0

Date: Monday, November 17, 1997 | Sheet 11 of 23

CDA1# is the default card detect used for slot A. If use of CDA2# is needed, delete R145 and populate R142 & R149.

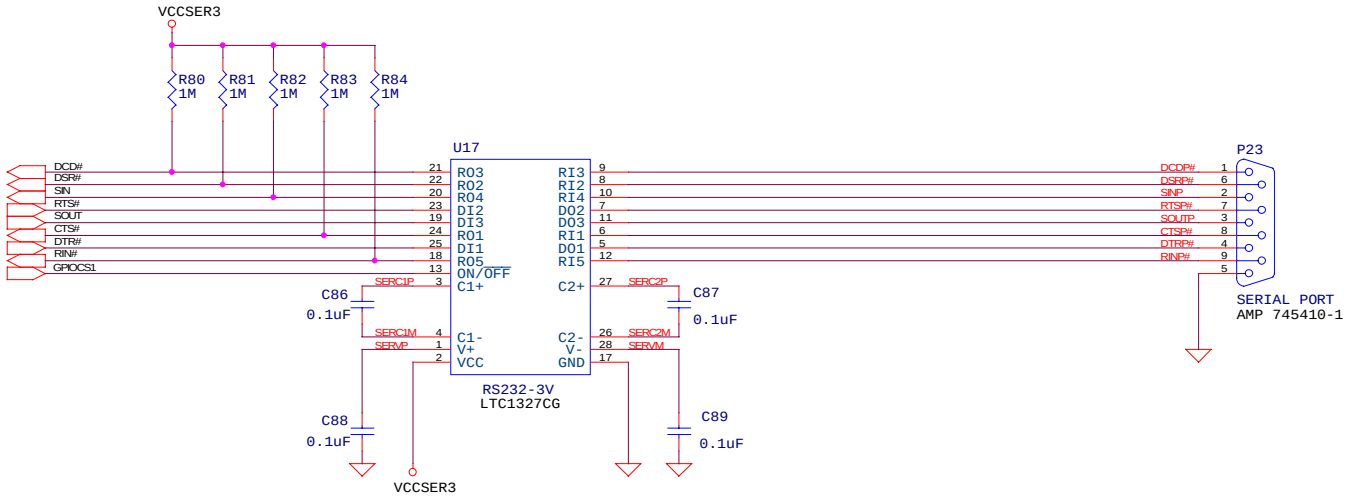


Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

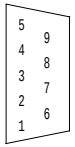
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title	ElanSC400 Verification Board
Size	Document Number: PCMCIA.SCH — Rev: 3.0
Date:	Monday, November 17, 1997 — Sheet 12 of 23

Elan SC400 Serial Port

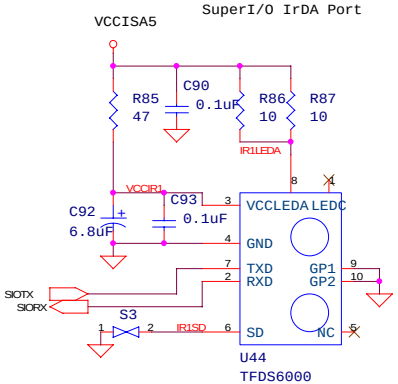


Serial Connector

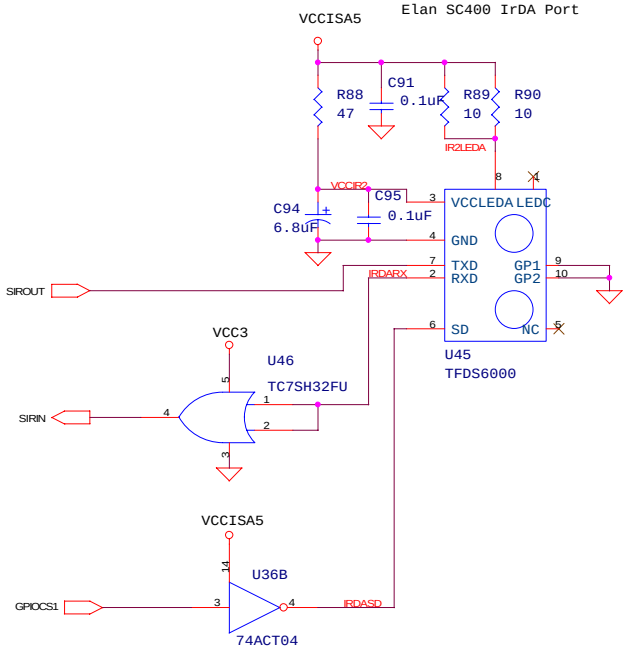


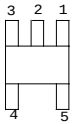
Rev 3.0

SuperI/O IrDA Port

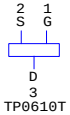


Elan SC400 IrDA Port

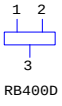




TC7SH32FU

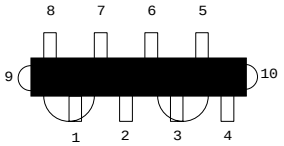


TP0610T



RB400D

TOP SIDE VIEW



TFDS6000

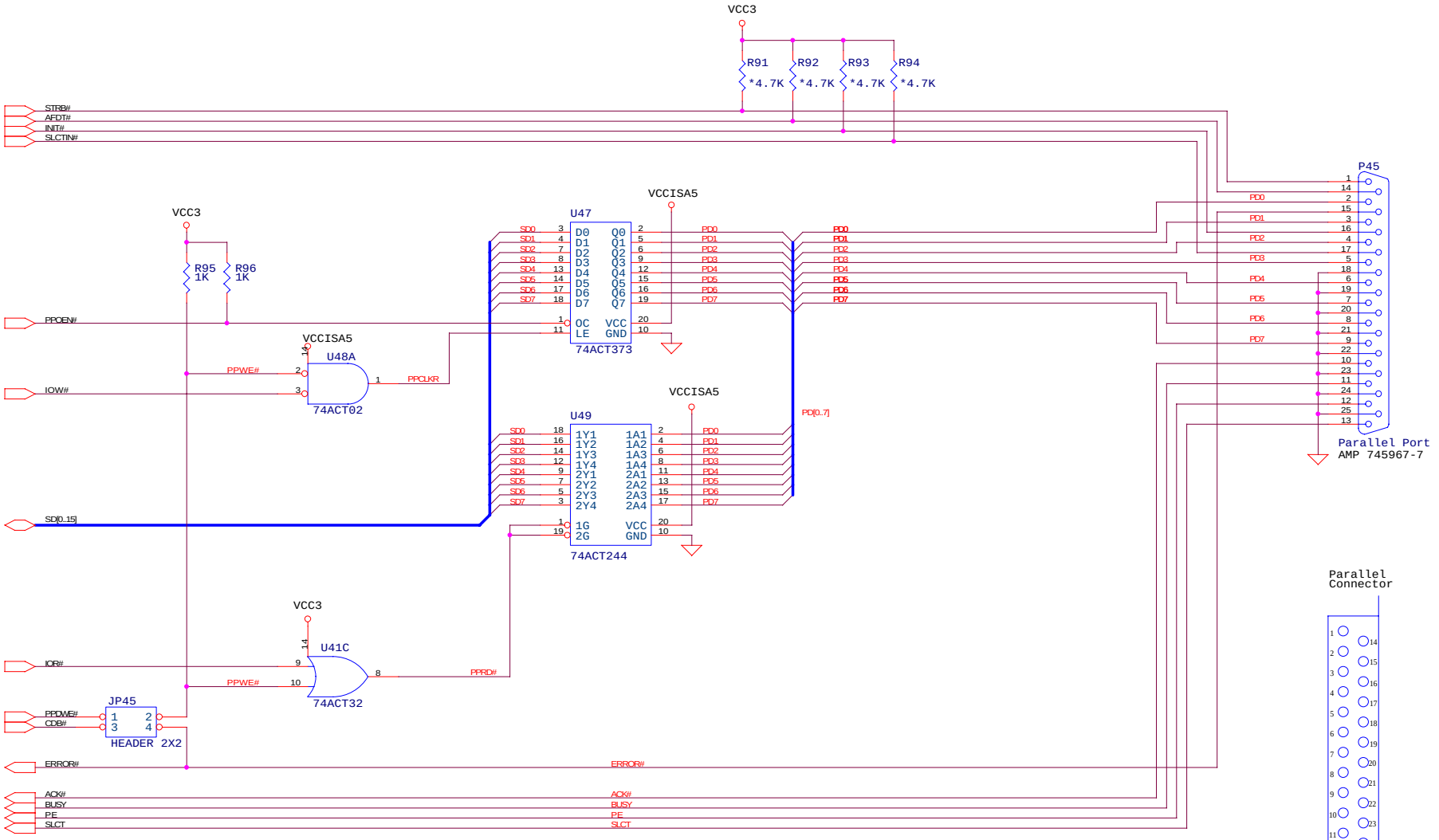
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size	Document Number	Rev
	SERIAL.SCH	3.0

Date: Monday, November 17, 1997 Sheet 13 of 23



The group of ElanSC400 pins GPIO16-31 are available for the following functions: GPIO16-31, PCMCIA Slot B, or Parallel Port. Refer to the table below for JP32 settings for the listed functions.

Function	JP30
GPIO	NC
PCMCIA Slot B	3-4
Parallel Port	1-2

When PCMCIA Socket B is selected, PPOEN# and PPDWE# are tri-stated.

R95 and R96 are needed, to eliminate the possibility of data contention from the parallel port.

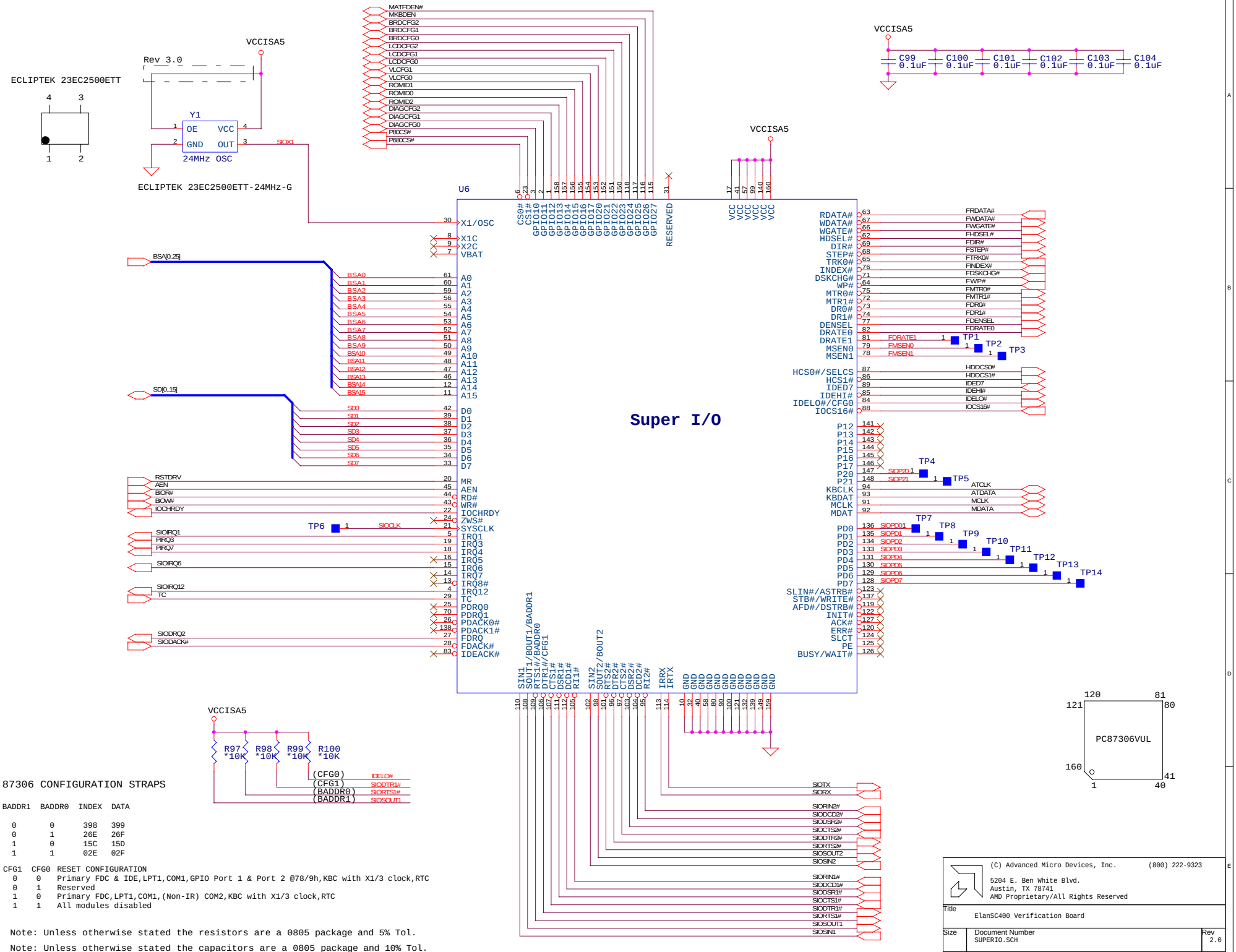
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size | Document Number: PARALLEL.SCH | Rev: 3.0

Date: Monday, November 17, 1997 | Sheet 14 of 23



87306 CONFIGURATION STRAPS

BADDR1	BADDR0	INDEX	DATA
0	0	398	399
0	1	26E	26F
1	0	15C	15D
1	1	02E	02F

CFG1	CFG0	RESET CONFIGURATION
0	0	Primary FDC & IDE,LPT1,COM1,GPIO Port 1 & Port 2 @78/9h,KBC with X1/3 clock,RTC
0	1	Reserved
1	0	Primary FDC,LPT1,COM1,(Non-IR) COM2,KBC with X1/3 clock,RTC
1	1	All modules disabled

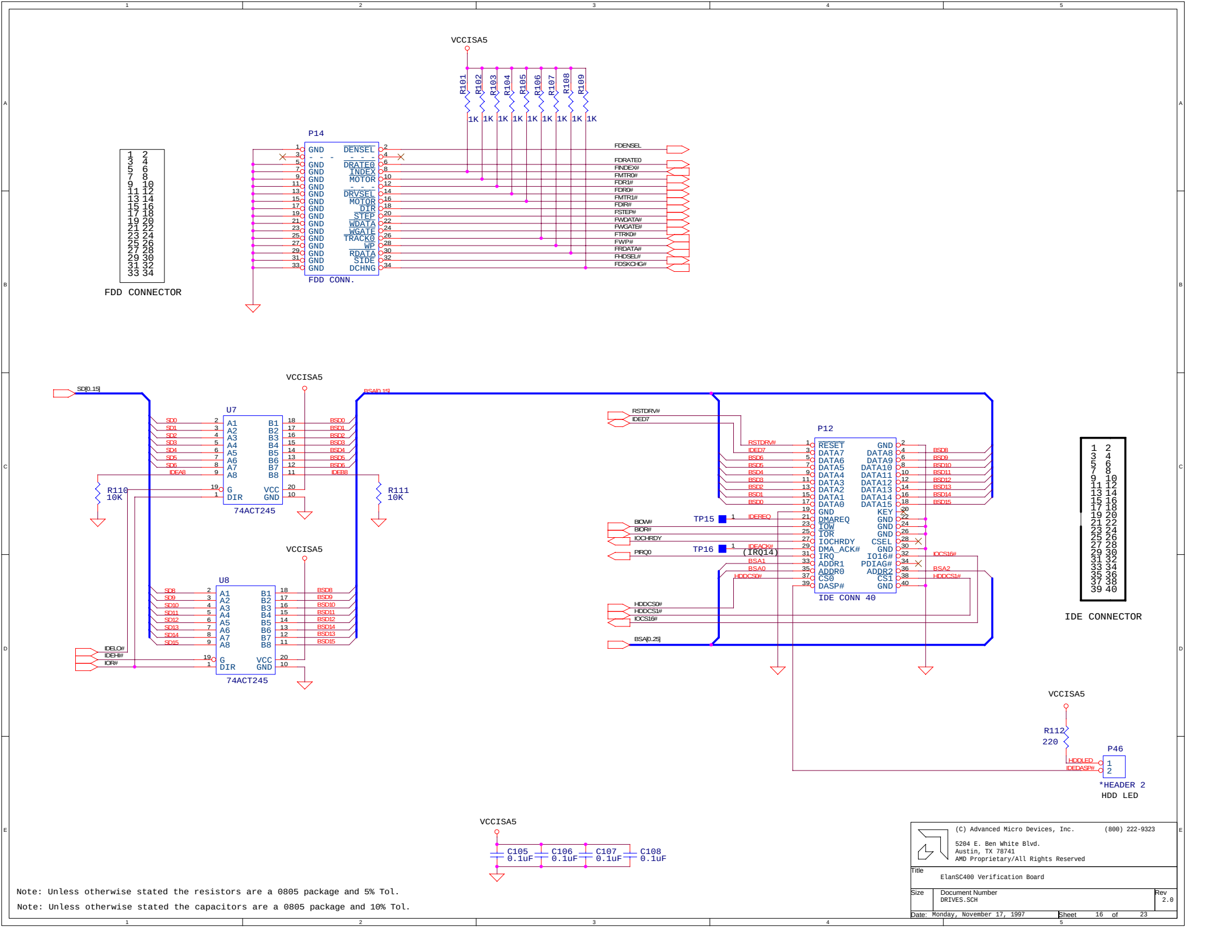
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size: | Document Number: SUPERIO.SCH | Rev: 2.0

Date: Monday, November 17, 1997 | Sheet 15 of 23



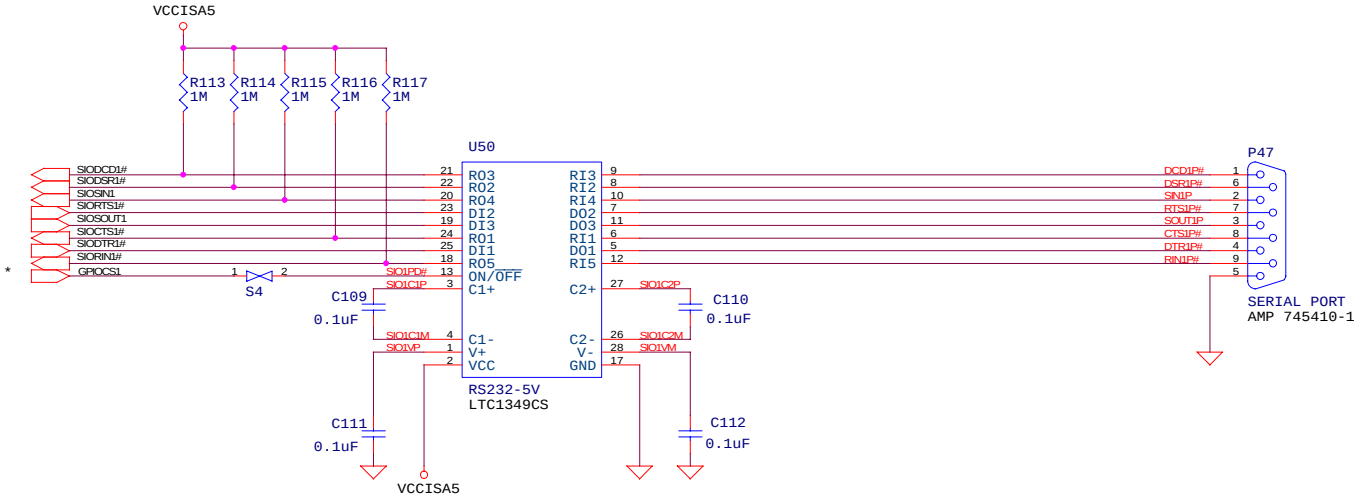
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

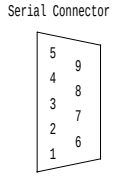
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

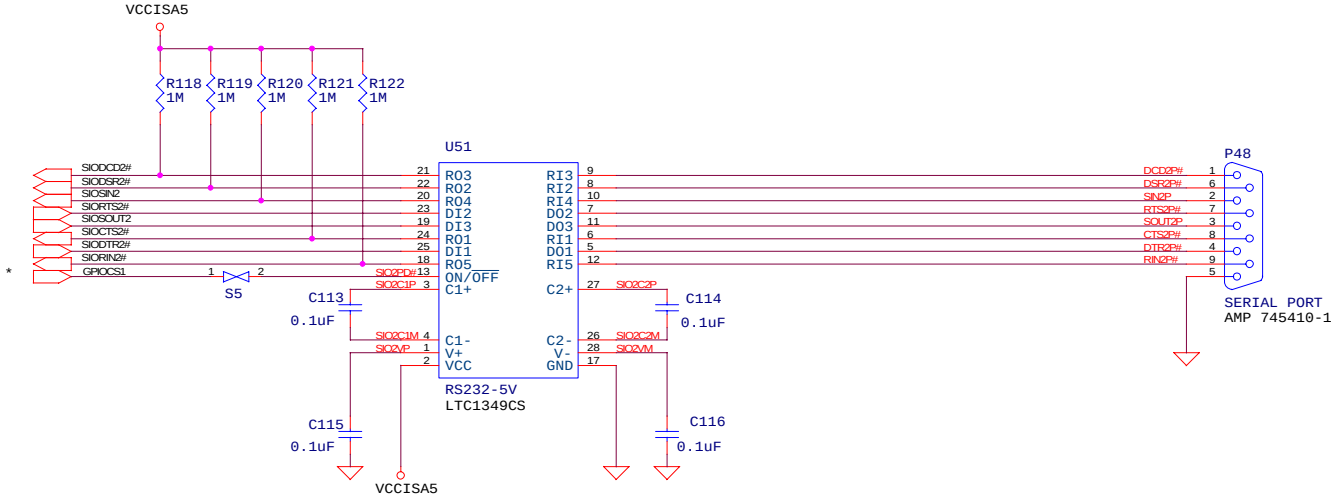
Title: ElanSC400 Verification Board

Size | Document Number: DRIVES.SCH | Rev: 2.0

Date: Monday, November 17, 1997 | Sheet 16 of 23







NOTE: * When turning off VCCISA5, make sure GPIOCS1 is low to prevent current draw.

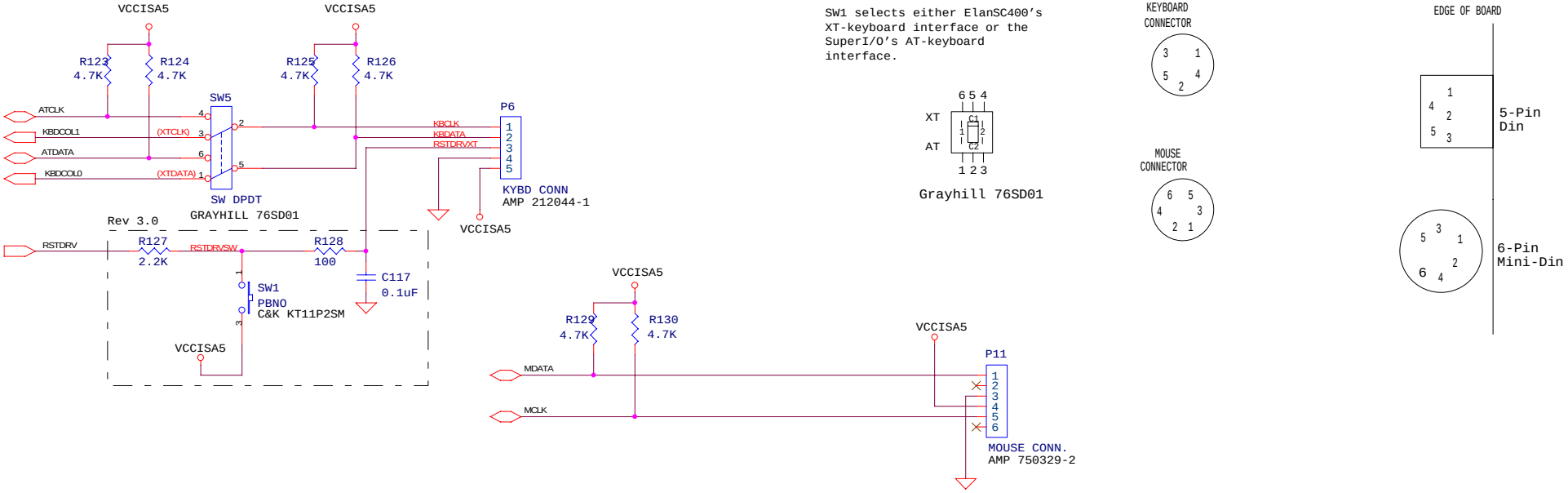
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

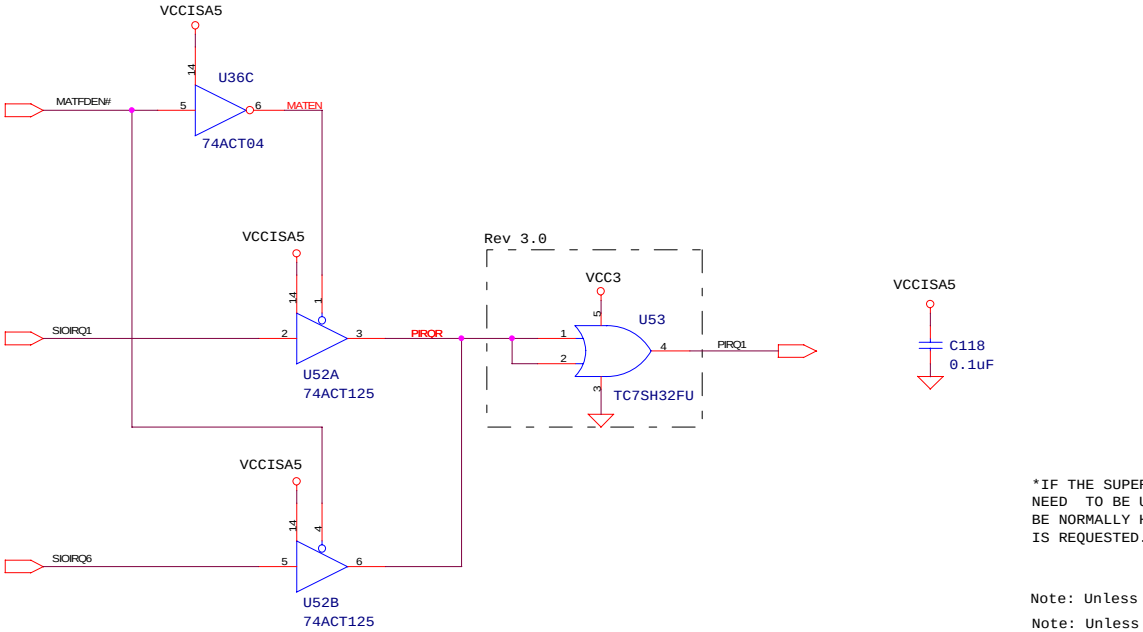
Size | Document Number: SIO232.SCH | Rev: 3.0

Date: Monday, November 17, 1997 | Sheet 17 of 23



SW1 selects either ElanSC400's XT-keyboard interface or the SuperI/O's AT-keyboard interface.

Grayhill 76SD01



*IF THE SUPERI/O FDD, MATRIX KEYBOARD, AND AT-KEYBOARD NEED TO BE USED TOGETHER, MATFDEN# IS CONFIGURED TO BE NORMALLY HIGH AND TO GO LOW WHEN A FLOPPY ACCESS IS REQUESTED.

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

(800) 222-9323

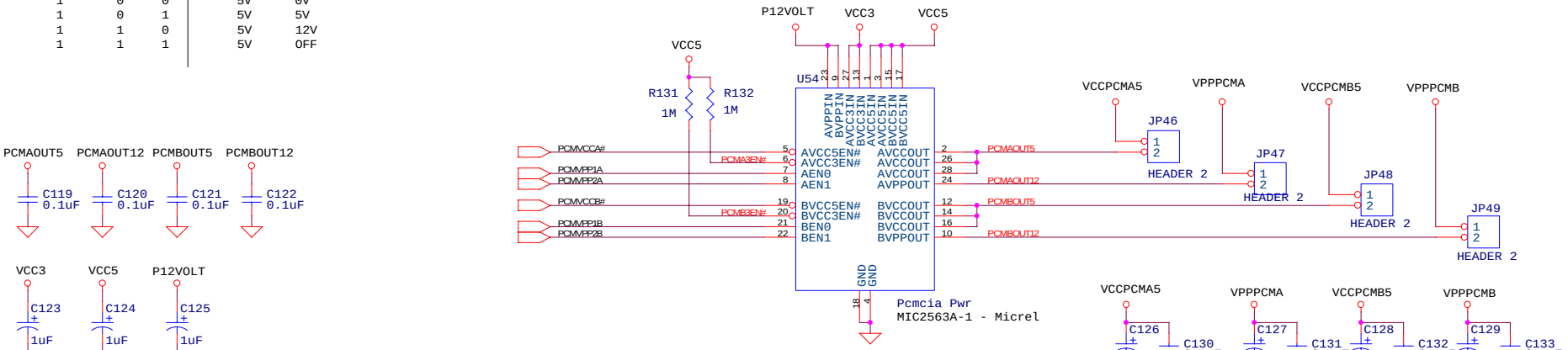
5204 E. Ben White Blvd.
Austin, TX 78741

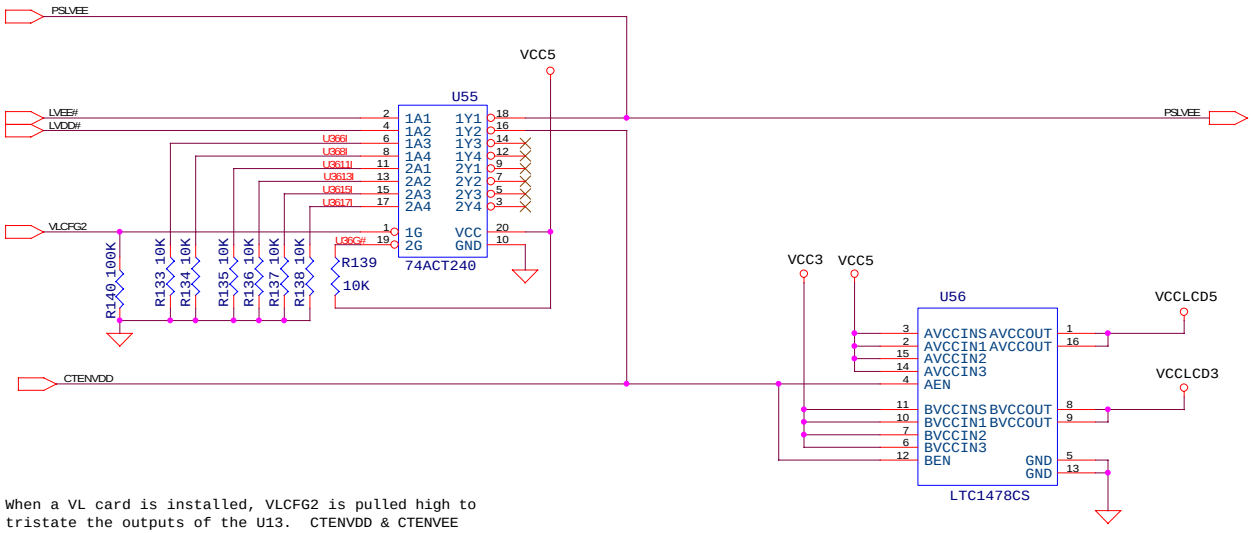
Title: ElanSC400 Verification Board

Size | Document Number: SIOKBRD.SCH | Rev: 3.0

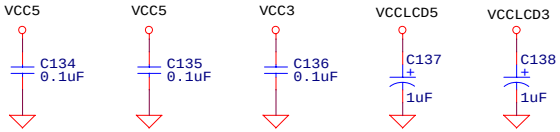
Date: Monday, November 17, 1997 | Sheet 18 of 23

XVCC5EN#	XVCC3EN#	XEN1	XEN0	XVCCOUT	XVPPOUT
0	1	0	0	5V	0V
0	1	0	1	5V	5V
0	1	1	0	5V	12V
0	1	1	1	5V	OFF





When a VL card is installed, VLCFG2 is pulled high to tristate the outputs of the U13. CTENVDD & CTENVEE will then control VCCLCDx & VEEx.



Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

Size | Document Number: PERIPWR.SCH | Rev: 3.0

Date: Monday, November 17, 1997 | Sheet 19 of 23

PS/2 POWER SUPPLY CONNECTORS

P12VOLT M12VOLT M5VOLT

P1
PC Power Conn
BURNDY GTC6R-1
P5VOLT
P12VOLT
M12VOLT
GND
GND

P2
PC Power Conn
BURNDY GTC6R-1
GND
GND
M5VOLT
P5VOLT
P5VOLT
P5VOLT

P5VOLT P12VOLT
C139 10uF
C140 10uF

POWER MODULE CONNECTORS

VCC5

P4
COND26
P12VOLT
VCC5
P5VOLT
P5VOLT
P12VOLT
VCC5
P5VOLT
PSLVEE

VCC3 VCCCPU VEEPOS VCCANLG3 VEENEG

P7
COND26
VCC3
VCCCPU
VEEPOS
VCCANLG3
VEENEG

VCCCPU VCCANLG3 VEEPOS VEENEG
C141 10uF
C142 10uF
C143 4.7uF
C144 4.7uF

3.84A MAX.
VCC3
JP50
HEADER 2X2
VCCDRAM3
C153 10uF
C154 10uF
C155 4.7uF
C156 0.1uF

JP51
25mA MAX.
VCCSER3
C165 10uF
C166 4.7uF
C167 0.1uF

JP52
VCC5
240mA MAX.
VCCROM5
C168 10uF
C169 10uF
C170 4.7uF
C171 0.1uF

~5A MAX.
JP53
HEADER 2X2
VCCISA5
C172 10uF
C173 4.7uF
C174 0.1uF

VCCDRAM3
C145 10uF
C146 10uF
C147 10uF
C148 10uF
C149 10uF
SIMM SOCKETS
VLBUS

VCCROM5
C150 10uF
C151 10uF
C152 10uF
ROMS
ROM DAUGHTER

VCCISA5
C157 10uF
C158 10uF
C159 10uF
C160 10uF
C161 10uF
C162 10uF
C163 4.7uF
C164 4.7uF
SUPER I/O
ISA BUFFERS
PORT 80
ISA SLOT
ISA SLOT
IDE
AT KBD
PS/2 MOUSE

1 2
3
BAT54C

VCCANLG3
D1
VCCRTC
COINA
BAT54C
R141 2.2K
BBATSEN
BT1 3.0 COIN CELL
C175 0.1uF

Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.

Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.

Title: ElanSC400 Verification Board

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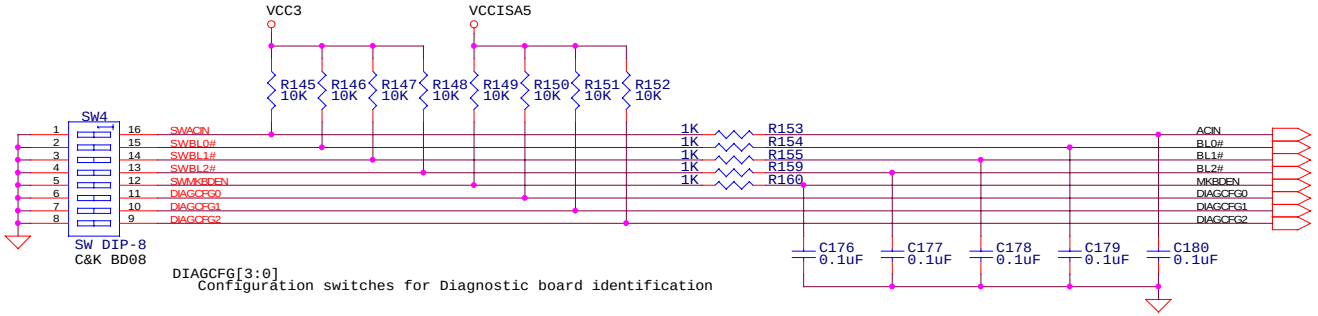
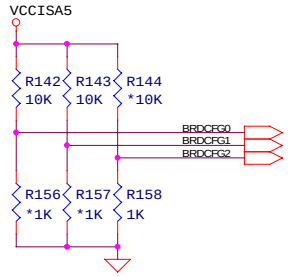


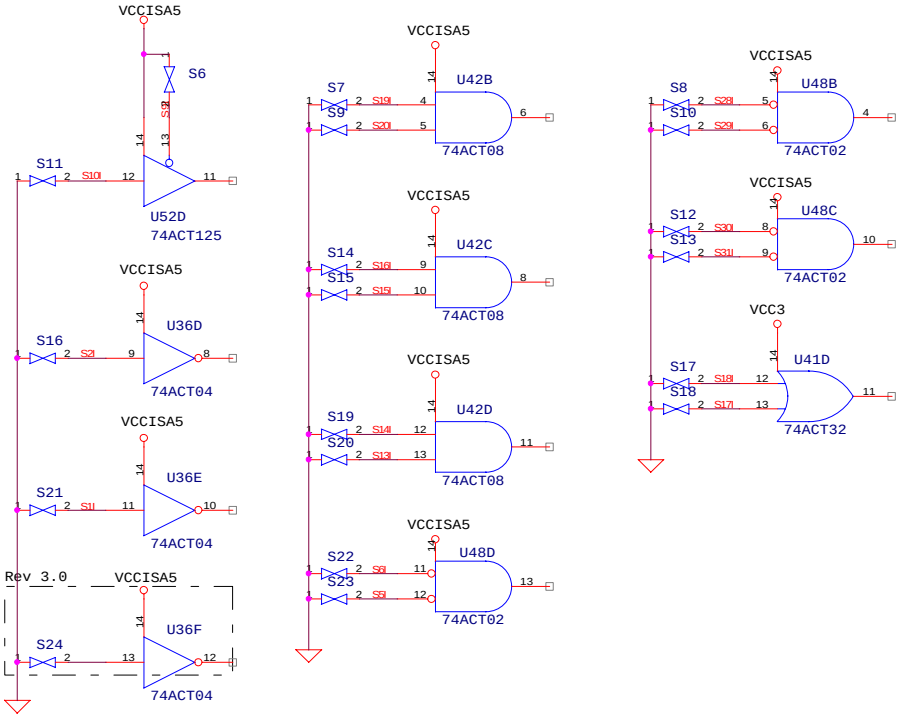
DIAGCFG[3:0]
Configuration switches for Diagnostic board identification

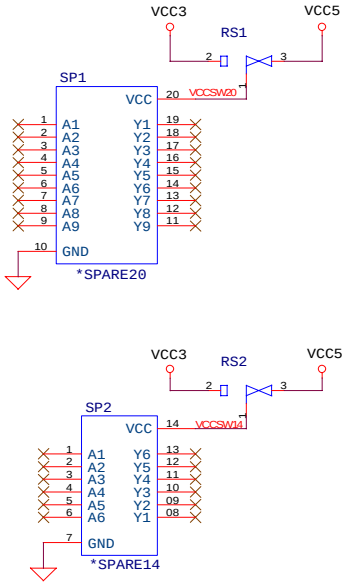


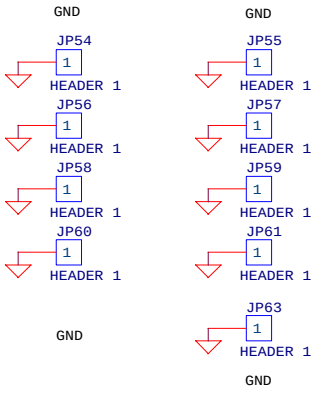
BRDCFG[2:0]:

Identifies the Revision of the board

N0TE: (*) Indicates that location is not populated







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Title: ElanSC400 Verification Board

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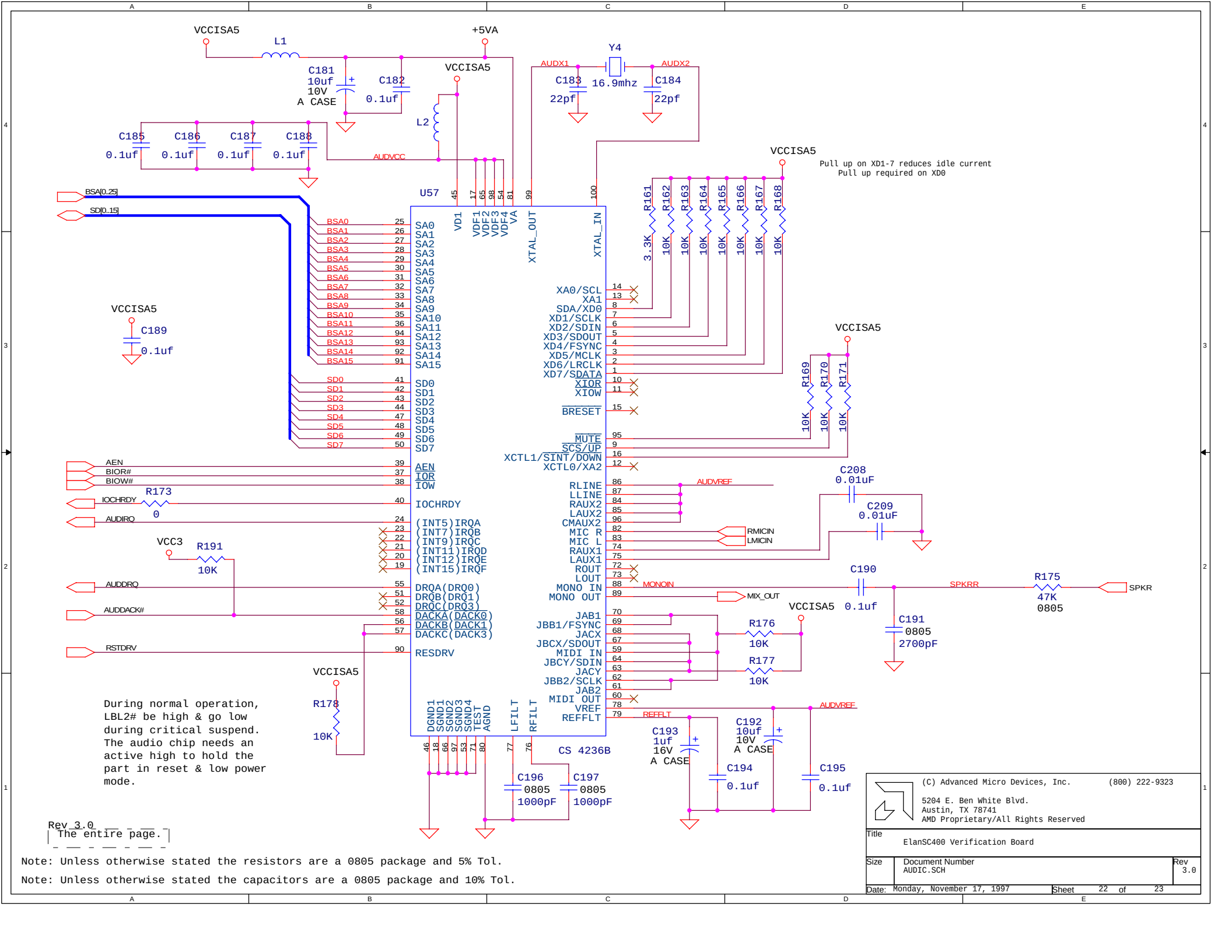
VCCISA5
L1
+5VA
C181
10uf
10V
A CASE
C182
0.1uf
VCCISA5
L2
AUDX1
Y4
AUDX2
C183
22pf
16.9mhz
C184
22pf
C185
0.1uf
C186
0.1uf
C187
0.1uf
C188
0.1uf
AUDVCC
VCCISA5
Pull up on XD1-7 reduces idle current
Pull up required on XD0
BSA[0.25]
SD[0.15]
U57
VD1
VDF1
VDF2
VDF3
VDF4
VA
XTAL_OUT
XTAL_IN
R161
R162
R163
R164
R165
R166
R167
R168
3.3K
10K
BSA0
BSA1
BSA2
BSA3
BSA4
BSA5
BSA6
BSA7
BSA8
BSA9
BSA10
BSA11
BSA12
BSA13
BSA14
BSA15
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
XA0/SCL
XA1
SDA/XD0
XD1/SCLK
XD2/SDIN
XD3/SDOUT
XD4/FSYNC
XD5/MCLK
XD6/LRCLK
XD7/SDATA
XIOR
XIOW
BRESET
VCCISA5
C189
0.1uf
VCCISA5
R169
R170
R171
10K
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
MUTE
SCS/UP
XCTL1/SINT/DOWN
XCTL0/XA2
AEN
BIOR#
BIOW#
AEN
IOR
IOW
R173
IOCHRDY
0
IOCHRDY
AUDIRQ
(INT5)IRQA
(INT7)IRQB
(INT9)IRQC
(INT11)IRQD
(INT12)IRQE
(INT15)IRQF
RLINE
LLINE
RAUX2
LAUX2
CMAUX2
MIC R
MIC L
RAUX1
LAUX1
ROUT
LOUT
MONO IN
MONO OUT
AUDVREF
C208
0.01uF
C209
0.01uF
RMICIN
LMICIN
VCC3
R191
10K
AUDDRQ
AUDDACK#
DRQA(DRQ0)
DRQB(DRQ1)
DRQC(DRQ3)
DACKA(DACK0)
DACKB(DACK1)
DACKC(DACK3)
MONOIN
MIX_OUT
C190
0.1uf
SPKRR
R175
47K
0805
SPKR
C191
0805
2700pF
JAB1
JBB1/FSYNC
JACX
JBCX/SDOUT
MIDI IN
JBCY/SDIN
JACY
JBB2/SCLK
JAB2
MIDI OUT
VREF
REFFLT
VCCISA5
R176
10K
R177
10K
RSTDRV
RESDRV
VCCISA5
R178
10K
DGND1
SGND1
SGND2
SGND3
SGND4
TEST
AGND
LFILT
RFILT
REFFLT
AUDVREF
C193
1uf
16V
A CASE
C192
10uf
10V
A CASE
C194
0.1uf
C195
0.1uf
CS 4236B
C196
0805
1000pF
C197
0805
1000pF
During normal operation,
LBL2# be high & go low
during critical suspend.
The audio chip needs an
active high to hold the
part in reset & low power
mode.
Rev 3.0
The entire page.
Note: Unless otherwise stated the resistors are a 0805 package and 5% Tol.
Note: Unless otherwise stated the capacitors are a 0805 package and 10% Tol.
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Austin, TX 78741
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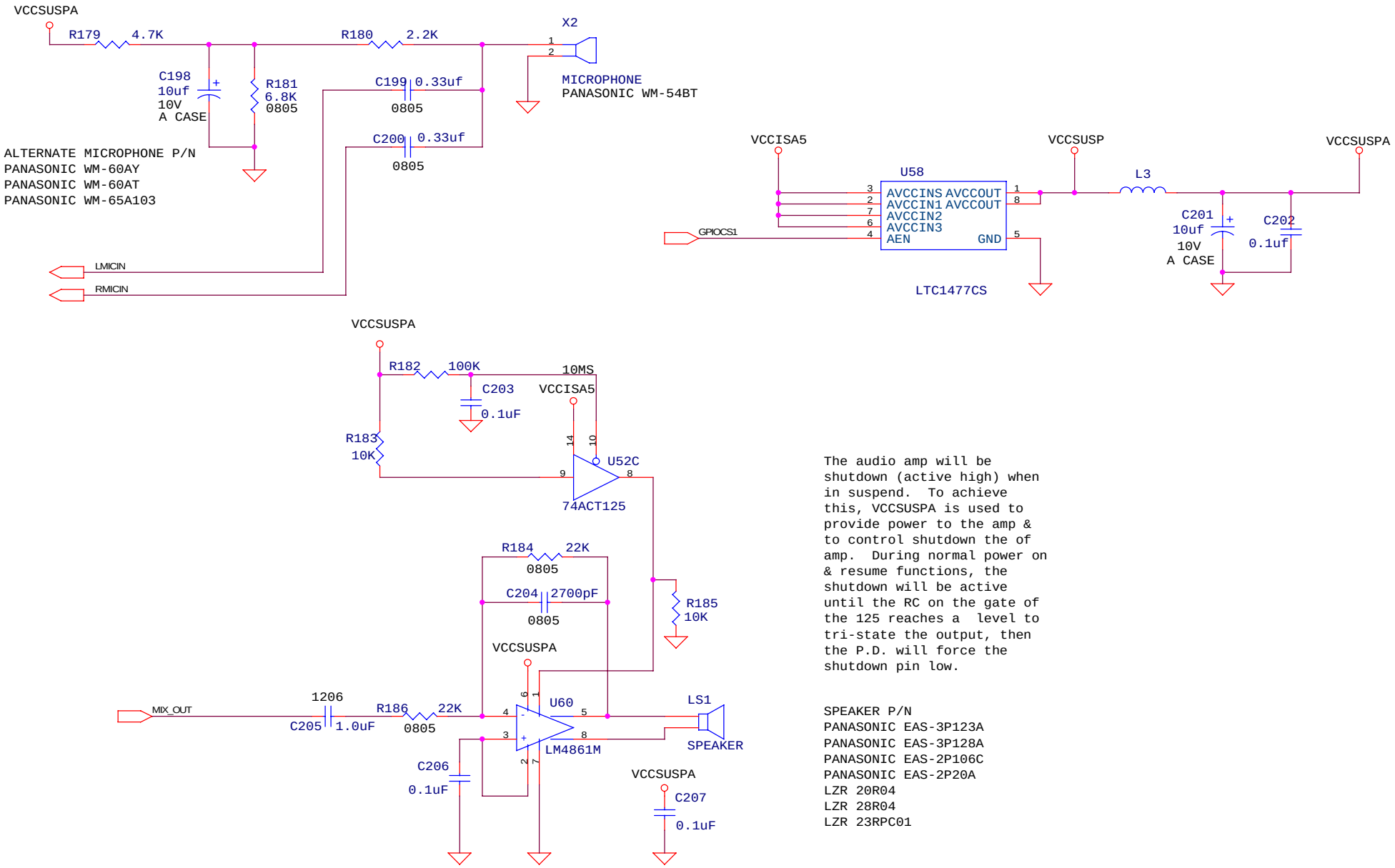

The audio amp will be shutdown (active high) when in suspend. To achieve this, VCCSUSPA is used to provide power to the amp & to control shutdown the of amp. During normal power on & resume functions, the shutdown will be active until the RC on the gate of the 125 reaches a level to tri-state the output, then the P.D. will force the shutdown pin low.

SPEAKER P/N
PANASONIC EAS-3P123A
PANASONIC EAS-3P128A
PANASONIC EAS-2P106C
PANASONIC EAS-2P20A
LZR 20R04
LZR 28R04
LZR 23RPC01

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The entire page.

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W