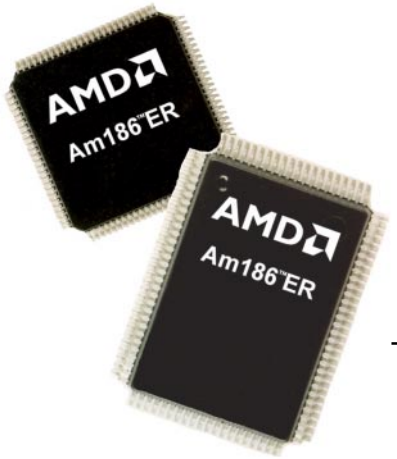
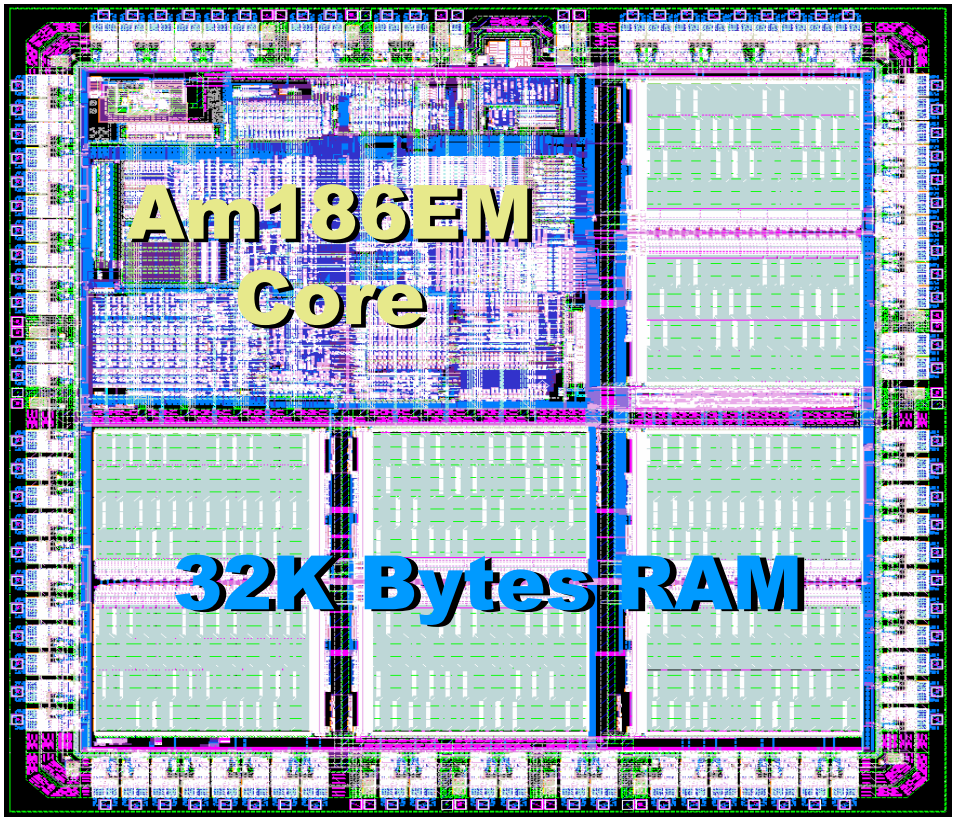
Am186ER/Am188ER
AMD continues 16-bit innovation

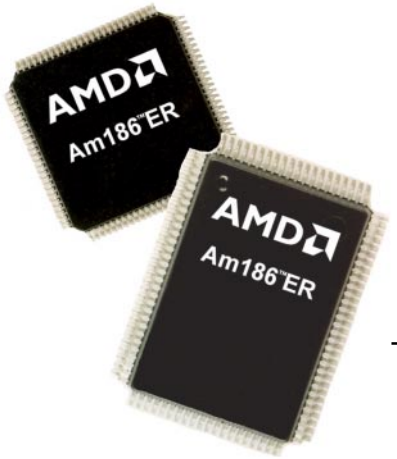


386-Class Performance, Enhanced System Integration, *and* Built-in SRAM

Systems in Silicon

Am186ER and Am188ER

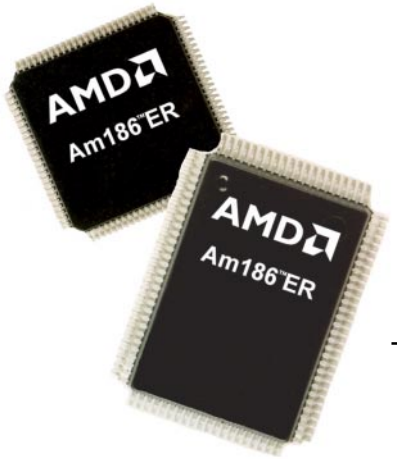




Systems in Silicon

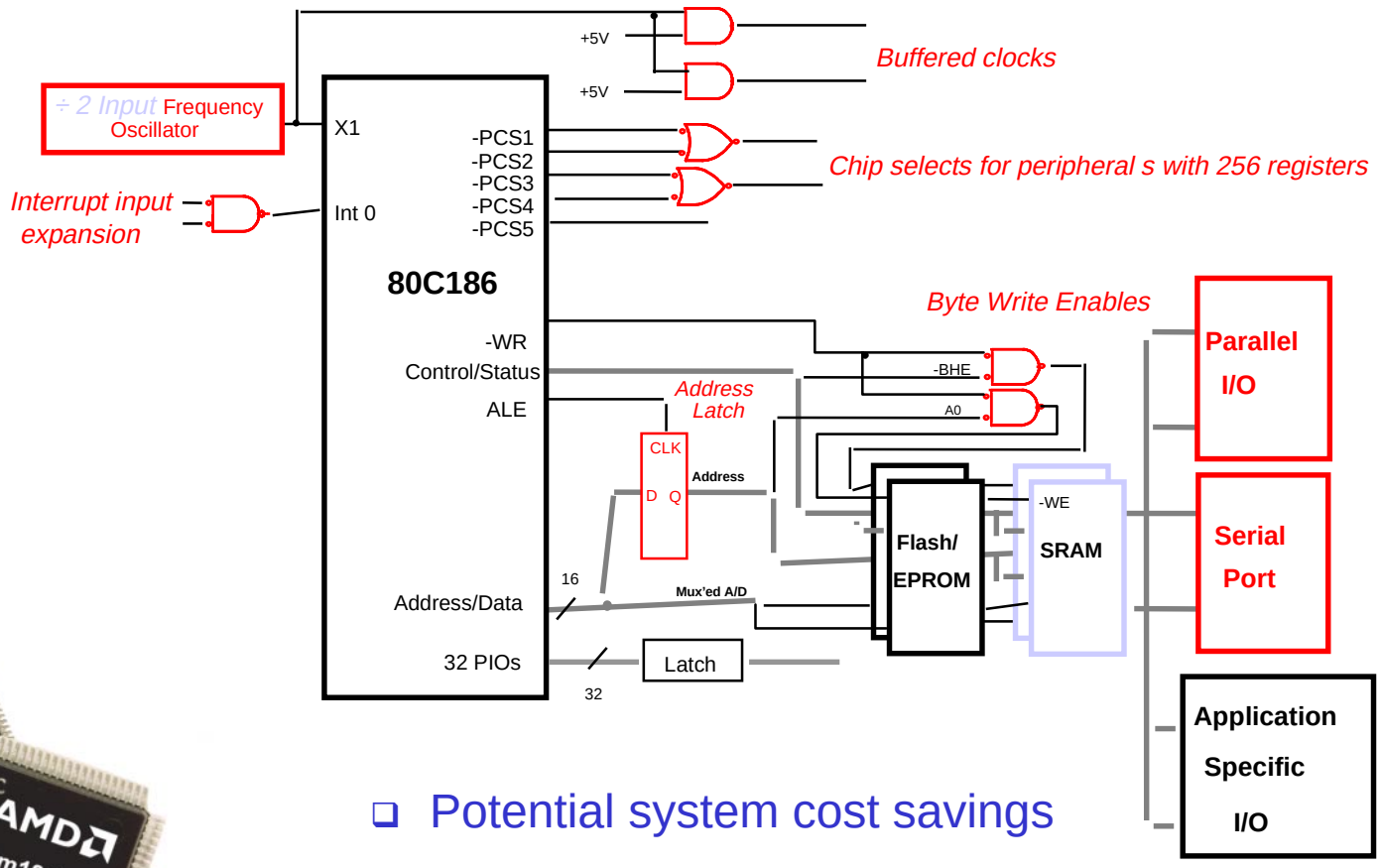
Am186 System Evolution

	80C186 Based 3.37 MIP System	Am186EM Based 5.35 MIP System	Am186ER Based 6.6 MIP System
Internal	CPU Basic System Logic	CPU Basic System Logic Advanced System Logic	CPU Basic System Logic Advanced System Logic RAM
External	Advanced System Logic RAM FLASH	RAM FLASH	FLASH

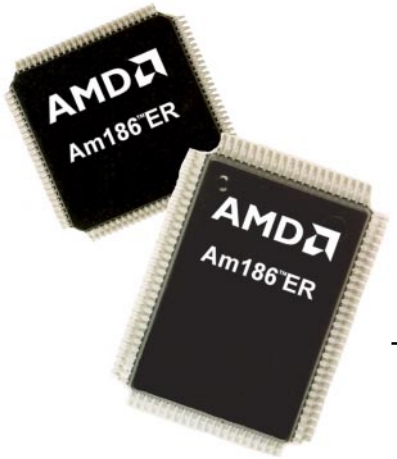


Systems in Silicon

Typical 80C186 Design

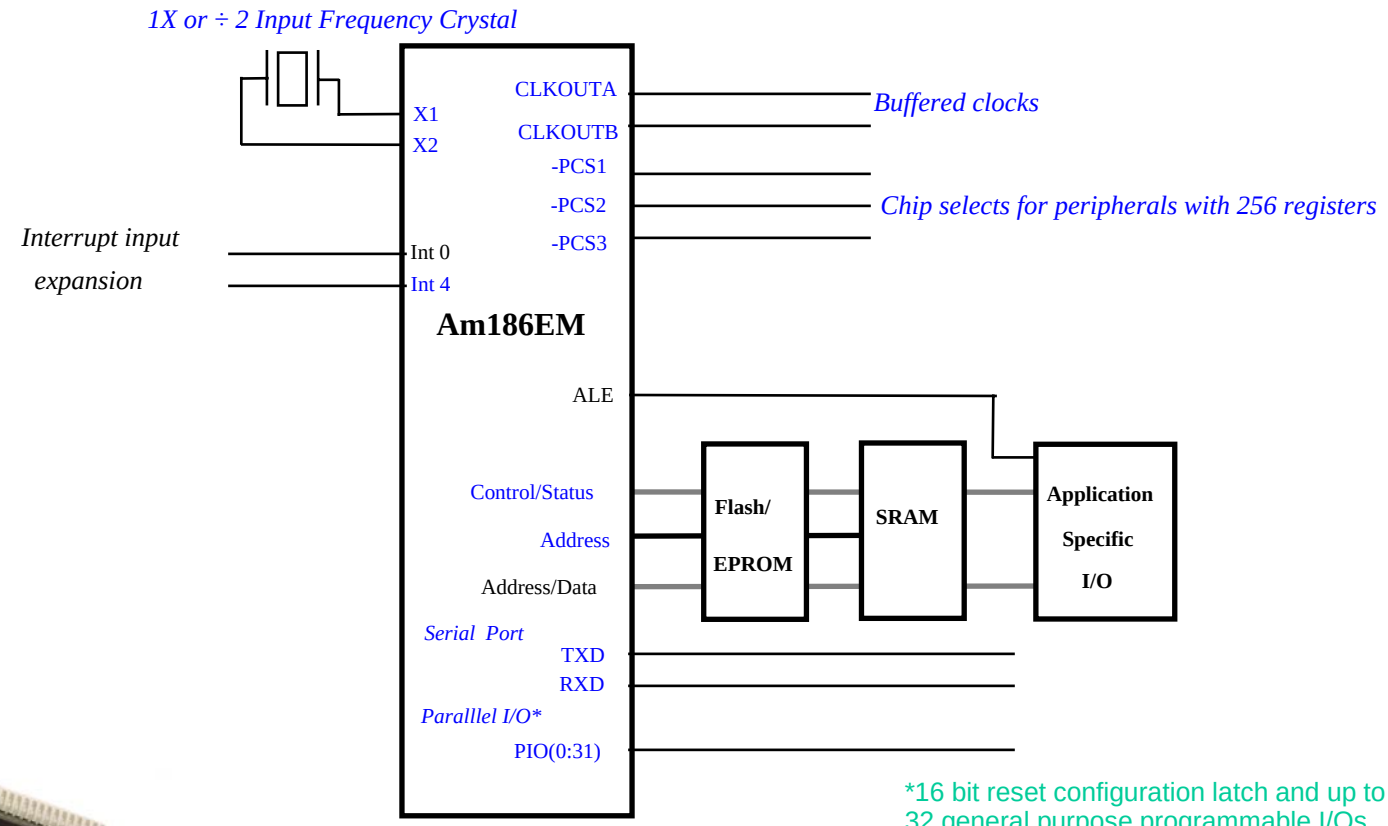


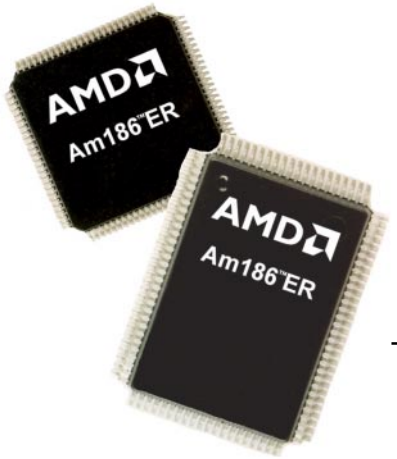
- Potential system cost savings



Systems in Silicon

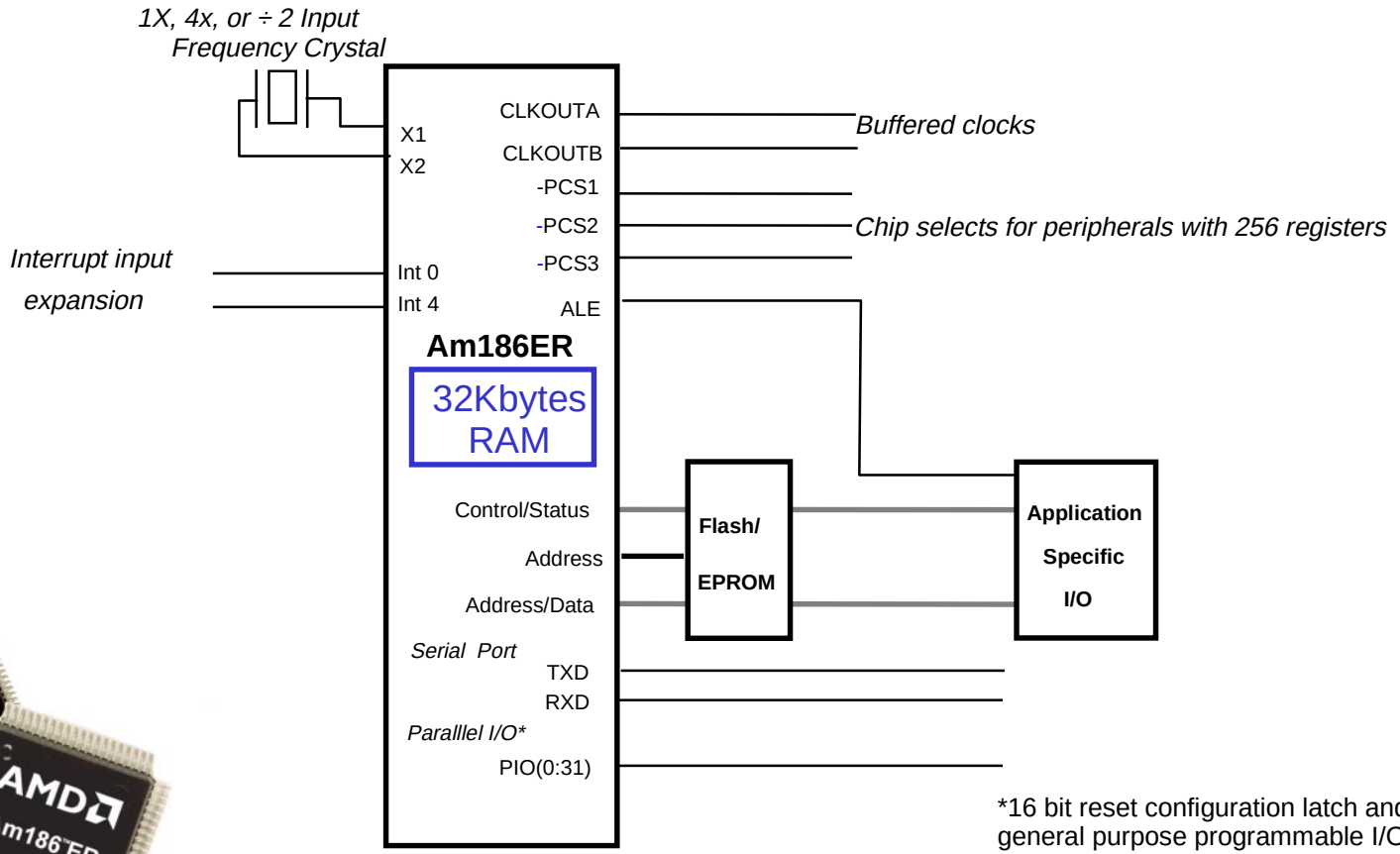
Typical 80C186EM Design
(Glueless System Bus)

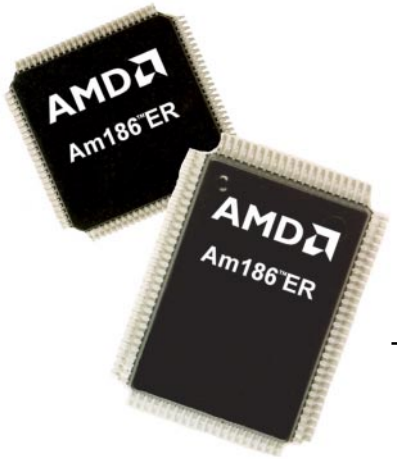




- **New or Enhanced Features**

Typical Am186ER Design
(Glueless System Bus & Integrated RAM)

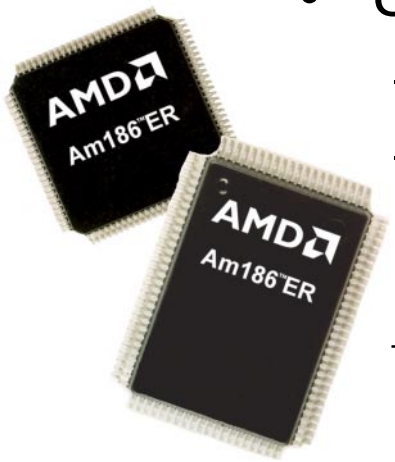




Systems in Silicon

Am186/188ER vs. 80C186/188

- Software compatible with 80C186/188
- 25 to 50MHz
  - Higher performance options
- Glueless connection to memory
  - Lower system cost
- Demultiplexed address bus
  - Zero wait state using commodity memories
- Use Am188ER to replace low frequency 80C186
  - 25 MHz Am188ER equals12 MHz 80C186 performance
  - Save on routing and space while using cheaper x8 components



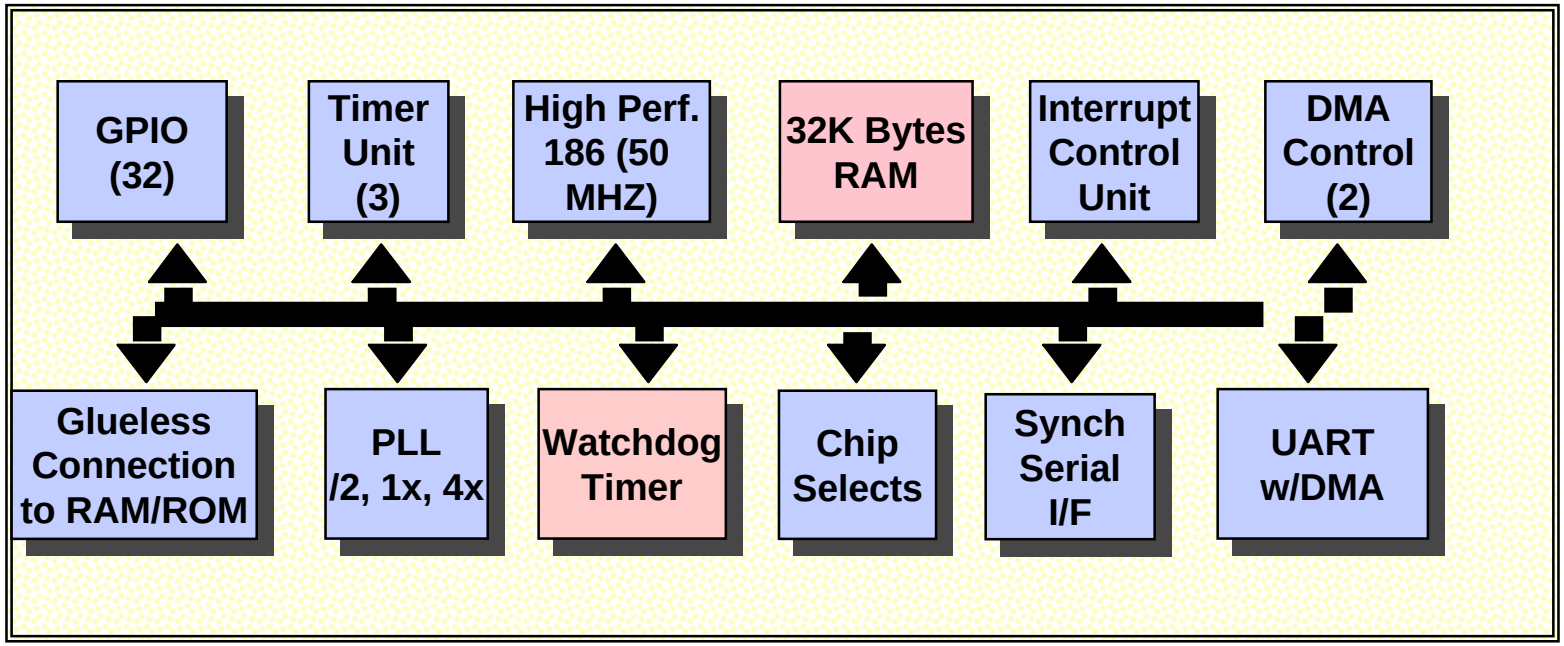
Systems in Silicon

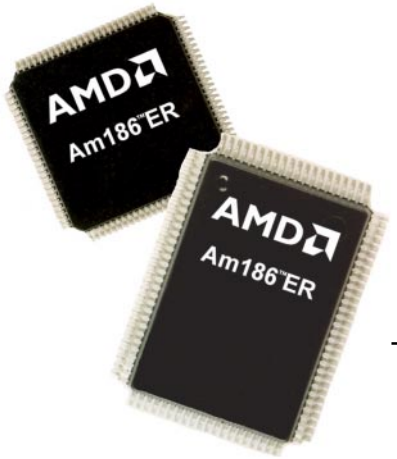
Am186/188EM vs. Am186/188ER

- No wait state internal RAM
  - 16Kx16 for Am186ER, and 32Kx8 for Am188ER
  - Visible for debugging
- Low Power
  - 3.3v Vcc with 5V tolerant IO
  - TTL compatible
  - Integration of RAM reduces system power
- Multiple clocking modes
  - ½x, 1x, and 4x system frequency vs. input frequency
  - Use a 12.5 MHz crystal for 50MHz system
- Same 100 pin TQFP and PQFP package/pinout

Systems in Silicon

Am186ER Block Diagram



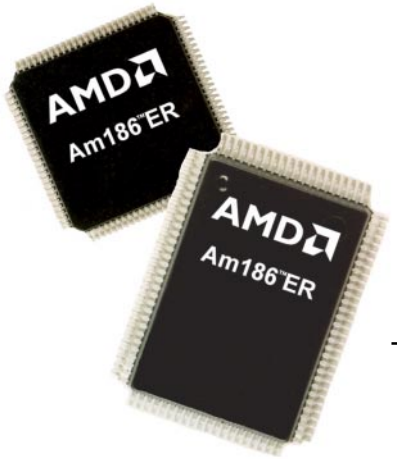


CPU voltage: ***3.3v w/5v tolerant I/Os***

Packages: ***100 PQFP and TQFP***

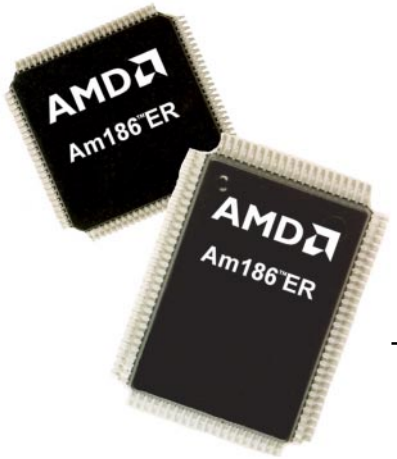
Systems in Silicon

Am186ER and Am188ER Features



Am186/188ER
New Features w/ Revision B

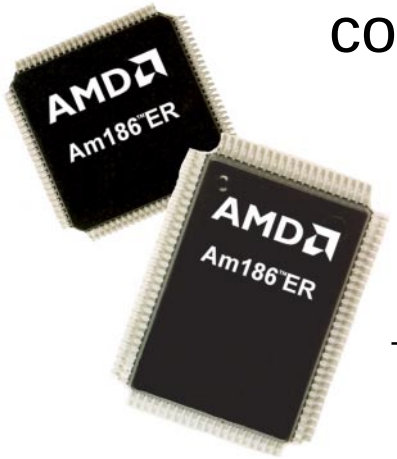
- Increased Performance - 50 MHZ - 6.6 MIPs
- DMA to/from asynchronous serial port
- Hardware Watchdog Timer
  - Generates NMI or reset



Am186/188ER Rev B Enhanced Features Con't

- Am186/188ER 40MHz max at Industrial Temp now available in both PQFP and TQFP
  - PQFP 25, 33 & 40MHz at Industrial Temp available
  - TQFP 25, 33 & 40MHz at Industrial Temp available

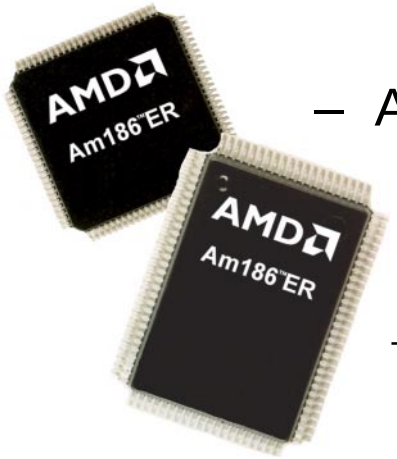
- If you are currently using an EM/EMLV or ES/ESLV and need to upgrade to a higher frequency industrial grade device (3.3V), consider the ER



Systems in Silicon

Am186ER/188ER Feature Set

- 32K Bytes of integrated RAM
- Asynchronous and synchronous serial ports
- Glueless interface to ROM, SRAM, PSRAM and FLASH
- 32 programmable I/Os
- Interrupt controller with 13 interrupt sources
- 3 timers (with pulse width modulation)
- 2 DMA channels and 13 chip selects
- Integrated PLL
  - two clockouts
  - system frequency is /2, 1x, and 4x the input frequency
- Am188ER gives 60% of the performance of Am186ER



On-Board RAM

- 16Kx16 for Am186ER and 32Kx8 for Am188ER
- Same performance as no-wait state external RAM
- Locatable on any 32 Kbytes Boundary
- Show reads on the address bus for easier debugging
  - Externally displays data from internal RAM reads
  - Show reads enabled in hardware or software
- Internal memory disable
  - Disable with hardware or software

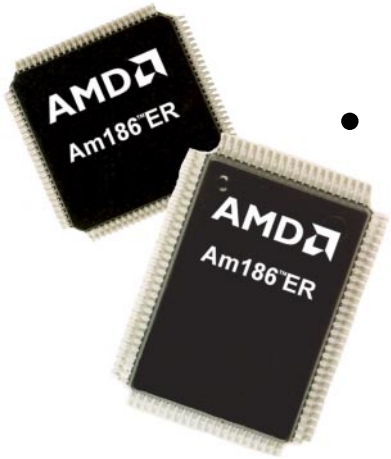
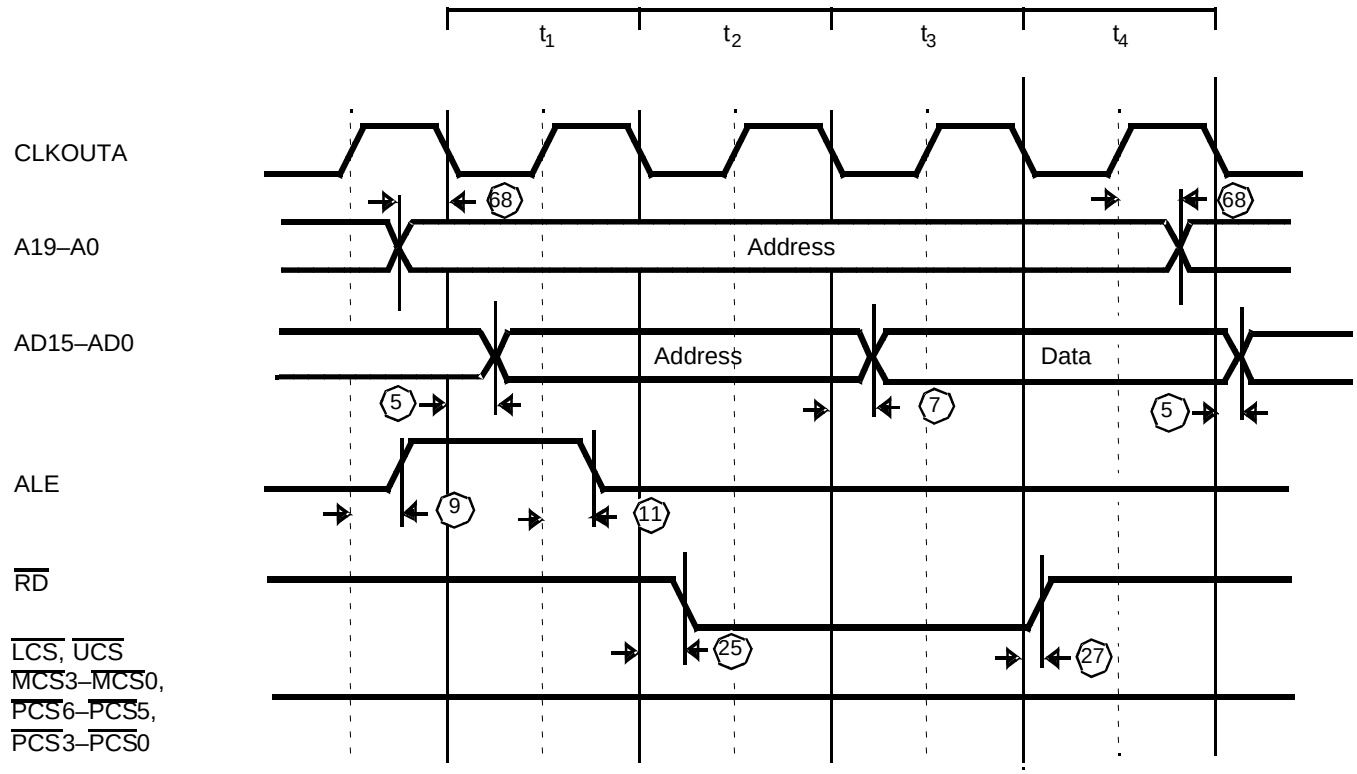
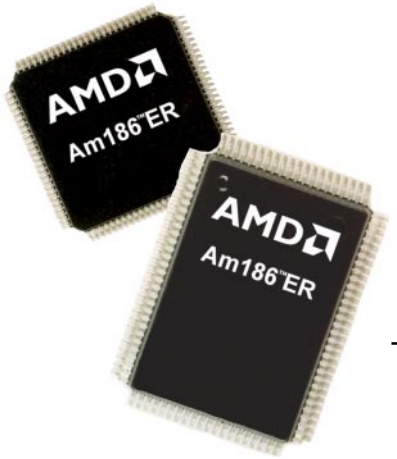


Diagram of the Show Reads

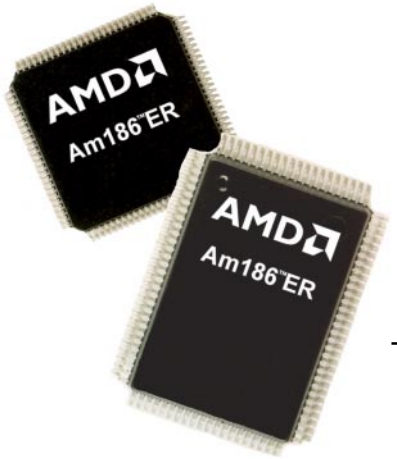
Internal RAM Show Read Cycle Waveform





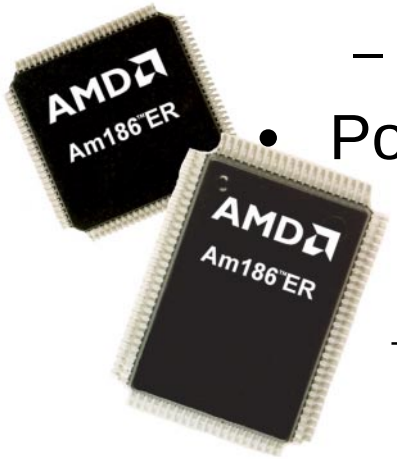
5V Tolerant I/Os

- Vcc on the Am186ER and Am188ER is 3.3V
  - Inputs are 5V tolerant
    - up to 2.6V over Vcc on inputs
  - Outputs drive TTL Logic
    - logic one to 2.4V
- Allows mixed voltage system
  - Supports legacy 5V components



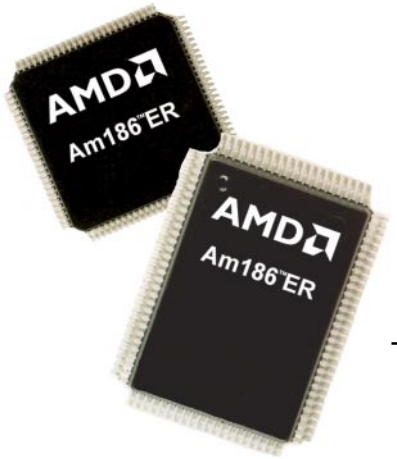
Clock and Power Management Unit

- Up to 50 MHz speeds
- Clock options
  - /2 for systems running lower than 20MHz
  - 1x for systems running between 16 and 40MHz
  - 4x for systems running between 16 and 50MHz
- 2 CLKOUT pins - program options:
  - Normal operating frequency
  - Power save frequency
  - Can be disabled
- Power save mode



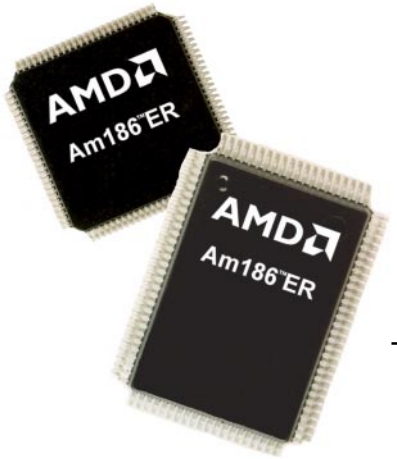
PRL Register

- Used for code to identify product and revision
  - Indicates the current release level of the processor
  - Specifies either the 8 bit or 16 bit controller
- Revision B
  - Am186ER = 28h
  - Am188ER = 29h



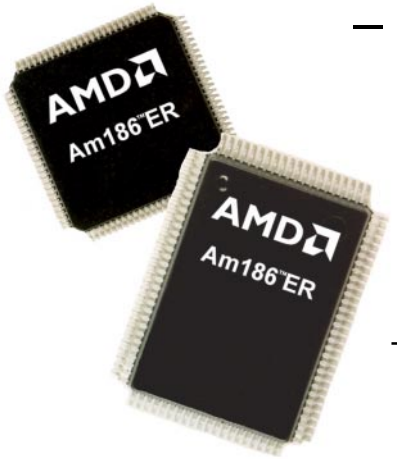
Systems in Silicon

ER and EM Family: Common Features

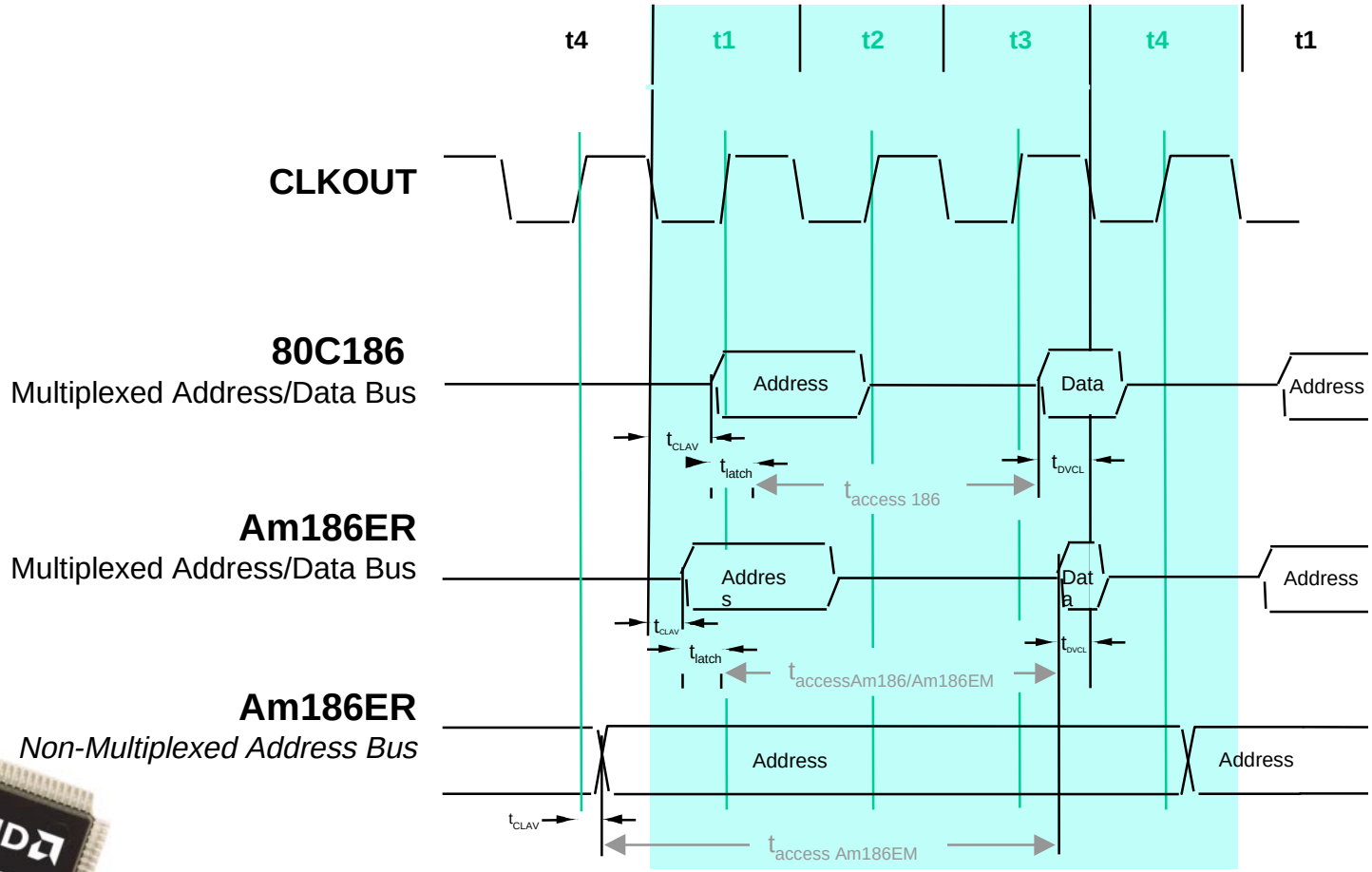


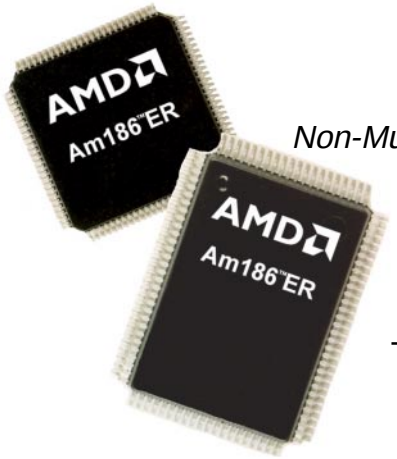
Demultiplexed Bus

- Am186ER demultiplexed address & data bus yields:
  - Higher performance
    - Address available time increased
    - No ALE required
    - Data setup time decreased
  - Lower system cost
    - Eliminates glue logic needed to latch memory address
    - Using commodity memory reduces cost
  - Multiplexed bus still supported for peripherals



Demultiplexed Bus Interface

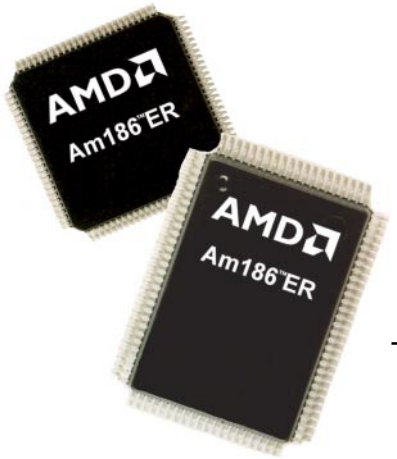




Systems in Silicon

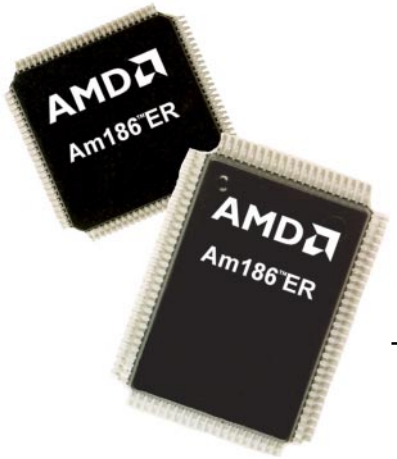
Asynchronous Serial Port

- Asynchronous protocol
  - Full duplex, 7 or 8 bit
  - Odd/even/no parity, 1 or 2 stop bits
- Interrupts
  - Tx, Rx, Break
  - Framing, parity, & overrun errors
- Baud rate generator
  - div = (CLK Freq) / (32 * Baud rate) - 1



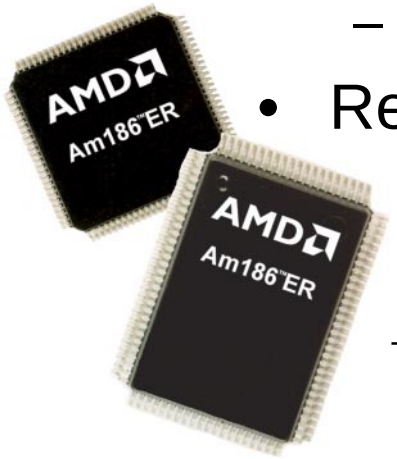
Synchronous Serial Interface

- High speed serial transfers
  - Up to 25 Mbits/s at 50MHz
  - Half-duplex bi-directional
  - ASIC or Mach™ control
  - Master with up to 2 slaves directly supported with enables
    - more than 2 slaves supported with PIOs
  - Operates in polled mode only
  - SCLK at 1/2, 1/4, 1/8 and 1/16 CPU clock



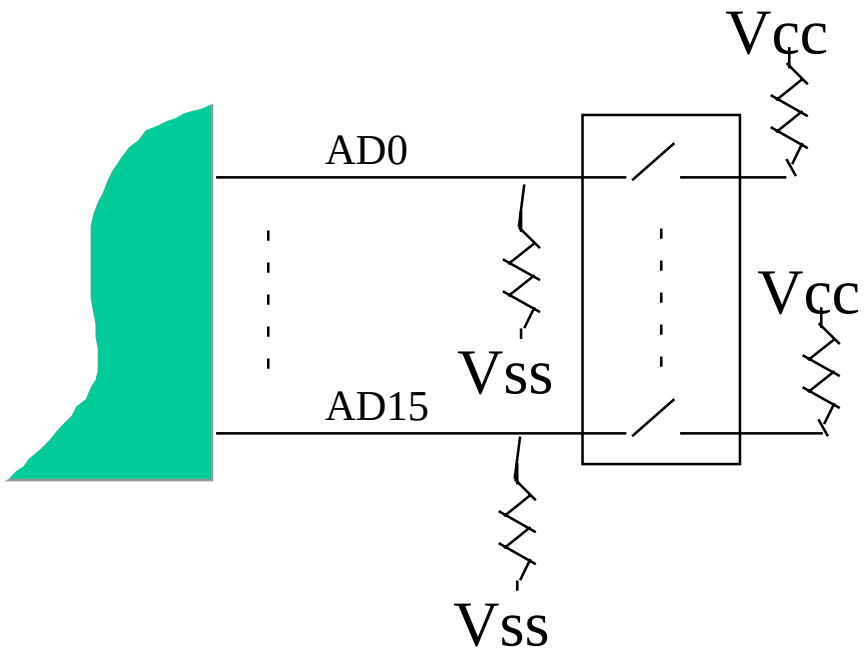
32 Programmable I/O Pins

- Up to 32 PIO pins are available for I/O if their alternate functions are unused
  - Input
  - Input with weak internal pull-up/pull-down
    - polarity depends on original pin
  - Output
  - Open-drain output
- Multiplexed with other signals
  - Default depends on pin
- Read or written through the peripheral control block



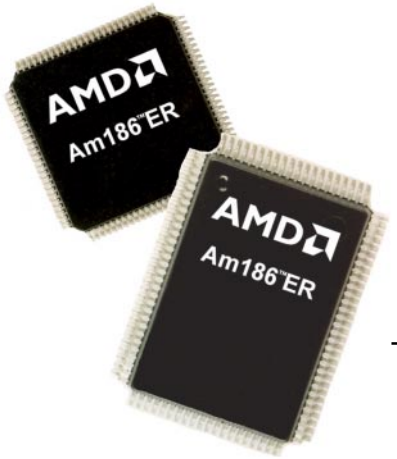
16-Bit Reset Configuration Register

The reset configuration register function is to store data from the AD bus at reset. The illustration below demonstrates this.



Systems in Silicon

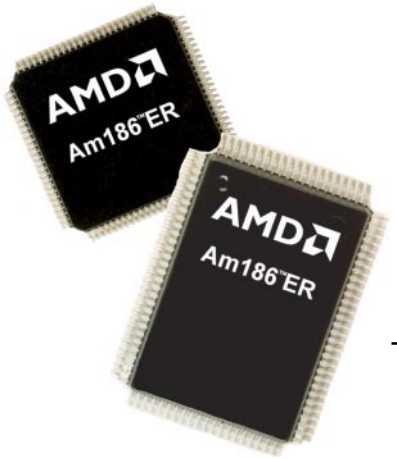
80C186, EM, and ER Family: Common Features



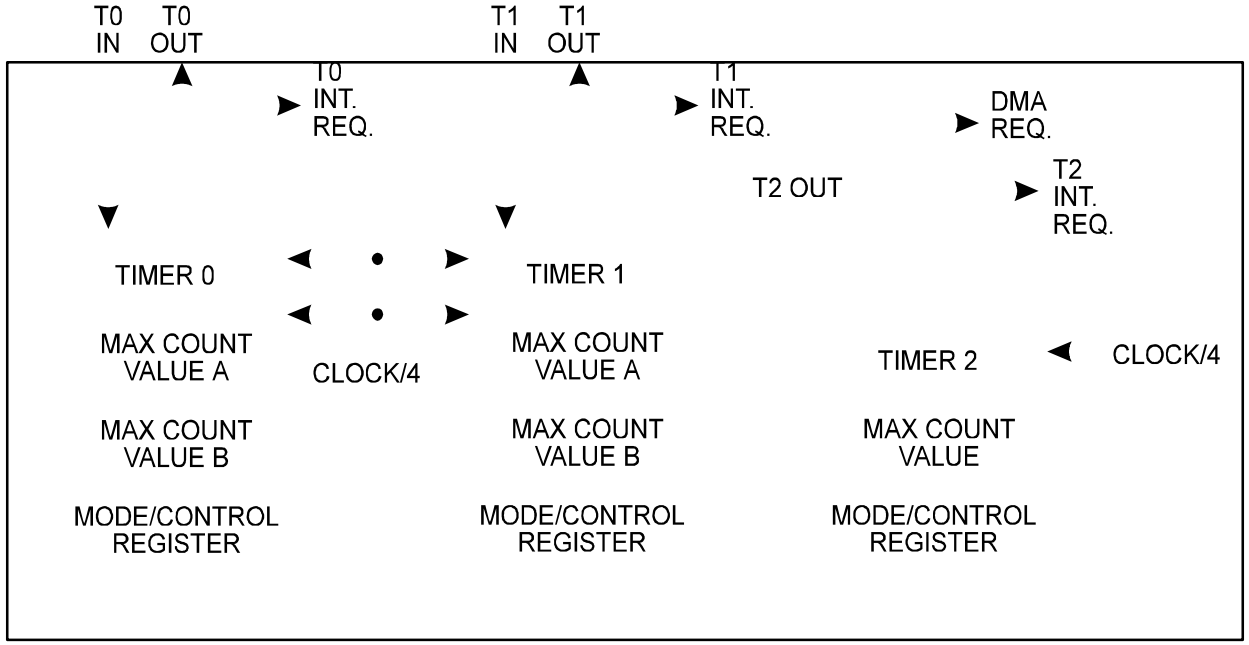
Systems in Silicon

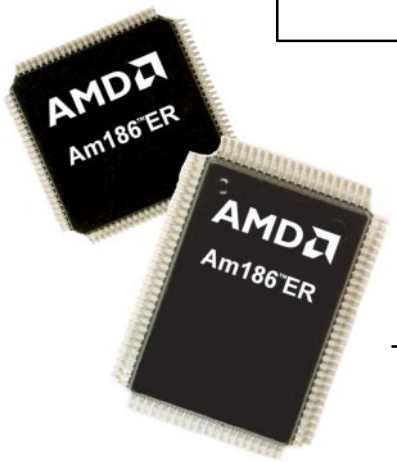
Three 16-bit Timers

- Same as the 80C186
- Watchdog timer functionality added to timer 1
- Supports pulse width modulation
- Can re-trigger on external events
- Continuous or one-shot count
- Can generate interrupt on terminal count
- Chainable interrupts



Three 16-bit Timers(cont.)



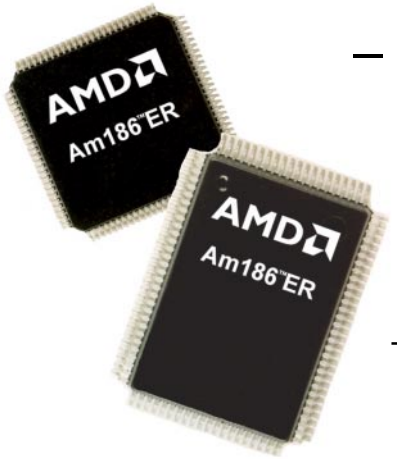


§ Inside the line indicates I/Os internal to the timers

Systems in Silicon

Chip Selects

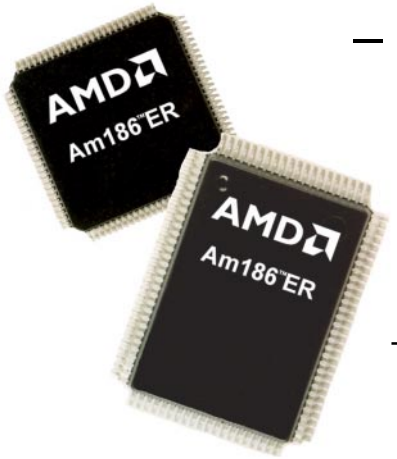
- 6 chip-selects (PCS) with a range of 256 bytes for use with peripheral devices
  - Mapped to memory or I/O space
- 4 chip-selects (MCS) with a range of 2K to 128Kbytes
- 2 chip select outputs (UCS and LCS) for use in the top and bottom of memory map
  - Good for system code and external RAM
  - UCS is initial chip select after reset



Systems in Silicon

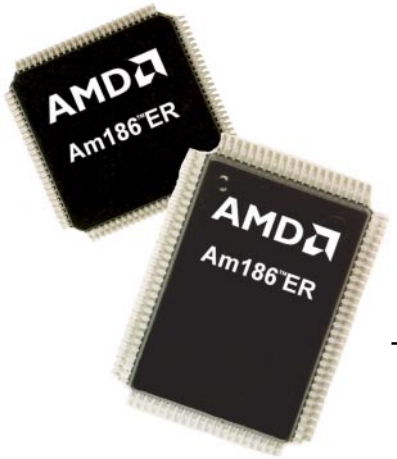
Two DMA Channels

- Same as 80C186
- DMA options
  - Mem-mem, mem-I/O, I/O-I/O
  - byte or word
  - 2 Bus cycles per transfer (read followed by a write)
  - Interrupt after last transfer
  - DMA channel priority
  - DMA pointer increment/decrement/static
  - Synchronization - source/destination/none



DRAM Refresh Control

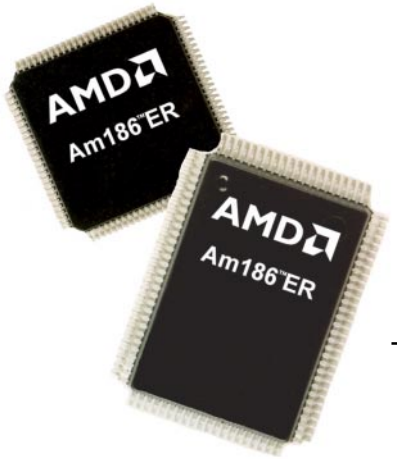
- Simplifies DRAM control logic
- Options
  - Refresh request rate
  - Enable/Disable refresh
  - PSRAM refresh handled with separate pin



Systems in Silicon

PIC - Peripheral Interrupt Controller

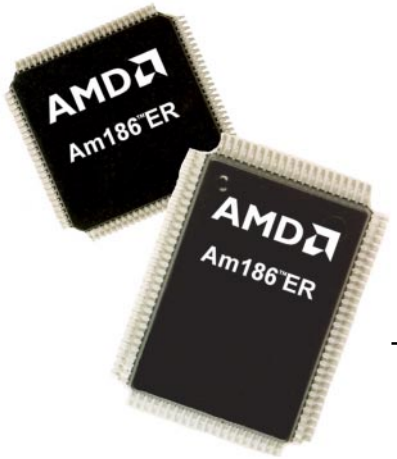
- Total of 13 interrupts
  - 7 internal interrupts
    - 3 timer interrupts
    - 2 DMA interrupts
    - asynchronous serial port interrupt
    - watchdog timer interrupt
  - 6 external interrupts
    - 5 maskable interrupt pins
    - 1 nonmaskable interrupt pin
- Edge or level sensitive
- Masked or slave mode options



Systems in Silicon

Hardware Watchdog Timer

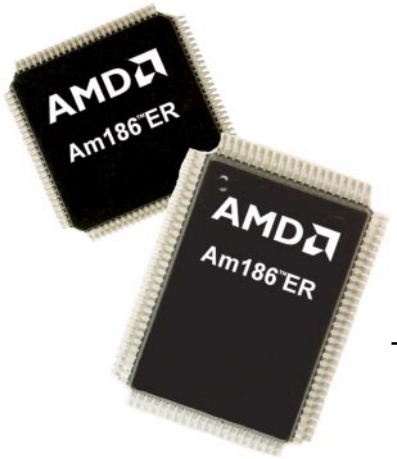
- Recover from software hangs
- Generates NMI or system reset
- 1.34 ns timeout at 50 MHz



Systems in Silicon

PCB - Peripheral Control Block

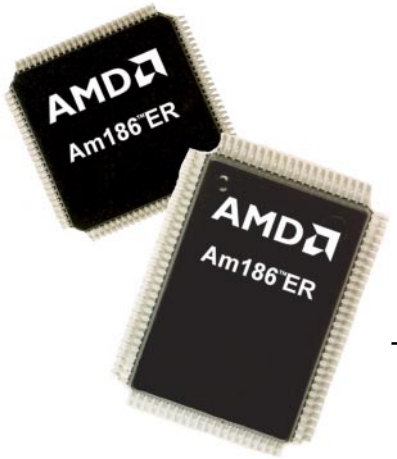
- 128 - contiguous 16-bit register
- Provides access to all internal peripherals
- Mapped anywhere in memory or I/O space



Systems in Silicon

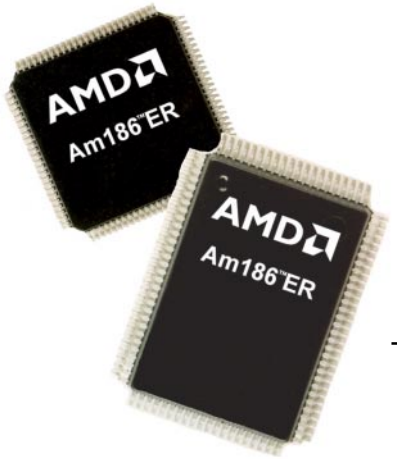
ONCE Mode
"On Circuit Emulation"

- Can be used for board testing
- Useful in debugging
- Tri-states all pins
- Activated by tying UCS & LCS low at reset



Systems in Silicon

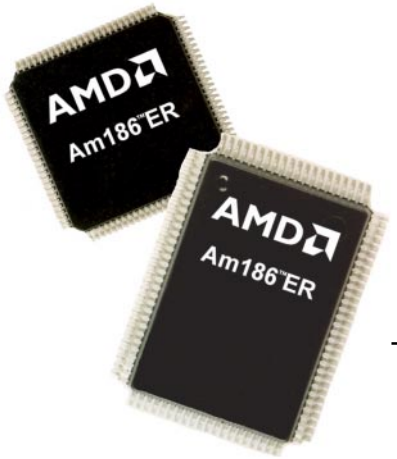
Options and Timeline for the Am186ER and Am188ER Revision B



Systems in Silicon

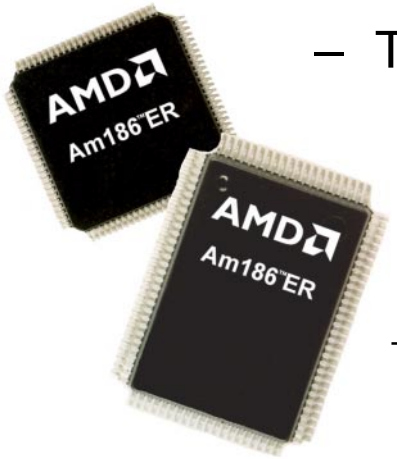
Schedule Am186/188 (Rev B)

- Announcement: March 31, 1998
- Data Sheet (printed) : March 31, 1998
- User's manual (printed): March 31, 1998
- General Samples Available: May 1998
- Demo Boards Available: May 1998
- Production Starts: 3Q98



Am186/Am188ER Notes

- The existing Am186/188ER is in full production.
- Rev B yields higher performance and more features.
- Design-ins should occur with Rev B silicon.
- Rev B is backward compatible with Rev A with only 1 exception.
  - In external clocking configuration for an oscillator, X2 pin should float instead of being grounded as in Rev A. For a crystal configuration, no changes are required.
  - This change was required to improve the oscillator.



Systems in Silicon

Options

-50 V C \W

Am186ER

LEAD FORMING

\W = Trimmed and Formed

TEMPERATURE RANGE

C = Commercial(Tc = 0 to 100 C)

Tc = Case temperature

DEVICE NUMBER/DESCRIPTION

Am186ER = High-Performance, 10C186-Compatible 16-Bit Embedded Microcontroller with 16Kx16 Internal RAM

Am188ER = High-Performance, 80C188-Compatible 16-Bit Embedded Microcontroller with 32Kx8 Internal RAM

PACKAGE TYPE

V=100-pin thin quad flat pack (TQFP)

K=100-pin plastic quad flat pack(PQFP)

SPEED OPTION

-25=25MHz

-33=33MHz

-40=40MHz

-50=50MHz