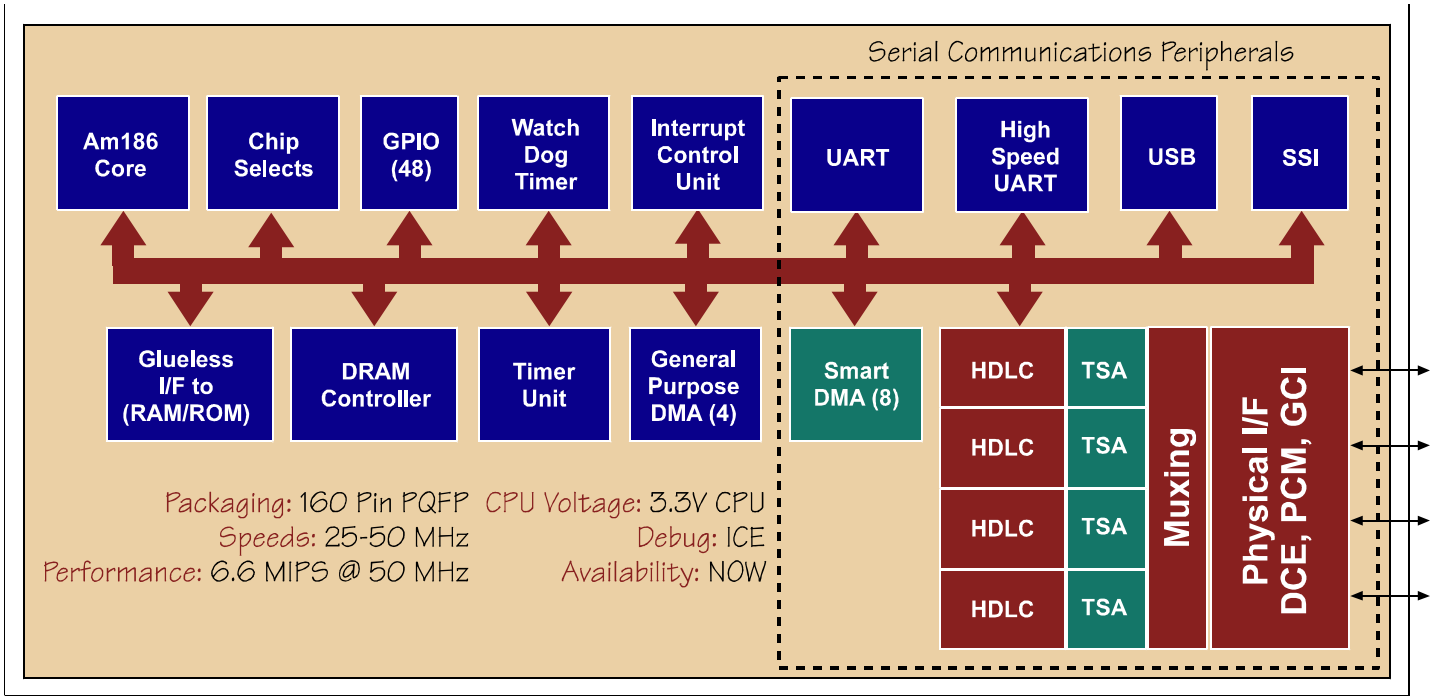
Systems in Silicon

Am186CC Microcontroller

Product Features

Am186CC Block Diagram



Am186CC Features
Performance, Package, Operating Range

- Enhanced, High performance 16 bit X86 core
- 6.6 MIPs (Dhrystone 2.1)
- 50MHz operation (Max.)
- 0.32 um CMOS
- 3.3v +/- 0.3v with 5v tolerant I/Os
- 25, 40, and 50MHz speed grades (commercial)
- 25 and 40 MHz speed grades (industrial)
- 1X, 2X, 4X clocking modes
- 160 pin PQFP

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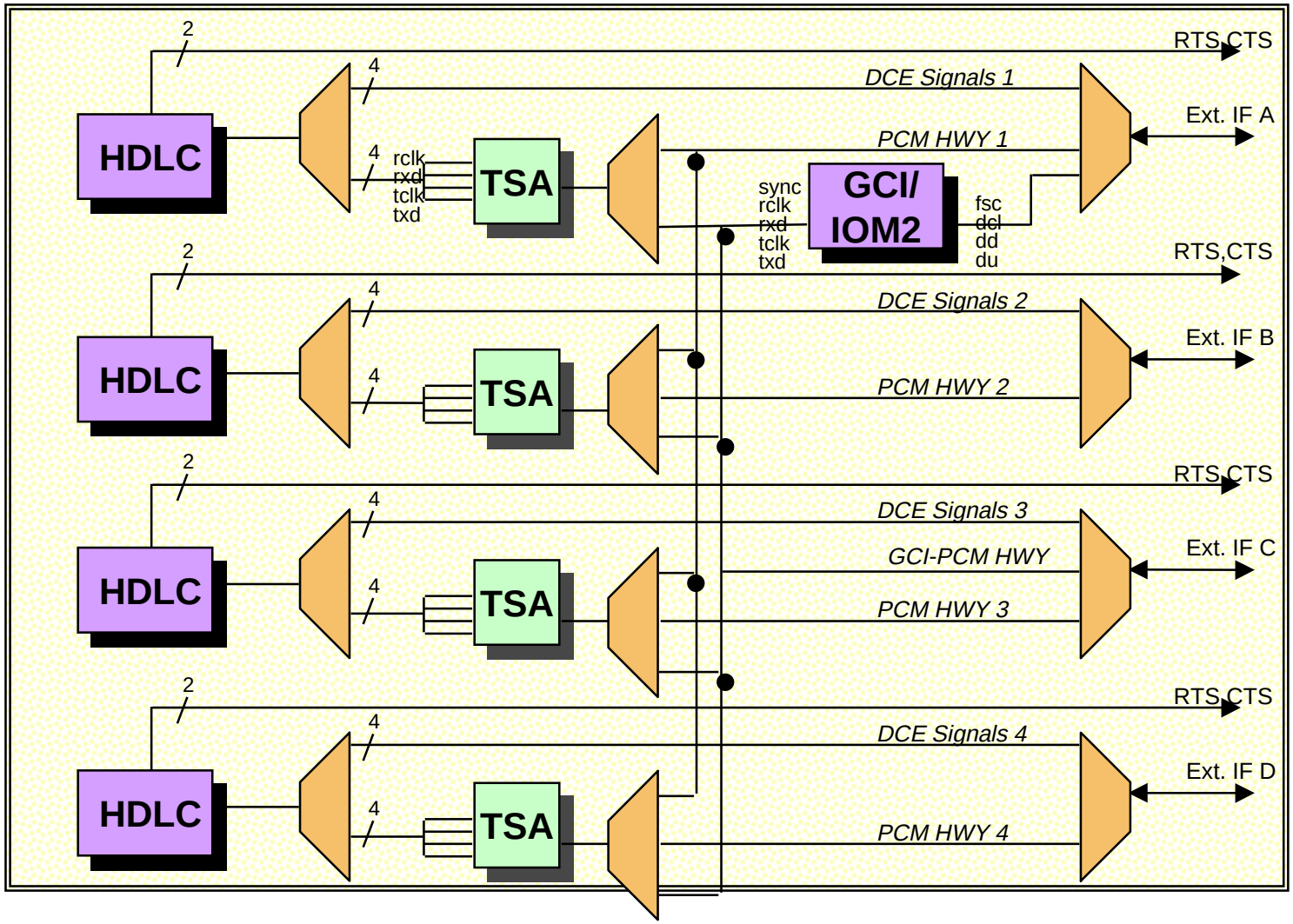
Communication Peripherals

HDLC, TSA, GCI, SmartDMA

Am186CC Serial Interfaces

- The Am186CC has 8 serial interfaces
  - 4 HDLC channels
  - USB
  - 2 UARTs (one muxed with HDLC channel D)
  - Synchronous Serial Interface

Am186CC: External Interfaces



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HDLC Highlights

- Data rates to 10Mbps
- Each HDLC controller may be configured as:
  - DTE device
    - Single drop or multidrop, half or full duplex
    - Flow control and collision detection
  - GCI/PCM highway controller
    - Time Slot Assigner allows selection of any contiguous set of bits in a frame
    - Direct interface (PCM highway) or shared channel A interface (either)
    - HDLC or transparent (voice) data

HDLC Highlights Part 2

- Protocol support includes HDLC, SDLC, LAPB, LAPD, PPP, V.110
- Polled/interrupt or SmartDMA operation
  - SmartDMA reduces software overhead
- 16 byte transmit FIFOs / 32 byte receive FIFOs
  - Reduces overflow/underflow conditions
- Address comparison on receive
  - Ignores frames destined for other devices (multidrop)

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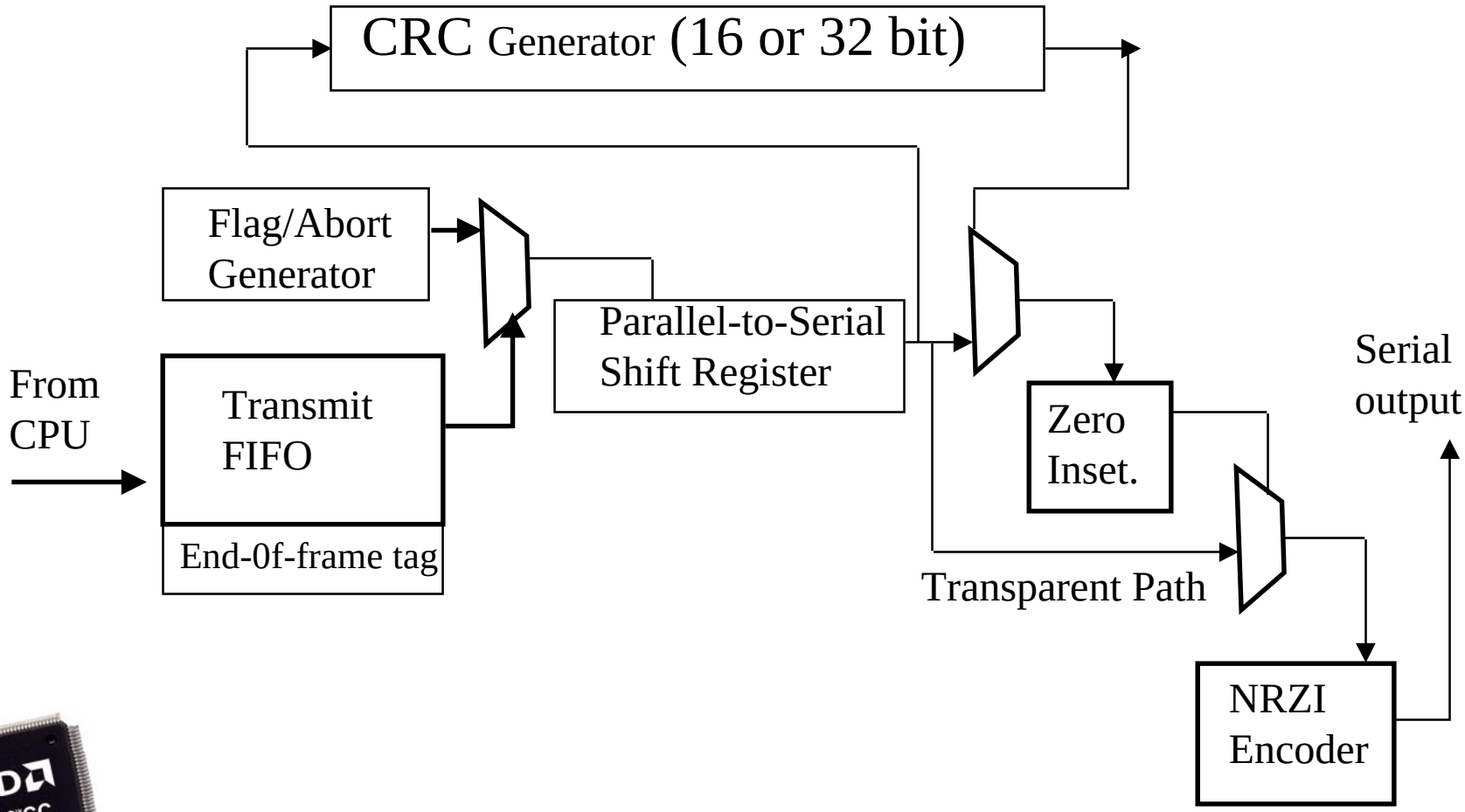
HDLC Highlights Part 3

- NRZ or NRZI operation
- Flags or mark idles
  - Flag idles maintain clocking in NRZ applications
  - Mark idles required for multidrop configurations
- Tri-state, open-drain, or totem-pole transmitter options
  - Open-drain useful for multidrop

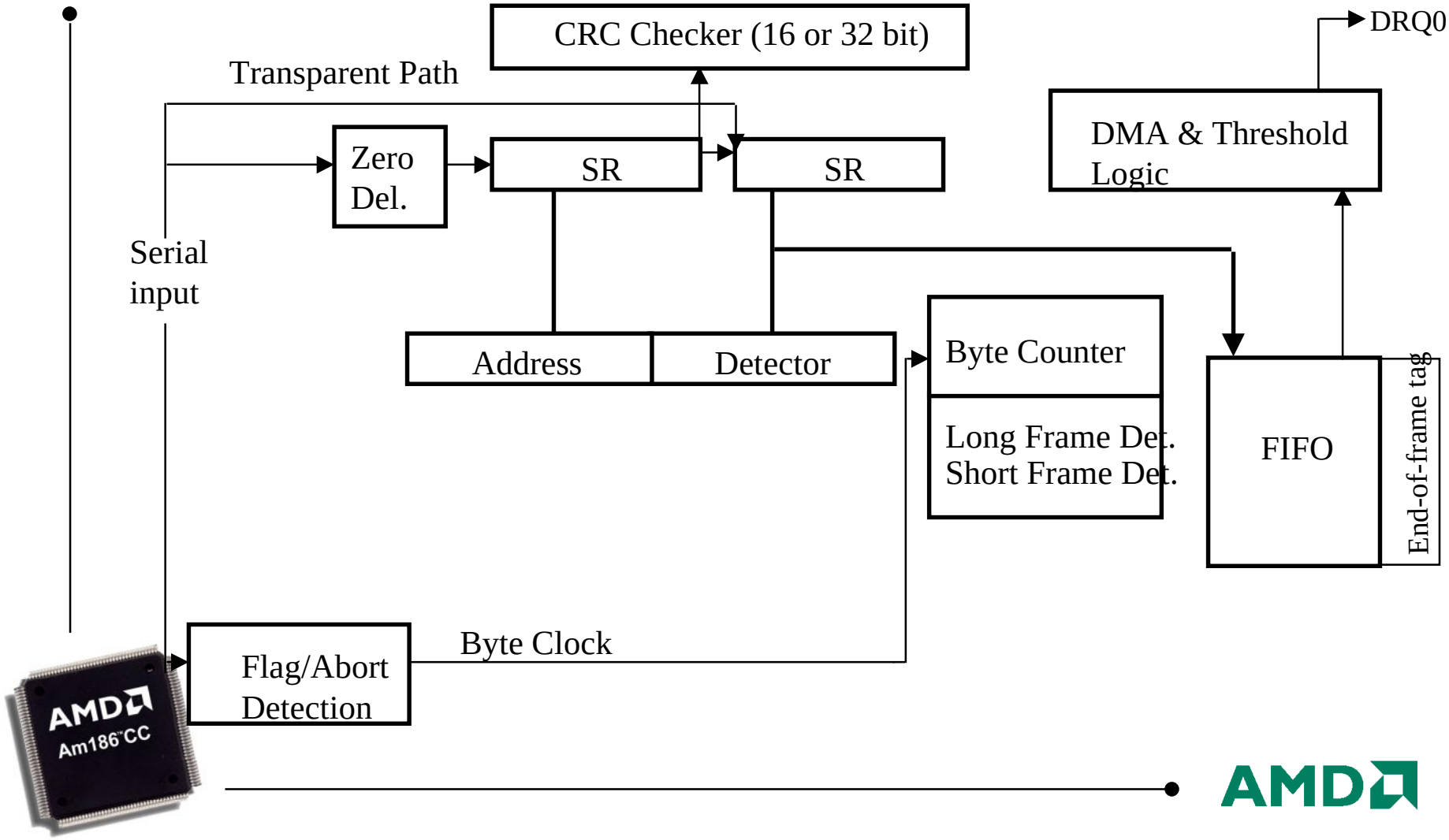
HDLC Highlights Part 4

- Collision detection operation
  - CTS tied to open-drain data output
  - Mark idles, NRZ programmed
- GCI D channel contention resolution
  - HDLC operates in conjunction with GCI controller to automatically contend for the D channel
- Transmit/receive clocks have programmable polarities
- Error statistics counters help monitor line quality

HDLC Transmitter Block Diagram



HDLC Receiver Block Diagram



Time Slot Assigners

- Four independent TSAs, each one dedicated to an HDLC.
- Ability to isolate time slots from 1 to 4096 sequential bits of the time division multiplexed (TDM) frame.
- Start and Stop bit times to isolate bits in frame
- TDM bus can have 512 8-bit time slots
- Support the isolation of B-channel and D-channel time slots from the HDLC to/from the IOM2 bus.
- TSA allows the HDLC to support reduced data rate channels of 8, 16, 24, 32, 40, 48, 56, or the full 64kbs data rate.
- IOM2, E1, T1, PCM Highway

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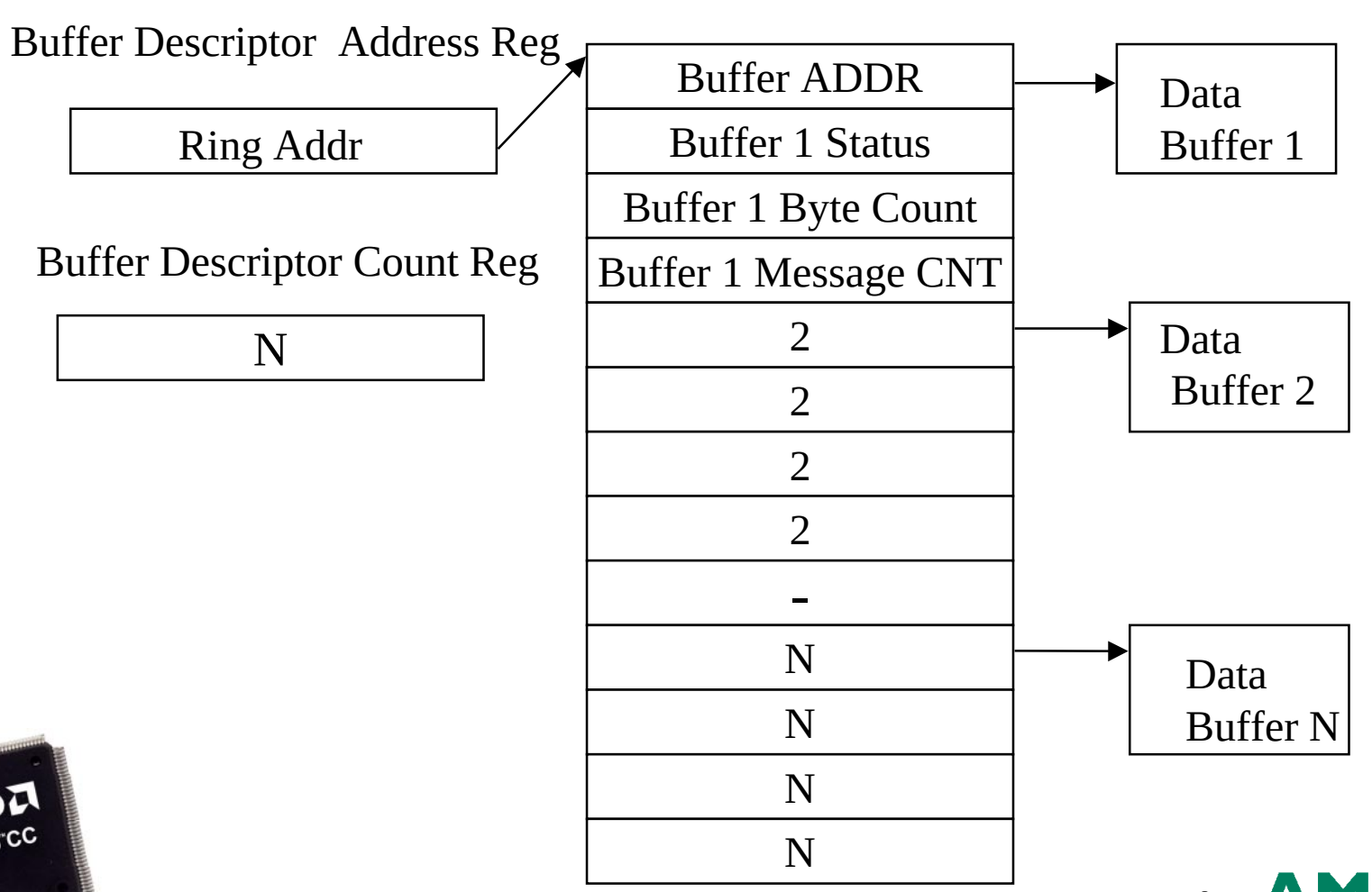
GCI Highlights

- GCI controller provides glueless connection to GCI/IOM2 XCVRs
- GCI Terminal mode only (not line card mode)
- 4 pin GCI connection (DD, DU, DCL, FSC)
- GCI ==> PCM Highway clock/frame synch conversion available for PCM Highway Codecs
- Supports Monitor, C/I, and TIC channels
- Supports Bus Reversal for Codec status/control

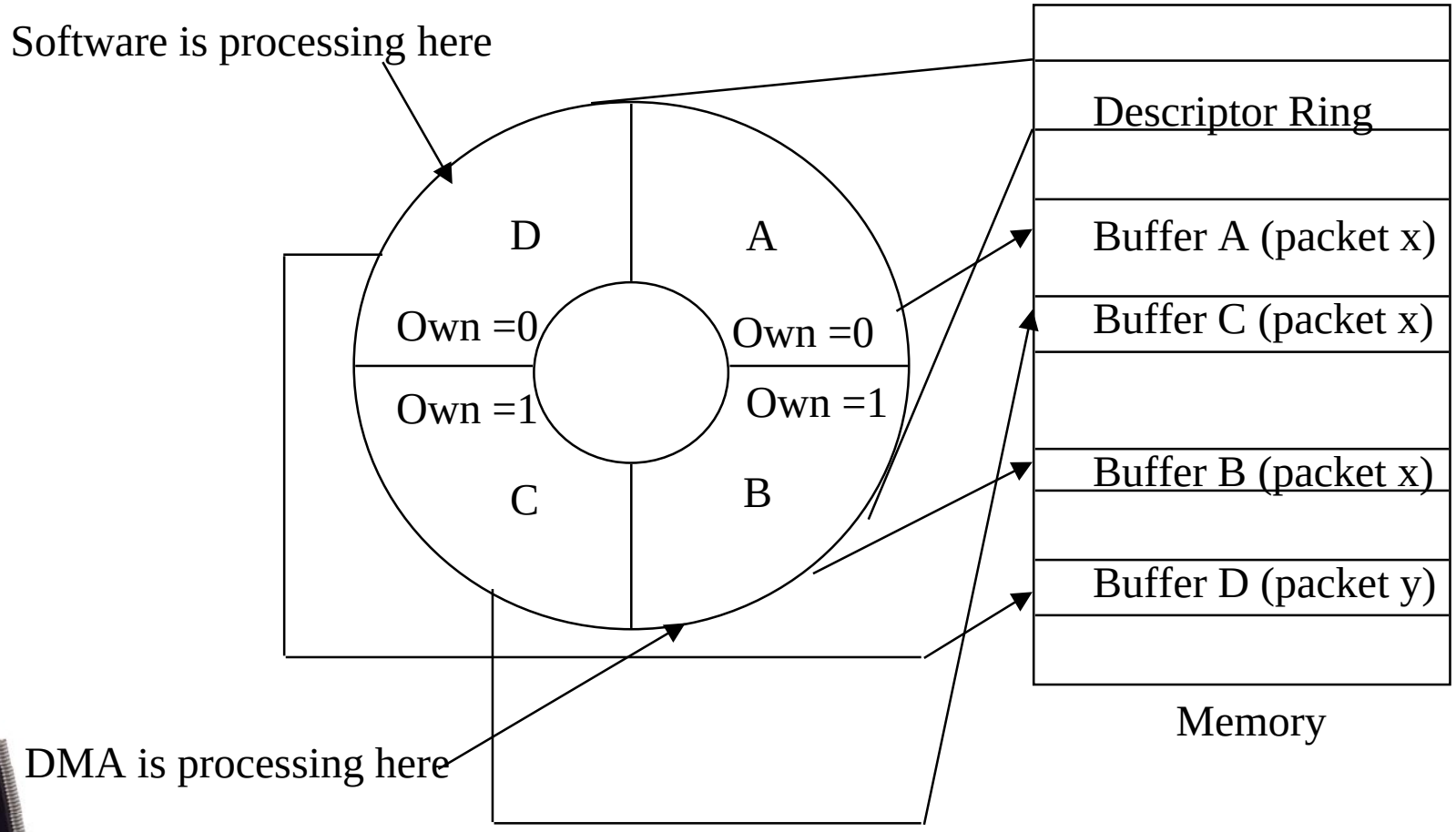
Am186CC SmartDMA Channels

- 4 pairs of SmartDMA channels
  - Each pair has one dedicated transmit channel and one dedicated receive channel
  - Pairs 0 and 1 are always mapped to HDLC channels A and B
  - Pair 2 may be mapped to HDLC channel C or to USB data endpoints A and B
  - Pair 3 may be mapped to HDLC channel D or to USB data endpoints C and D
  - Each pair has a programmable priority

SmartDMA descriptor buffer



SmartDMA Descriptor Ring



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Am186CC USB

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Am186CC USB Controller

- USB version 1.0, 1.1 & 2.0 Full speed device compliant - external short protection required for 1.1 & 2.0 compliance
- Self powered applications
- Integrated USB transceiver (D+/D-)
- 6 total endpoints (control, interrupt, 4 data endpoints)
- 3 configurations supported, 8 interfaces
- 7 alternate settings per interface
- General purpose or SmartDMA support available

Am186CC USB Controller

- Endpoints
  - Control endpoint: Bidirectional, max packet size of 8 bytes
  - Interrupt endpoint: In, max packet size is 8 or 16 bytes (16 byte FIFO)
  - 4 Data endpoints (A, B, C, D)
    - A: In or Out, 16 byte FIFO, interrupt, bulk or isochronous
    - B: In or Out, 16 byte FIFO, interrupt, bulk or isochronous
    - C: In or Out, 64 byte FIFO, interrupt, bulk or isochronous
    - D: In or Out, 64 byte FIFO, interrupt, bulk or isochronous
- SmartDMA or general purpose DMA support for data endpoints.

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Am186CC System Peripherals

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Am186CC System Peripherals

- High Speed UART
  - 460Kbaud, autobaud detection, FIFOs, special character/address matching, DMA support, independent baud rate generator input
- Low Speed UART
  - Typically used for debug, 7,8 or 9 bit transfers, DMA support, independent baud rate generator input
- Synchronous Serial Interface (SSI)
  - 25 Mbps maximum transfer rate, 3 pin, half duplex, bidirectional I/F
- Timers
  - Three 16-bit flexible timer/counters
- General purpose DMA
  - 4 Channels, 2 external DMA request lines

Am186CC System Peripherals (Con't)

- Chip selects
  - 14 chip selects for DRAM, ROM, I/O devices
- DRAM controller
  - EDO or Fast Page mode, 2 banks, symmetric 256Kx16 DRAMs supported
- General Purpose Programmable I/Os
  - 48 GPIOs, SET and CLEAR registers, 8 PIOs are interrupt sources
- Interrupt Controller
  - 17 external interrupt sources
- Hardware Watchdog Timer
  - Generates either Am186CC reset, system reset or NMI

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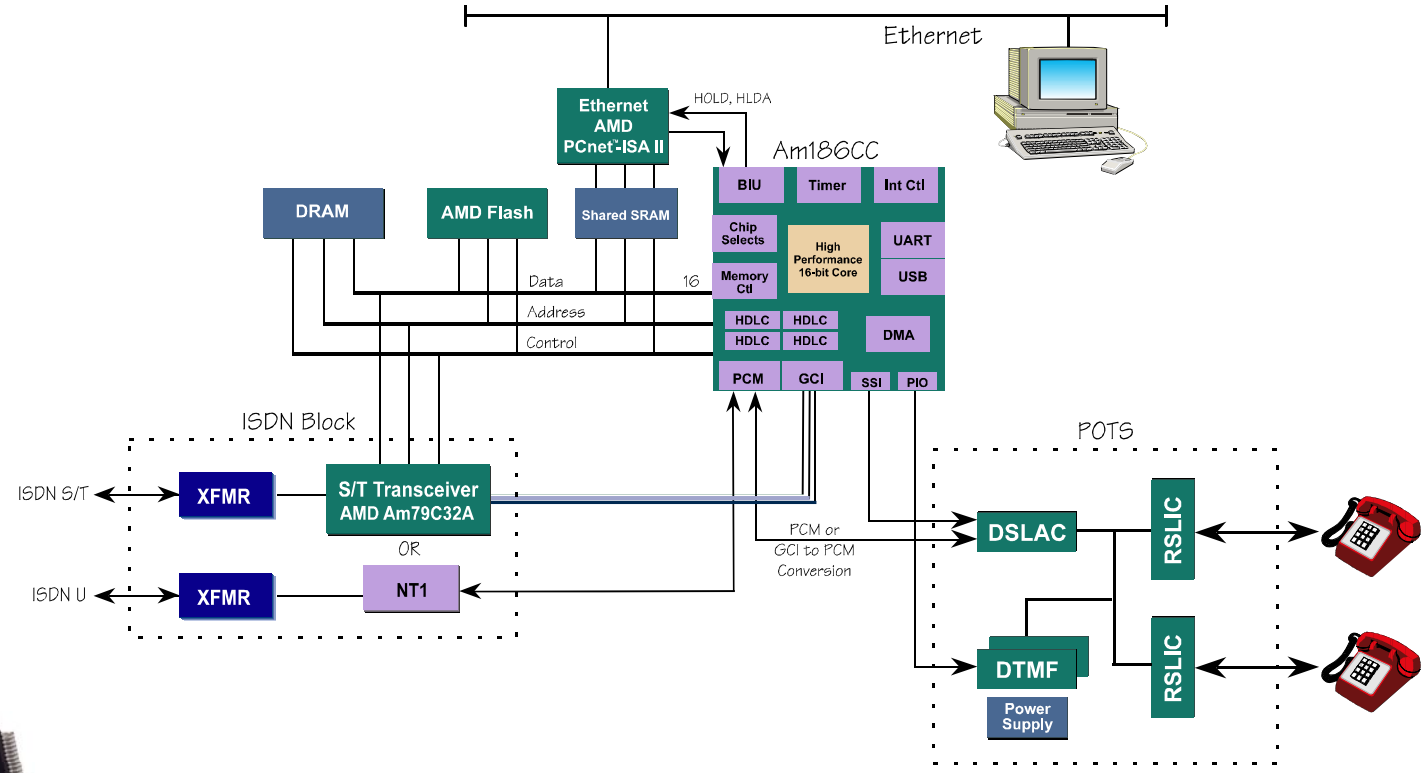
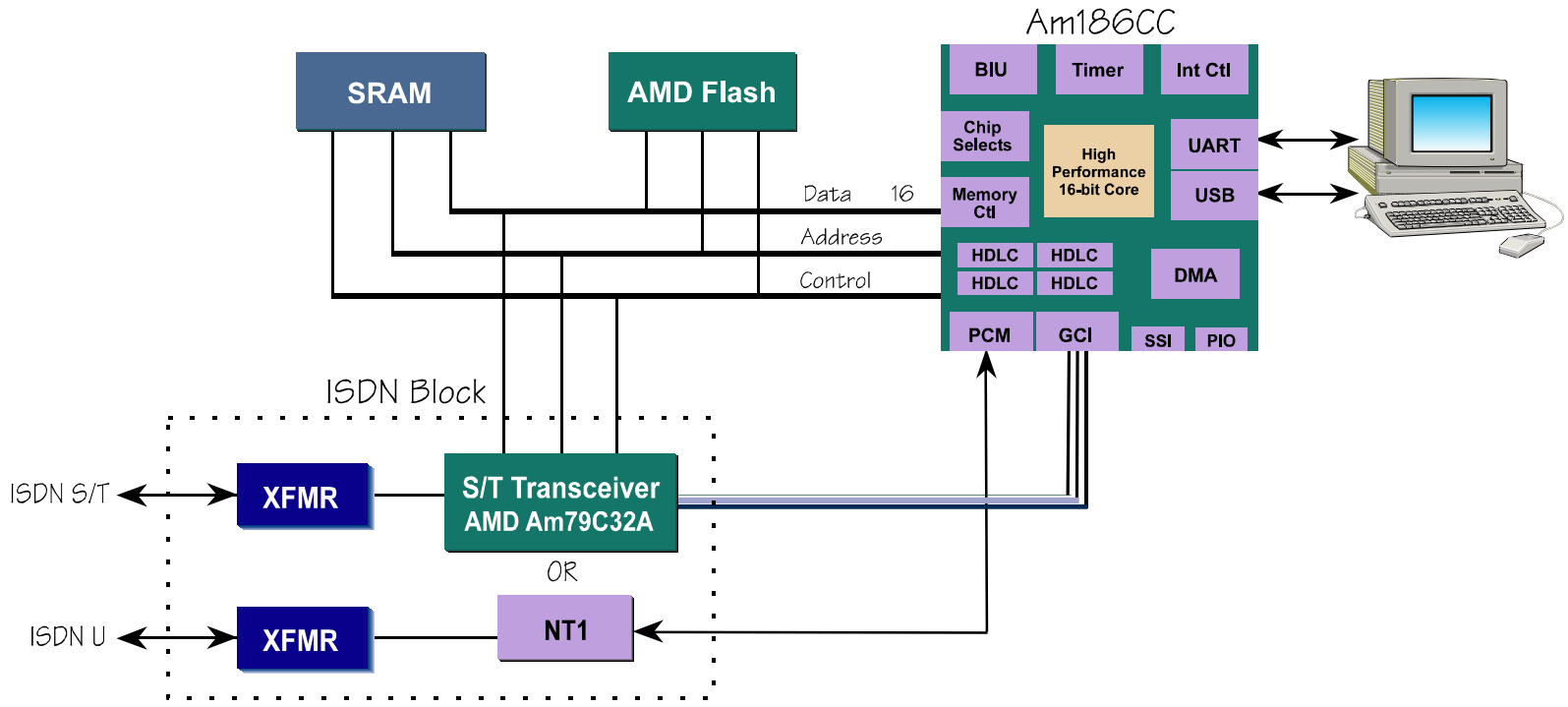
Am186CC Applications

Am186CC-Based
Low-End Router Reference Design



Am186CC-Based ISDN TA Reference Design



Am186CC-Based 32-Channel Linecard Design