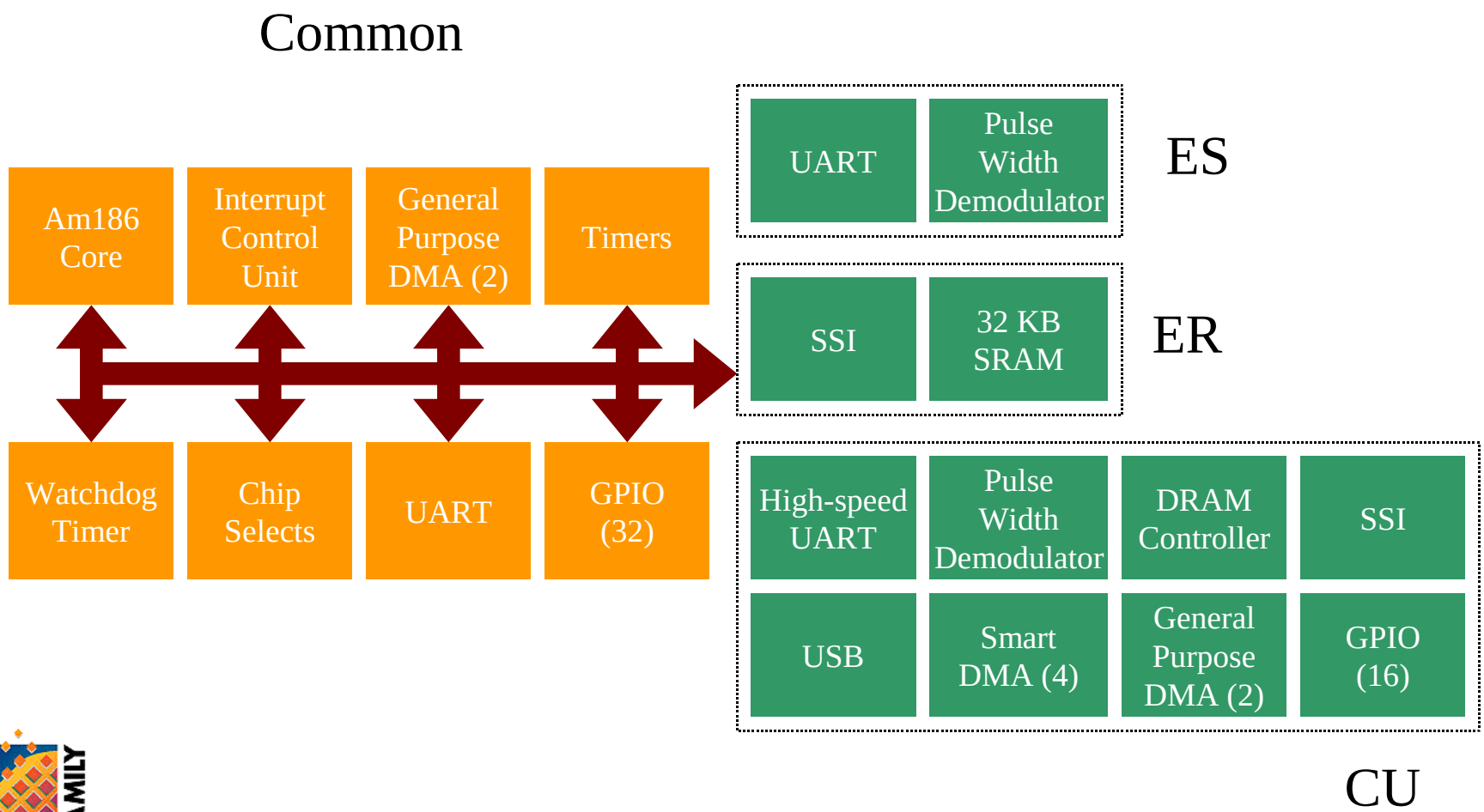
Am186™ES/ESLV, Am188™ES/ESLV Microcontrollers Migration Path

October 24, 2001

Summary

- Am186ES, Am188ES, Am186ESLV, Am188ESLV microcontrollers are not recommended for new design
- New customers interested in Am186/188ES/ESLV are encouraged to consider Am186/188ER or Am186CC/CH/CU
- Existing Am186/188ES/ESLV customers are encouraged to migrate to Am186/188ER or Am186CU
- AMD provides long term support on Am186/188ER and Am186CC/CH/CU microcontrollers

ES, ER and CU Block Diagram Comparison



Migrating to Am186/188ER

ES to ER Summary

- Applicable when don't need two UARTs
- Extra features provided by 186ER
  - Higher speed
  - Lower power consumption
  - 32KB on-chip SRAM
  - Synchronous Serial Interface (SSI)
  - Enhanced PLL, 4x mode available
- Pinout is compatible
  - Both 100-pin PQFP and 100-pin TQFP package available
- Register set is mostly compatible
- Minor software modification might be required
- Minor hardware redesign required

ES to ER Hardware Consideration

- Vcc
  - ER is 3.3V, requires 5V to 3.3V voltage regulator
  - The I/Os of ER are 5V tolerant and TTL compatible, can still work with 5V memory and peripheral parts
- PLL
  - ES supports /2, PLL x1 mode
    - Pinstrap S6/CLKDIV2# pin to decide which mode
    - Internal pullup, default to PLL x1 mode (without external pulldown)
  - ER supports /2, PLL x1, PLL x4 mode
    - Pinstrap S6/CLKSEL1#, UZI#/CLKSEL2# to decide which mode
    - Internal pullup on both pins, default to PLL x4 mode (without external pulldown on either pins)
- UART
  - ER has only one UART
  - The UART of ER does not support hardware flow control

ES to ER Hardware Consideration (Cont'd)

- Chip Select
  - ER doesn't support programmable bus width of LCS, MCS & I/O space
  - ER doesn't support unified MCS mode
- Pulse Width Demodulation (PWD)
  - ER doesn't support PWD
  - Can be implemented using two timers and two interrupts
- External interrupt request source
  - ES has 2 more interrupt request sources (INT5, INT6), multiplexed with DRQ0 and DRQ1 pins respectively

ES to ER Software Consideration

- A few Peripheral Control Block registers are different
  - Refer to <<Am186EM/ER/ES/ED/CU Peripheral Control Block Register Map Comparison>>
- Watchdog Timer
  - The WDT of ES is active after reset
  - The WDT of ER is inactive after reset
- Internal RAM of ER
  - Can be configured to locate at any 32K boundary within the 1Mbyte memory address space
  - Internal RAM was disabled after processor reset
  - IMCS register does not need to be programmed if internal RAM is not used

Higher Speed Available with the Migration from ES to ER

- Commercial temperature range
  - Both PQFP and TQFP packages
    - ES to ER: from 40MHz to 50MHz
    - ESLV to ER: from 25MHz to 50MHz
- Industrial temperature range
  - PQFP package
    - ES to ER: from 25MHz to 50MHz
    - ESLV to ER: from 20MHz to 50MHz
  - TQFP package
    - ES to ER: from unavailable to 50MHz
    - ESLV to ER: from unavailable to 50MHz

Migrating to Am186CU

ES to CU Summary

- 186CU provides all the features of 186ES, plus some extra
- Hardware redesign required
  - The package of 186CU is bigger than ES
    - 160 pin PQFP vs. 100 pin PQFP/TQFP
  - CU is 3.3V operation (5V tolerant I/O), requires 5V to 3.3V voltage regulator
- Software modification required
  - The Peripheral Control Block register set of CU is not compatible with ES
  - Only low level drivers (accessing Peripheral Control Block) need to be modified
- HW & SW rework required for migrating ES design to CU is much less than migrating to other platform

186CU Extra Features over 186ES

- Higher performance
  - 50 MHz max. frequency
- Synchronous Serial Interface
- Two more general-purpose DMA channels
- Higher performance UARTs
  - High-speed UART can run as high as 460kbps with autobaud detection
- Integrated DRAM controller
  - Support up to 2 banks, symmetric 256Kx16 EDO DRAM supported
- Ability to boot from either 8-bit or 16-bit ROM
  - No 8-bit version (188CU) needed
- More PIOs (48 vs. 32)
- Others (might not be needed)
  - USB, SmartDMA

ES to CU Hardware Consideration

- Vcc
  - CU is 3.3V operation, requires 5V to 3.3V voltage regulator
  - The I/Os of CU are 5V tolerant and TTL compatible, can still work with 5V memory and peripheral parts
- PLL
  - ES supports /2, PLL x1 mode
    - Pinstrap S6/CLKDIV2# pin to decide which mode
    - Internal pullup, default to PLL x1 mode (without external pulldown)
  - CU supports PLL Bypass, PLL x1, PLL x2 and PLL x4 mode
    - Pinstrap HLDA/CLKSEL1, PCS4#/CLKSEL2 to decide which mode
    - Internal pullup on both pins, default to PLL x2 mode (without external pulldown on either pins)
- Static operation
  - CU is a fully static design and can be placed in static mode by stopping the input clock (PLL Bypass Mode only)

ES to CU Hardware Consideration (Cont'd)

- Power save mode not available on CU
  - Can be implemented with external clock generator (PLL Bypass Mode), Application Note & Codekit available
- Interrupt controller of CU does not support cascade mode (external 8259) and slave mode
- UART
  - DCE/DTE hardware flow control protocol no longer available (affected when using external modem)
  - UART of CU can also be driven from the UART clock input (UCLK), as well as derived from CPU clock
- UZI# pin not available on CU
- CLKOUTB pin not available on CU

ES to CU Software Consideration

- Some Peripheral Control Block registers are different
  - Refer to <<Am186EM/ER/ES/ED/CU Peripheral Control Block Register Map Comparison>>
- Peripheral Control Block (PCB) of CU is bigger than ES
  - 1 Kbyte vs. 256 byte
  - Offset of PCB registers are different

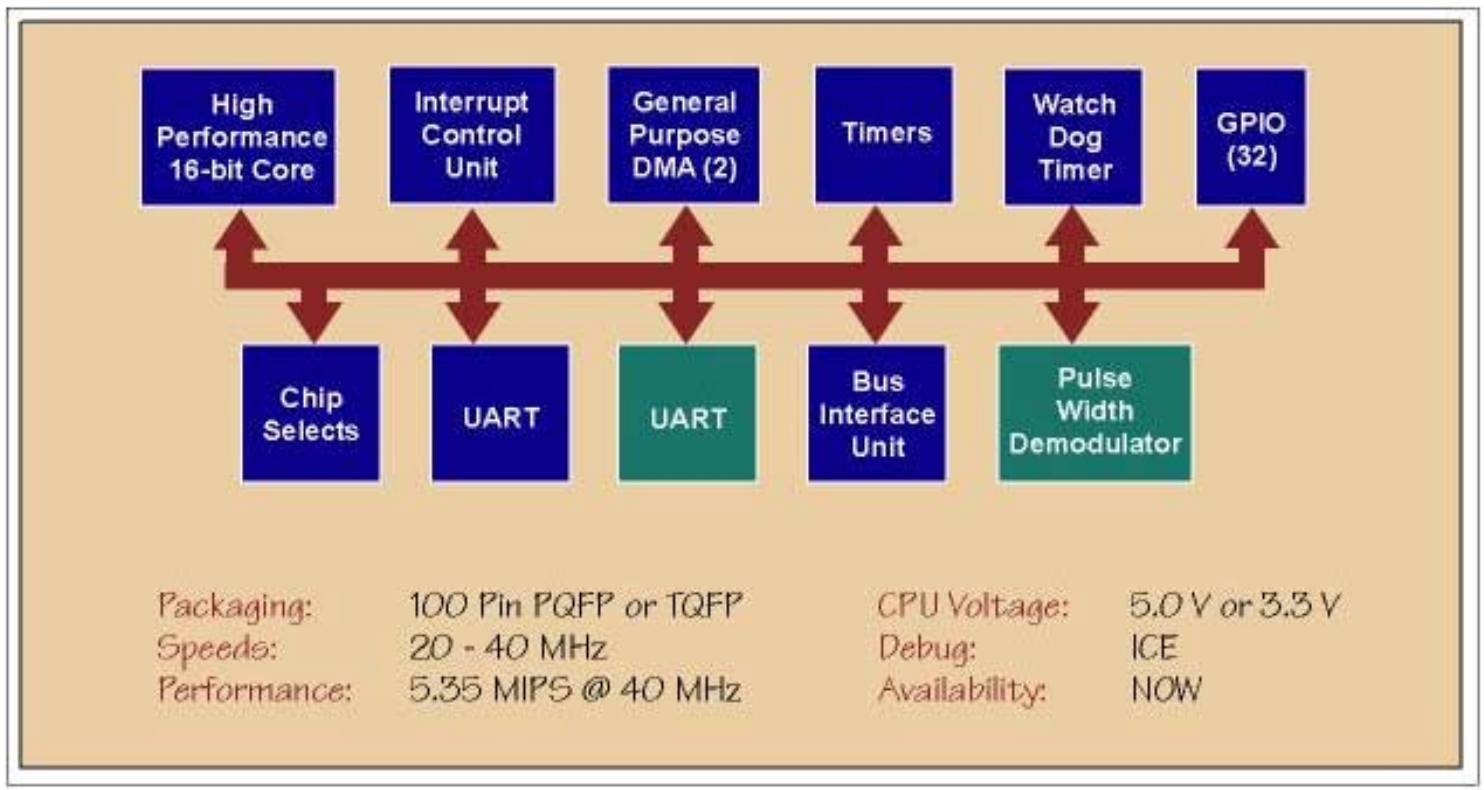
Higher Speed Available with the Migration from ES to CU

- Commercial temperature range
  - PQFP package only
    - ES to CU: from 40MHz to 50MHz
    - ESLV to CU: from 25MHz to 50MHz
- Industrial temperature range
  - PQFP package only
    - ES to CU: from 25MHz to 40MHz
    - ESLV to CU: from 20MHz to 40MHz
- 186CU does not offer TQFP package

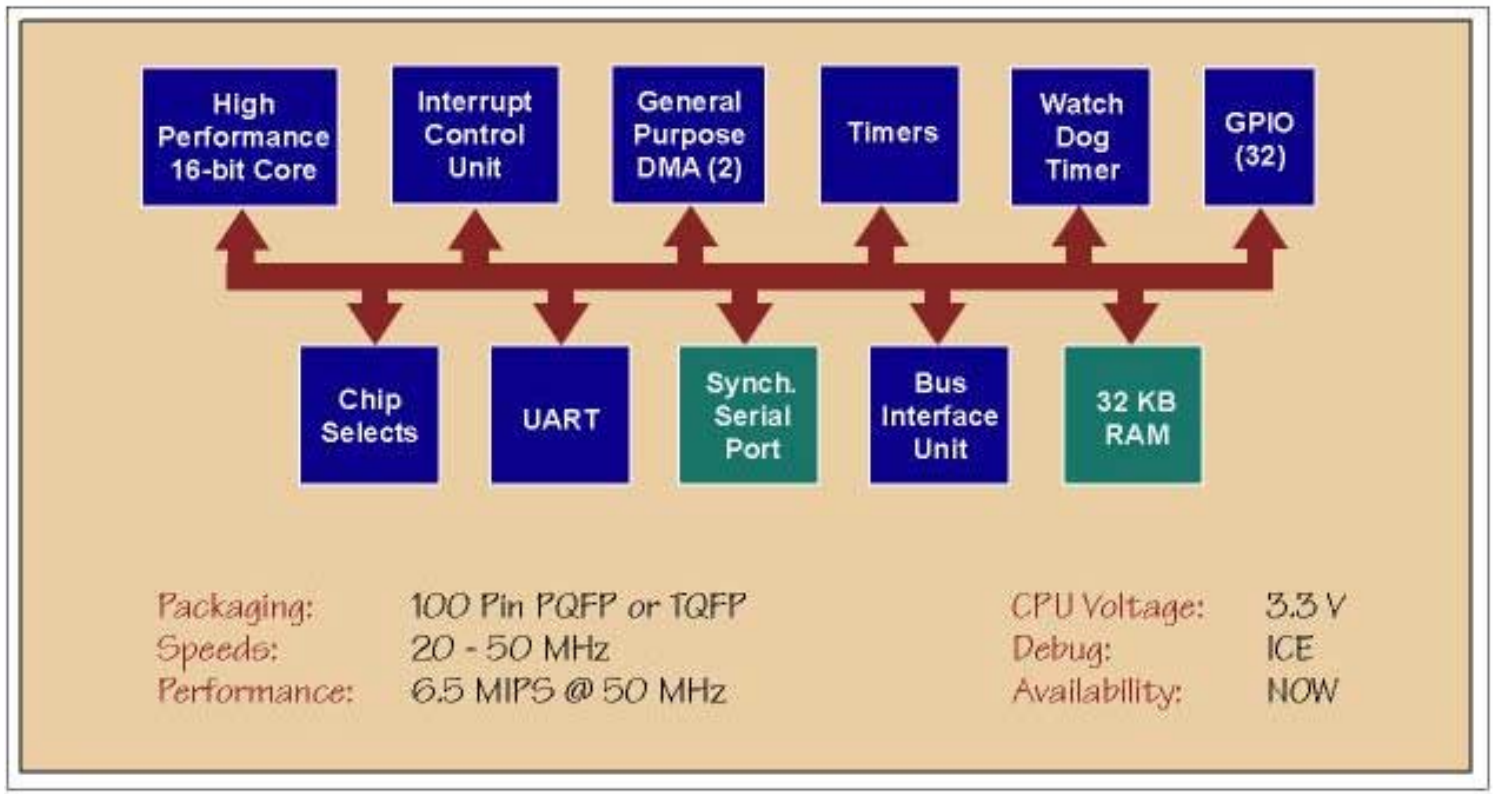
Backup

Am186ES, Am186ER, Am186CU Microcontrollers Block Diagrams

Am186ES Block Diagram



Am186ER Block Diagram



Am186CU Block Diagram