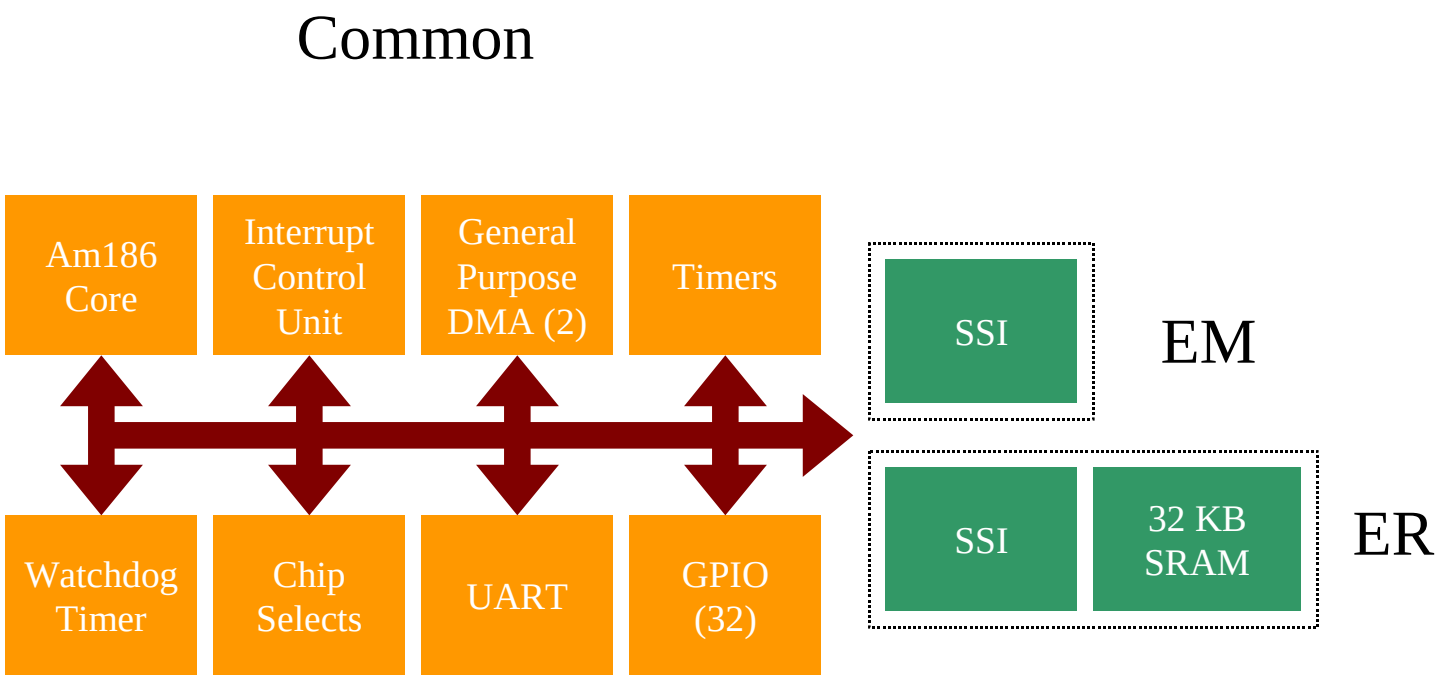
Am186™EM/EMLV, Am188™EM/EMLV Microcontrollers Migration Path

October 24, 2001

Summary

- Am186EM, Am188EM, Am186EMLV, Am188EMLV microcontrollers are not recommended for new design
- New customers interested in Am186/188EM/EMLV are encouraged to consider Am186/188ER
- Existing Am186/188EM/EMLV customers are encouraged to migrate to Am186/188ER
  - The migration is very easy with minor hardware rework
- AMD provides long term support on Am186/188ER and Am186CC/CH/CU microcontrollers

EM and ER Block Diagram Comparison



EM to ER
– Easy Migration Path

- Am186ER provides all the features of Am186EM, plus:
  - Higher speed
  - Lower power consumption
  - 32KB on-chip SRAM
  - DMA to/from UART
  - Hardware Watchdog Timer (WDT)
  - Enhanced PLL, 4x mode available
- Pinout is compatible
  - Both 100-pin PQFP and 100-pin TQFP package available
- Register set is compatible
- Software modification not needed
- Minor hardware redesign required

Hardware Consideration

- Vcc
  - ER is 3.3V, requires 5V to 3.3V voltage regulator
  - The I/Os of ER are 5V tolerant and TTL compatible, can still work with 5V memory and peripheral parts
- PLL
  - EM supports /2, PLL x1 mode
    - Pinstrap S6/CLKDIV2# pin to decide which mode
    - Internal pullup, default to PLL x1 mode (without external pulldown)
  - ER supports /2, PLL x1, PLL x4 mode
    - Pinstrap S6/CLKSEL1#, UZI#/CLKSEL2# to decide which mode
    - Internal pullup on both pins, default to PLL x4 mode (without external pulldown on either pins)

Software Consideration

- No modification required on software
- ER has 2 more registers in Peripheral Control Block than EM
  - Watchdog Timer Control Register (WDTCON), offset E6h
    - WDT is inactive after reset
    - WDTCON do not need to be programmed if WDT is not used
  - Internal Memory Chip Select Register (IMCS), offset ACh
    - Internal RAM was disabled after processor reset
    - IMCS do not need to be programmed if internal RAM is not used

Feature Enhancement

- Watchdog Timer (WDT)
  - EM can configure Timer1 as WDT, can cause a maskable WDT interrupt
  - ER has a hardware WDT, can cause NMI or system reset
- UART supports DMA operation
- 32 Kbyte on-chip SRAM
  - Can be configured to locate at any 32K boundary within the 1Mbyte memory address space

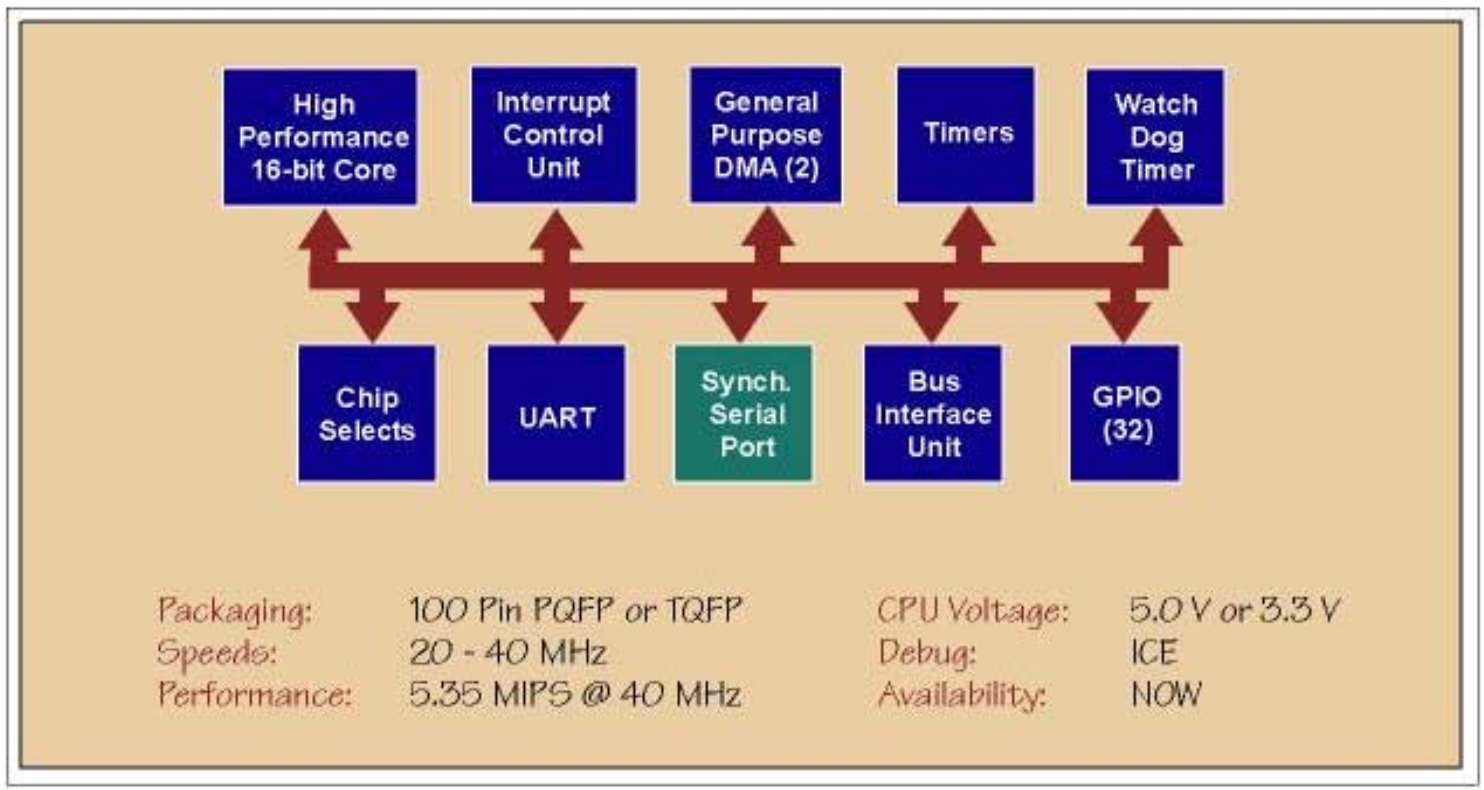
Higher Speed Available with the Migration

- Commercial temperature range
  - Both PQFP and TQFP packages
    - EM to ER: from 40MHz to 50MHz
    - EMLV to ER: from 25MHz to 50MHz
- Industrial temperature range
  - PQFP package
    - EM to ER: from 25MHz to 50MHz
    - EMLV to ER: from 20MHz to 50MHz
  - TQFP package
    - EM to ER: from unavailable to 50MHz
    - EMLV to ER: from unavailable to 50MHz

Backup

Am186EM, Am186ER Microcontrollers
Block Diagrams

Am186EM Block Diagram



Am186ER Block Diagram